Chapter 9
An 802.15.4 IR-UWB Transmitter SoC with Adaptive-FBB-Based Channel Selection and Programmable Pulse Shape

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9.1 Introduction

Smart sensors for the Internet-of-Things (IoT) embed four main functions: sensing of the physical world, data processing, wireless communications, and power management as represented in Fig. 9.1. To avoid the economical cost and environmental footprint of battery replacement [1], IoT smart sensors should operate on energy-harvesting sources such as micro PV cells or thermoelectric generators. This put a serious constraint on the average system power consumption: the sensing, processing, and communication functions should fit in a 1–100 μW power budget, depending on the harvester type and size, as well as on the conditions of the environment. Among these functions, sensing can be performed in a pretty low-power way with energies down to 8 pJ/sample for audio sensing [2], 17 pJ/pixel sample for image sensing [3], and 2 pJ/sample for ECG biomedical sensing [4]. Wireless communications are much less energy efficient for several reasons including protocol overhead and physical limitations of the air as a communication channel [5]. In IoT smart sensors, communications are typically asymmetric with more data to be transmitted than data to be received. The transmit operation is thus critical with respect to energy efficiency. State-of-the-art short-range WPAN radio transceivers consume down to 3.7nJ per raw bit transmitted over the air for Bluetooth Low-Energy (BLE) [6], which leads to 10nJ/bit at the application level when considering the protocol overhead [5]. With these solutions, it is possible to meet the energy-harvesting power budget for simple applications with low data

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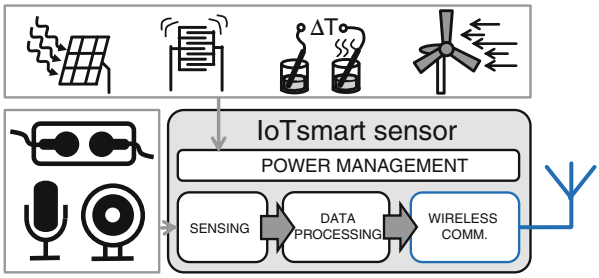


Fig. 9.1 General architecture of an IoT smart sensor

rates below 10 kbps such as motion-based room occupancy monitoring [7] but the transmitter power remains prohibitive in applications with medium continuous data rates in the 0.1–10 Mbps range. As an alternative, local data processing directly in the IoT smart sensor can be used to limit the wireless communications data rates [8] by extracting the relevant information from the sensed data. Ultra-low-power (ULP) design is thus required for local data processing and this is enabled by FD-SOI technology for microcontrollers [9], memories [10], and application-specific processors [11]. However, local data processing comes at the expense of flexibility, computational power, and interaction between smart sensors in short-range networks. Some applications thus cannot fully rely on local data processing and still require medium data rates in the range of 0.1–10 Mbps.

In this chapter, we study how the unique wide-range back-bias control in FD-SOI can be used to build ULP radios by focusing on their transmitter (TX) side. We apply this idea to the design of a TX SoC for impulse-radio ultra-wideband (IR-UWB) communication codenamed SleepTalker. IR-UWB communication is an efficient physical-layer (PHY) solution for high-data rate, short-range, and low-power communications due to the duty-cycled nature of the output signal as well as the potential for low-complexity and low-power TX architectures [12]. These characteristics can lead to strong power savings for asymmetric communications in smart sensor applications and have thus been the driving force behind the development of the IEEE 802.15.4 UWB PHY standard [13]. This standard has two distinct bands: 3–5 GHz and 6–10 GHz, and combines binary burst pulse position modulation (BPPM) with binary phase-shift keying (BPSK) modulation. It provides data rates from 0.11 to 27.24 Mbps. The highest data rate encodes each symbol in just one 2 ns pulse, which results in the lowest energy consumed per bit bit but also the shortest communication range. For the lowest data rates, multiple 2 ns pulses are concatenated in bursts. Each burst encodes one symbol to increase range at the cost of the energy consumed per bit. The burst position within the BPPM time slot is controlled by a pseudo-random sequence. This burst pulse position scrambling improves the spectral smoothness of the output power by limiting spectral lines to meet spectral regulations.

SleepTalker TX SoC can operate in the three channels of the 3–5 GHz 802.15.4 UWB low band with carrier frequencies of 3.5/4.0/4.5 GHz, respectively.

SleepTalker is capable of both BPPM and BPSK modulation and covers seven data rates from 0.11 to 27.24 Mbps, compliant with the IEEE 802.15.4 UWB standard.

In IR-UWB communications, the challenge is to optimize the power consumption of the three common TX functions (frequency synthesis, modulation, and power amplification) while complying with the FCC regulation mask and enabling the wide data rate range of 802.15.4 UWB standard. In SleepTalker, we use a digital TX architecture to exploit the back biasing capability of FD-SOI for implementing these functions at ULP as follows.

- *Feature 1:* a body-biased-controlled ring oscillator (BBCO) is used as a low-jitter local oscillator (LO) with instantaneous startup. This enables the use of a PLL-free digital TX architecture with aggressive LO duty cycling within the BPPM time slot to reduce jitter accumulation and power consumption.
- *Feature 2:* tuning of the BBCO to oscillate at the carrier frequency (CF) of the selected 802.15.4 UWB channel is automatically performed on-chip with a programmable forward back-bias (FBB) generator.
- *Feature 3:* programmable pulse shaping is implemented by a digital power amplifier (PA) for meeting spectral compliance with the FCC regulation with back-bias control of the TX output power.
- *Feature 4:* continuous-time NMOS/PMOS current matching is performed by an adaptive FBB loop with a back-gate-driven amplifier for voltage range compatibility.
- *Feature 5:* ultra-low-voltage (ULV) operation down to 0.55 V of the high-frequency TX up to 4.5 GHz is enabled by 28 nm FD-SOI process with wide-range FBB up to 1.8 V for NMOS (BBN) and −1.8 V for PMOS (BBP), as explained in Chap. 3.

This chapter is organized as follows. The general digital TX architecture operated at 0.55 V is presented in Sect. 9.2. The TX design is explained in Sects. 9.3–9.5, which focus on the innovations enabled by the back biasing technique: duty-cycled frequency synthesis based on the BBCO (*Features 1* and *2*), pulse-shaping digital PA with back-bias controlled output power (*Feature 3*), and FBB generators with current-matching loop (*Feature 4*). The capability of FD-SOI to operate high-speed logic at ULV (*Feature 5*) is not discussed in this chapter, see Chaps. 2 and 3 for more details on this. The architecture of the full SoC including the back-bias drivers and the NMOS/PMOS current-matching loop *Feature 4* is presented in Sect. 9.6 with measurement results in Sect. 9.7. Let us mention that this chapter is largely inspired from [14, 15] where SleepTalker was first presented.

9.2 Architecture of the Digital TX

Figure 9.2 shows 802.15.4 UWB PHY symbols with BPPM and BPSK modulation, which highlights the highly duty-cycled nature of the 802.15.4 UWB output signal. Indeed, the duty cycle is only 0.78 and 3.12% with data rates using a pulse repetition

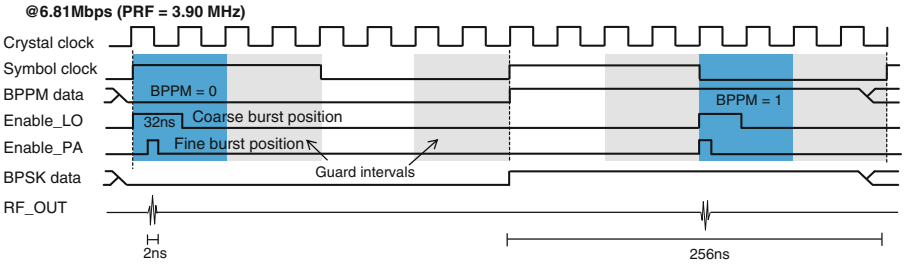


Fig. 9.2 Principle of the aggressive hierarchical duty cycling within the BPPM time slot. The LO is active for one cycle of the 31.25 MHz crystal clock (coarse burst position) and the PA is active only during the pulse burst emission (fine burst position)

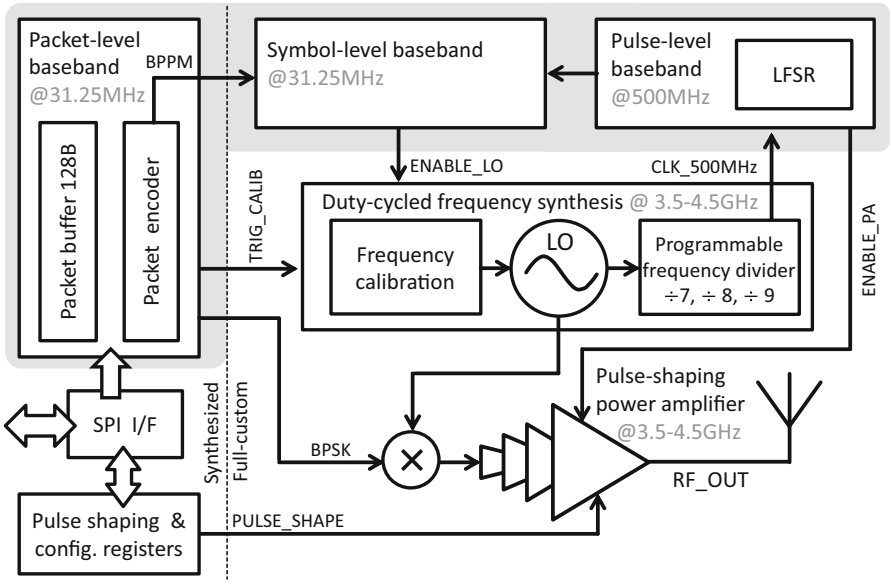


Fig. 9.3 Architecture of the duty-cycled PLL-free digital TX

frequency (PRF) of 3.9 and 15.6 MHz, respectively. The architecture of the proposed digital TX shown in Fig. 9.3 implements this 802.15.4 UWB PHY with aggressive hierarchical duty cycling to leverage this characteristic. The LO generates the 3.5–4.5 GHz carrier frequency depending on the selected channel with both positive and negative polarities. The pulse-shaping power amplifier (PA) performs the BPSK modulation by selecting the pulse burst polarity. BPPM modulation is performed by enabling the rest of the TX only during the used BPPM time slot and thus disabling it in the guard intervals and the unused time slot. Within this BPPM time slot, the coarse burst position is computed with a 32 ns time resolution corresponding to the crystal-clock cycles, with the output of the 802.15.4 linear feedback shift register (LFSR) implementing the pulse burst position scrambling. This enables the LO

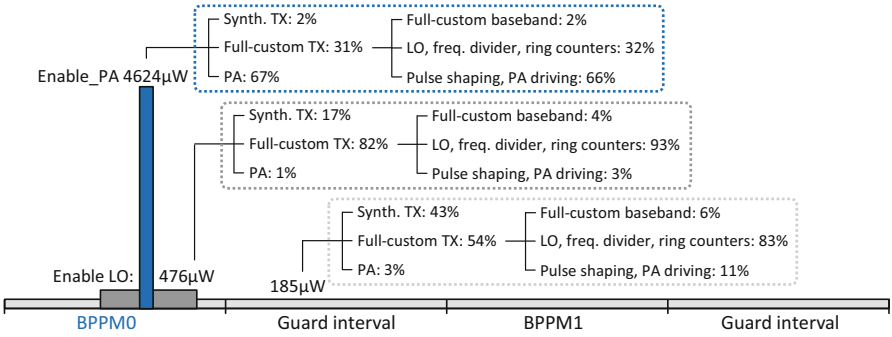


Fig. 9.4 Simulated power breakdown between the different parts of the TX depending on the duty cycling mode during the symbol duration

(Enable_LO signal) only during this coarse burst position for durations between 16 and 64 ns depending on the selected data rate. The fine pulse burst position has a 2 ns time resolution and is performed by the pulse-level baseband processor, which is clocked at 500 MHz by the LO clock divided. This enables the PA (Enable_PA signal) for durations between 2 and 64 ns depending on the selected data rates only when the pulses need to be emitted. Such an aggressive duty cycling of the PA and the LO directly results in strong power savings as the subsequent TX logic is clocked either directly by the LO output or by its 500 MHz divided clock.

The LO frequency is calibrated periodically as triggered by the TRIG_CALIB signal as will be detailed in Sect. 9.3. The PA performs pulse shaping (see Sect. 9.4) with the pulse shape programmable through configuration registers. A 128-byte packet buffer is embedded with forward error-correction encoding (Reed–Solomon) in the packet encoder. An SPI interface is used for sending data and programming configuration registers including the pulse shape, the channel, and the data rate. The 31.25 MHz packet-level baseband processor is synthesized from standard cells along with the SPI interface and configuration registers. The rest of the TX results from a full-custom transistor-level design.

Figure 9.4 illustrates the interest of duty cycling for reducing the power consumption of the TX during a symbol. The baseline power consumption when the LO and the PA are disabled is 185 µW. This rises to 476 µW when enabling the LO and thus the pulse-level baseband processor. When the PA is enabled, the power is 4.6 mW, i.e., 25× the baseline power.

9.3 Duty-Cycled Frequency Synthesis

As the 802.15.4 UWB bursts are BPSK modulated, there is a strong requirement on the frequency accuracy and stability for correct coherent demodulation. Following the analysis from [16], we can define an upper bound for the total phase noise at the

end of the burst in order to ensure correct demodulation of the BPSK-encoded data. By taking some margin into account, we set the maximum phase noise allowable to $\pi/4$ which corresponds to a maximum accumulated jitter of 27.7 ps after 32 ns at 4.5 GHz.

The aggressive duty cycling of the LO prevents the use of a PLL because of its prohibitive settling time and forces the choice of an architecture based on a free-running LO. LC-based oscillators can offer low jitter at the cost of high power, large area, and large settling time. To avoid these drawbacks, previous low-power TX relied on ring oscillators (ROs) duty-cycled to a quarter of the symbol period. However, in the case of low data rate, the quarter symbol period is quite long and leads to high jitter accumulation due to the degraded phase noise of ROs compared to LC oscillators. Figure 9.5 shows that a current-starved differential RO at nominal 1 V supply voltage suffers from a 10 ns integrated jitter for a run time corresponding to the longest symbol duration (0.11 Mbps rate). As shown in Fig. 9.5a, the aggressive within-BPPM LO duty cycling from Sect. 9.2 significantly limits the jitter accumulation. Nevertheless, it is still prohibitive for BPSK data encoding. Therefore, to get rid of the current-starving delay control of the delay elements, we further improve jitter by first using a back-bias control of their delay. To do so, independent and symmetric FBB voltages are applied to NMOS (BBN_LO voltage) and PMOS (BBP_LO voltage) transistors. The LO is thus a BBCO. Second, we use a differential multipath RO based on feedforward loops, similar to the one proposed in [17]. The 7-stage architecture illustrated in Fig. 9.5 improves both the switching speed as well as the noise performance thanks to its fast transitions. The proposed BBCO is disabled by slightly modifying two of the seven delay elements in the chain to implement NOR and NAND functions in order to gate the oscillation in both the main and feedforward paths. They are sized to feature the same delay as

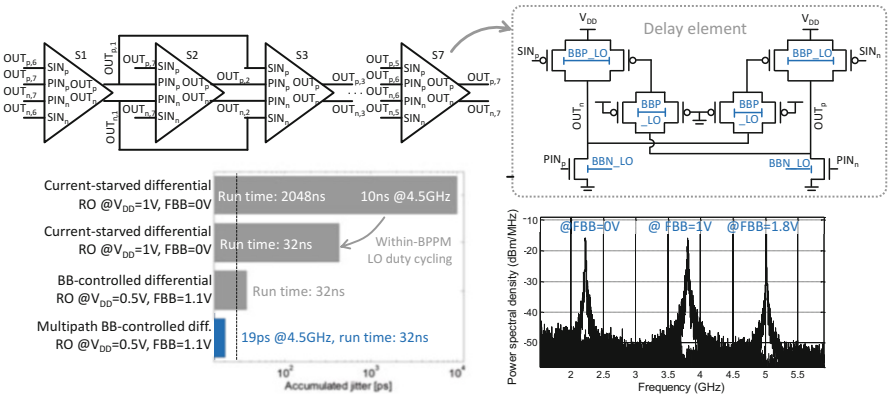


Fig. 9.5 Local oscillator: architecture of the proposed multipath back-bias-controlled oscillator (BBCO) with schematic of the delay element. Its frequency is controlled through the FBB voltages applied to the NMOS (BBN) and the PMOS (BBP). Simulated accumulated jitter and power spectral density

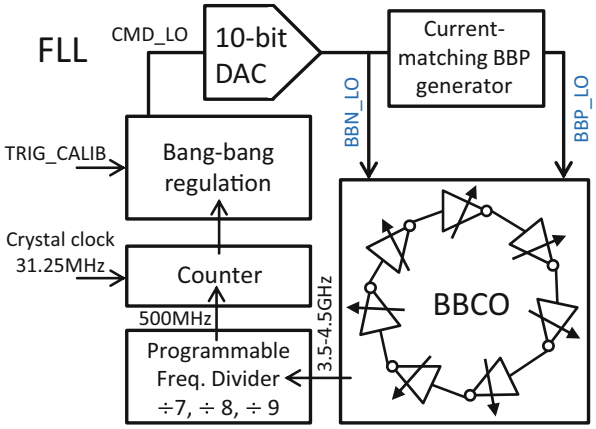


Fig. 9.6 Block diagram of the frequency-locked loop (FLL) performing LO frequency calibration through adaptive FBB

the regular delay elements. Figure 9.5 also shows the wide BBCO frequency range from 2.2 to 5 GHz by sweeping the FBB between 0 V (BBN = BBP = 0 V) and 1.8 V (BBN = −BBP = 1.8 V). This is of course a unique feature of FD-SOI technology thanks to the good control of the transistor V_t through FBB.

The free-running BBCO LO is integrated inside a duty-cycled frequency-locked loop (FLL) represented in Fig. 9.6 to periodically calibrate its frequency. The BBCO output is divided by the programmable frequency divider to generate the pulse-level 500 MHz clock. A control logic compares the divided LO output to a reference crystal clock at 31.25 MHz and adapts the BB voltage command CMD_CF in a bang-bang fashion to lock the LO frequency on the desired 3.5/4.0/4.5 GHz CF of the selected channel. A 10-bit DAC generates the NMOS BB voltage (BBN_LO) and a current-matching loop adapts the PMOS BB voltage (BBP_LO) to keep the NMOS/PMOS ON current ratio constant as described in Sect. 9.5. The CF calibration is performed once before packet transmission.

9.4 Pulse-Shaping Digital Power Amplifier

FCC regulations impose to limit emissions below −75 dBm/MHz of power spectral density (PSD) in the 960–1610 MHz band, which makes the design of digital PA difficult without high-order off-chip filtering. Indeed, as studied in [12], capacitive coupling of the digital PA output alone does not provide a sufficient roll-off to meet the FCC regulation limit when transmitting in the 3–5 GHz UWB bands. In SleepTalker, we designed a fully digital pulse-shaping filter integrated within the PA to improve the roll-off. Figure 9.7 illustrates the spectral impact of shaping a rectangular pulse to a Gaussian pulse with the same duration. For a Gaussian pulse

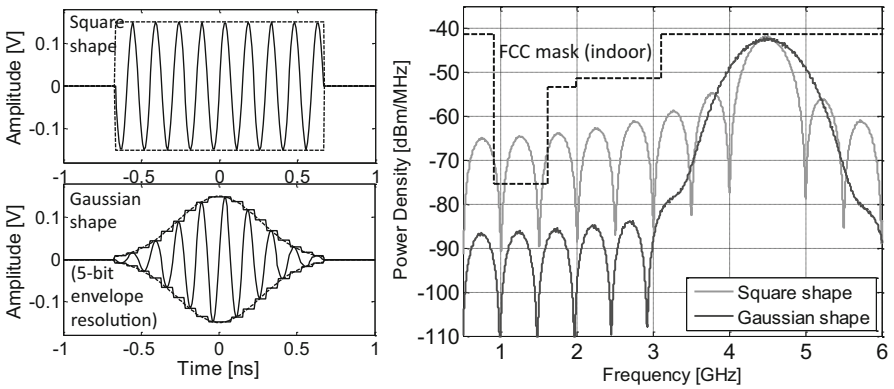


Fig. 9.7 Left: continuous-time square and Gaussian pulse shapes (envelope quantized at 5-bit resolution). Right: impact of the pulse shape on the output PSD. For the same maximum power inside the band, the square-shaped pulse features significant PSD in the prohibited 960–1610 MHz band. The Gaussian-shaped pulse results in much lower out-of-band emissions

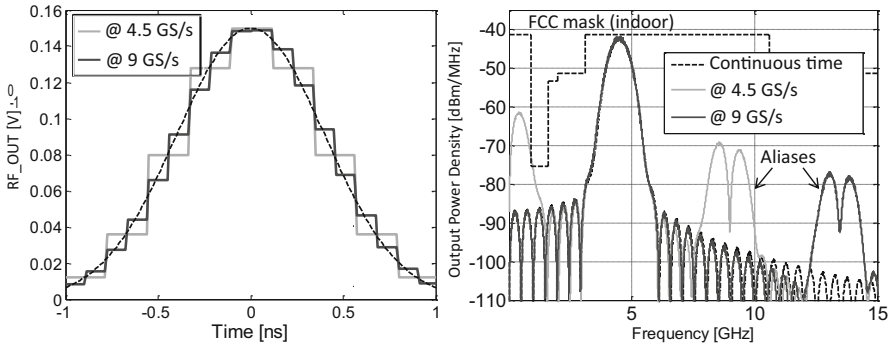


Fig. 9.8 Impact of the pulse shape temporal resolution. Left: Gaussian pulse shape sampled at 4.5 ($@f_{LO}$) or 9 ($@2 \times f_{LO}$) GS/s. Right: spectral folding caused by the sampling frequency of the shape. A sampling at f_{LO} leads to a folding peak at DC and spectral content in the 0.96–1.61 GHz band, which violates the FCC regulation mask. Sampling at $2 \times f_{LO}$ eliminates the folding around DC

shape with its envelope quantized at 5-bit resolution, the spectral content in the prohibited 960–1610 MHz band can be reduced by more than 20 dB. To implement the shaping functionality, the digital power amplifier is split in independent parallel stages to act as a 32-stage current DAC, leading to the 5-bit envelope resolution.

Figure 9.8 illustrates the impact of the pulse shape temporal resolution on the output PSD. If the sampling is performed at the LO central frequency (222 ps temporal resolution at 4.5 GHz), spectral folding causes significant power close to the prohibited 960–1610 MHz band. To avoid this problem, the pulse-shaping digital PA is operated at 2× the LO frequency, which pushes the spectral folding away from the restricted bands.

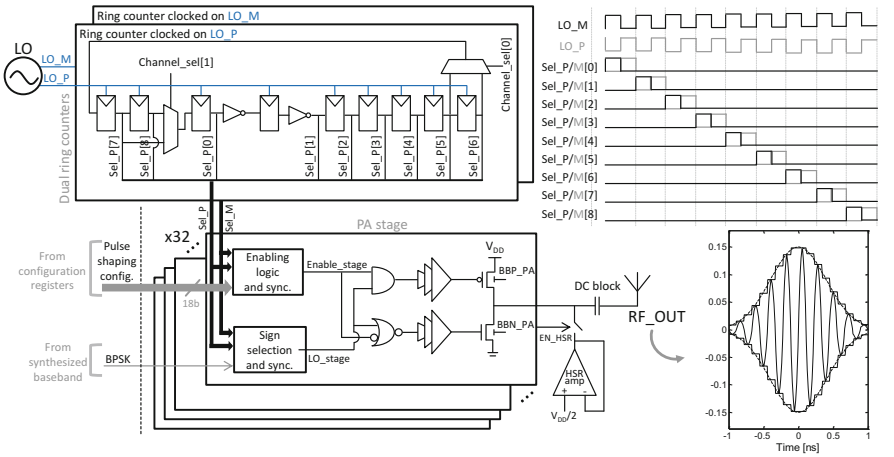


Fig. 9.9 Architecture of the programmable pulse-shaping digital PA. The pulse-shaping functionality is implemented by a 5-bit 9 Gs/s current DAC controlled by the ring counters outputs. The PA output is precharged at $V_{DD}/2$ by a high-slew-rate (HSR) amplifier and a DC blocking MiM capacitor filters the DC value. Right: stage-select signal sequence generated by the ring counters and simulated RF output waveforms

The complete pulse-shaping digital PA architecture is shown in Fig. 9.9. The dual ring counters are clocked on the LO positive and negative edges, respectively, and generate 7 to 9 enable signals with duty cycles varying from 1/7 to 1/9 depending on the selected channel from 3.5 to 4.5 GHz. The symbol-level baseband generates the BPSK-encoded and scrambled data controlling the polarity of the pulses. The 5-bit 14–18-sample programmable envelope of the pulse shape is stored in the pulse-shaping configuration registers. They are converted to thermometer code to control the 32 parallel PA stages. The ring counter output signal is used to control the cyclic selection of the 14–18 samples of the pulse shape and to control the enable of each of the 32 stages. The BPSK-encoded data are used to select the LO phase to use, which modulates the pulse polarity. The PA output stage is a tri-state inverter sized so that the 32 parallel stages with mid-range back biasing are able to drive the antenna with a peak-to-peak voltage of 350 mV at 4.5 GHz. The tri-state output stages offer the advantage of being fully turned off to save power between pulse bursts. Programmable FBB in the last stage of the PA is used to tune the RF output power and to compensate for PVT variations by controlling the current of the PA output stage.

For high PA efficiency, its output swing needs to be close to rail-to-rail with a DC component at $V_{DD}/2$. However, the delay mismatch of the signals driving the output-stage NMOS and PMOS transistors can lead to asymmetric pulses leaving a DC voltage at the end of the pulse different from $V_{DD}/2$. To alleviate this effect, the PA output is precharged to $V_{DD}/2$ between the pulse bursts. The precharge amplifier needs to drive the output node back to $V_{DD}/2$ in less than 16 ns, which is the duration of 1 guard interval in the fastest data rate, which leads to a slew rate of

17 V/μs. For this purpose, we designed a high-slew-rate (HSR) amplifier based on the super-class-AB OTA topology from [18] (Fig. 9.10). It features adaptive biasing of the input differential pair depending on the differential-input large signal to automatically boost the bias current and achieve high slew rate while maintaining a low quiescent current. It also features a local common-mode feedback first described in [19] implemented with two 10 kΩ matched resistors in order to boost the current efficiency. The HSR is supplied at 1.2 V to reach the stringent slew-rate requirement. Two common-source stages level shift the inputs from the 0.55 V domain for voltage compliance and an enabling signal EN_HSR disconnects the HSR output to the output of the PA stages during the pulse bursts as shown in Fig. 9.9. Figure 9.10 illustrates the adaptive biasing as well as Monte-Carlo post-layout simulations of the tri-state outputs converging after the end of a pulse.

9.5 FBB Generation and Current-Matching Loop

The generation of the back-bias voltages for NMOS transistors (BBN_LO and BBN_PA) is implemented by two capacitive DACs depicted in Fig. 9.11 over a [0;1.65 V] voltage range. The BBN voltage of the full-custom TX is generated by a 10-bit DAC to achieve fine tuning of the central frequency to the selected 802.15.4 UWB channel with 5 MHz frequency resolution. The output buffer is a 2-stage Miller-compensated OTA with cascoding to limit the impact of supply noise on the LO frequency accuracy. As the output of capacitive DACs drifts due to the switch leakage, a periodic refresh of the DAC is mandatory to avoid frequency drift during transmission. To do so, the packet-level baseband logic refreshes the DAC before each 802.15.4 packet, composed of maximum 83 preamble symbols and 1209 data symbols. At the lowest 0.11 Mbps data rate, the packet duration exceeds 10ms, which imposes heavy constraints on the switch leakage. To relax these design constraints, for this specific data rate, the DAC refresh is performed during each guard interval. The BBN voltage applied to the PA output stage does not require high accuracy as it is used only to compensate the impact of PVT variations on the output power by increasing or decreasing the peak-to-peak amplitude of the pulses. To generate this BBN, a 5-bit capacitive DAC is used with a similar architecture, output buffer, and refresh pattern.

To generate the back-bias voltages for the PMOS transistors (BBP_LO and BBP_PA), we designed continuous-time current-matching loops shown in Fig. 9.11 and similar to [3]. Replicas of an inverter or a PA output stage are used to determine the correct BBP that needs to be applied to balance the current between NMOS and PMOS transistors. An output buffer supplied by −1.8 V is used to drive the BBP back gate capacitance. The amplifier input range is 0 and 0.55 V, while the output can be driven down to −1.8 V leading to a voltage compatibility challenge even when using 1.8 V I/O transistors. To circumvent this, the Miller-compensated 2-stage OTA output buffer uses a bulk-driven NMOS input pair. This allows voltage range compatibility between the OTA output buffer and the replicas without the use

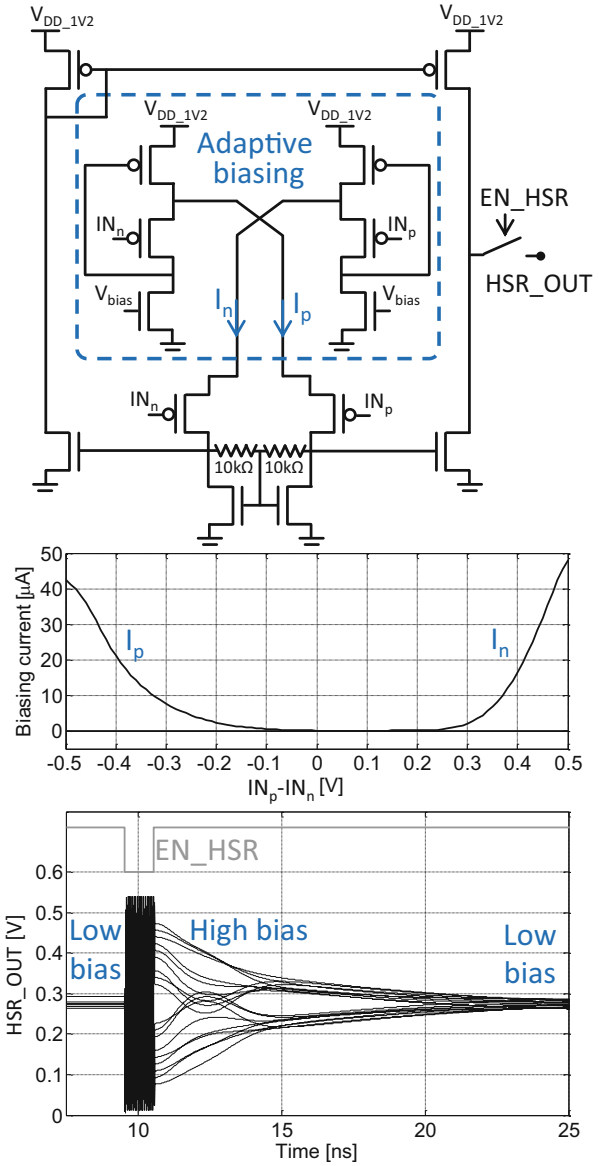


Fig. 9.10 Schematic of the HSR amplifier along with post-layout simulation results of the adaptive biasing and output node, which is quickly driven to $V_{DD}/2$ after the pulse over Monte-Carlo runs

of explicit level shifting, by implementing the output buffer with thick-oxide 1.8 V I/O transistors and the 0.55 V replica with thin-oxide core devices. Let us mention that the DACs are also implemented with thick-oxide 1.8 V I/O transistors.

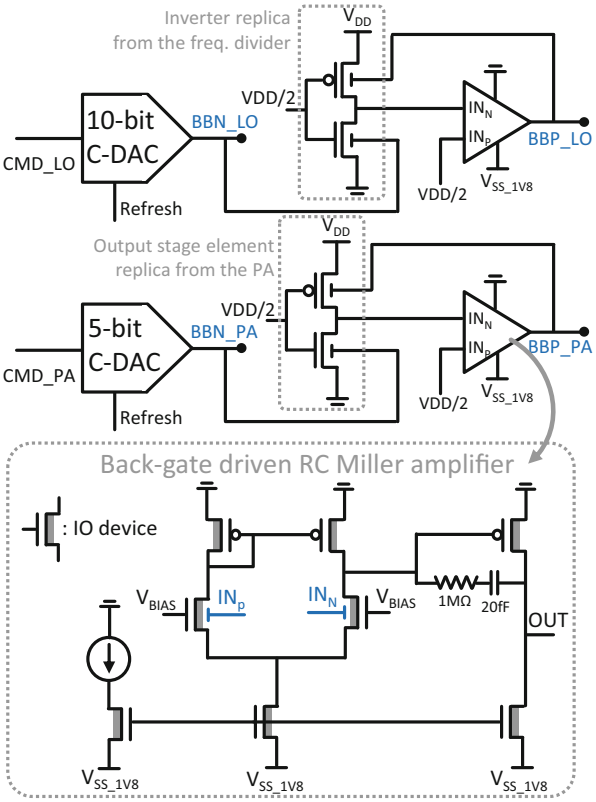
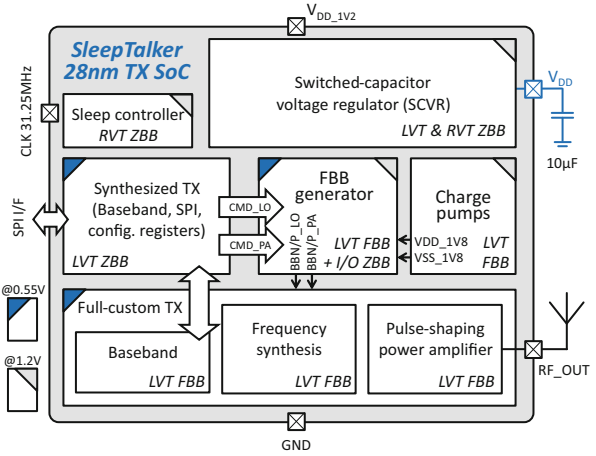


Fig. 9.11 FBB generator architecture. BBN is generated by DACs to tune the LO frequency for channel selection and the PA output power. The corresponding BBP voltages are generated from the BBNs through a current-matching structure with a back-gate-driven amplifier

9.6 SoC Integration

The SleepTalker SoC shown in Fig. 9.12 requires a single 31.25 MHz reference clock and a single 1.2 V external supply. The TX from Sect. 9.2 is supplied at 0.55 V by an on-chip switched-capacitor voltage regulator (SCVR) with high-density MiM caps. For speed concern at 0.55 V, only low-V_t (LVT) devices are used to implement both the full-custom and the synthesized TX blocks. The synthesized TX has zero back bias (ZBB, i.e., with BBN and BBP tied to ground) and uses standard cells with upsized gate length as the clock frequency is moderate (31.25 MHz). As the full-custom 0.55 V TX operates at higher frequencies (500 MHz and 3.5–4.5 GHz), minimum gate length is used with the FBB voltages for NMOS and PMOS transistors that are used to control the BBCO (BBN_LO and BBP_LO). Charge pumps generate the ± 1.8 V supplies for the FBB drivers. An always-on sleep controller supplied at 1.2 V is used to manage sleep mode by disabling the SCVR,



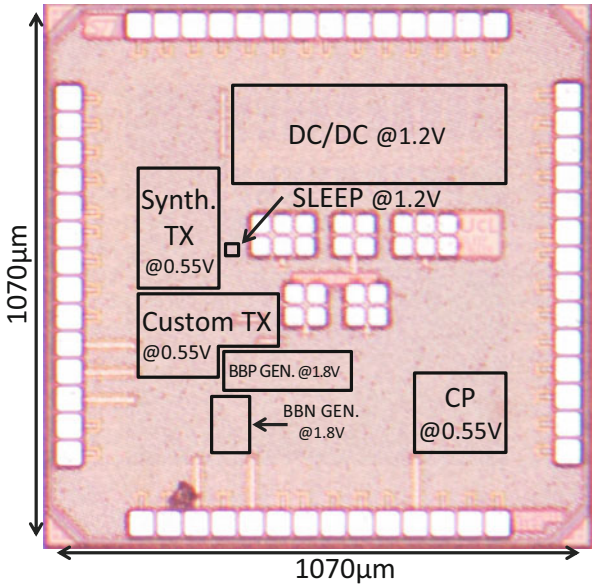


Fig. 9.12 SleepTalker SoC architecture

Fig. 9.13 SleepTalker die microphotograph. The SoC core area is 0.93 mm^2 and the TX only occupies 0.095 mm^2

thereby power gating the 0.55 V power domain. To reduce its leakage power, the sleep controller is implemented with regular-V_T devices and zero back bias. The transition from sleep mode to active is completed in less than 1ms and can be done between 2 packet transmissions.

The *SleepTalker* testchip was designed and manufactured in a 10-metal 28 nm FD-SOI CMOS process with high-density MIM capacitance option. The 0.93 mm^2 die in Fig. 9.13 has a total active area of 0.55 and 0.095 mm^2 for the TX.

9.7 Measurement Results

The characteristics of the FBB generation through the BBN DACs and the BBP current-matching loop are represented in Fig. 9.14. The achievable measured BBN and BBP ranges are, respectively, [0;1.6 V] and [0;−1.7 V]. In these measurements, the current-matching loop automatically applies a stronger FBB to the PMOS transistors than to the NMOS transistors compared to the NMOS FBB. This indicates a strong imbalance between NMOS and PMOS in the near-threshold domain, which was already reported in [20]. Figure 9.14 further illustrates this NMOS/PMOS imbalance by showing the BBN/BBP gap for 8 measured dies originated from a single wafer. Without the current-matching adaptive FBB, this NMOS/PMOS imbalance would lead to strong robustness degradation. Nevertheless, the BBP saturation at −1.7 V suggests that the imbalance is not fully compensated when BBN reaches [0.6;1 V] (depending on the die). For next-generation ULP SoCs in 28 nm FD-SOI, we recommend designing an asymmetric FBB generator with a

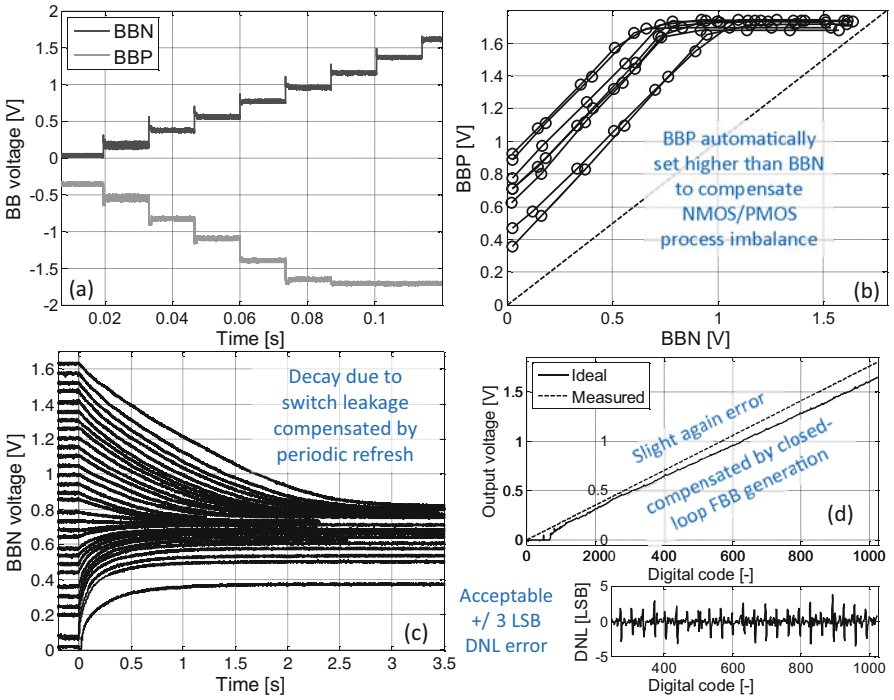


Fig. 9.14 Measured characteristics of the FBB generation: (**a**) dynamic functionality of the 10-bit BBN DAC with the BBP current-matching loop, (**b**) static BBN/BBP transfer function from the current-matching loop showing the die-to-die variations mismatch for 8 dies, (**c**) decay of the 10-bit BBN DAC for various digital input codes and (**d**) DNL performance of the 10-bit BBN DAC

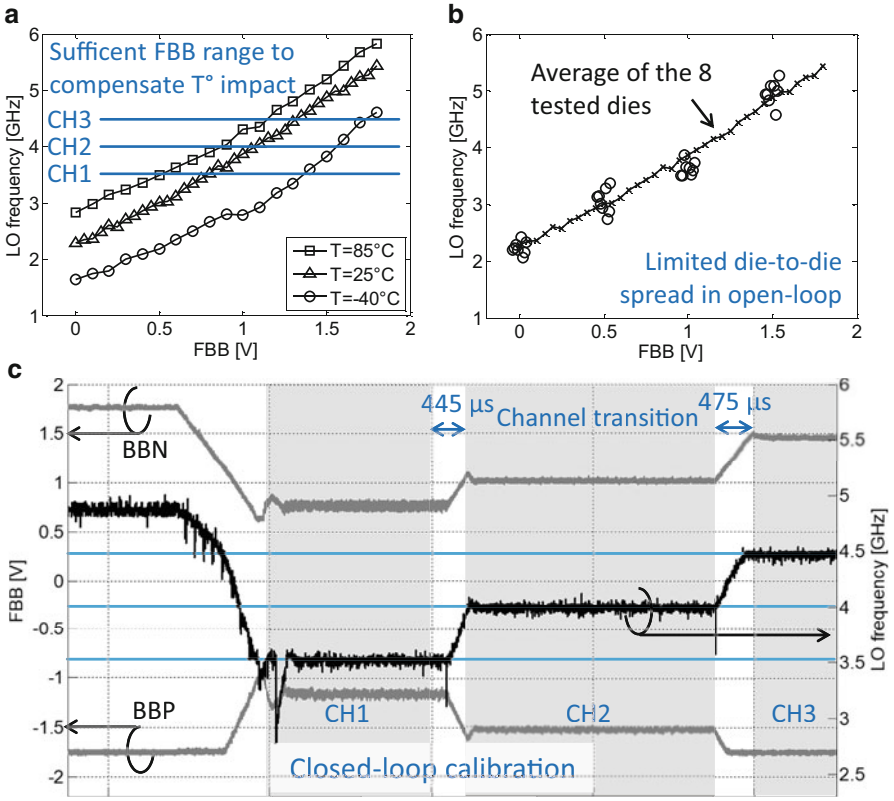


Fig. 9.15 Measured characteristics of BBCO local oscillator: (**a**) impact of FBB and temperature on the LO frequency of a typical die, (**b**) die-to-die variations of LO frequency for 8 tested dies, (**c**) closed-loop calibration of the LO frequency for a typical die

wider range for the PMOS transistors than for the NMOS transistors to fix this imbalance at ULV, see Sect. 3.2.5, and practically implemented in SleepRunner MCU from [9].

We measured the FBB control of the LO carrier frequency through the BBCO. The results are summarized in Fig. 9.15. Despite the aforementioned NMOS/PMOS imbalance, which is not fully compensated by the current-matching BBP loop, the LO frequency range is wide enough to cover the three 802.15.4 UWB channels over the full temperature range. The BBCO gain in typical conditions is in the order of 2 GHz/V. The impact of the FBB is also much stronger than the die-to-die variations. The automatic on-chip LO frequency calibration process performed before a packet transmission is also demonstrated in Fig. 9.15 with less than 500 µs for transition between adjacent channels and a typical lock time around 2 µs for two consecutive packets transmitted in the same channel.

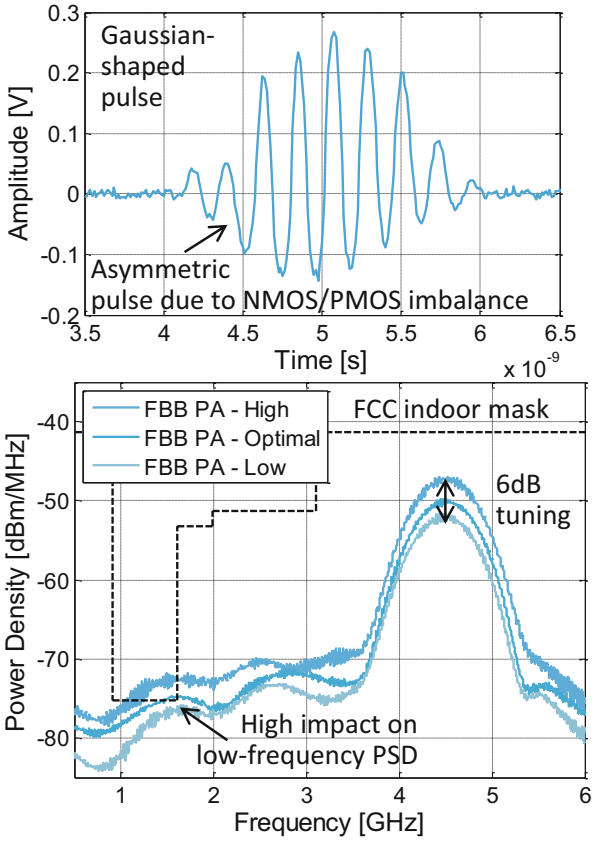


Fig. 9.16 Measured pulse waveform with Gaussian shape and output power spectral density for 27.2 Mbps data rate in channel 3 (4.5 GHz)

The TX functionality was assessed in the seven available data rates and for the three 802.15.4 UWB channels (3.5/4.0/4.5 GHz). We successfully measured pulses at a supply voltage of 0.55 V and validated the pulse-shaping functionality at up to 9 GS/s. The typical transmitted Gaussian-shaped pulse is represented in the time domain in Fig. 9.16 with the associated PSD. The shape is not fully symmetrical, which results in higher PSD in the prohibited 960–1610 MHz band than expected with simulations (Fig. 9.8). This effect is attributed to the strong NMOS/PMOS imbalance, which is not fully compensated by the current-matching BBP loop. As previously explained, this could be fixed with asymmetric FBB (wider BBP range than BBN range) or by optimizing the programmable pulse shape to compensate for this effect. This should be possible thanks to the unique flexibility of the proposed pulse-shaping PA. Figure 9.16 also demonstrates that the output power level can be controlled by the FBB level applied to the PA. The tuning range is limited to 6 dB due to the BBP saturation as soon as BBN reaches 0.6–1 V, depending on the tested die.

	Decawave, DW1000, 2014	Ryckaert, JSSC, 2007	Mercier, JSSC, 2009	Liu, RFIC, 2018		This work de Streel, JSSC, 2017		
Technology	90nm CMOS	90nm CMOS	90nm CMOS	22nm FinFET		28nm FDSOI		
TX active area [mm²]	N/A	0.066	0.07	0.085		0.095		
Carrier freq. [GHz]	3.5-6.5	3-10	2.1-5.7	8		3.5-4.5		
Operation mode	Coherent	Coherent	Non-coherent	Non-coherent	Coherent	Coherent		
Datarates [Mbps]	0.11-6.8	16	15.6	0.11		0.11	6.8	27.2
TX active power [mW]	168†	0.65	4.36	0.264	0.3	0.1	0.2	0.38
Average output power [dBm]	N/A	N/A	-16.4	-16.2	-16	> -26‡	-20	-20
TX efficiency	N/A	N/A	0.53%	9.1%	8.3%	> 2.5%‡	5%	2.6%
TX energy per bit [nJ]	24.7† (6.8 Mbps)	0.041 (16 Mbps)	0.28 (15.6 Mbps)	2.4 (0.11 Mbps)	2.7 (0.11 Mbps)	0.95 (0.11 Mbps)	0.030 (6.8 Mbps)	0.014 (27.2 Mbps)

† Includes TX and RX power. ‡ The output power is lower at 110 kbps due to lower pulse repetition frequency. It can be increased by configuring the PA FBB to a higher level.

Fig. 9.17 Measured performances compared to the IEEE 802.15.4 IR-UWB TX state of the art

Measured characteristics of the full TX (i.e., all blocks from Fig. 9.3) inside the SleepTalker SoC are summarized in Fig. 9.17 and compared to state-of-the-art IEEE 802.15.4 UWB transmitters. The output power and power consumption are reported for channel 3 (4.5 GHz) for three data rates. The low jitter resulting from the duty cycling of the LO within the BPPM time slot is compatible with a coherent receiver, recovering the bit coded in the pulse phase (BPSK modulation). The output power is −20 dBm for the highest data rates featuring a pulse repetition frequency (PRF) of 15.6 MHz and −26 dBm for the lowest data rates using a PRF of 3.9 MHz. It is limited by the asymmetric pulse shape coming from the strong NMOS/PMOS imbalance and could be overcome with a wider BBP range.

The TX power consumption is 100–380 μW as a function of the data rate. It leads to decent TX efficiency up to 5% despite the limited output power. The resulting energy per bit is lower at high data rates as the power consumption is amortized on more transmitted bits. The data rate to be selected depends on the used RX and of the target range as a lower data rate relies on a higher number of pulses per symbol, which increases the SNR at the RX side and thus mitigates path loss. achieved energy is excellent between 0.95 nJ/bit and 14 pJ/bit, which to the authors' knowledge is better than all the previously reported 802.15.4 UWB TX including the one from [21] in 22 nm FinFET CMOS.

9.8 Conclusions

In a range of IoT applications, the power consumption of smart sensors can be dominated by the wireless data transmission when the continuous data rate exceeds 100 kbps. This prevents energy-harvesting operation. In this chapter, we have shown through the design of an IR-UWB transmitter SoC that the exploitation of the unique wide-range back biasing capability of FD-SOI can also be used to significantly save power for RF circuits. The way we used the back biasing capability is the control of the carrier frequency and the output power with a body-biased-controlled oscillator and a digital PA, respectively. The BBCO allows to get rid of current-starving technique to control its frequency, which improves jitter at low power. Moreover, the BBCO features instantaneous startup, which can be used to aggressively duty cycle the frequency synthesis circuit of RF transceivers to further save power. The measured energy per bit reaches record values for 802.15.4 UWB communication, values between 950 and 14 pJ/bit depending on the selected data rate.

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