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Exploring and Suppressing Kink Effect of Black Phosphorus Field-Effect Transistors Operating in Saturation Regime

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With continuous device scaling, avalanche breakdown in the two-dimensional (2D) transistors severely degrades device output characteristics and overall reliability. It is highly desirable to understand the origin of such electrical breakdown for exploring the high-performance 2D transistors. Here, we report an anomalous increase in drain currents of the black phosphorus (BP)-based transistors operating in saturation regime. Through the comprehensive investigation of various channel thicknesses, channel lengths and operating temperatures, it is attributed such novel behavior to the kink effect originating from impact ionization and related potential shift inside the channel, which is further confirmed by device numerical simulations. Furthermore, Nitrogen plasma treatment is carried out to eliminate the current anomalous increase and suppress the kink effect with improved saturation current. This work not only sheds light on the understanding of carrier transport within the BP transistor, but also could open up new potential for achieving high-performance and reliable electronic devices based on the 2D materials.

Introduction

Two-dimensional (2D) layered semiconducting materials such as graphene,[1,2] MoS_2 and black phosphorus have been attracting extensive scientific interest,[3-6] owing to their atomic thickness, quantum confinement effects and the dangling bond free surface *etc*.[4,7,8] Among these 2D materials, black phosphorus (BP), in distinct contrast to the gapless nature of graphene and the relatively low mobility of MoS_2,[9] shows its unique thickness-dependent energy band gap (0.3-2.0 eV with decreasing thickness from the bulk to the monolayer)[10,11] and excellent electrical properties (high mobility of ~1,000 $cm^2 V^{-1} s^{-1}$)[12,13] and has been intensively explored for the applications in the high-performance electronic and optoelectronic devices, including photodiode or image sensor,[5,14] and GHz-frequency power amplifier,[15] flexible demodulator as well as the low-power tunneling field-effect transistors (FETs) based on the BP heterostructures.[16,17]

In the 2D FETs, the channel thickness is approaching its physical limitation, *i.e.* the atomic thickness. With respect to this issue, it is also crucial to understand the carrier transport mechanism and device physical properties with thickness scaling down. Especially, while the FETs are operating in the saturation regime, the channel can easily be exposed to a high electric field (*E*-field), which may result in the phenomena of the negative transconductance,[18] electrical breakdown, band to band tunneling (BTBT) and so on.[19,20] Anomalous current increase phenomena have been observed in various 2D-layered semiconducting devices, and greatly affect their applications in the next-generation electronics.[19-21] The pronounced 'kink' was discussed in a top-gated graphene field-effect transistor,[22] where a model was proposed by impact ionization inducing carrier generation in graphene at moderate *E*-field. Electrical breakdown phenomenon was observed in MoS_2-based FETs,[19] originating from the avalanche multiplication with different layer thicknesses and channel lengths while drain-source voltage larger than 40 V and the *E*-field on the level of MV cm^{-1}. Similarly, in the BP-based FETs, the device drain current has also been observed to exhibit an 'up-kick' in the saturation regime, which severely degrades the device reliability and limits their high-performance and low-power applications.[21,23] But neither detailed interpretation nor thorough understanding of the origin of the electrical breakdown in BP FETs has been explored, up to date.

To understand the in-depth physical mechanism and suppress the kink effect in the 2D-layered BP FETs, we comprehensively investigate the current 'up-kick' characteristics (kink effect) in the BP FETs operating in the

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† Electronic Supplementary Information (ESI) available: The transfer characteristic of the BP FETs with varied channel thicknesses (Fig. S1). Leakage current of the BP FETs (Fig. S2). The transfer and output characteristic curves of the BP FETs with 100 nm SiO2 as dielectric layer (Fig. S3). Transfer characteristic of the BP FETs with varied channel length (Fig. S4). Transfer characteristic of the BP FETs under different N_2 plasma treatment duration (Fig. S5). See DOI: 10.1039/x0xx00000x
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saturation regime, with varied BP flake thicknesses, channel lengths and operation temperatures. Device numerical simulations with SILVACO/Atlas are also performed to explore the effect of the device geometry on the potential distribution and current density inside the channel, demonstrating the corresponding transport mechanism. Lastly, nitrogen (N_2) plasma treatment is designed to suppress the kink effect and improve electrical performance of the BP FET.

Results and discussion

The BP FETs with varied channel thicknesses

Fig. 1a illustrates a schematic of the BP FET fabricated in this research (see the Methods section for details). Fig. 1b shows the output curves (*i.e.* drain-source current versus drain voltage, I_{DS}—V_{DS}) of the BP FETs probed in a vacuum condition of ~10^{-4} Torr, at room temperature (300 K) and gate bias V_{GS} of -5.0 V, with the corresponding transfer curves (*i.e.* drain-source current versus gate voltage, I_{DS}—V_{GS}) shown in the Fig. S1†. Gate leakage current (versus drain voltage, I_{GS}—V_{DS}) shown in the Fig. S2† remains on the level of 10^{-12} A, indicating there is no leakage current passing through the gate dielectric insulator in these devices. The threshold voltages V_{TH} of the BP FETs in Fig. 1b are -2.00, -0.83, -0.73 and 0.91 V respectively, increasing with the BP channel thickness. It can be clearly seen from Fig. 1b that the output currents I_{DS} of the BP FETs with ~5 and ~9 nm-thick channels reach their saturation plateau as -V_{DS} increasing above the saturation voltage V_{DSat}, featuring typical output characteristics of an idealized FET. However, an anomalous increase of the I_{DS} at higher -V_{DS} occurs in the BP FETs with ~11 and ~19 nm-thick channels (Fig. 1b, blue and red curves), which is often related to a 'kink' effect or an electrical breakdown when the device is operating in saturation regime. The detailed source-drain conductance (G_{DS}) is correspondingly shown in Fig. 1c the black dotted lines denote the values of the voltage $V_{D\text{-}Kink}$ where the current up-kick starts in the I_{DS}—V_{DS} curves.[24] The source-drain conductance calculated by the equation:

$$G_{DS} = \partial I_{DS} / \partial V_{DS} \tag{1}$$

where I_{DS} is the source-drain current, and V_{DS} is source-drain voltage. With thicker (~19 nm) channel, the 'kink' effect is more evident and prone to occur at lower -V_{DS}. In general, three possible mechanisms have been proposed for the current increase up-kick phenomena in the FETs: drain-induced barrier lowering (DIBL), BTBT and avalanche multiplication.[19,20,25] DIBL mainly occurs in the short-channel devices, where drain bias decreases the source barrier. Moreover, DIBL has a merely limited effect on the saturation drain current in the long-channel.[25] BTBT often occurs in non-overlapping local gate structure transistors, accompanied by a significant negative differential resistance.[26] Neither of these situations meet our experimental observations. Therefore, in this respect we believe that the anomalous current increase observed in the output characteristics of the BP FETs (Fig. 1(b and e)) is related to the avalanche multiplication induced by impact ionization. In addition, two conditions are required to induce kink effect in a FET, *i.e.* a high drain electric field (*E*-field) and a potential well/hill (for the holes/electrons, respectively) in the channel region.[27] They could be met in our devices as the output current 'up-kick' characteristics of the BP FETs are impacted by both the BP channel thickness (*i.e.* the potential distribution inside the channel under the back-gate biasing) and the drain voltage V_{DS} (as discussed in Fig. 1b). For further investigation of the kink effect, more details about the ~19 nm-thick BP FET are presented in Fig. 1(d-f). The scanning electron microscopy (SEM) and AFM images are shown in Fig. 1d. Fig 1(e and f) illustrate the I_{DS}—V_{DS} and the corresponding G_{DS} curves at various gate voltages V_{GS} ranging from 4.0 to -5.0 V. In Fig. 1e, the avalanche multiplication phenomena are obviously observed in the BP FET at various V_{GS}, once the V_{DS} goes beyond the saturation voltage V_{DSat}, *i.e.* in saturation regime. As the saturation voltage V_{DSat} is dependent on the V_{GS},[28] the $V_{D\text{-}Kink}$ (indicated as the black dashed line in Fig. 1f) is consequently impacted by the V_{GS} and decreases from -1.6 to -3.5 V as V_{GS} sweeping from 4.0 to -5.0 V. The V_{GS} modulates the carrier concentration inside the BP channel, and also affects the lateral *E*-field due to the electric field coupling between the drain and the back-gate electrodes. It is worth noting that the back-gated BP FET with a 100 nm-thick SiO_2 as the gate dielectric also shows weaker avalanche multiplication, which could be attributed to the degraded electrostatics of the device (Fig. S3 in the ESI†).[29] These results indicate that the current up-kick phenomena in the BP FETs are mainly related to the BP film thickness and the *E*-field inside the channel. Note that as it is known that BP is an anisotropic material, the electrical anisotropy may result in the varied carrier mobility in the BP FETs, but it is not a key factor while discussing the kink effect in this research.

Device numerical simulations of kink effect

Modeling approach based on an analytic Schottky barrier MOSFET has been explored to analyze the BP transistors,[30] with quantitative description and demonstration of the device transfer characteristics. In this work, to understand the insight mechanism of the kink effect regarding to the BP thickness and the drain and gate biases, we implement the two-dimensional (2D) back-gated BP FET into SILVACO/Atlas.[31] Based on the E_g dependence on the BP thickness, different channel thicknesses of 5, 10 and 20 nm are simulated for the BP FETs, and respectively set with energy band gap E_g of 0.63, 0.39 and 0.33 eV,[4,11,30,32,33] with fixed electron affinity of 4.10 eV.[32,33] Normally, the BP film is intrinsically *p*-type doped as the asymmetric ambipolar behavior was observed in the BP transistor.[34] Therefore, the hole *p* and electron *n* densities can be expressed and calculated by

$$p = n_{\mathrm{i}} e^{\frac{E_{\mathrm{i}} - E_F}{k_B T}} \tag{2}$$

$$n = n_{\mathrm{i}} e^{\frac{E_F - E_{\mathrm{i}}}{k_B T}} \tag{3}$$

where

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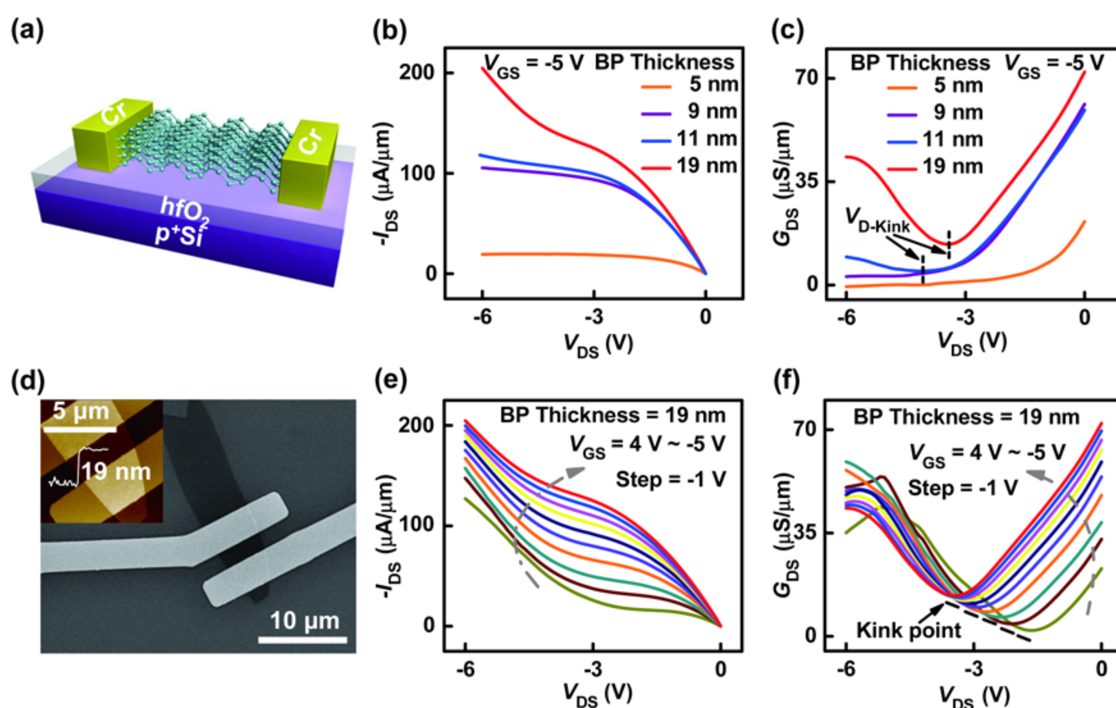

Fig. 1 Characterizations of the BP FETs with the varied thickness of the channel. (a) Schematic view of a back-gated BP FET. (b) Output curves (I_{DS}—V_{DS}) and (c) the corresponding source-drain conductance of the BP FETs at V_{GS} = -5.0 V, with different BP thicknesses of 5, 9, 11 and 19 nm and fixed channel length L of 3 μm. (d) SEM and AFM (the inset) images of the BP FET with 19 nm-thick channel. (e) Output curves (I_{DS}—V_{DS}) and (f) the corresponding source-drain conductance of the 3 μm-long BP FET with 19 nm-thick channel, as V_{GS} varies from 4.0 to -5.0 V and V_{DS} varies from 0 to -6.0 V.

$$n_i = 2.509 \times 10^{19} \left(\frac{m_e m_h}{m_0^2}\right)^{3/4} \left(\frac{T}{300}\right)^{3/2} e^{\frac{E_g}{2k_B T}} \quad (4)$$

is the intrinsic carrier density.[35] m_o is the mass of the free electron, E_g is the bandgap of BP, T is the temperature, and k_B is the Boltzmann constant. Other input parameters included in the model are the effective masses of electron and hole m_e^* = 0.15 and m_h^* = 0.14 from literature.[30] Considering the impact ionization process by using the local electric field model (Selberherr's impact ionization model),[31] electrical simulation results are presented in Fig. 2, where the Schottky contact is implemented into the source and drain contact, with a metal work function of 4.45 eV. The device I_{DS}—V_{DS} characteristics in Fig. 2a with the varied thicknesses of 5, 10 and 20 nm quantitatively fit the experimental observations (Fig. 1b), which demonstrates that the kink effect occurs to the BP FETs under a moderate lateral electric field (default value of > 4×10^5 V cm^{-1} in simulation) only when the channel is thick enough (10 and 20 nm in the simulations, ~11 and ~19 nm in the experiments). As depicted in Fig. 2b, the detailed vertical potential distributions at 0.25 μm distant from the source boundary is checked through the BP film with the different thicknesses, at fixed V_{GS} = -5.0 V and V_{DS} = -8.0 V (above the V_{DSat}), with and without impact ionization (II). The potential (e.g. without II) goes more negative for the reduced thickness owning to the back-gate vertical electrical field coupling with the film and hence the potential distribution. And a potential hill is obviously formed in the 10 and 20 nm-thick *p*-type channels, with the thickness increasing from 5 to 20 nm. Viewing the energy band diagram, the holes get accelerated with sufficient kinetic energy under the moderate *E*-field and generate new electron-hole pairs by impact ionization, thereafter the generated holes enter the valence band and are injected into the drain end, and the electrons enter the conduction band. Considering impact ionization process, at V_{GS} = -5.0 V and V_{DS} = -8.0 V in Fig. 2b, electron-hole pairs are generated at the drain end of the channel (with the highest generation rate).[19,36] The schematic view is depicted in inset to Fig. 2b. Holes generated by impact ionization will be immediately injected into the drain (negatively biased), and the generated electrons migrate towards the upper-part BP where the potential is higher and will be trapped if there is a potential hill between source and drain (in the BP FETs with the 10 and 20-nm thick channels).[27] The electrons accumulation provokes a decrease of the potential (*i.e.* the negative shift in Fig. 2b) to allow extra current flow from source to potential hill region in the channel. This decrease of the upper-channel potential is at the origin of the current up-kick in the device output characteristics, *i.e.* the kink effect as stated.[27] However, a potential increase is observed in the 5

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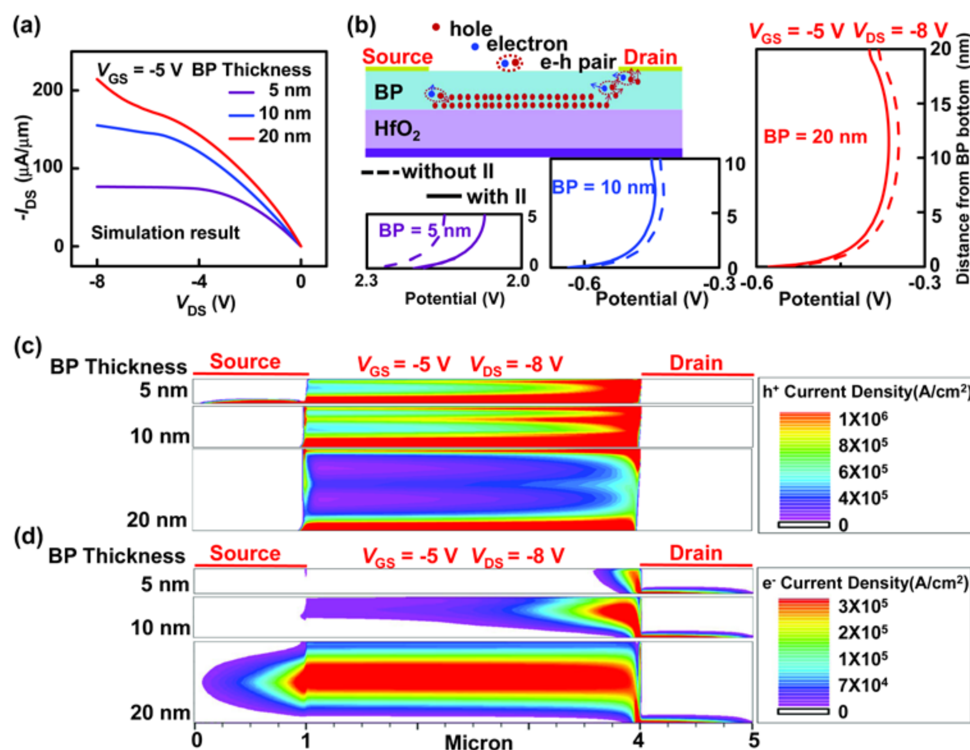

Fig. 2 Device numerical simulations of the kink effect in the BP FETs. (a) Output characteristics (I_{DS}—V_{DS}) of the 3 μm-long BP transistor with varied channel thicknesses of 5, 10 and 20 nm, under back-gate bias V_{GS} = -5.0 V, obtained in SILVACO/Atlas. (b) Potential distributions inside the BP channel, 0.25 μm distant from the source boundary at fixed V_{GS} = -5.0 V and varied V_{DS} = 0 and -8.0 V below and above the V_{DSat}, with and without impact ionization (II) (the inset depicts a schematic view of the impact ionization under moderate electrical field). (c) Hole and (d) Electron current densities inside the transistor channel with different BP thicknesses of 5, 10 and 20 nm, under V_{GS} = -5.0 V and V_{DS} = -8.0 V, obtained in SILVACO/Atlas.

nm-thick channel after impact ionization which indicates the increased holes current inside the channel resulting from the impact ionization, where no kink effect is observed due to the absence of the potential hill.

In order to analyze the current formation inside the BP channel and interpret how the kink effect occurs, we mainly present the electron and hole currents (in scalar) along the BP channel direction. Distributions of the hole- and electron-current concentrations at V_{GS} = -5.0 V and V_{DS} = -8.0 V are depicted in Fig. 2(c and d) respectively. It is clearly seen that in all cases, the device output currents are mainly contributed by the holes component in Fig. 2c, which is controlled by the back-gate bias and mostly located inside several nanometer distant from the channel/gate dielectric interface.[37] For the ultra-thin channel thickness below 10 nm, the carriers inside the FET channel are mostly the holes. In contrast, the electrons are swept away due to the dominant electrical control of the negative gate bias (*e.g.* V_{GS} = -5.0 V), leading to very negative potential inside the film.[27] While increasing channel thickness ≥ 10 nm, the potential hill starts to form in the upper part of the BP channel (Fig. 2b) regardless of the gate voltage, showing an almost quasi-neutral value at the mid-depth part.[27] In the device with channel thickness of 20 nm, the carriers' concentration in the upper part of the BP film can't be effectively modulated by the back-gate bias. Electrons generated by impact ionization while V_{DS} beyond the $V_{D\text{-}Kink}$ are mostly accumulated in the upper-part BP (the potential hill region Fig. 2(b and d)), which leads to the potential decrease and the formation of electrons current channel, and is responsible for the up-kick in the I_{DS}—V_{DS} characteristics. From the experimental and simulation observations, we conclude that this anomalous current increase is the kink effect induced by the impact ionization process under the moderate *E*-field and potential hill (for the electrons) formed in the channel region. We also note the electrons current formed inside the channel is at a lower concentration, indicating the dominance of the holes current. It is worth noting that in a top-gate configuration, the kink effect can be suppressed to some extent (explored via device simulations in SILVACO/Atlas). The 'up-kick' current is mitigated where the channel carrying the current is closer to the gate in the top-gate structure. However, in the experiments, the deposition of the top-gate dielectric HfO_2 will damage the BP surface as well as induce defects and disordered structure, in this work we therefore investigate the electrical properties of the bottom-gate device.

Kink effect in the BP FETs with varied channel lengths

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As the aggressive miniaturization of the field-effect transistors, the channel length is shrinking down to sub-micrometer regime. To further clarify impact of the channel scaling down on the kink effect, the 2D-layered BP FETs fabricated from same sheets of the mechanically exfoliated flake (thickness of ~20 nm) with various channel lengths *L* = 0.3, 3.0 and 10.0 µm are investigated. An optical view of the fabricated devices is shown in Fig. 3a, and the device output characteristics with different *L* are separately presented in Fig. 3(b-d). In the long channel, as the *L* is much larger than the length of the electron mean free path, the FET is mainly operated in the diffusive regime.[38] The I_{on} current and the transconductance ($\partial I_{DS}/\partial V_{GS}$) increase with the decreasing channel length, which is inversely proportional to *L*. Carrier mobility μ_{FET} is calculated by the equation:

$$\mu_{FET} = \frac{d(I_{DS})\cdot \mathrm{L}}{d(V_{GS})\cdot W\cdot V_{DS}\cdot C_{ox}} \quad (5)$$

where *W* is the device width, C_{ox} is the oxide capacitance. The μ_{FET} is 180.0 $cm^2\ V^{-1}\ s^{-1}$ and 185.0 $cm^2\ V^{-1}\ s^{-1}$ at *L* = 3 and 10 µm respectively, and decreases to 50.7 $cm^2\ V^{-1}\ s^{-1}$ while *L* scaling down to 0.3 µm, extracted from the I_{DS}—V_{GS} curves in the Fig. S4(a)†. From Fig. S4† we can see the I_{DS}—V_{GS} curves at V_{DS} = -1.0 and -0.1 V, as the applied V_{DS} gets more negative in the Schottky barrier MOSFET, the barrier on the drain side becomes lower, thereafter leading to the higher OFF current at V_{DS} = -1.0 V.[30] Usually, the mobility would remain constant.[38] However, at the short channel (Fig. 3d) the carrier velocity (equal to $\mu_{FET}\times E$) is getting saturated with the increased *E*-field, resulting in the decrease of μ_{FET}. With the *L* reduced from 10 to 0.3 µm, the V_{DSat} also decreases due to the enhanced *E*-field (the *E*-field is inversely proportional to the channel length), which leads to the kink effect is prone to occur at lower -V_{DS}, *i.e.* impact ionization occurs at smaller -V_{DS}. At V_{GS} = -5.0 V, the values of the $V_{D\text{-}Kink}$ and the average electrical field (E_{AR}, equal to $V_{D\text{-}Kink}/L$) are extracted in Fig. 3e. It can be seen that the $V_{D\text{-}Kink}$ changes from -4.8 to -1.4 V with the *L* decreasing from 10 to 0.3 µm, and shows a nonlinear relationship to the channel length. With the channel length shrunk down to sub-micrometer region (0.3 µm), the kink effect occurs at higher E_{AR} because the carrier velocity tends to be saturated. In this case, the short-channel device gets more difficult to operate in the saturation regime. The mobility of 50.7 $cm^2\ V^{-1}\ s^{-1}$ extracted in the BP transistor with the 0.3 µm-long channel also confirms the existence of the high *E*-field. However, the E_{AR} values in Fig. 3e are much lower than the critical electric fields in MoS_2 (on the level of MV cm^{-1}).[19] indicating it is not lateral avalanche breakdown in these BP FETs. Qualitative demonstration of the device modeling is illustrated in Fig. 3f, with the $V_{D\text{-}Kink}$ increasing from -6.6 to -4.4 V obtained in SILVACO/Atlas. The higher values of -$V_{D\text{-}Kink}$ and E_{AR} in simulations could be related to the idealized material properties considered in the modeling (*i.e.* merely a bulk defect density of 10^{20} $cm^{-3}eV^{-1}$ is considered in the BP top surface with 1 nm depth, without any other defect or charge). This is may also related to the impact ionization parameters which are not calibrated for the BP FETs in this research.

Temperature impact on the kink effect

To further explore the kink effect in the BP FETs, different

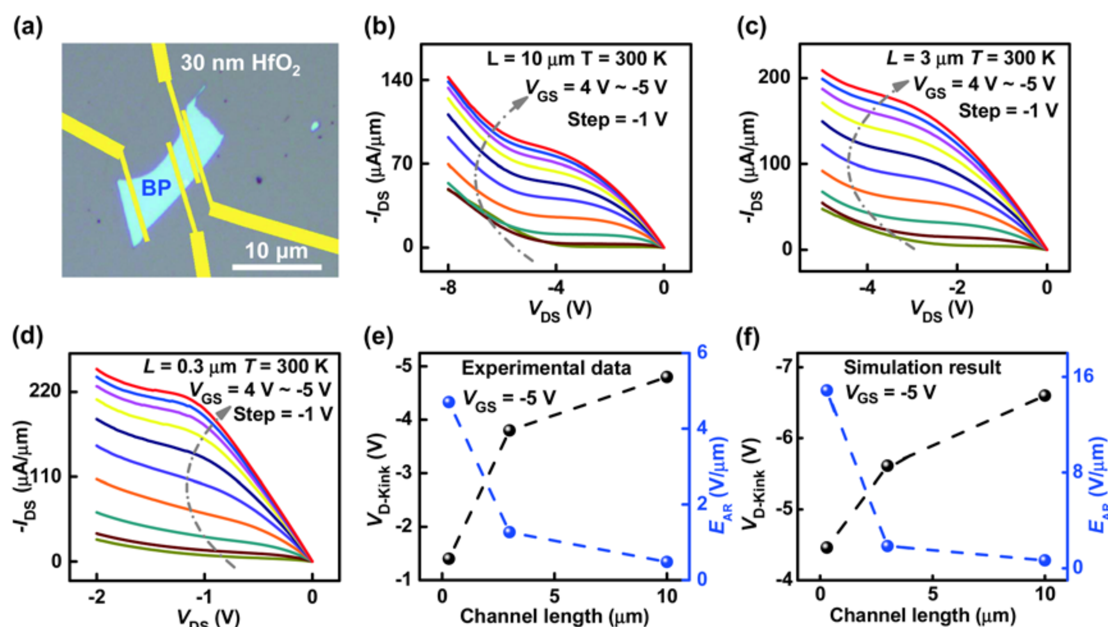

Fig. 3 The BP FETs with varied channel lengths. (a) Optical view of the BP FETs with 0.3, 3 and 10 µm channel lengths. Output curves (I_{DS}—V_{DS}) of the BP transistors with various channel lengths *L* of: (b) 10 µm, (c) 3 µm, (d) 0.3 µm. The $V_{D\text{-}Kink}$ and E_{AR} values versus the channel length of the BP FETs in (e) experiments and (f) simulations.

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device operating temperatures are considered. Lowering temperature can reduce the scattering and therefore improve electrical carrier mobility.[39-41] Electrical measurements at 11 and 300 K are carried out in the BP FET with L of 3 μm and channel thickness of ~20 nm to investigate the temperature impact on the kink effect. Fig. 4a depicts the representative transfer curves (I_{DS}—V_{GS}) of the BP FET, where the device demonstrates the pronounced ambipolar behavior with an enhanced *p*-type drain current and thereafter a moderate *n*-type drain current as the V_{GS} goes from the negative to positive bias. A higher on/off ratio is achieved in the BP FET operating at 11 K than that at 300 K, thanks to the increased on-current and reduced off-current at 11 K. The reduced scattering effect and the frozen trap charges at lower temperature of 11 K results in the increased carrier mobility μ_{FET} , *i.e.* a maximum of 206.8 cm^2 V^{-1} s^{-1} improved by a factor of about 2 as comparing to the μ_{FET} at 300 K. Moreover, the anomalous dependence of the E_g on temperature was observed in the 2D-layered BP, where the E_g decreases with the reduction of temperature.[42,43] Such temperature dependent E_g can result in higher holes concentration around the BP bottom surface and also the lowering source-channel barrier (-0.170 V at 11 K, -0.185 V at 300 K). In the on-state, carriers can easily tunnel across the Schottky barrier at the contacts and charge transport is mainly limited by scattering in the channel,[41] which can explain the increased on-current I_{on} of the BP FET operated at 11 K comparing to the I_{on} at 300 K in Fig. 4b. The off-current I_{off} is mainly determined by thermal emission through the Schottky barrier at the source/drain Schottky contacts and also related to the n_i which decreases

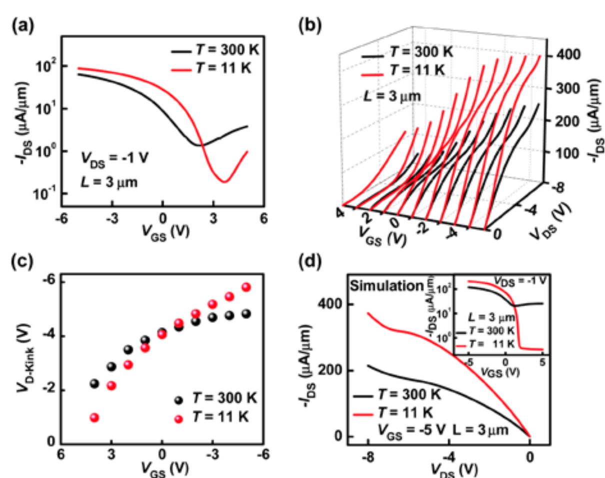

Fig. 4 The BP FETs operating at 300 K and 11 K. (a) Device transfer characteristics (I_{DS}—V_{GS}). (b) Output currents I_{DS} as a function of the V_{GS} and V_{DS}. (c) The extracted $V_{D\text{-}Kink}$ values versus V_{GS} in the BP transistor with channel length = 3 μm and BP thickness = 20 nm, at temperatures of 300 K and 11 K. (d) Simulated output and transfer characteristics of the BP FET at operating temperatures of 300 K and 11 K.

with temperature,[44] and is hence decreased with temperature lowering. The positive shift in the I_{DS}—V_{GS} characteristics from operating temperature of 300 K to 11 K,[28,35] affects the $V_{D\text{-}Kink}$ value due to the dependence of the V_{DSat} on the V_{GS}.[45] The $V_{D\text{-}Kink}$ values at 300 and 11 K are extracted in Fig. 4c, as a function of the V_{GS}. The $V_{D\text{-}Kink}$ at 300 K (resp. 11 K) varies from -2.24 to -4.83 V (resp. -0.98 to -5.81 V) while the V_{GS} is ranging from 4.0 to -5.0 V. As indicated in Fig. 4a, the flat band voltage V_0 (the minimum current point in the I_{DS}—V_{GS} curve) of the BP FET is 2.0 V at 300 K and 3.5 V at 11 K, therefore we mainly discuss the $V_{D\text{-}Kink}$ of Fig. 4c while $V_{GS} \leq 1.0$ V (300 K) and 3.0 V (11 K), *i.e.* when the BP FET works as a *p*-type FET. The $V_{D\text{-}Kink}$ in the BP FET presents a recognizably enhanced dependence on the V_{GS} at 11 K compared to 300 K, which can be relevant to the decreased scattering effect and the frozen trap charges and therefore the increased carrier mobility at 11 K.[44] The impact ionization are obviously observed in the BP FET at various V_{GS}, once the V_{DS} goes beyond the saturation voltage (V_{DSat}). Since the V_{DSat} is dependent on the V_{GS},[28] the $V_{D\text{-}Kink}$ is consequently impacted. At low temperatures, scattering effect and trap charges is also reduced, the gate modulates device is more effective (i.e. higher ON/OFF ratio) as well as the obvious dependence of V_{DSat} on V_{GS}. An improved $V_{D\text{-}kink}$ dependence on V_{GS} at the low temperature (11 K) is observed in the SILVACO/Atlas simulations, with the trap implementation as described before. Enhancement in the device mobility and current also confirms the reduced scattering from both traps and phonons at the low temperature.[45] With respect to these issues, device operating at 300 K suffers more scattering and trap effect hence the $V_{D\text{-}Kink}$ features less dependence on the V_{GS}. Device output characteristics under different temperatures are simulated and depicted in Fig. 4d, in the BP FET with 20 nm-thick and 3 μm-long channel. Considering the anomalous energy band gap (varying from 0.33 to 0.26 eV while temperature decreasing from 300 to 11 K),[42] the improved output current of 374 μA μm^{-1} at 11 K (in comparison to 214 μA μm^{-1} at 300 K) at V_{DS} of -8.0 V, validates the above physical interpretation and further demonstrates the enhanced impact ionization at lower temperature.

Doping implementation to suppress the kink effect

The kink effect leads to device instability and high-power consumption, which limits the applications of the BP FETs in next-generation low-power electronics. Based on the aforementioned comprehensive understanding and physical mechanism of the kink effect in the BP FETs, blocking-up the formation of the potential hill for the electrons (in Fig. 2b) as well as of the electrons aggregation in the channel (Fig. 2d) could be effective to eliminate the anomalous current increase and suppress the kink effect (Fig. 1 and 2). Chemical doping (via plasma treatment) is a straightforward and feasible approach to modulate the carrier concentration inside the BP FET.[46,47] Nitrogen (N_2) plasma treatment (as shown in Fig. 5a) is proposed and carried out in this research to modulate the carrier distribution inside the BP channel. Fig. 5b presents the foresighted simulation results in the BP FET (with 20 nm-thick and 3 μm-long channel), with different concentrations of the

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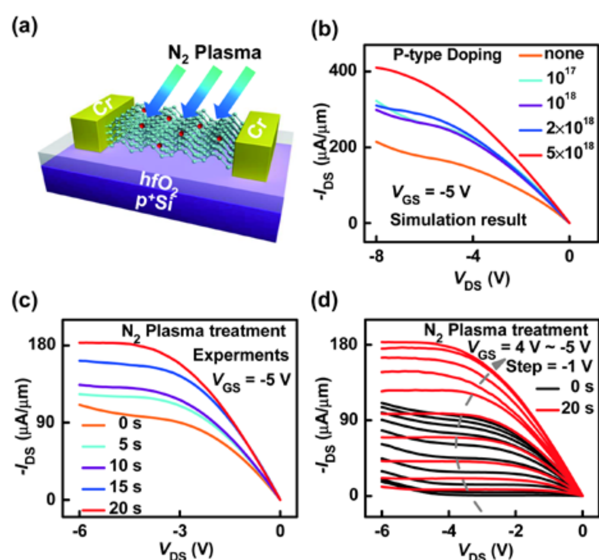

Fig. 5 Doping effect on the output characteristics of the BP FET. (a) Schematic view of N_2 plasma treatment to the BP FET. (b) Effect of one *p*-type doping on the output curves of the BP transistor in SILVACO/Atlas. (c) Output characteristics of the BP FET under different N_2 plasma treatment duration at V_{GS} = -5.0 V. (d) Output characteristics of the BP FET without and with N_2 plasma treatment of 20 seconds duration, with the V_{GS} ranging from 4.0 to -5.0 V

p-type doping inside the channel, *e.g.* 1×10^{17}, 1×10^{18}, 2×10^{18} and 5×10^{18} cm^{-3}. With increasing the *p*-type doping concentration, the kink effect in the BP FET starts to be decreased, then the kink effect is effectively suppressed by a doping concentration of ≥ 2×10^{18} cm^{-3}. Beside the greatly suppressed kink effect, the device output currents I_{DS} (Fig. 5b) can also be largely enhanced, owing to the increased *p*-type carriers concentration inside the channel. Source-channel barrier extracted in the BP FETs with different doping concentration, are almost the same with un-doped case, *i.e.* -0.185 V at 300 K. Under a *p*-type doping concentration of 2×10^{18} cm^{-3} where the kink effect is suppressed in Fig. 5b, the height of the potential hill has been observed with -0.017 V increment comparing to the case of the un-doped BP. This decrease in the potential hill inside the upper-part BP channel results in that no potential shift is observed in the BP FETs (with doping level of 2×10^{18} cm^{-3}) after the impact ionization, *i.e.* no electron accumulation inside the BP upper-channel, which originates the kink in the device output current. The p-type doping technique is also feasible in the short-channel devices (0.3 μm). However, the kink effect can be suppressed with an increased *p*-type doping concentration (>5×10^{18} cm^{-3}), which is not as effective as in the relatively long-channel case due to the short-channel effect somehow. Based on the mechanism prediction in simulations, the experimental device output characteristics (I_{DS}—V_{DS}) at V_{GS} = -5.0 V with different N_2 plasma treatment durations: 5, 10, 15 and 20 seconds are shown in Fig. 5c, with the corresponding transfer curves (I_{DS}—V_{GS}) at V_{DS} = -1.0 V depicted in the Fig. S5†. As the positive charges are introduced during the N_2 plasma treatment, the intrinsic carrier concentration is increased in the BP transistor after the treatment, which leads to a slight increase in the OFF-state current of the BP transistors. After treating the BP FETs with the 5 and 10 seconds, the output currents feature in a decreased trend of 'up-kick' kink currents in saturation region. With the 20 second-duration N_2 plasma treatment, the kink effect is completely eliminated and the device is recovered to normal output characteristics as the standardized FET in Fig. 5c. By using atomic force microscopy, the thickness of the BP flake is also measured, where the BP flake is almost not etched by the plasma treatment, e.g., with the thickness of 18.4 nm (before) and 18.2 nm (after the 20 second-duration N_2 plasma treatment). Therefore, it indicates that the suppressed 'up-kick' current is not related to the decreased channel thickness while implementing the N_2 plasma treatment to the BP transistor. In the experiments, the device saturation current I_{DSat} is also observed to increase with increasing the plasma treatment duration in Fig. 5d, as well as the improved device stability where the device still features in current saturation characteristics while the V_{DS} reaching -6.0 V. Such good agreement achieved between the experimental observations and the simulation results, reveals that the N can act as an acceptor and introduce positive charges into the BP channel. Furthermore, this technique shows a promising direction to suppress the kink effect in 2D-layered transistor and improve the device high-performance, low-power and reliable applications.

Conclusions

In summary, the kink effect of the 2D-layered BP FETs was systematically investigated by fabricating the BP transistors with various thicknesses, channel lengths, as well as operating temperatures. From the detailed analysis of the thickness-dependent output characteristics, we conclude that the anomalous current increase (kink effect) in the BP FETs (with 11, 19, 20 nm-thick channel) is induced by the impact ionization under the moderate electric field. Furthermore, N_2 plasma treatment has been designed in this research as one *p*-type doping technique to suppress the kink effect and improve device electrical performances, by decreasing the potential hill and blocking up the electrons accumulation inside the BP channel. Quantitative and qualitative agreement between the experimental observations and the simulation results (from SILVACO/Atlas) demonstrates the physical mechanism of the kink effect. This work provides in-sight physical investigation and experimental techniques to comprehensively explore the lower-power and more reliable applications of the high-performance BP transistor, as well other 2D FETs in general.

Methods

Experimental Fabrication of the BP FETs

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Firstly, a 30 nm thick HfO_2 layer was grown onto a heavily p-doped silicon substrate by atomic layer deposition using KE-MICRO TALD-200A system at temperature of 95 °C. The BP flakes were exfoliated from bulk BP crystals (Smart-element) and transferred onto a heavily *p*-doped silicon substrate with 30 nm HfO_2 dielectric. Then the substrates are immediately spin coated with methyl methacrylate (MMA) and polymethyl methacrylate (PMMA), the electron beam lithography (JEOL 6510 with NPGS) was employed to define the source/drain patterns and 15/50 nm thick Cr/Au film was deposited by thermal evaporator followed by lift off process to form source and drain electrodes. N_2 plasma treatment is employed with power of 10W under 10 Pa pressure.

Electrical Measurements.

Electrical characterizations were conducted by using the Lake Shore TTPX Probe Station and Agilent B1500A semiconductor parameter analyzer under vacuum environment. The thickness of BP FETs was measured by atomic force microscopy (Bruker Multimode 8).

Conflicts of interest

There are no conflicts to declare

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