Substrate RF Non-Linear Characterization and Modeling

Dr. Martin Rack

Université catholique de Louvain, Belgium UCLouvain

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Outline

Introduction / Context / Motivation

- Why linearity?
- Substrates for RF

Physics of RF substrates

- Charge Balance
- Trap Passivation
- Dynamic Effects (finite time constants)

Modelling (CPW lines)

TCAD + T-line theory

- Instantaneous substrate impedance
- Correlation to measurements

Modelling of arbitrary layouts

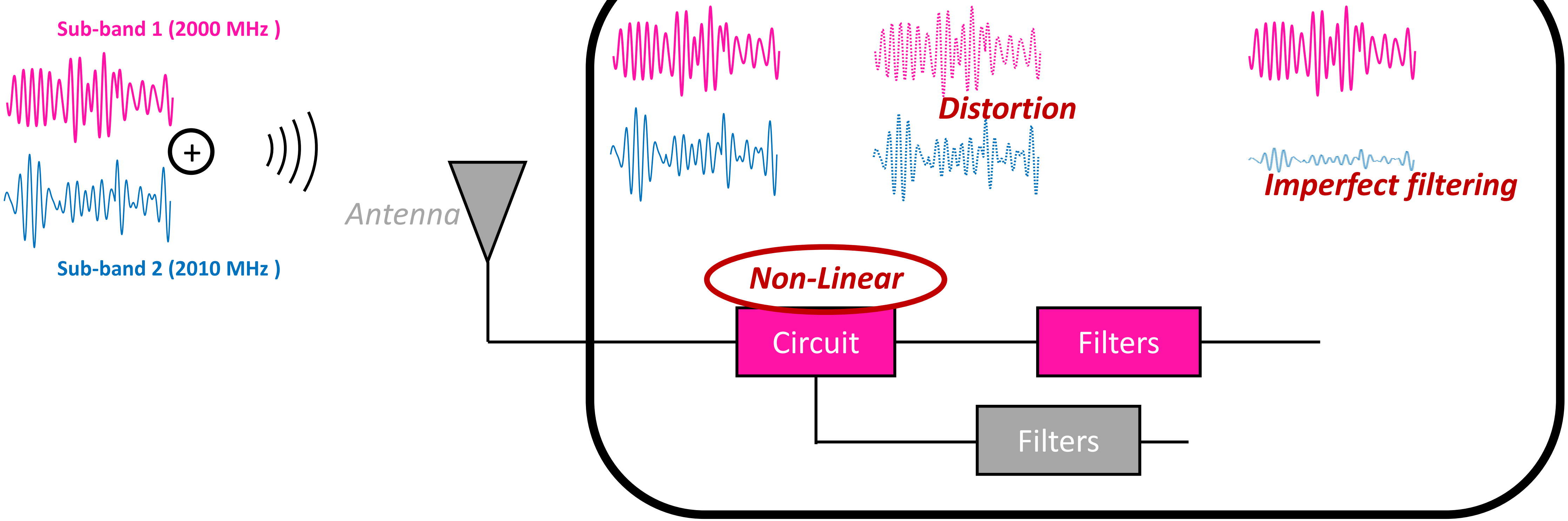
TCAD + EM simulations

- Approach and initial results

Introduction / Context / Motivation

- Non-linearity Recap
- Substrate Requirements at RF

Signal Distortion / System Linearity



Non-linearity = spectral “smearing”.

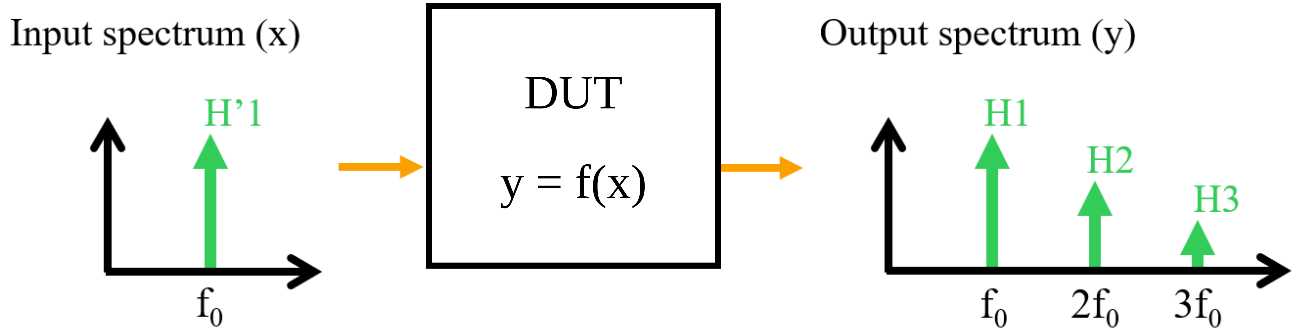
⇒ adjacent band spectral contamination

⇒ Ever more stringent **<u>linearity</u>** specifications for FEMs

Network	Linearity IIP3 [dBm]
2G	55
3G	65
4G LTE	72
4G LTE + CA	Up to 90

Linearity Requirements by Network Standard

Substrate Requirements for RF



Ideal linear transfer function: $y = f(x) = a \cdot x$

Real non-linear transfer function: $y = f(x) = a \cdot x + b \cdot x^2 + c \cdot x^3 + \dots$

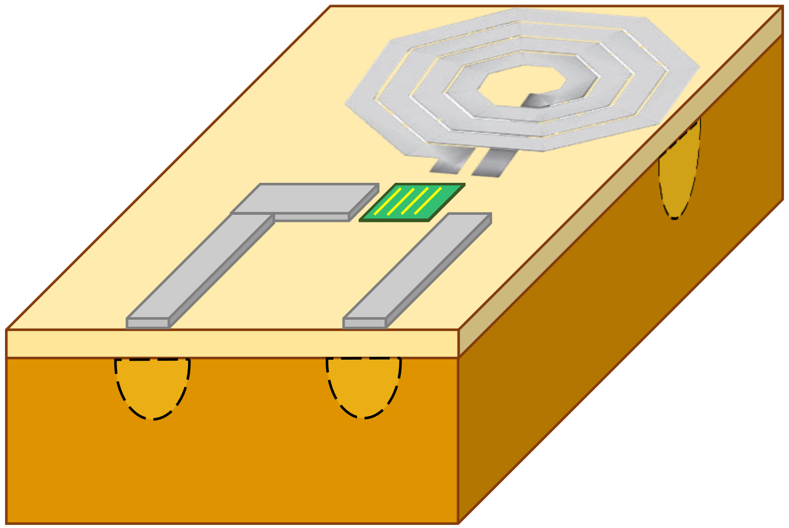
Substrate FoMs:

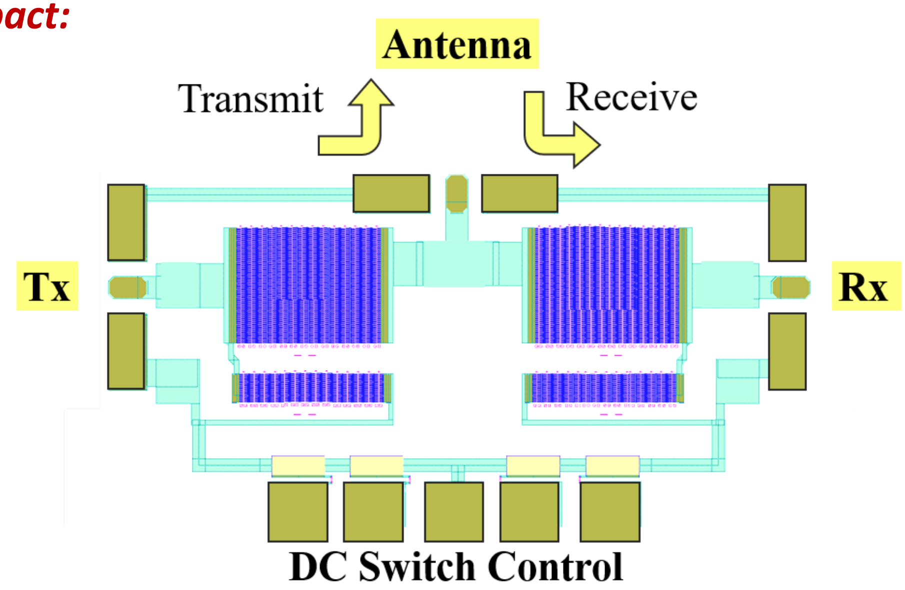
- Losses / coupling / ρ_{eff}

  (TCAD+EM non-uniform material stack)

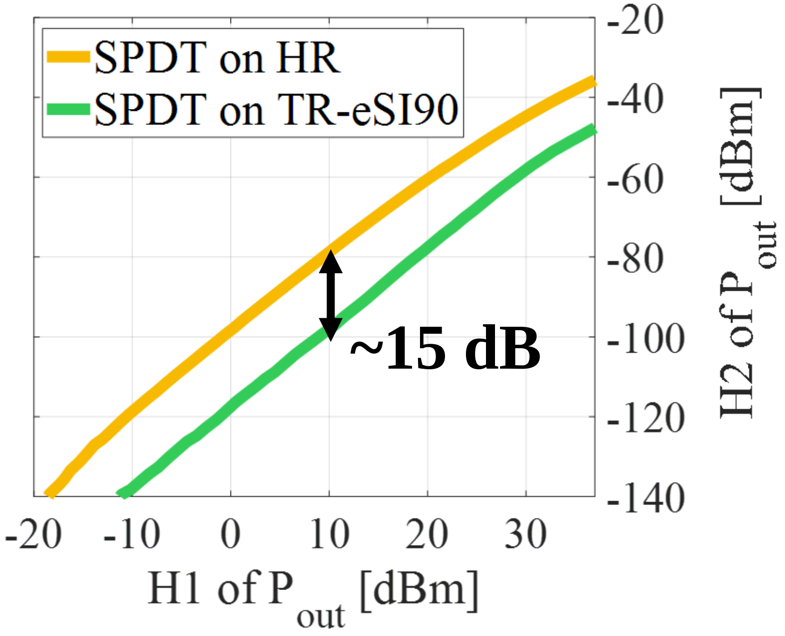
- **Linearity / HD** → ***talk's focus***

Example of substrate impact:





$$f_0 = 900\ MHz$$



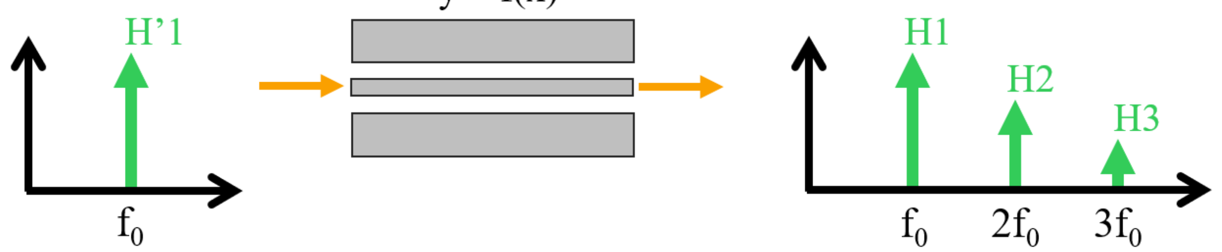
Substrate Requirements for RF

Standard-Si ***vs.*** *High-Res.* ***vs.*** *Trap-Rich*

Substrate FoMs:

- Losses / coupling / ρ_{eff}

  (TCAD+EM non-uniform material stack)

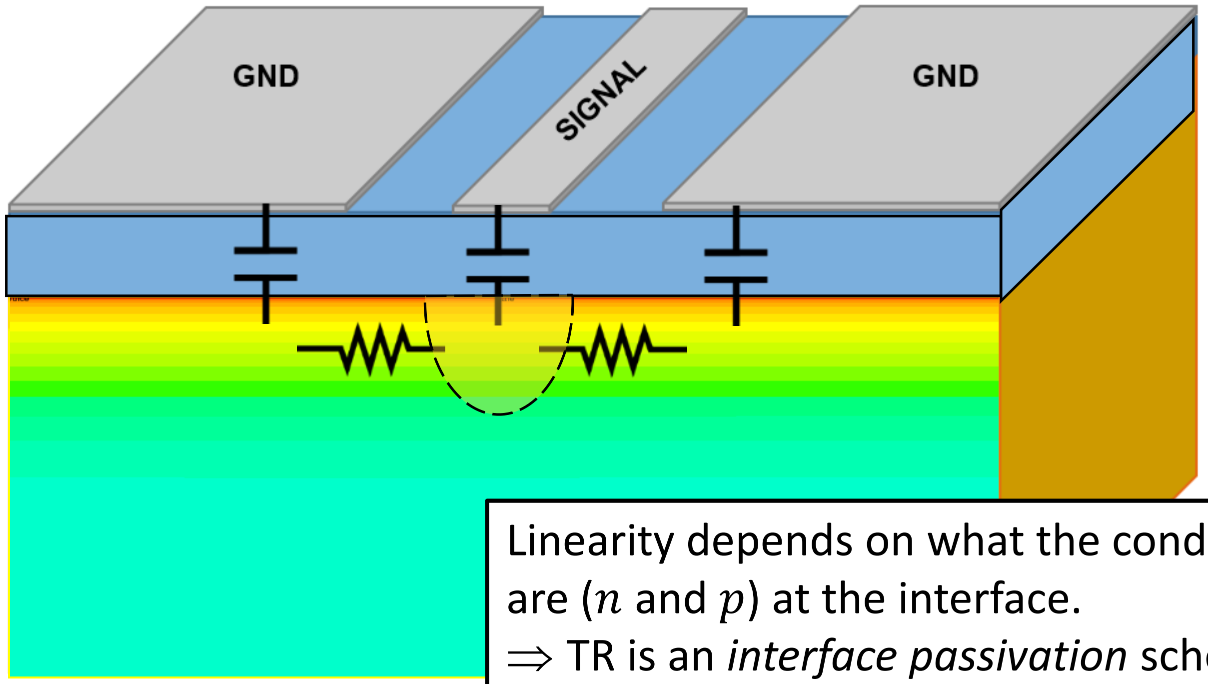


Ideal linear transfer function: $y = f(x) = a \cdot x$

Real non-linear transfer function: $y = f(x) = a \cdot x + b \cdot x^2 + c \cdot x^3 + \ldots$

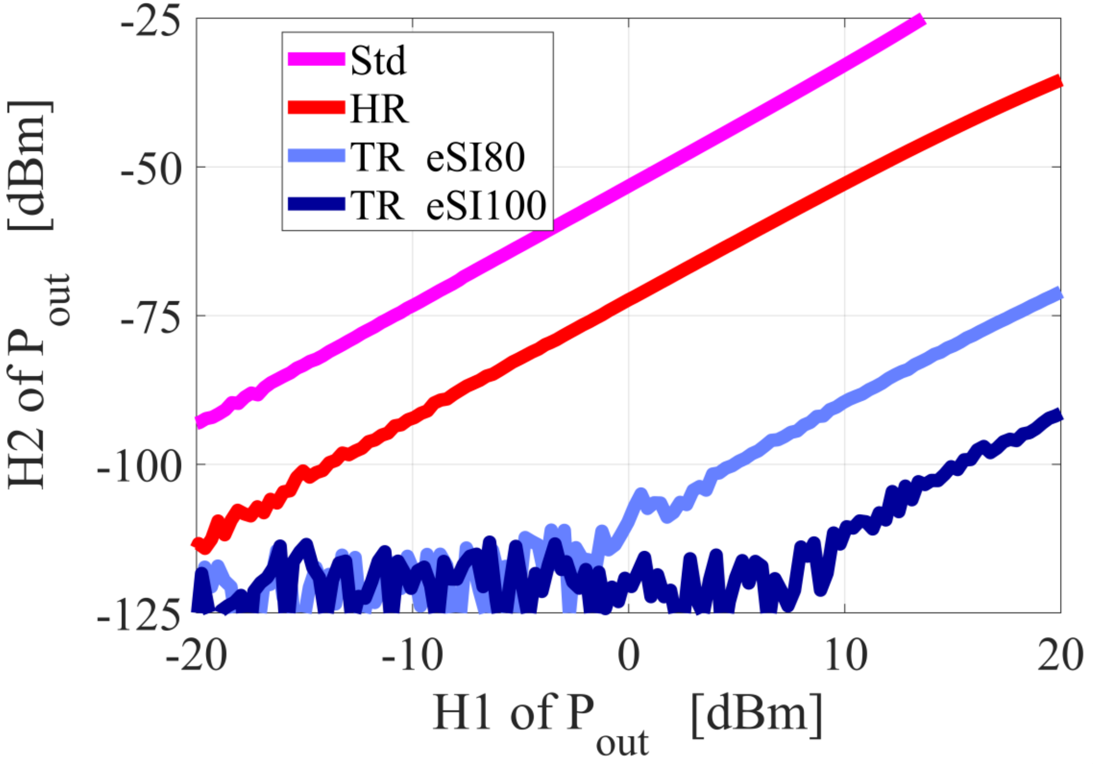
- **Linearity / HD**

Semiconductors are non-linear by nature (field-effect).

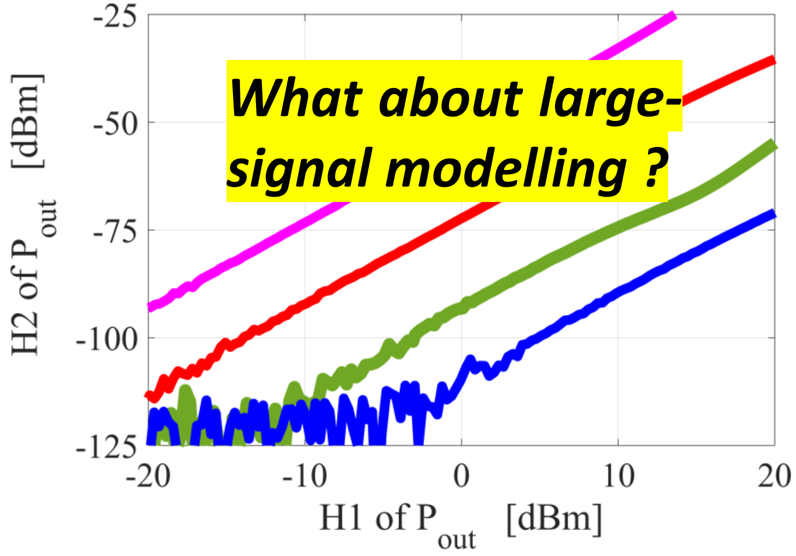


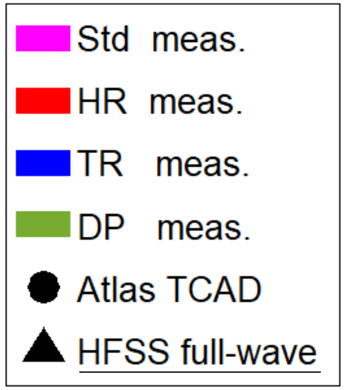
Linearity depends on what the conditions are (n and p) at the interface.
$\Rightarrow$ TR is an *interface passivation* scheme.

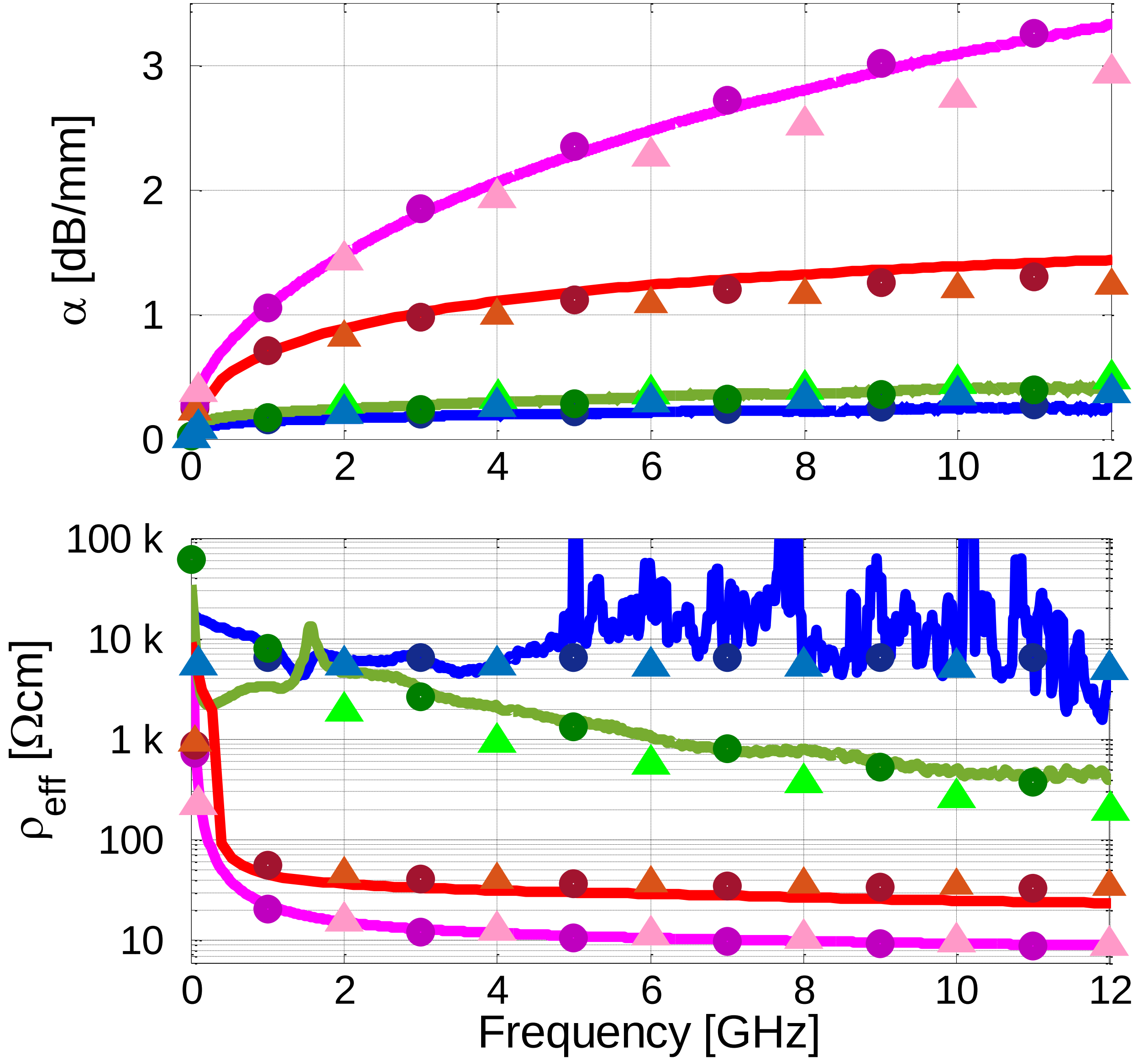
$$f_0 = 900\ MHz$$

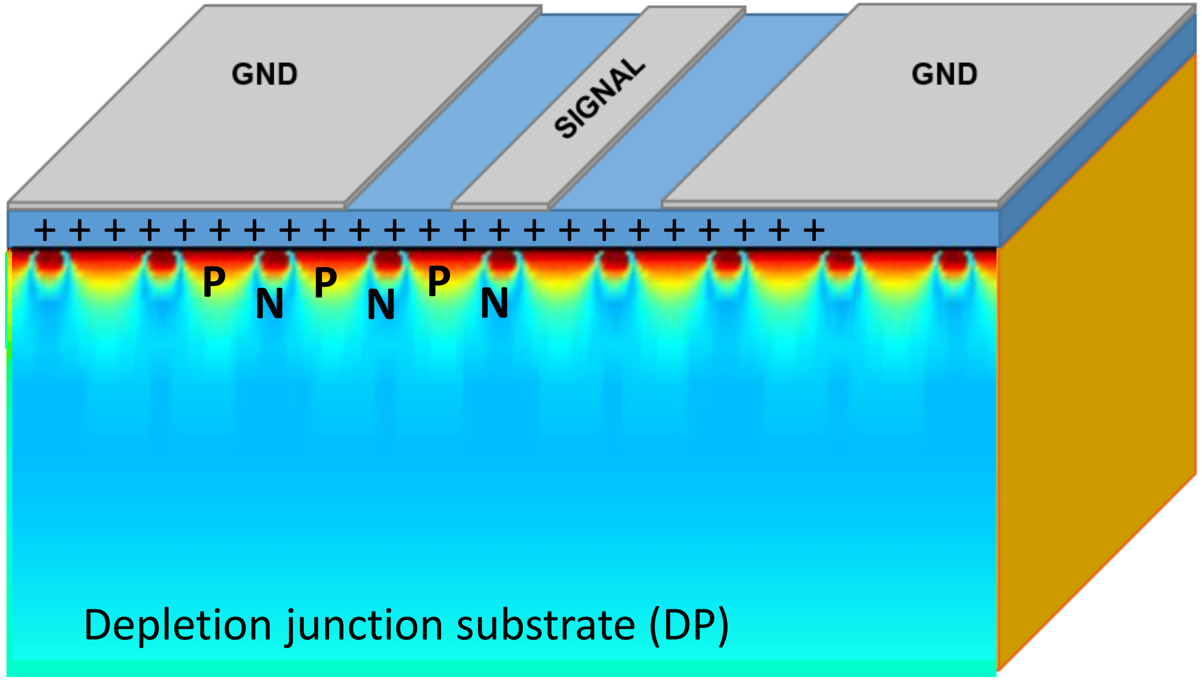


Substrate Requirements for RF





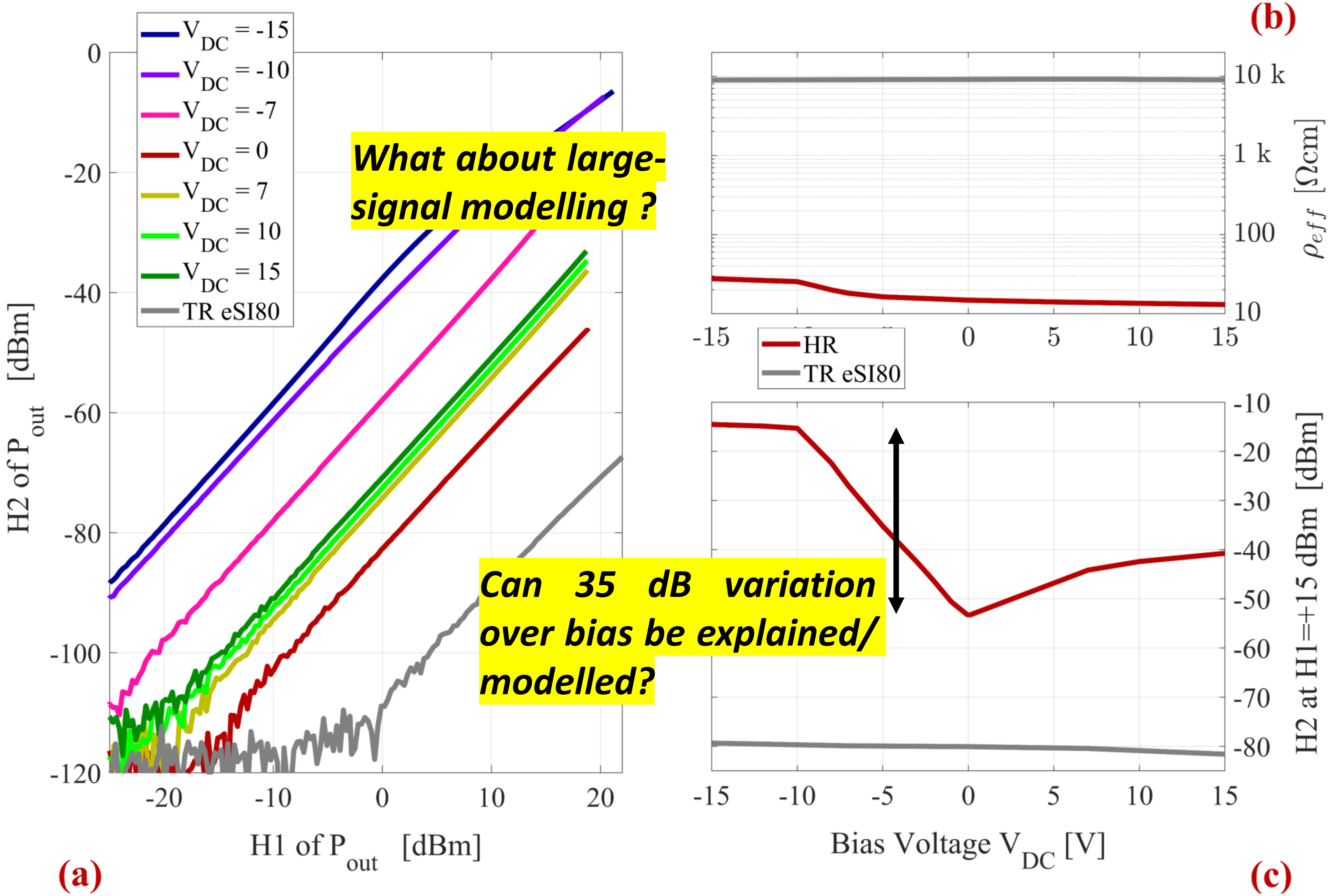




EM + TCAD can be combined to simulate a range of RF passives on highly non-uniform Si-based substrates.

⇒ ***Small-signal modelling OK !***

Substrate RF FoMs plotted vs bias



What about large-signal modelling ?

Can 35 dB variation over bias be explained/ modelled?

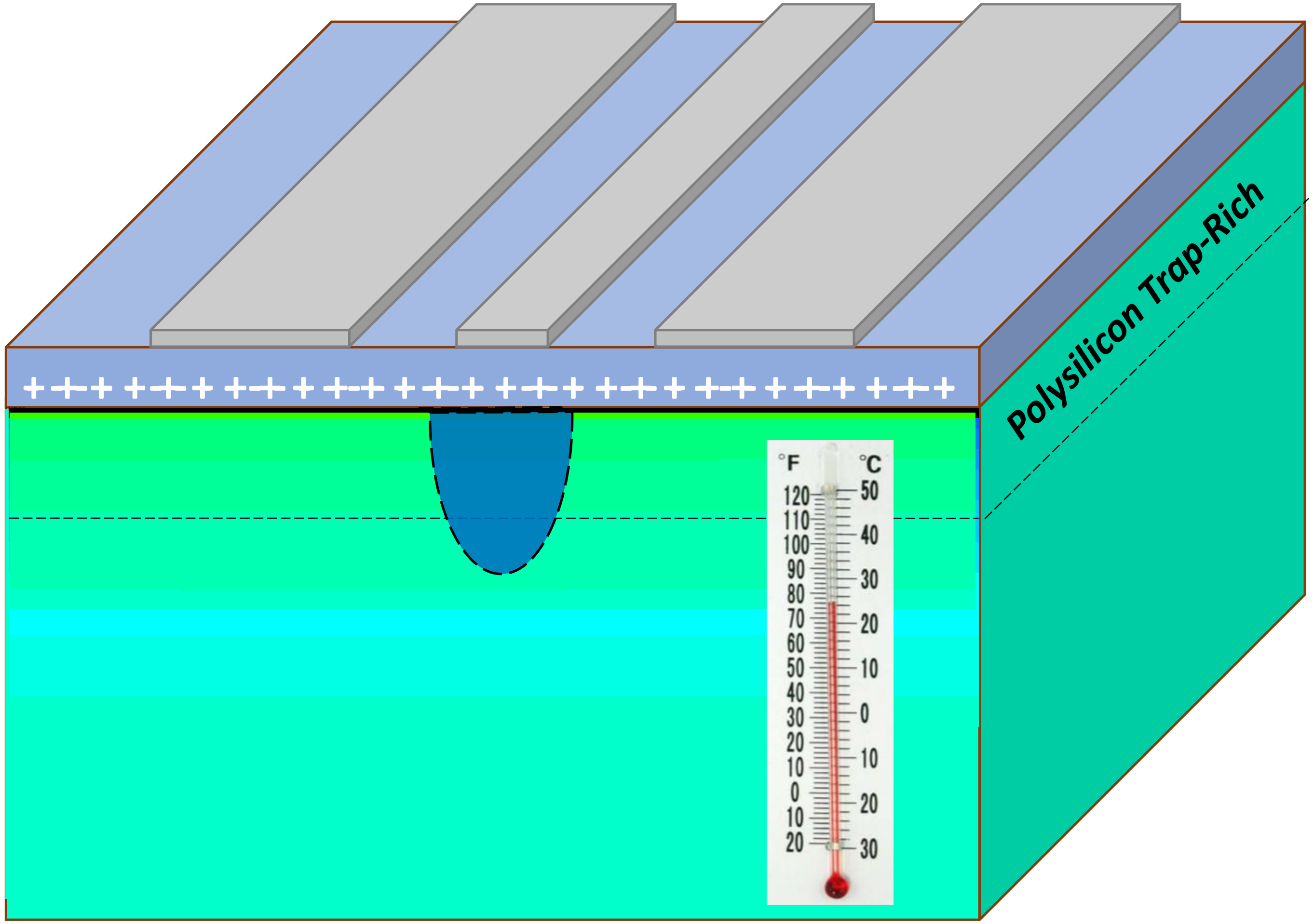
Answer: Yes !

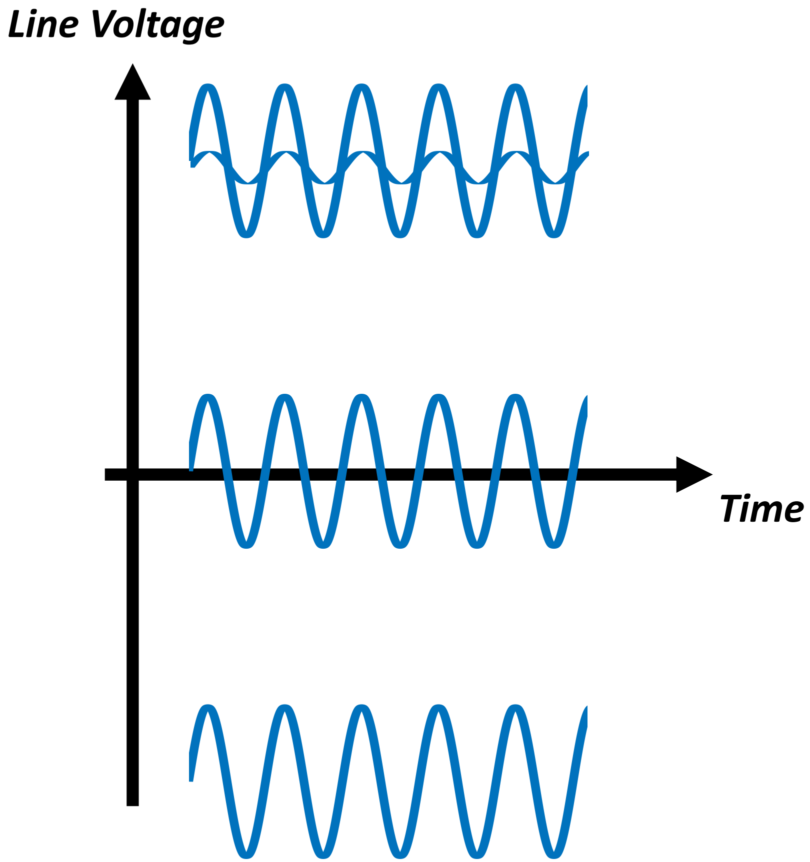
→ Model of in this presentation validated over many parameters.

Full References:

- *Modeling of Semiconductor Substrates for RF Applications: Part I - Static and Dynamic Physics of Carriers and Traps,* doi: 10.1109/TED.2021.3096777.
- *Modeling of Semiconductor Substrates for RF Applications: Part II - Parameter Impact on Harmonic Distortion,*doi: 10.1109/TED.2021.3096781.

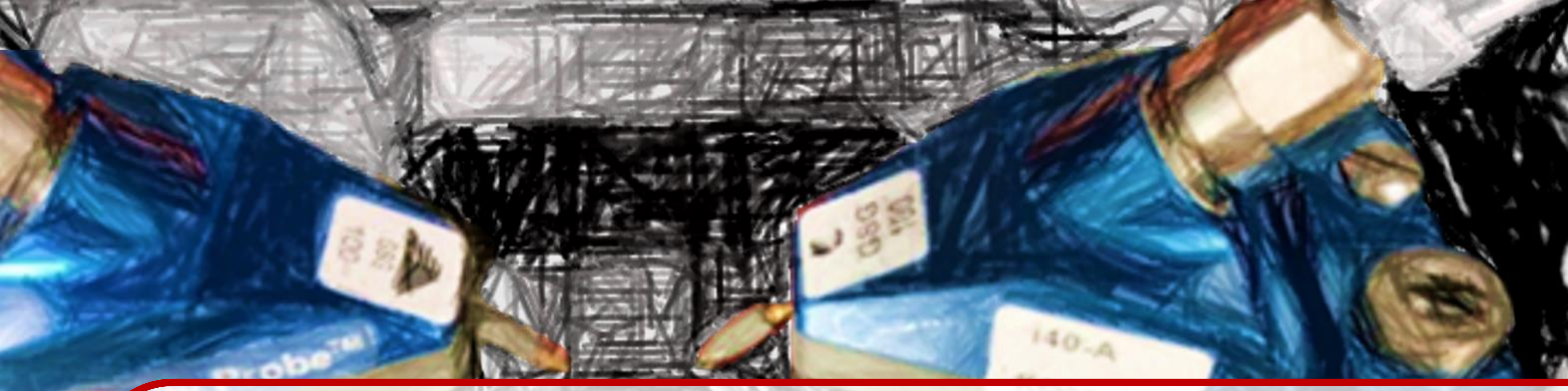
- Amplitude RF
- Point DC
- Fixed interface charge
- Interface traps and *trap-rich* passivation
- Dimensions of CPW
- Frequency
- Temperature





Motivation and Objectives of a Large-Signal Substrate Model

- Can we predict HD of a given material stack?
- How to model, taking into account all semiconductor effects
- Gain physical insight into parameter impact (future substrate developments, IC design, etc.)

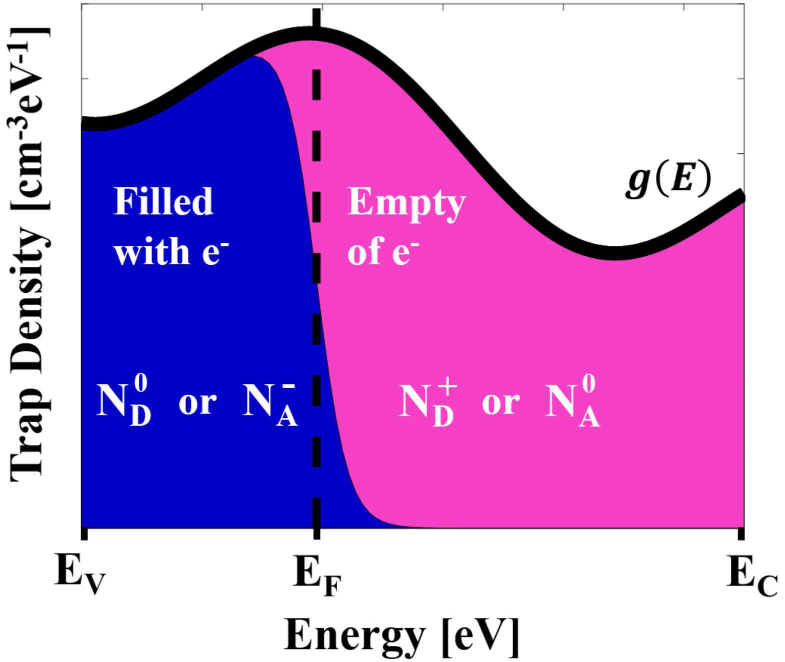


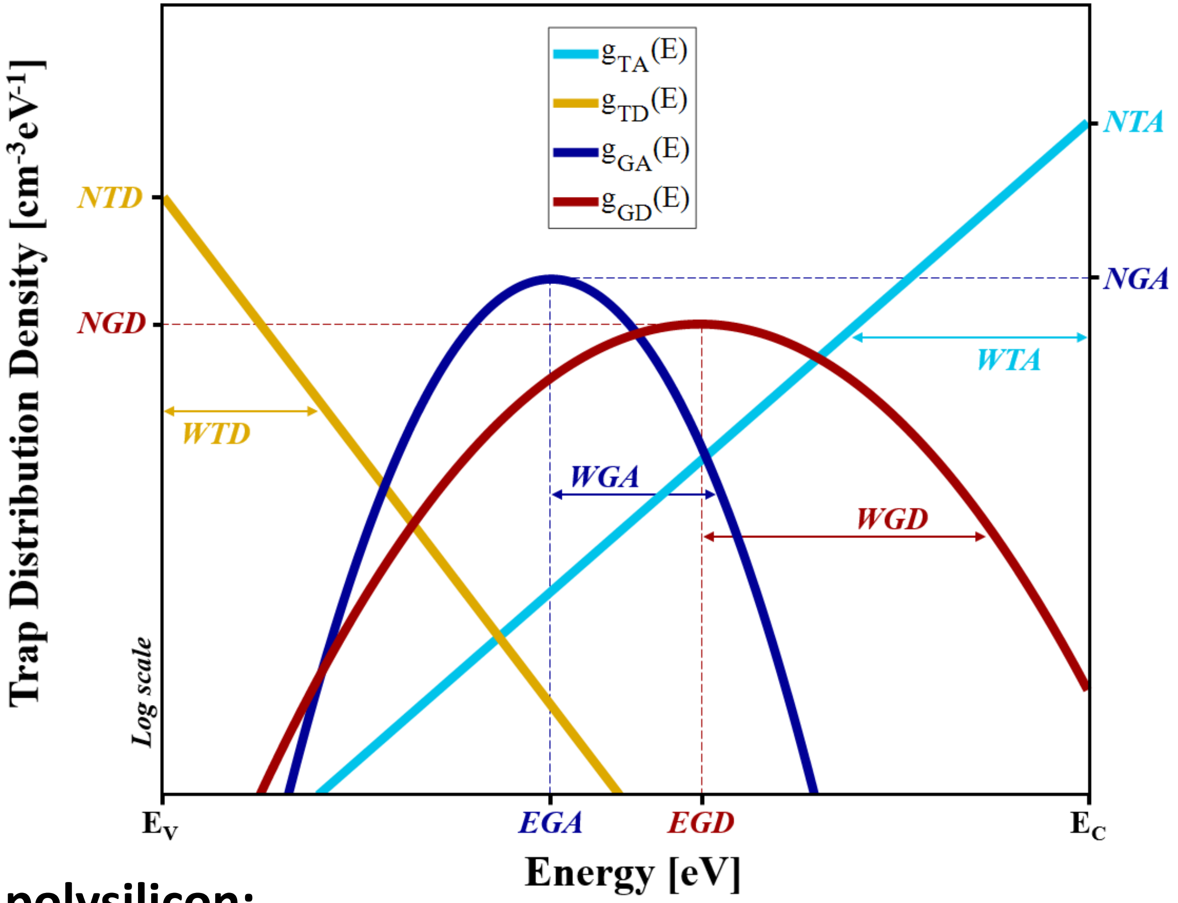
Physics of RF Substrates

- Quantitative Analysis and Understanding
- Fundamentals of Interface Trap Passivation
- Dynamic effects (finite time constants)

Quantitative Charge Balance

How does Trap-Rich interface passivation work?





For Acceptor Traps: $Q_{Empty} = 0$, $Q_{Filled} = -q$

For Donor Traps: $Q_{Empty} = +q$, $Q_{Filled} = 0$

Traps in polysilicon:

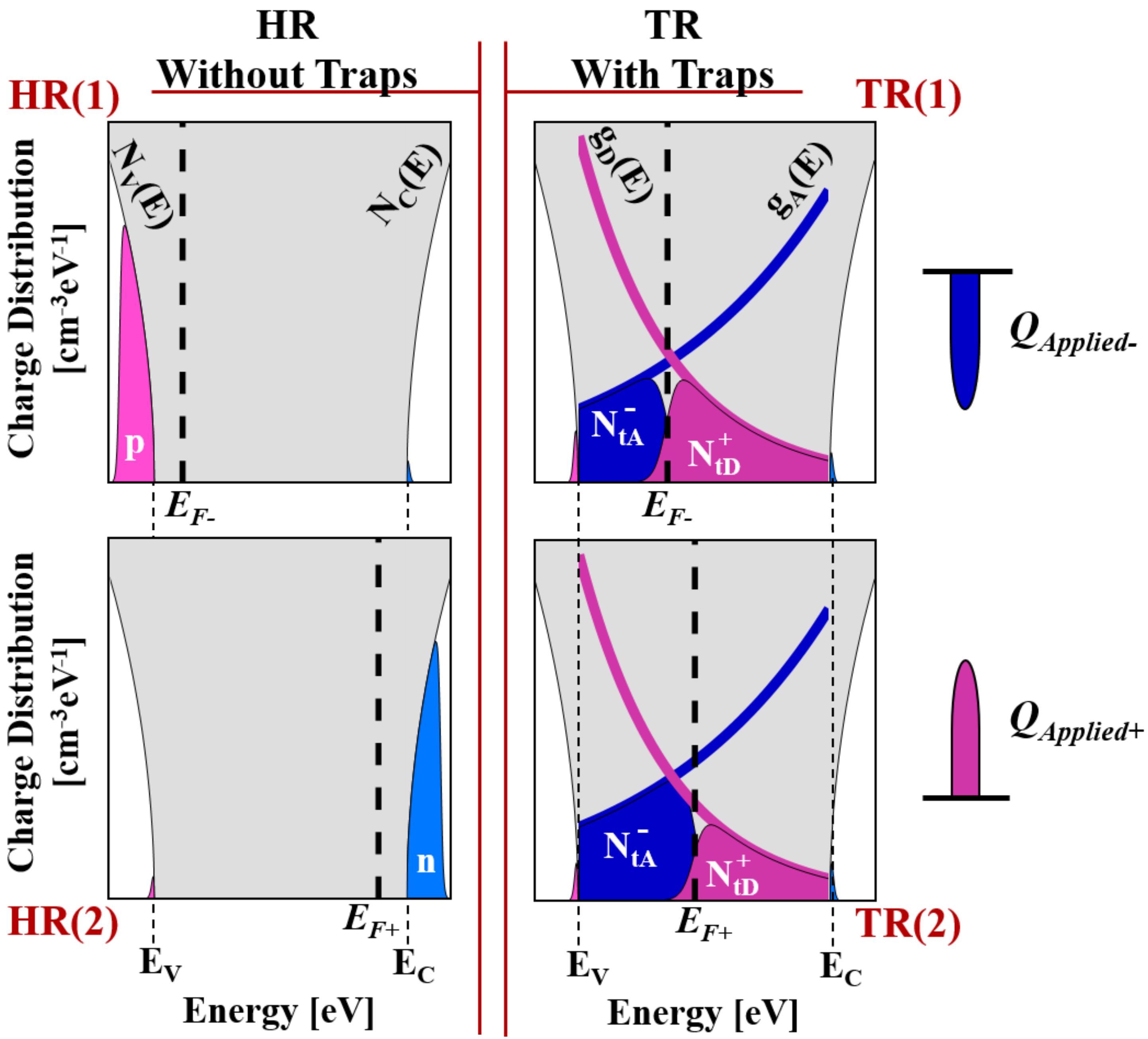
$$g_{GA}(E) = NGA \cdot \exp\left\{-\left(\frac{EGA - E}{WGA}\right)^2\right\} \quad [\text{cm}^{-3} \cdot \text{eV}^{-1}] \quad \textbf{(3.45)}$$

$$g_{GD}(E) = NGD \cdot \exp\left\{-\left(\frac{EGD - E}{WGD}\right)^2\right\} \quad [\text{cm}^{-3} \cdot \text{eV}^{-1}] \quad \textbf{(3.46)}$$

$$g_{TA}(E) = NTA \cdot \exp\left\{\frac{E - E_C}{WTA}\right\} \quad [\text{cm}^{-3} \cdot \text{eV}^{-1}] \quad \textbf{(3.47)}$$

$$g_{TD}(E) = NTD \cdot \exp\left\{\frac{E_V - E}{WTD}\right\} \quad [\text{cm}^{-3} \cdot \text{eV}^{-1}] \quad \textbf{(3.48)}$$

Charge compensation: HR vs. TR



$$N_{free} = \int_0^{t_Q} p(y) - n(y)\,dy \qquad [cm^{-2}]$$

$$N_{trap} = \int_0^{t_Q} N_{tD}^{+}(y) - N_{tA}^{-}(y)\,dy \qquad [cm^{-2}]$$

$$N_{Applied}(V) = N_{ox} + C_{ox}(V - V_{MS}) \qquad [cm^{-2}]$$

In all generality:

$$-N_{Applied} = N_{free} + N_{trap}$$

In a HR:

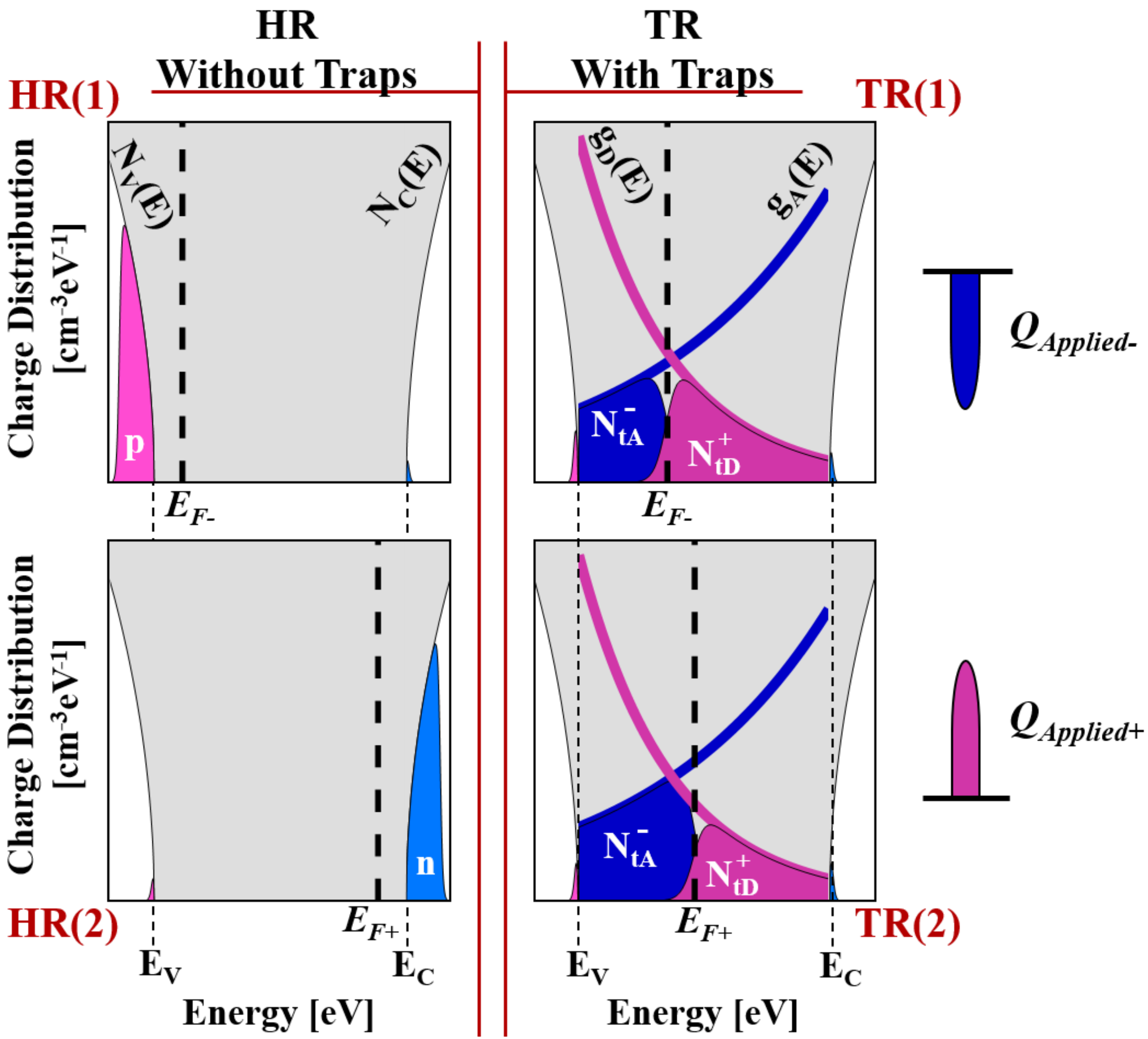
$$-N_{Applied} = N_{free}$$

In a « good » TR:

$$-N_{Applied} \approx N_{trap}$$

For any usual value of $N_{Applied}(V)$

Charge compensation: HR vs. TR



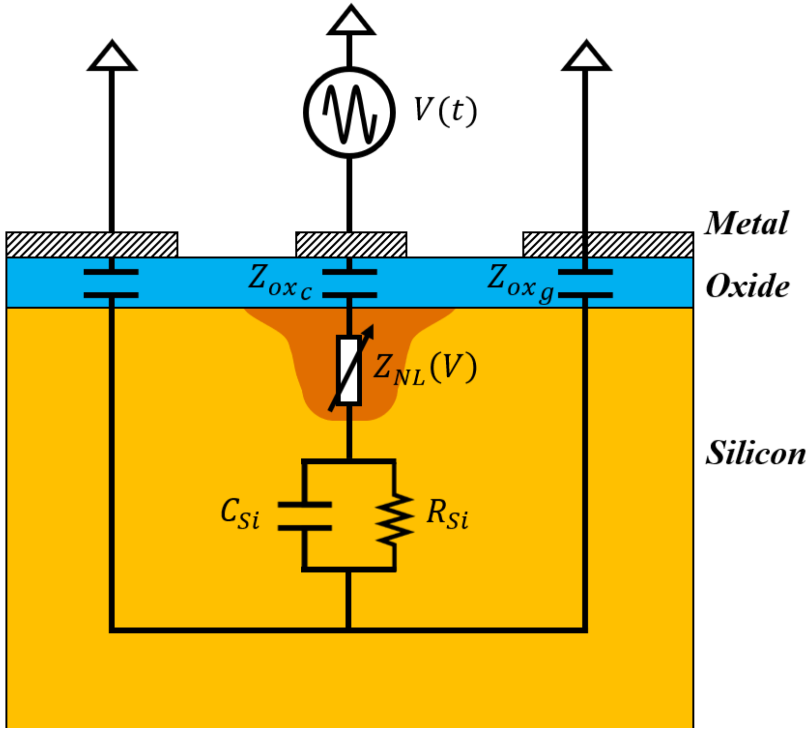
In a HR:

n and $\boldsymbol{p}$ vary strongly with the applied signal $V(t)$

In a « good » TR:

n and $\boldsymbol{p}$ remain very low for "any" signal $V(t)$

Concept of *Fermi-level pinning* → *Quasistatic*



Charge compensation: HR vs. TR

Charges in the Semiconductor

Applied Charge

Donor Distr.
Acceptor Distr.
Fermi Level

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<u>HR substrate</u>

Large variations in n and p

$\Rightarrow$ Large variations in substrate impedance

$\Rightarrow$ Highly voltage-dependent (non-linear)

Quasistatic analysis (DC or low-freq)

Charge compensation: HR vs. TR

Charges in the Semiconductor

Applied Charge

[Movie Animation Not Included in PDF Format]

<u>TR substrate</u>

Small variations in n and p

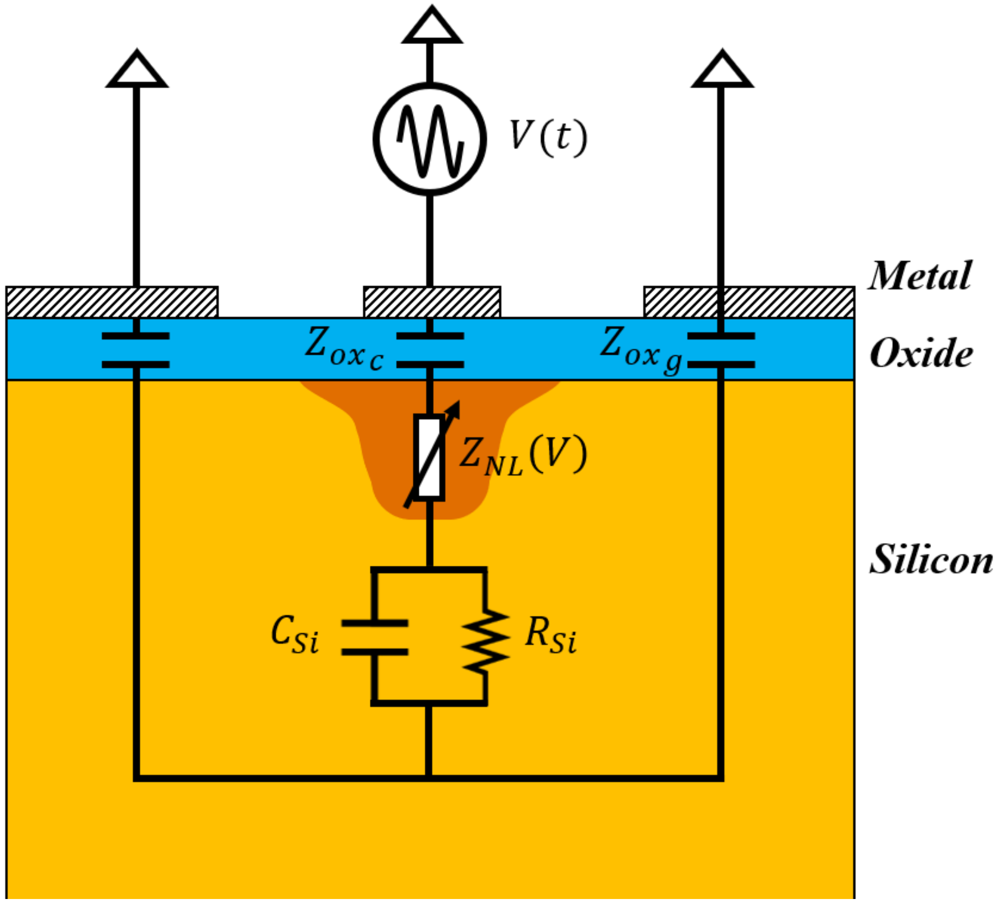
$\Rightarrow$ Small variations in substrate impedance

$\Rightarrow$ Little voltage-dependency (at low freq. !!)

Quasistatic analysis (DC or low-freq)

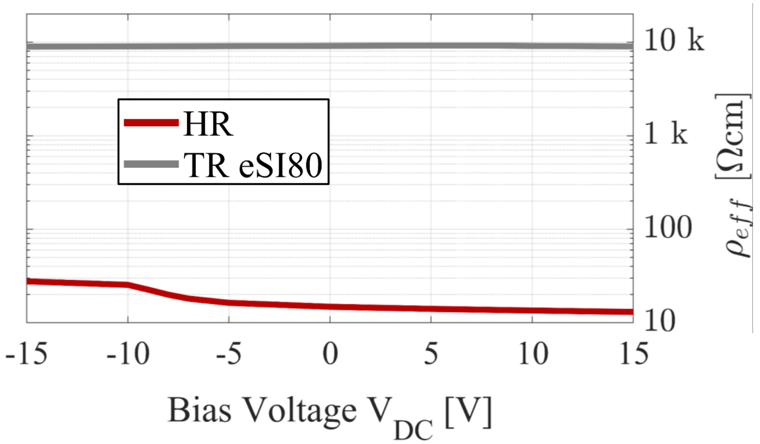
At RF, full description involves E_{QFn}, E_{QFp}, $E_{QFtrap1}$, $E_{QFtrap2}$, etc.

For Large-Signal Substrate Modelling…



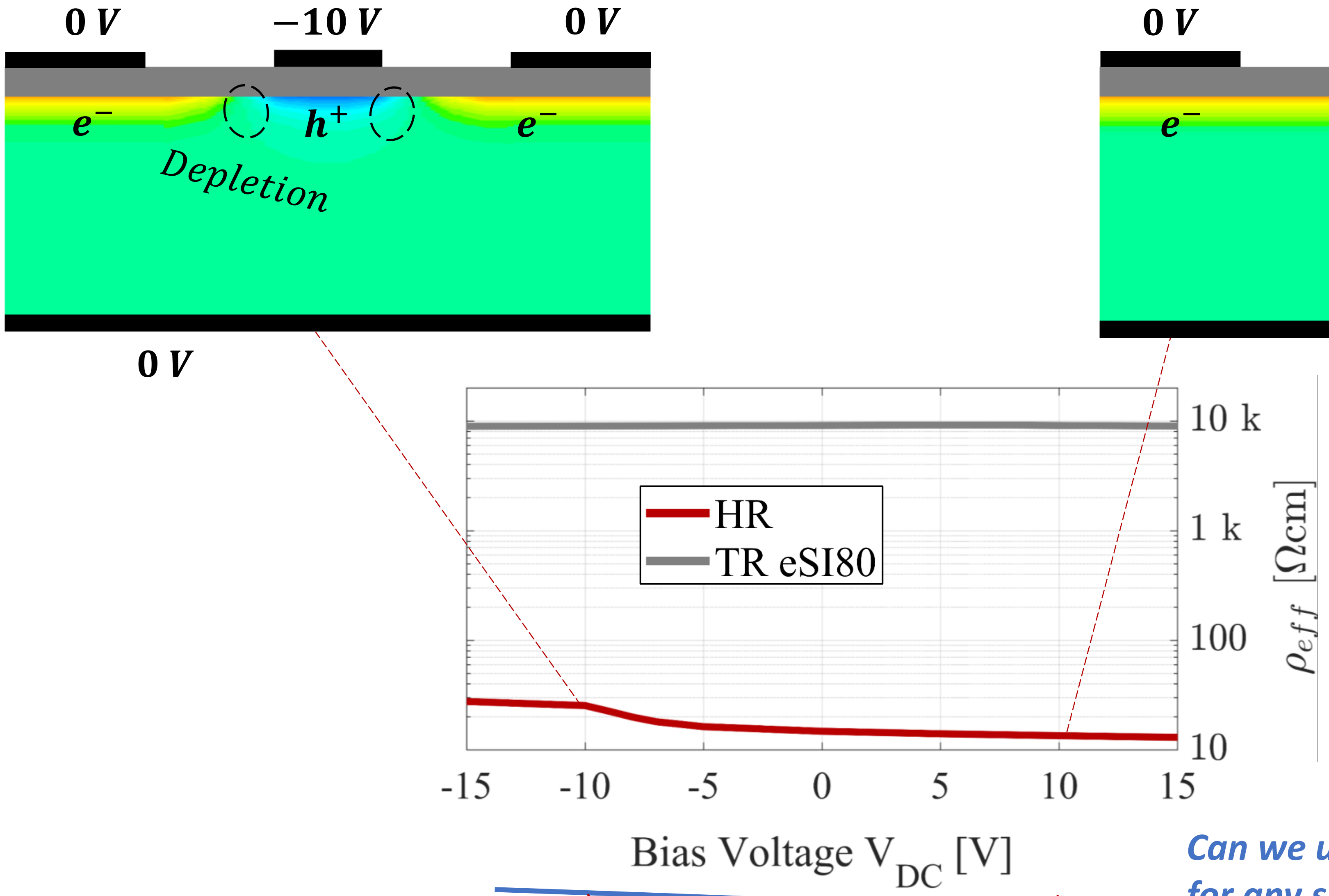
… interested in the behaviour of substrate impedance with the applied voltage signal.

$$Z_{NL}(V)$$



== Substrate impedance $Z_{sub}(V)$

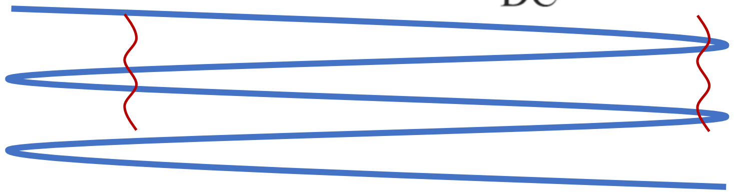
Substrate impedance vs. voltage



== Substrate impedance $Z_{sub}(V)$

Can we use this $Z_{sub}(V)$ transfer function, for any signal $V(t)$?

How does the substrate respond under large-signal excitation?



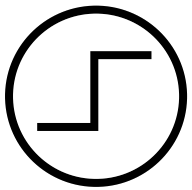
Flip between these states in ~ ns ??

Non-Equilibrium Dynamics

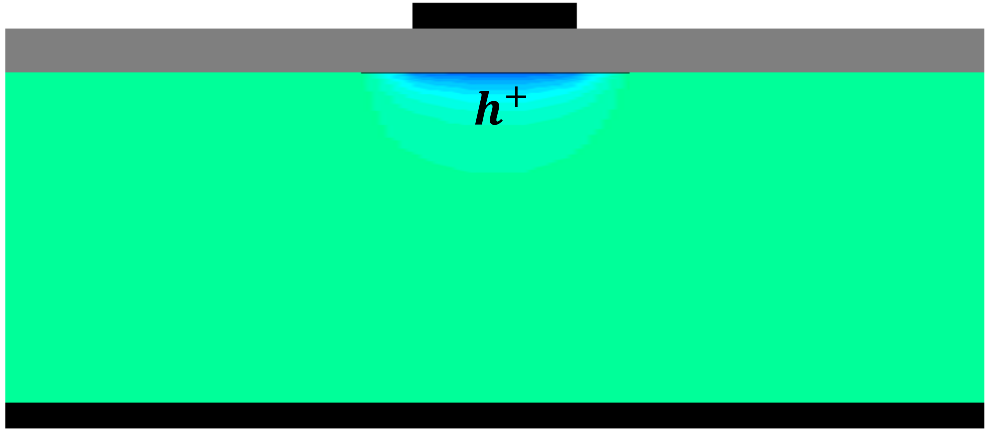
Voltage step applied to MOS device.

$N_{ox} = 0 \quad cm^{-2}$

$V(t)$

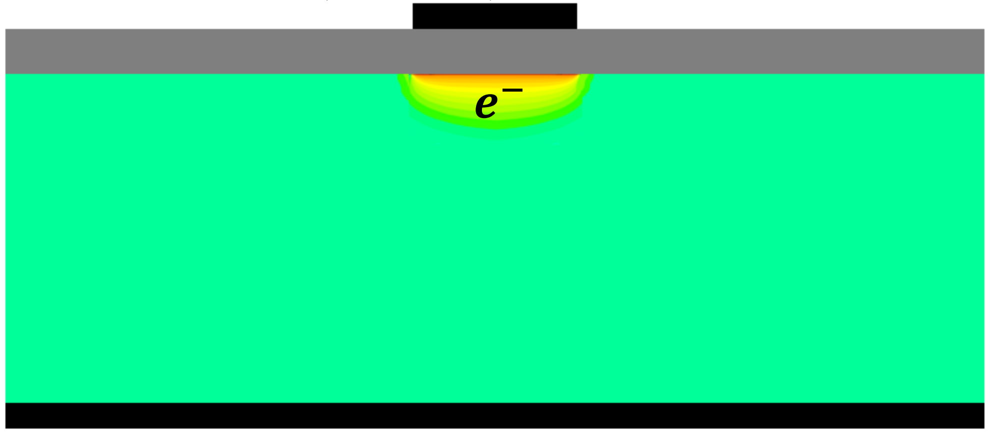


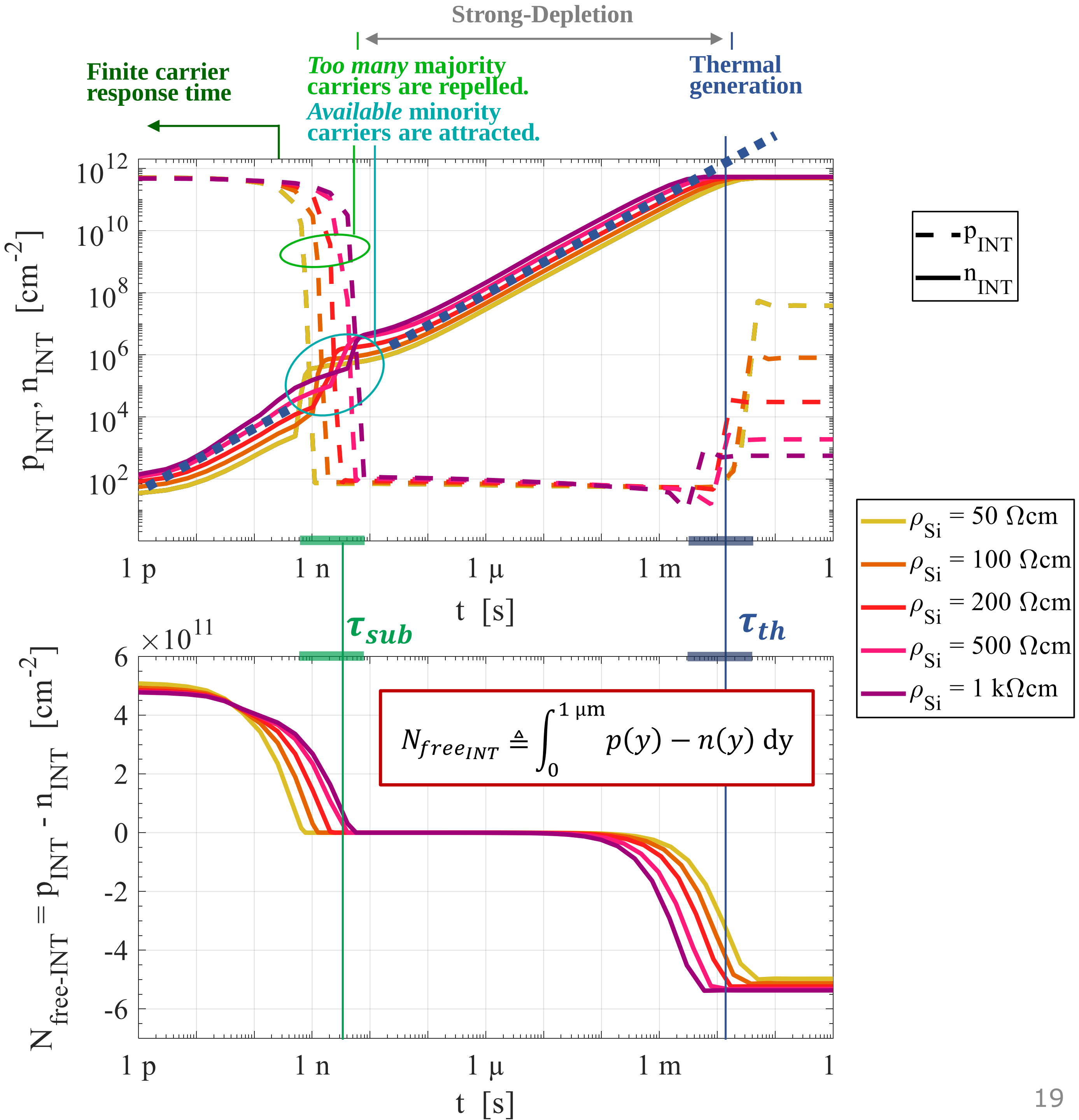
$V(t = 0^-) = -10\ V$



Color map
$n(x, y)$

$V(t = +\infty) = +10\ V$



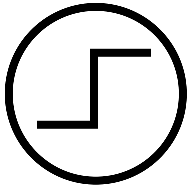


Non-Equilibrium Dynamics

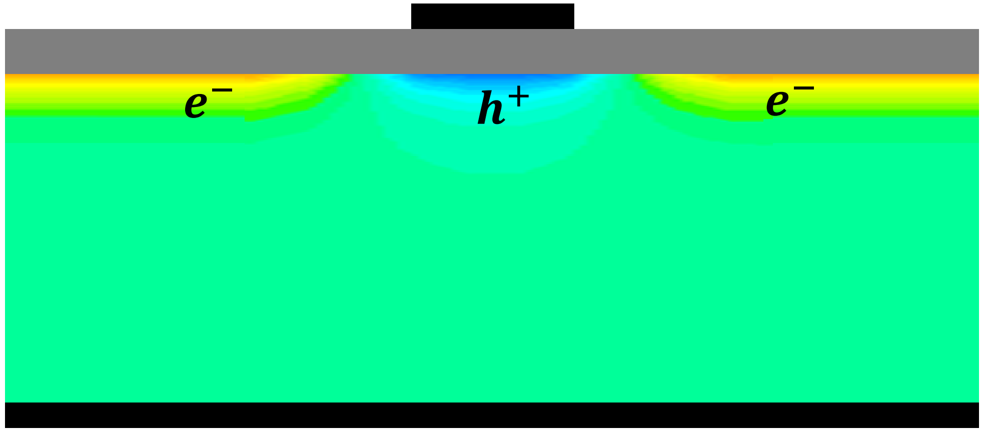
Voltage step applied to MOS device.

$N_{ox} = 10^{11} \quad cm^{-2}$

$V(t)$

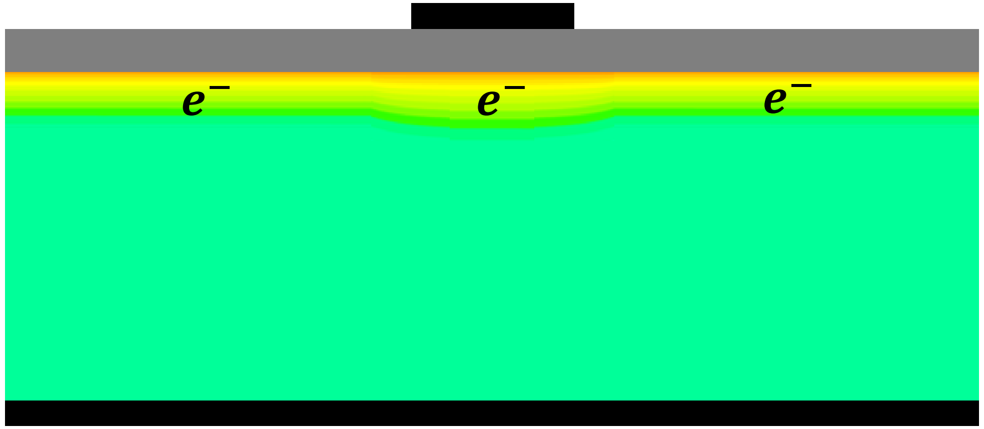


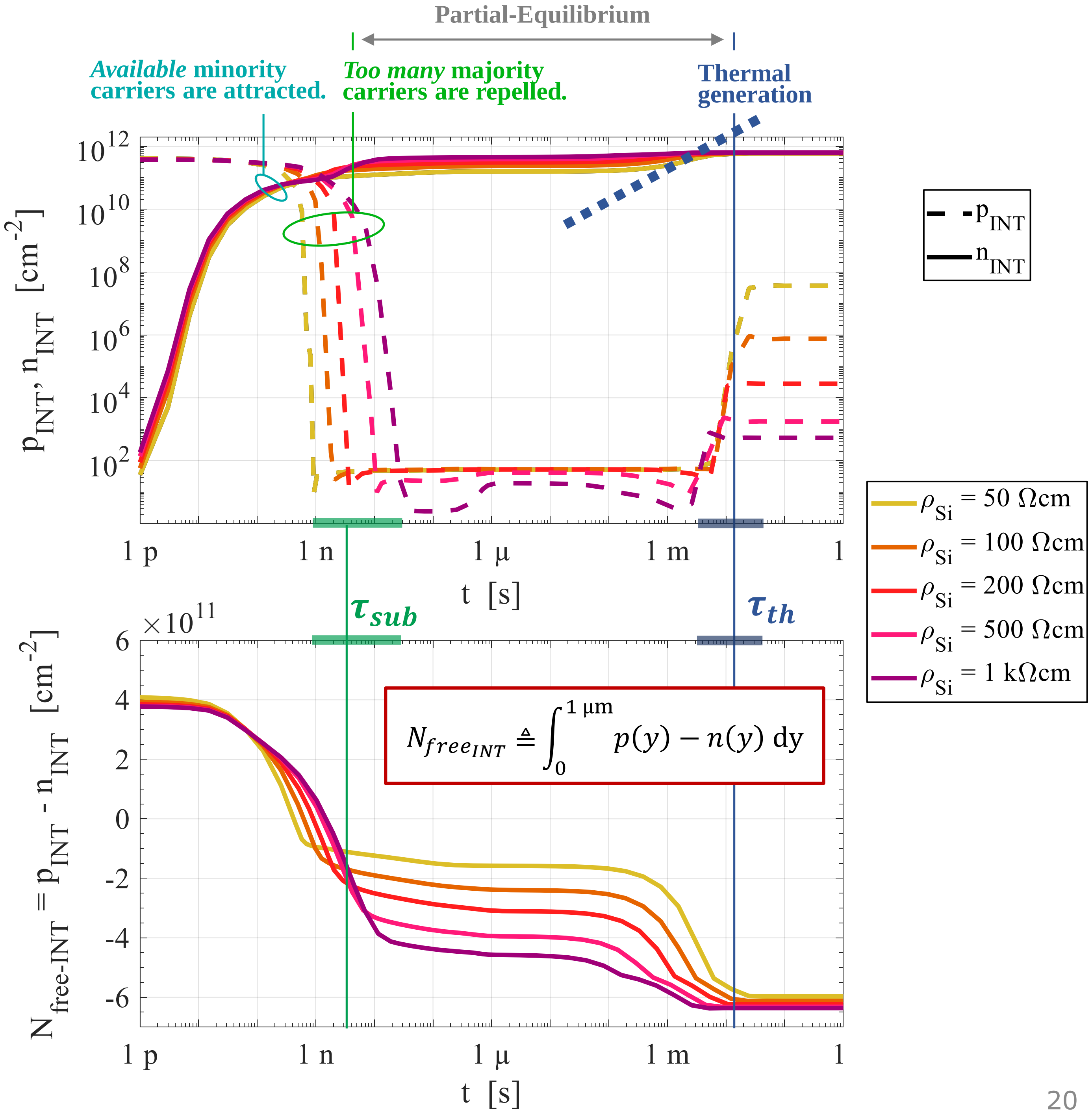
$V(t = 0^-) = -10\ V$



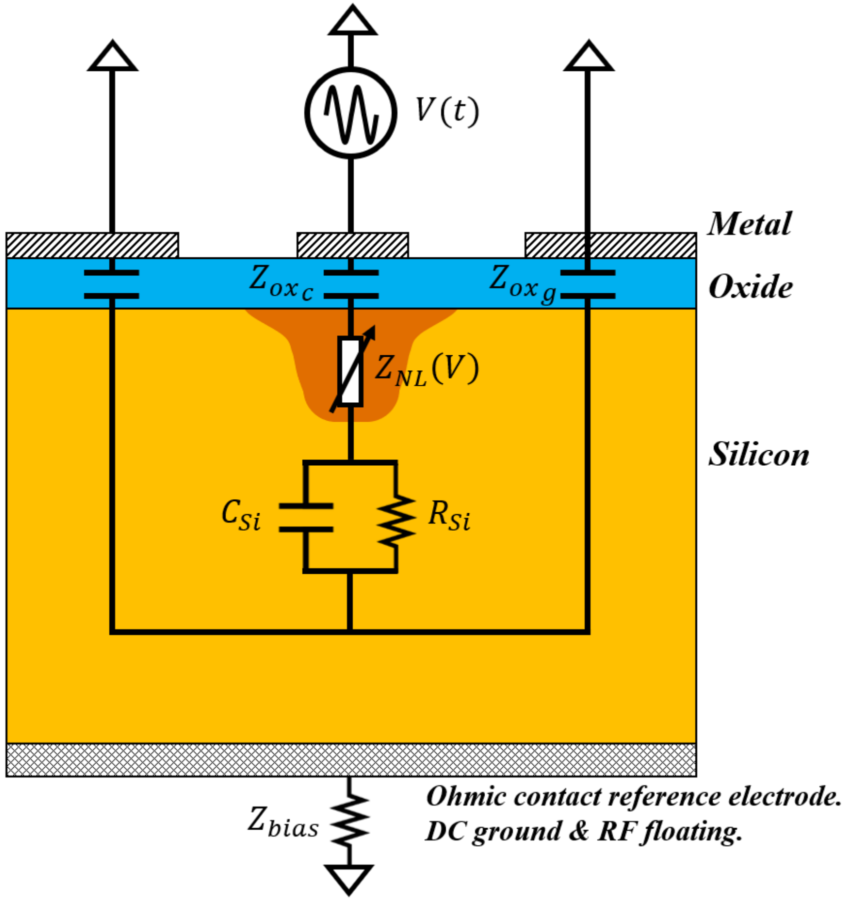
Color map
$n(x, y)$

$V(t = +\infty) = +10\ V$

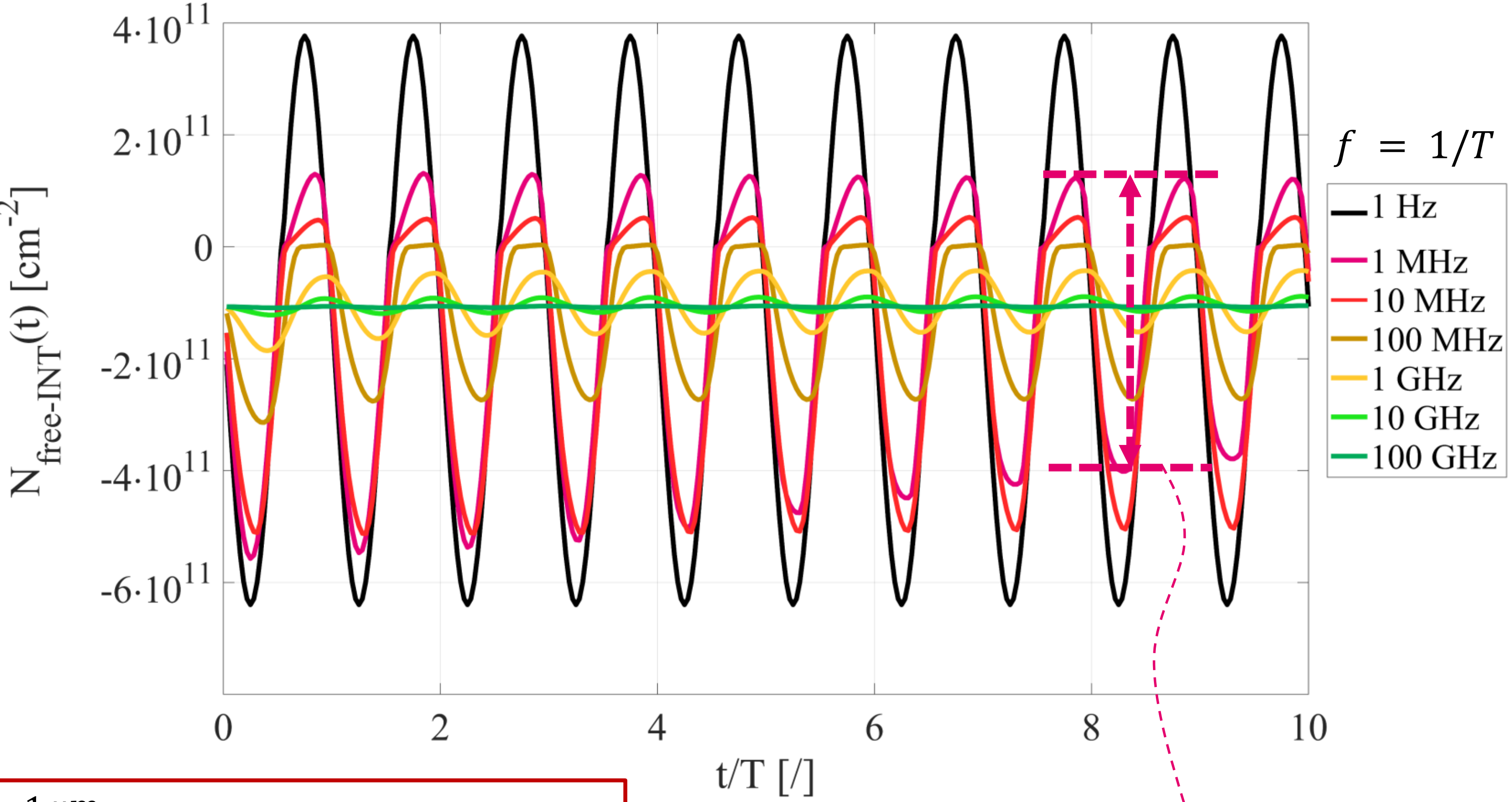




Non-Equilibrium Dynamics Sinusoïdal $V(t)$ - RF analysis



HR $\rho_{Si} = 1\ \text{k}\Omega\text{cm}$ (P-type),
$t_{ox} = 400\ \text{nm}$, $N_{ox} = 10^{11}\ \text{cm}^{-2}$

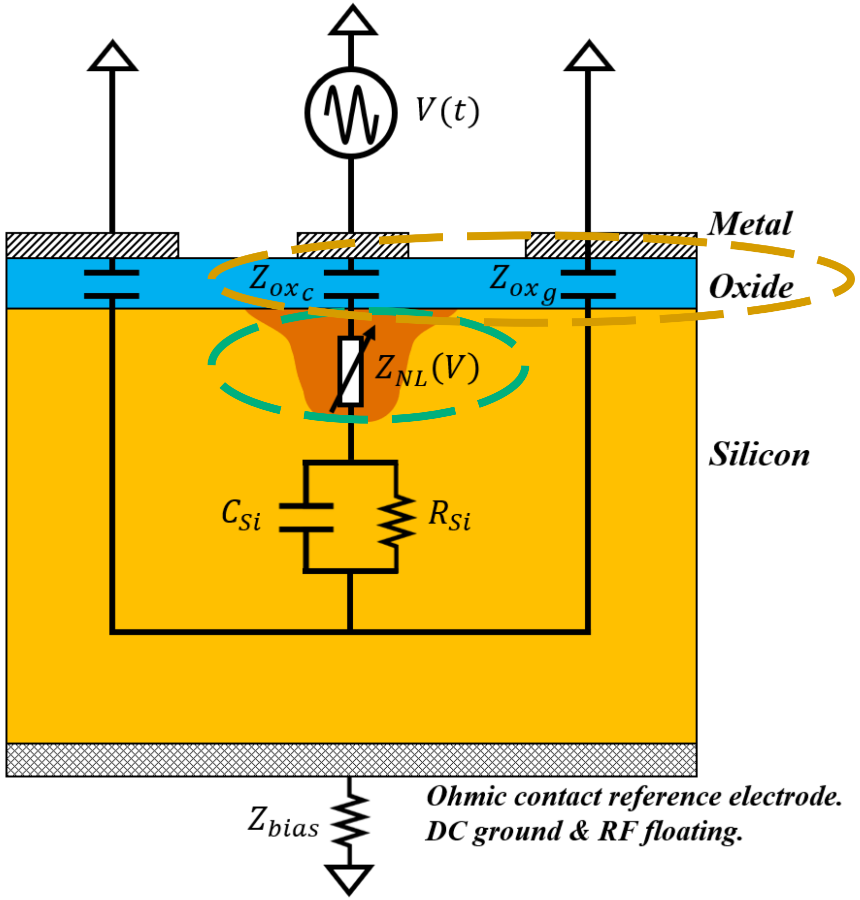


$$N_{free_{INT}} \triangleq \int_0^{1\ \mu\text{m}} p(y) - n(y)\ \text{d}y \qquad [\text{cm}^{-2}]$$

$2 \cdot \mathrm{A}\{N_{free_{INT}}(t)\}$
At 1 MHz

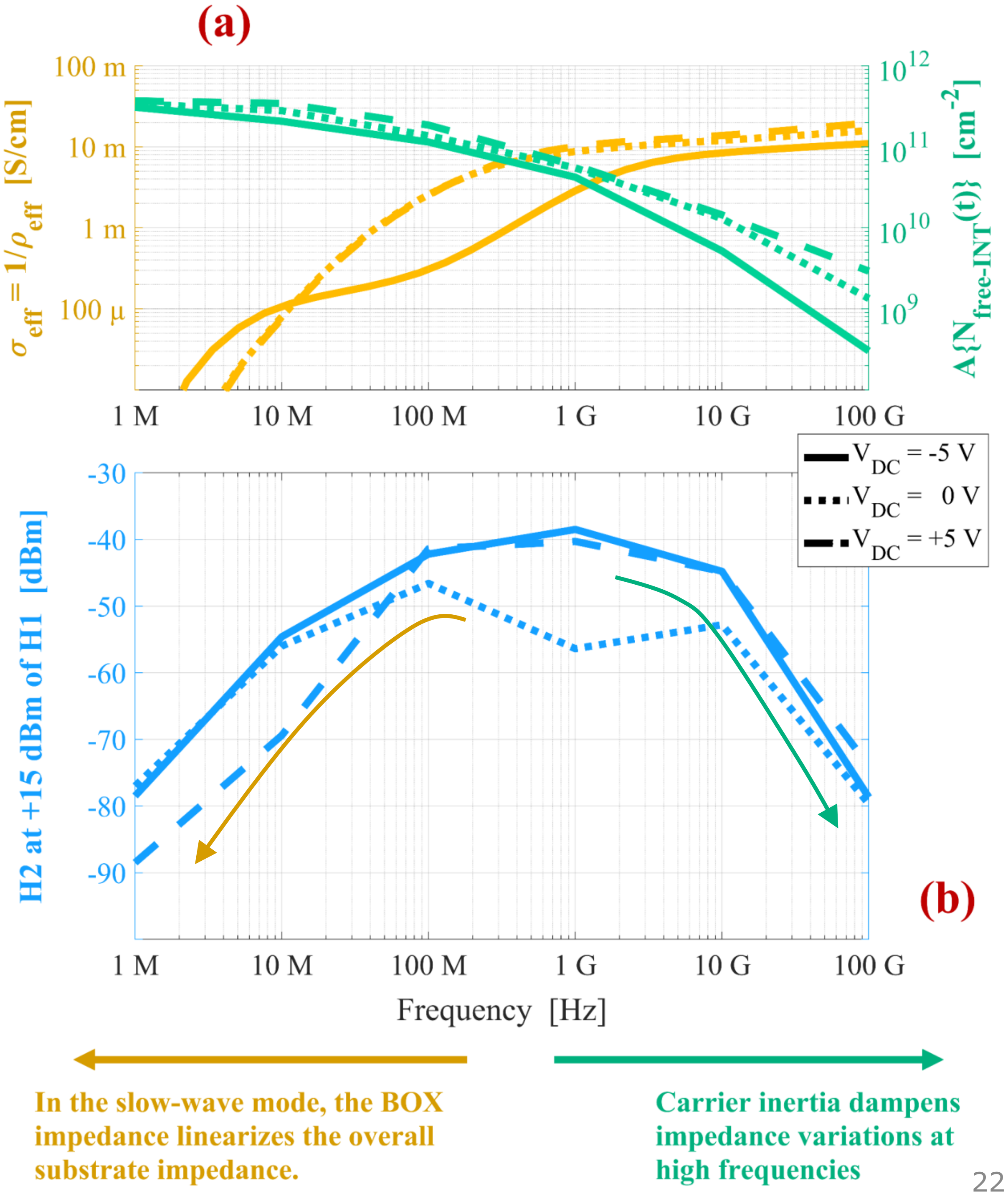
As f increases: only a spatial rearrangement of existing *available carriers through time*
no (significant) generation/recombination

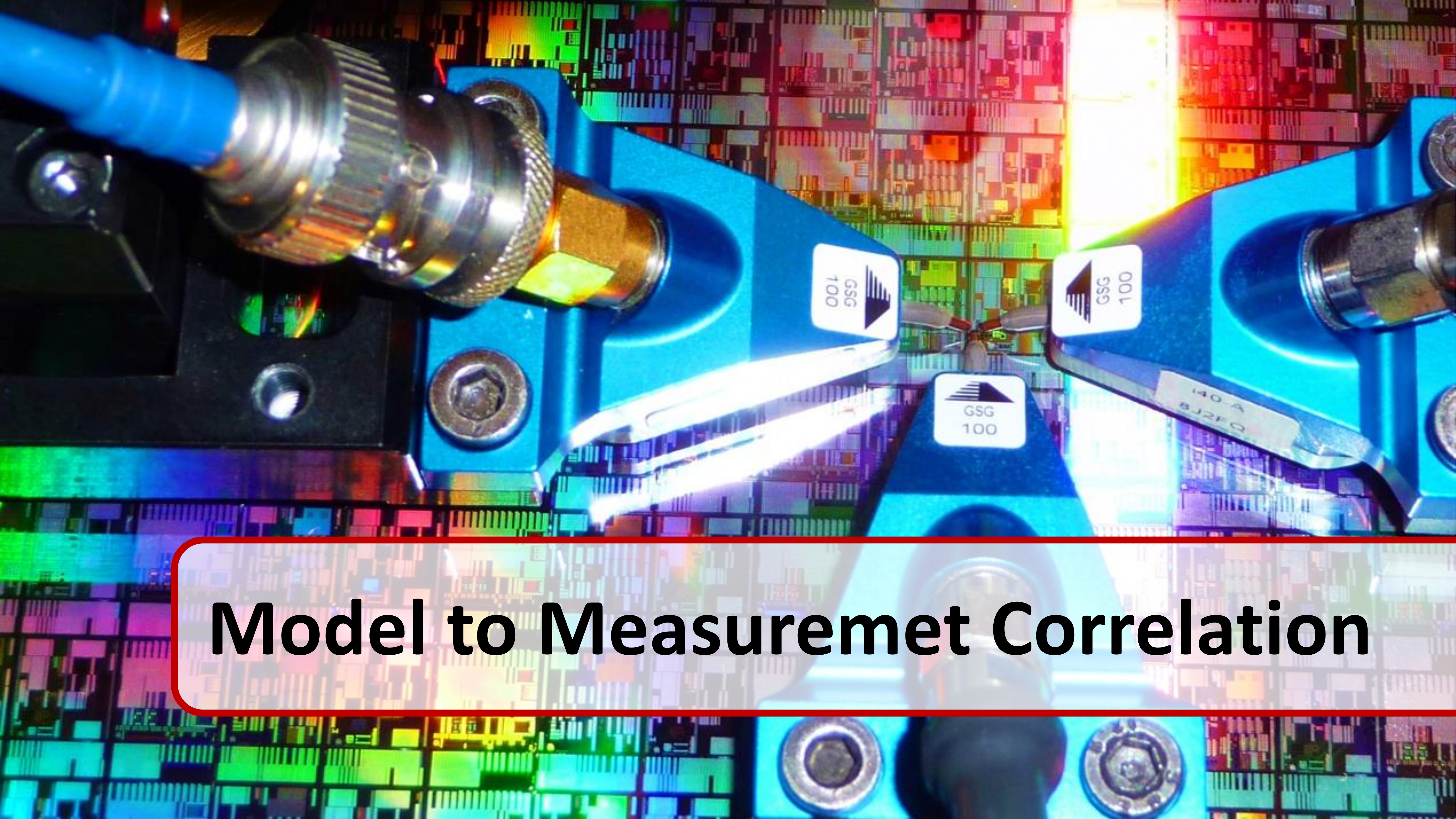
Non-Equilibrium Dynamics RF analysis



HD is maximum just after the end of the slow-wave mode f_{SW}

	ρ_{eff} [Ωcm]	f_{SW}
Standard Si	~10	5 - 15 GHz
HR with strong PSC	< 50	5 - 15 GHz
HR with weak PSC	50 – 200	1 - 5 GHz
TR	10k	10 - 50 MHz

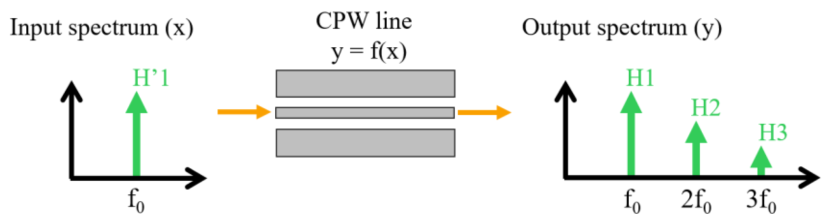




Model to Measuremet Correlation

HD is maximum just after the end of the slow-wave mode f_{SW}

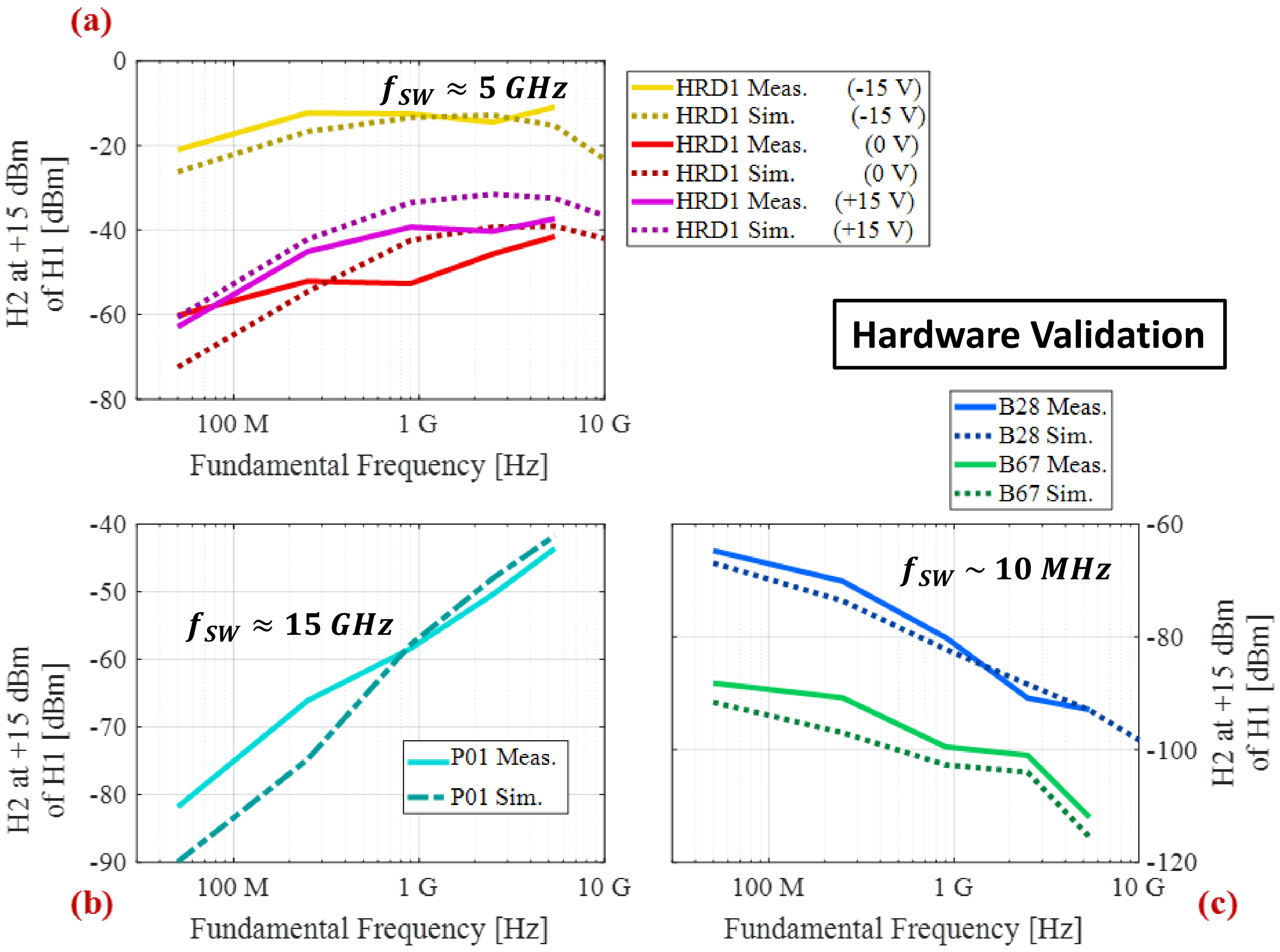
Observe these trends in measurements?



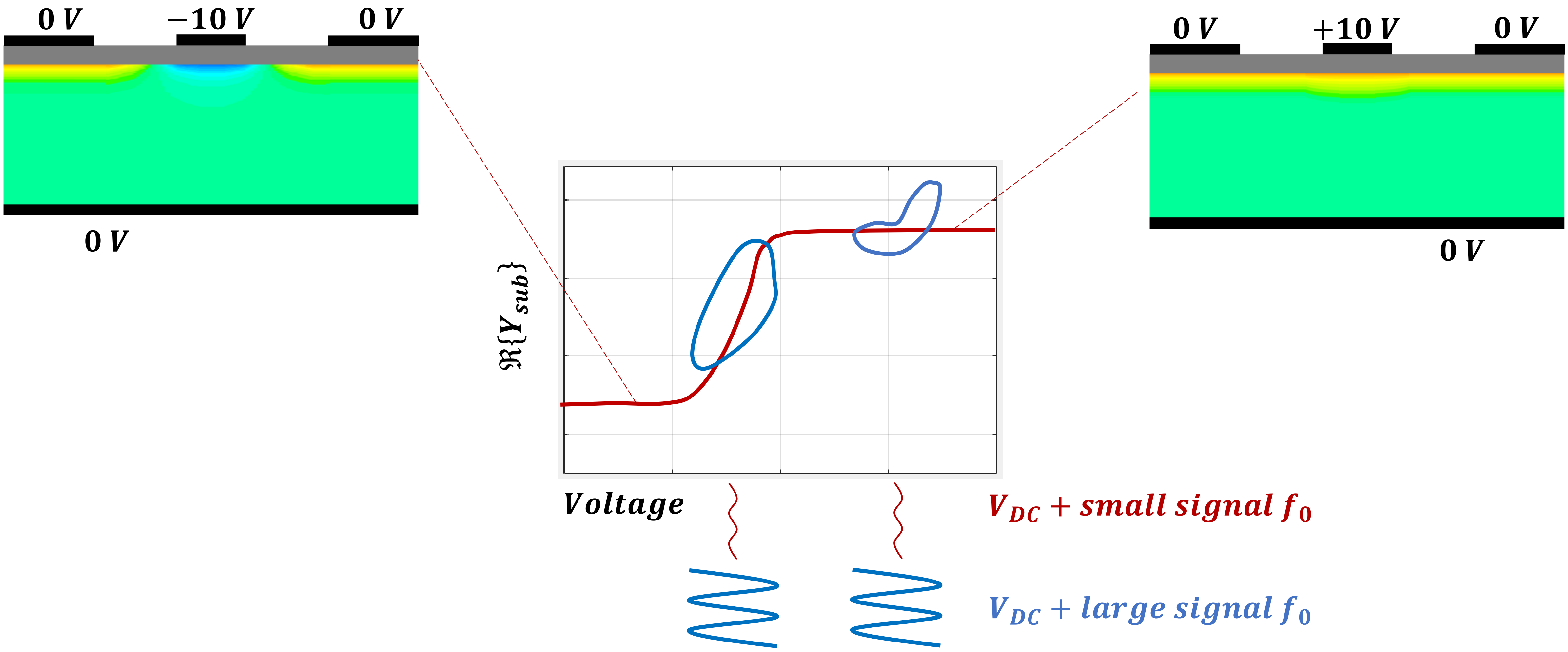
⇒ We set-up measurement benches at: **50 MHz**, **250 MHz**, **900 MHz**, **2.5 GHz** and **5.4 GHz**

(each setup uses dedicated filters and power amplifier)

Hardware Validation



Substrate impedance vs. voltage



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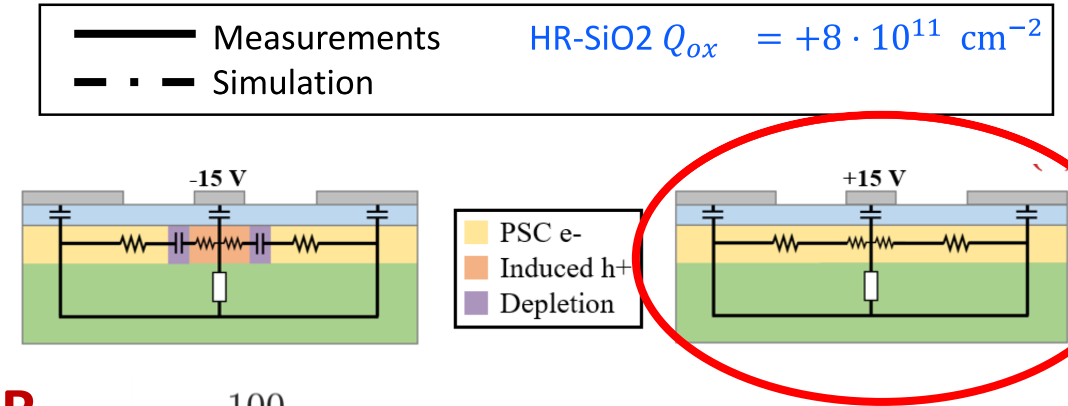
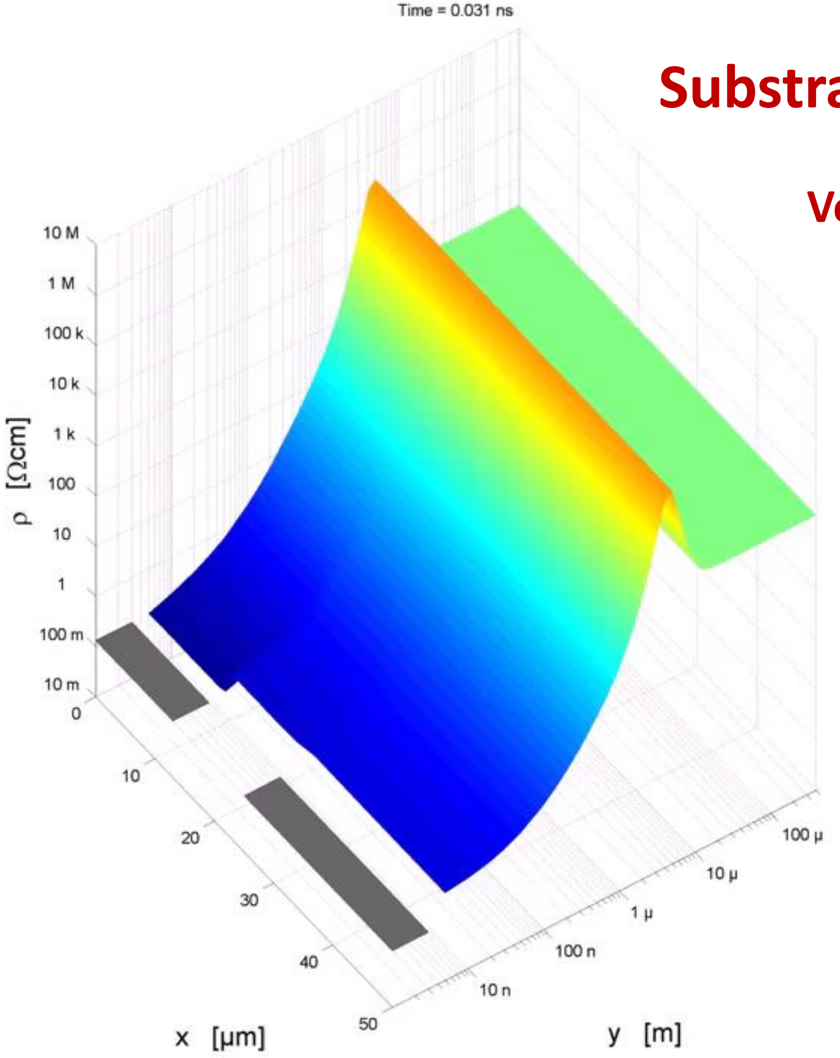
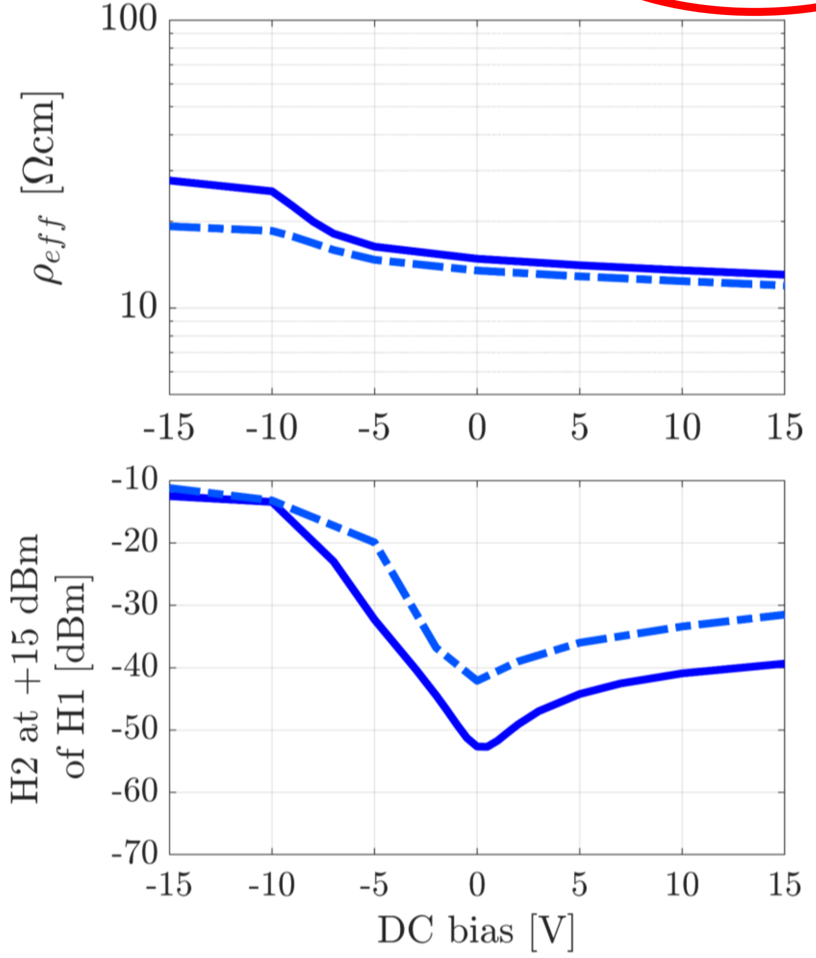




Substrate response in biased HR

Voltage Signal: **f = 900 MHz**
A = 2.5 V
DC = +15 V



Substrate impedance variation gives rise to -35 dBm of H2 distortion

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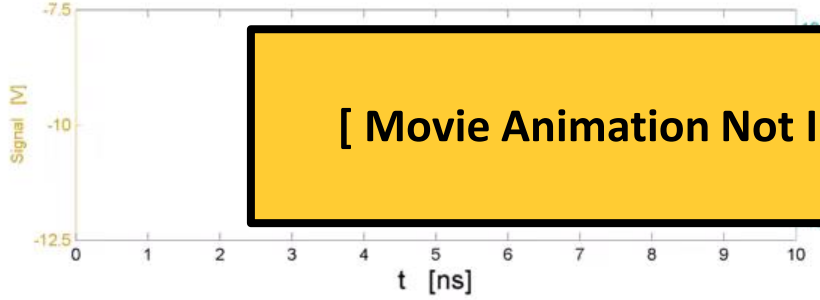
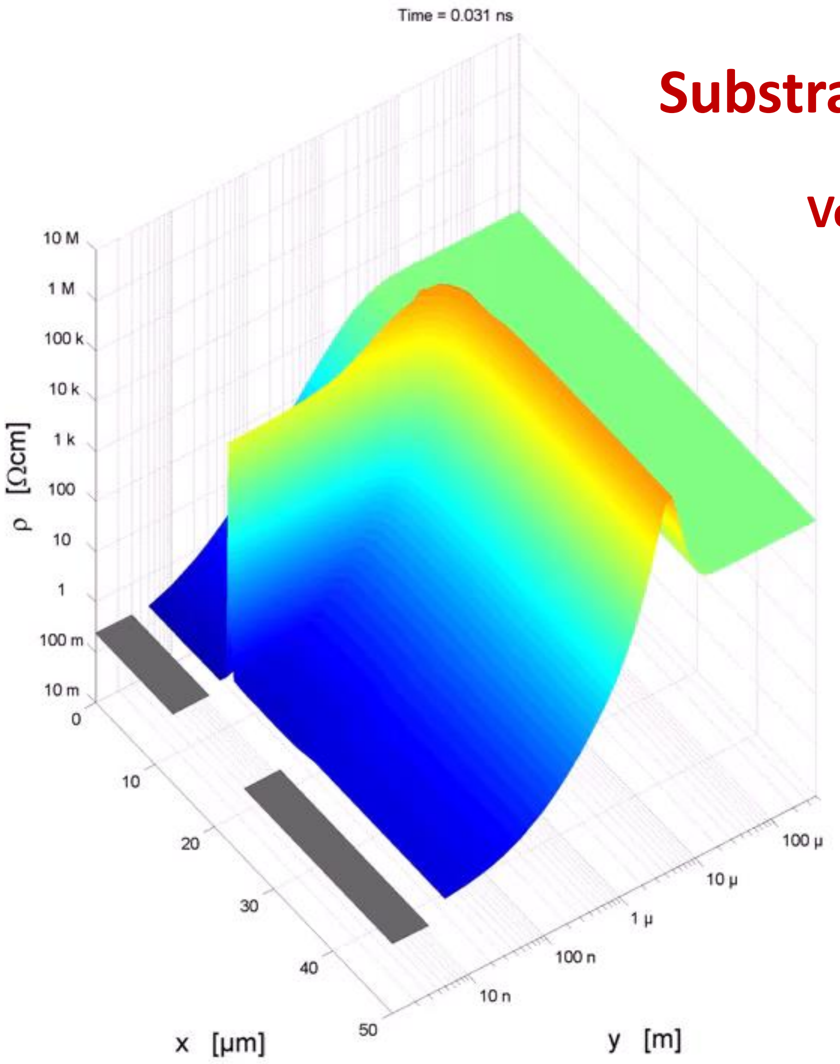




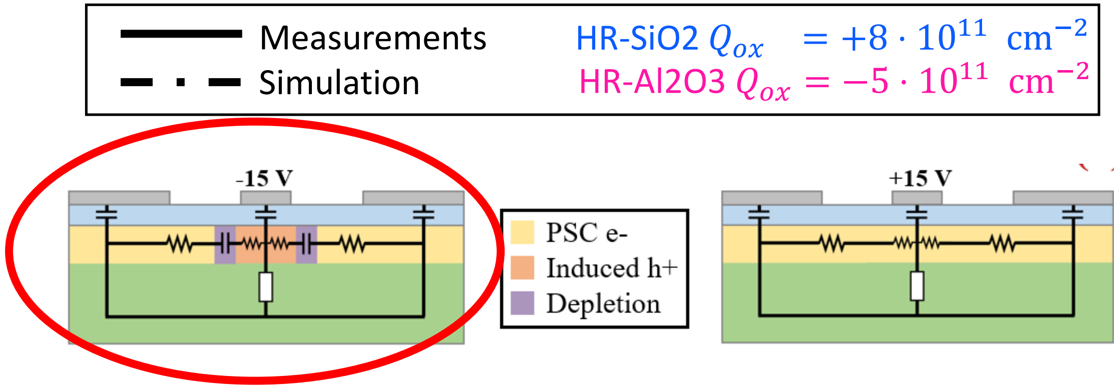
Substrate response in biased HR

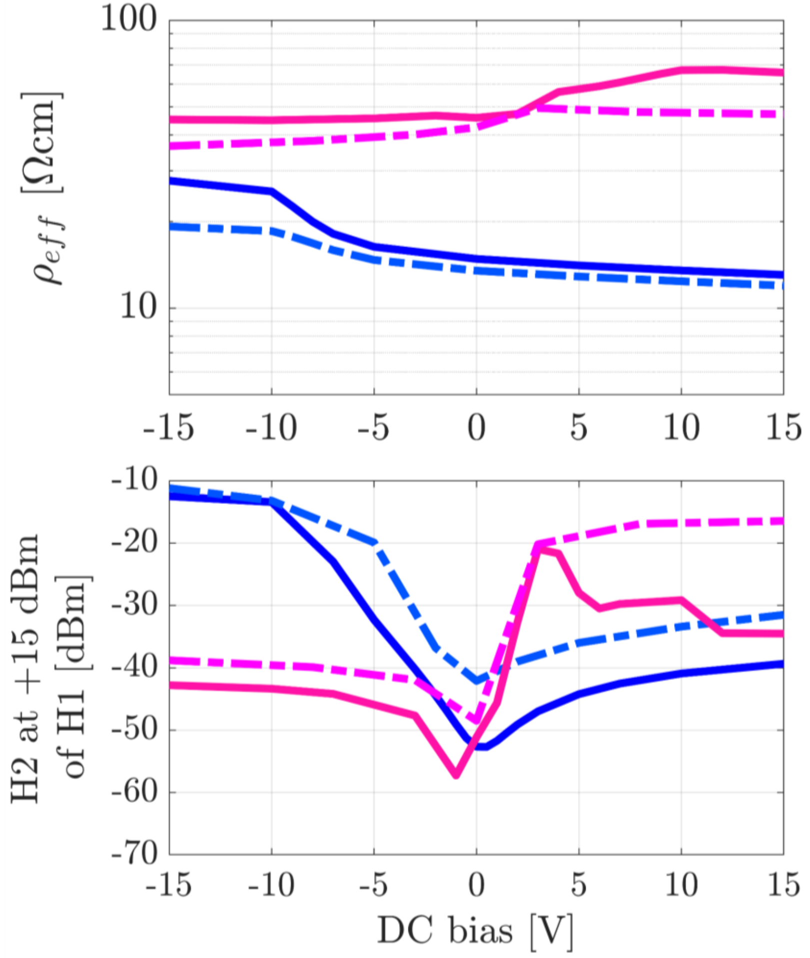
Voltage Signal: **f = 900 MHz**

A = 2.5 V

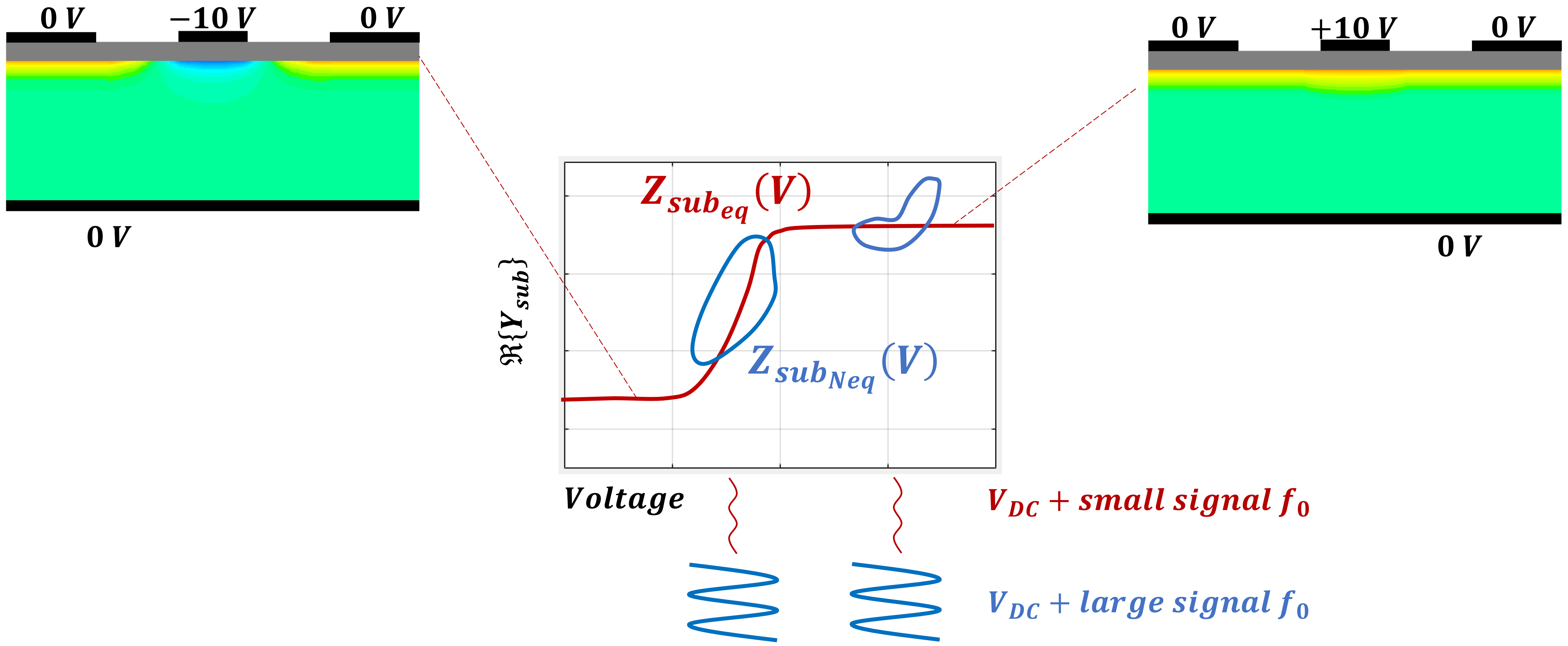
DC = -15 V

Larger impedance variation gives rise to -12 dBm of H2 distortion





Substrate impedance vs. voltage



The substrate is always out of equimibrium is response to a large-signal $V_{RF}(t)$

The equilibirum $Z_{sub_{eq}}(V)$ curve's information is irrelevant !

Even more obvious for Trap-Rich (next slides)

Non-Equilibrium Dynamics

-Dynamics of traps

Don't let all previous slides mislead you into thinking that:

TR substrates are very linear, because ionized traps provide the compensation charge so that free carriers do not have to.

$\Rightarrow$ This statement is false !

To compensate for a change in applied charge $+\Delta Q$, there are four compensation mechanisms:

$n \nearrow$ $p \searrow$	Drift to/from other parts of the substrate
$N_{tA}^{-} \nearrow$	Requires capturing an electron
$N_{tD}^{+} \searrow$	Requires capturing an electron (equivalent to emitting a hole)

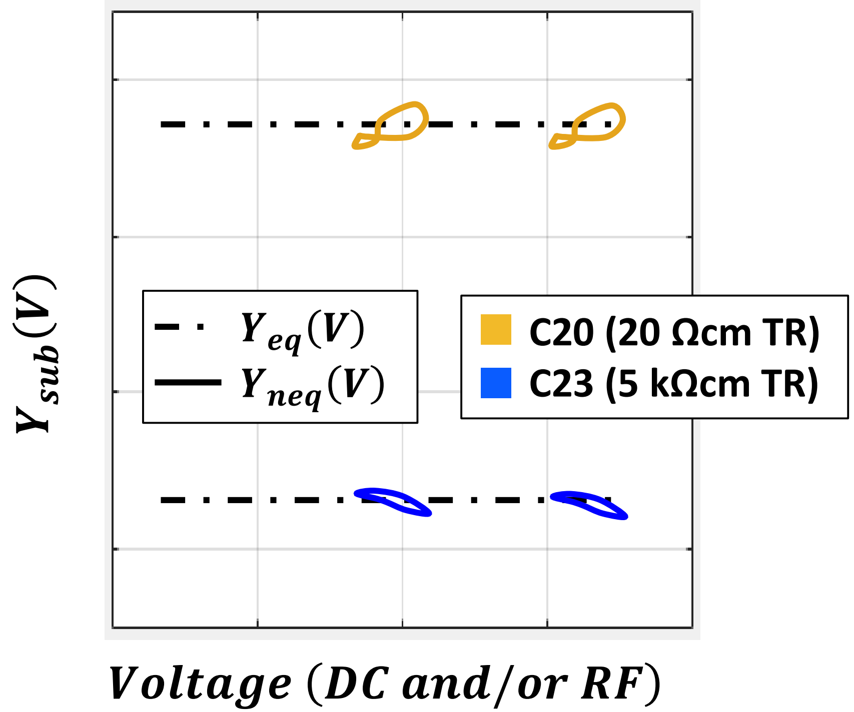
(for the last two mechanisms:)

n and p must vary first.
τ_{tn} and τ_{tp} are long, because n and p are low (TR)

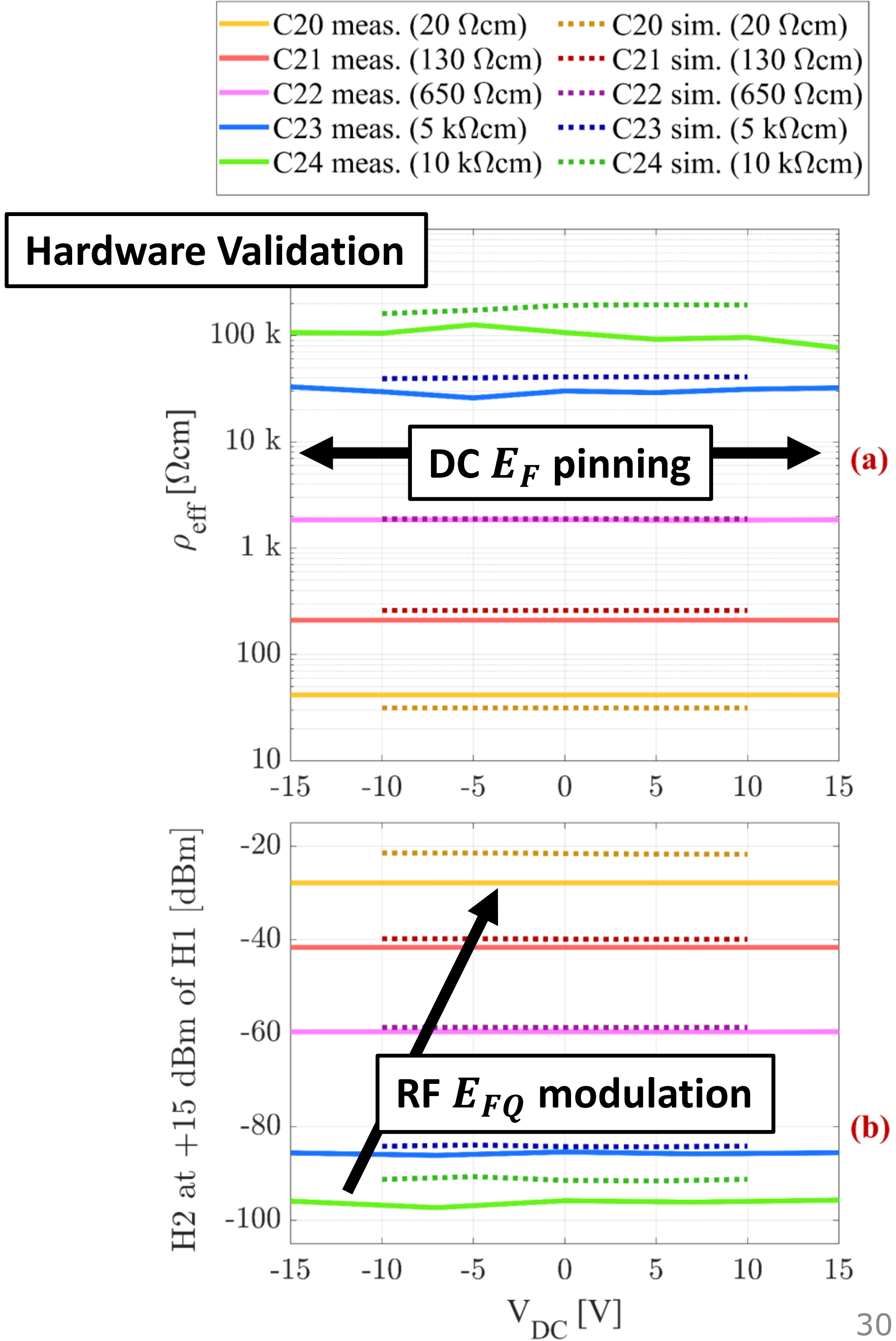
Non-Equilibrium Dynamics

-Dynamics of traps

- Flat $Y_{eq}(V)$ curves: DC Fermi-level pinning
- Non-flat $Y_{neq}(V)$ curves: RF Fermi-level variations; Modulation of the *available carriers*



Instantaneous $Y_{neq}(V)$ curves do not follow the equilibrium $Y_{eq}(V)$ curves.



Further Model-Hardware Correlation

→ Model of in this presentation validated over many parameters:

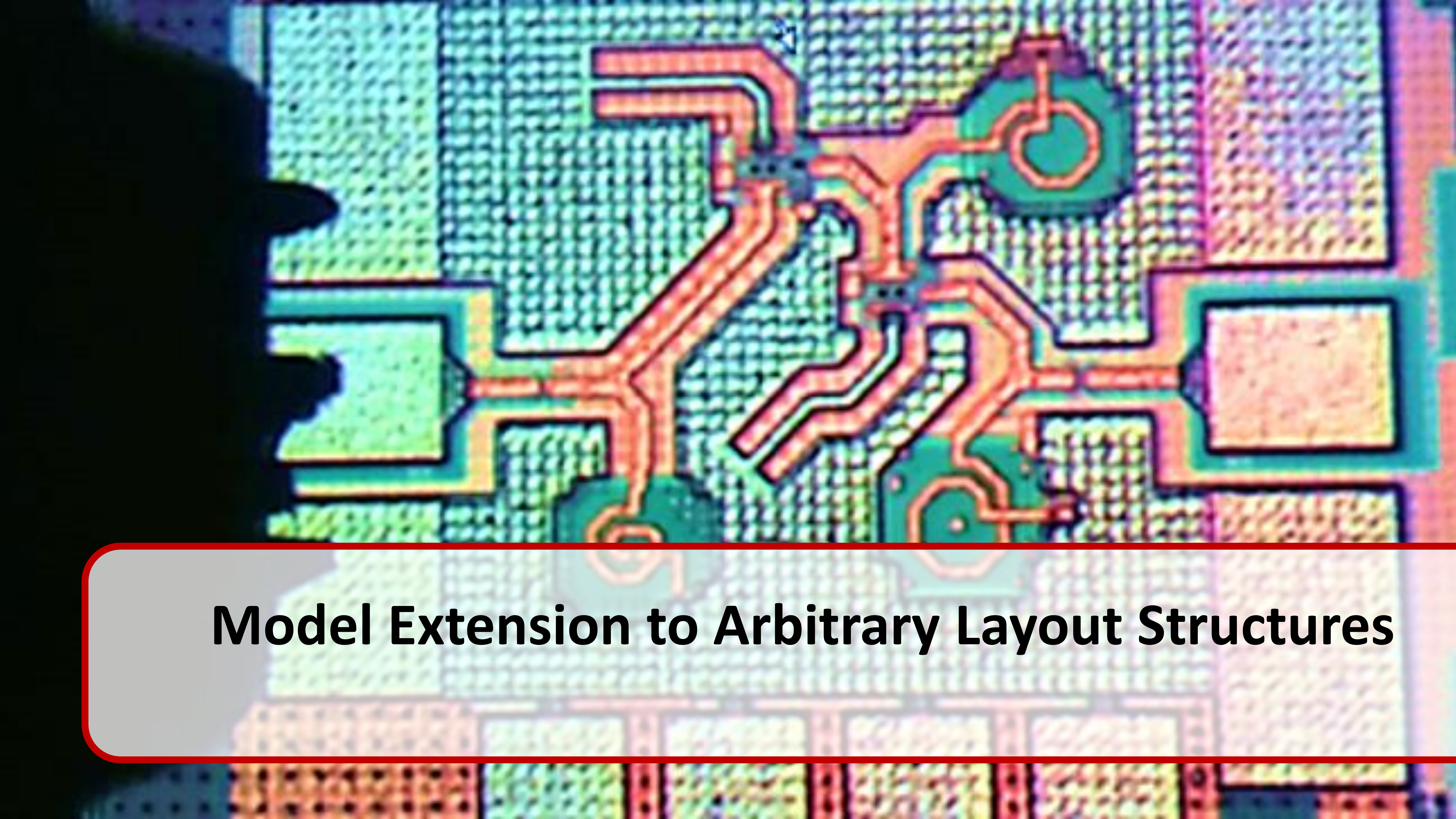
- Amplitude
- DC bias
- Fixed interface charge
- Interface traps and *trap-rich* passivation
- Dimensions of CPW
- Frequency
- Temperature

Full References:

- *Modeling of Semiconductor Substrates for RF Applications: Part I - Static and Dynamic Physics of Carriers and Traps,* doi: 10.1109/TED.2021.3096777.
- *Modeling of Semiconductor Substrates for RF Applications: Part II - Parameter Impact on Harmonic Distortion,*doi: 10.1109/TED.2021.3096781.

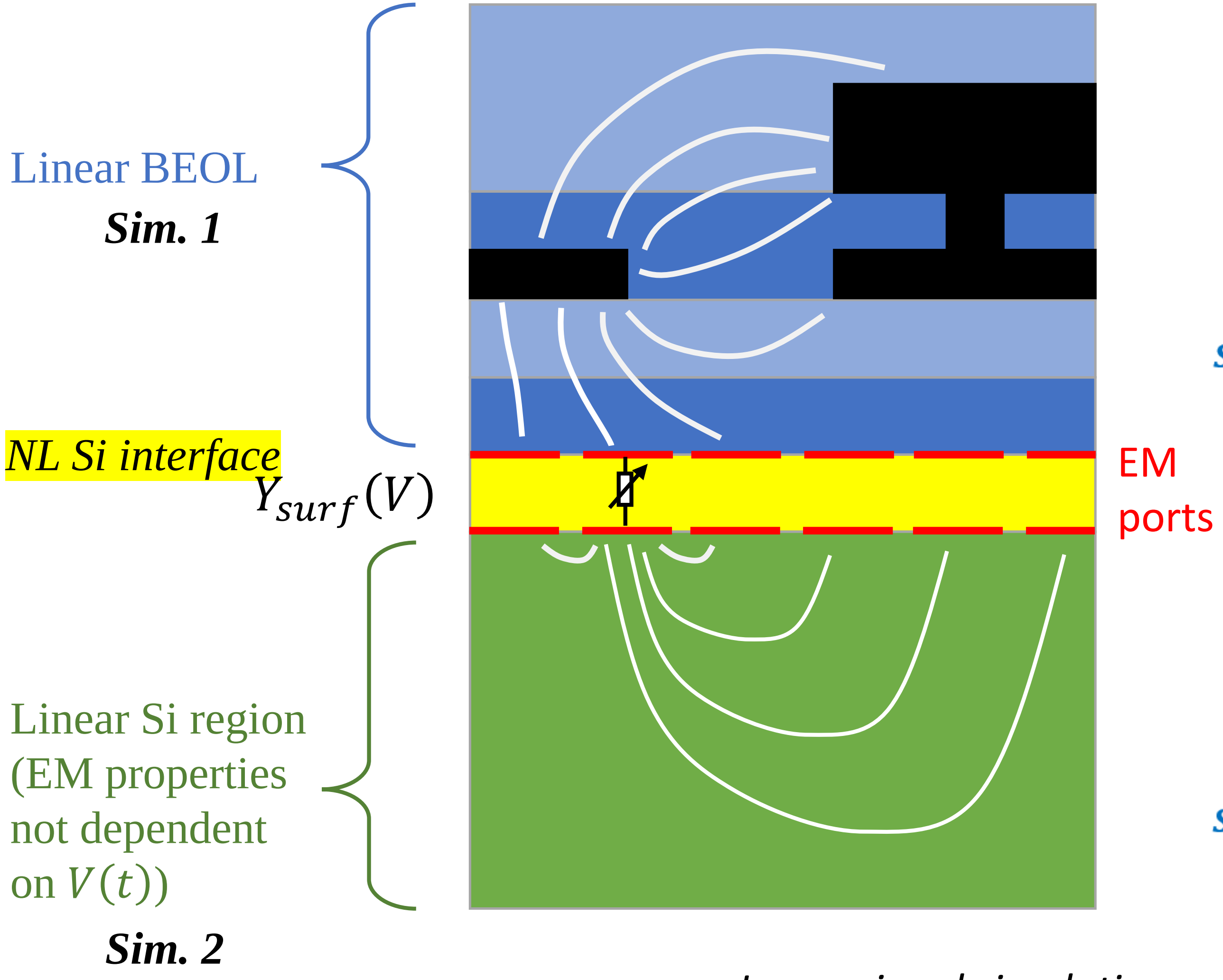
→ Model applied solely to CPW lines !

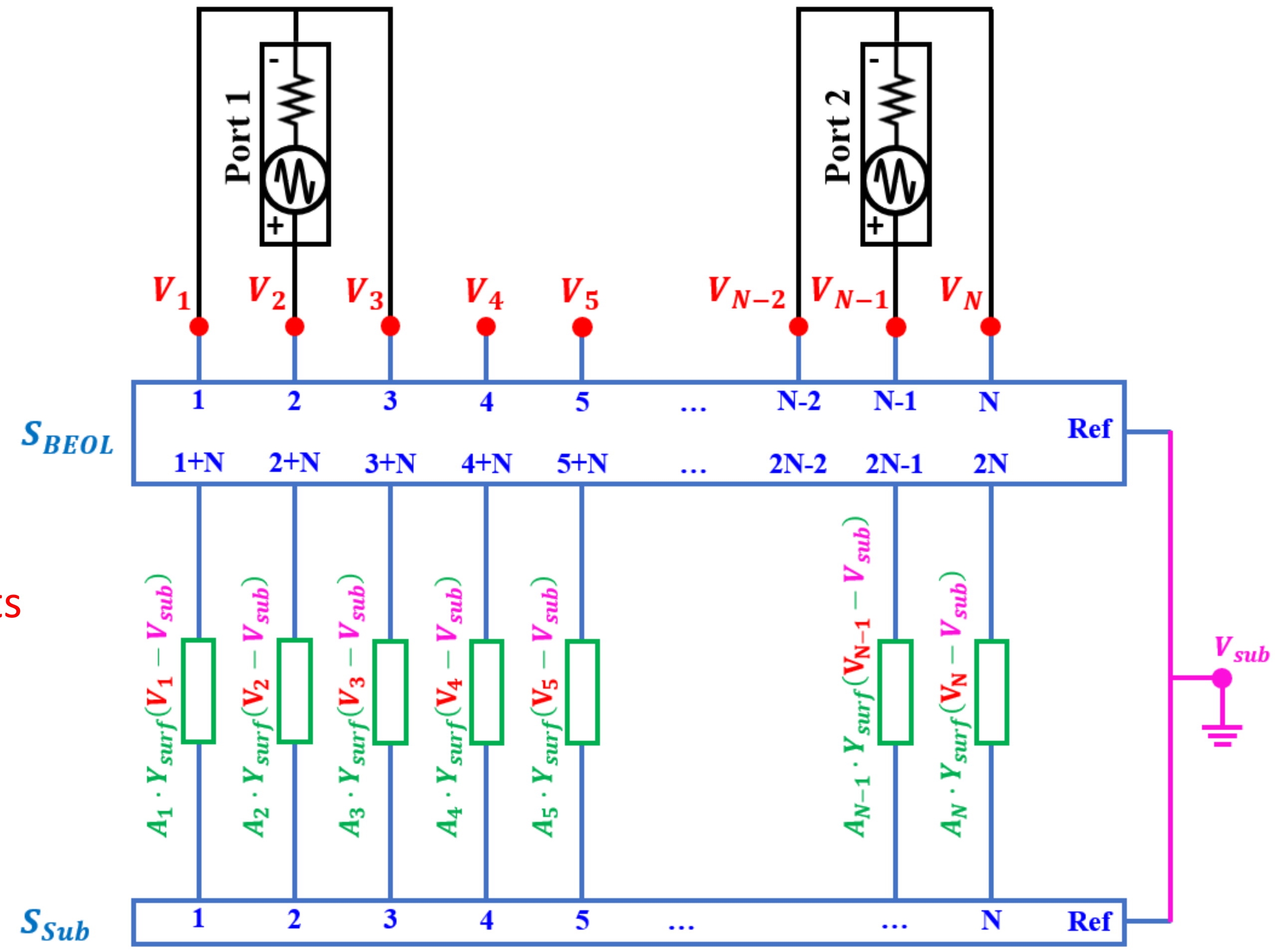
→ Could it be extended to arbitrary passive RF layouts ?



Model Extension to Arbitrary Layout Structures

Arbitrary layout simulation - A proposed approach

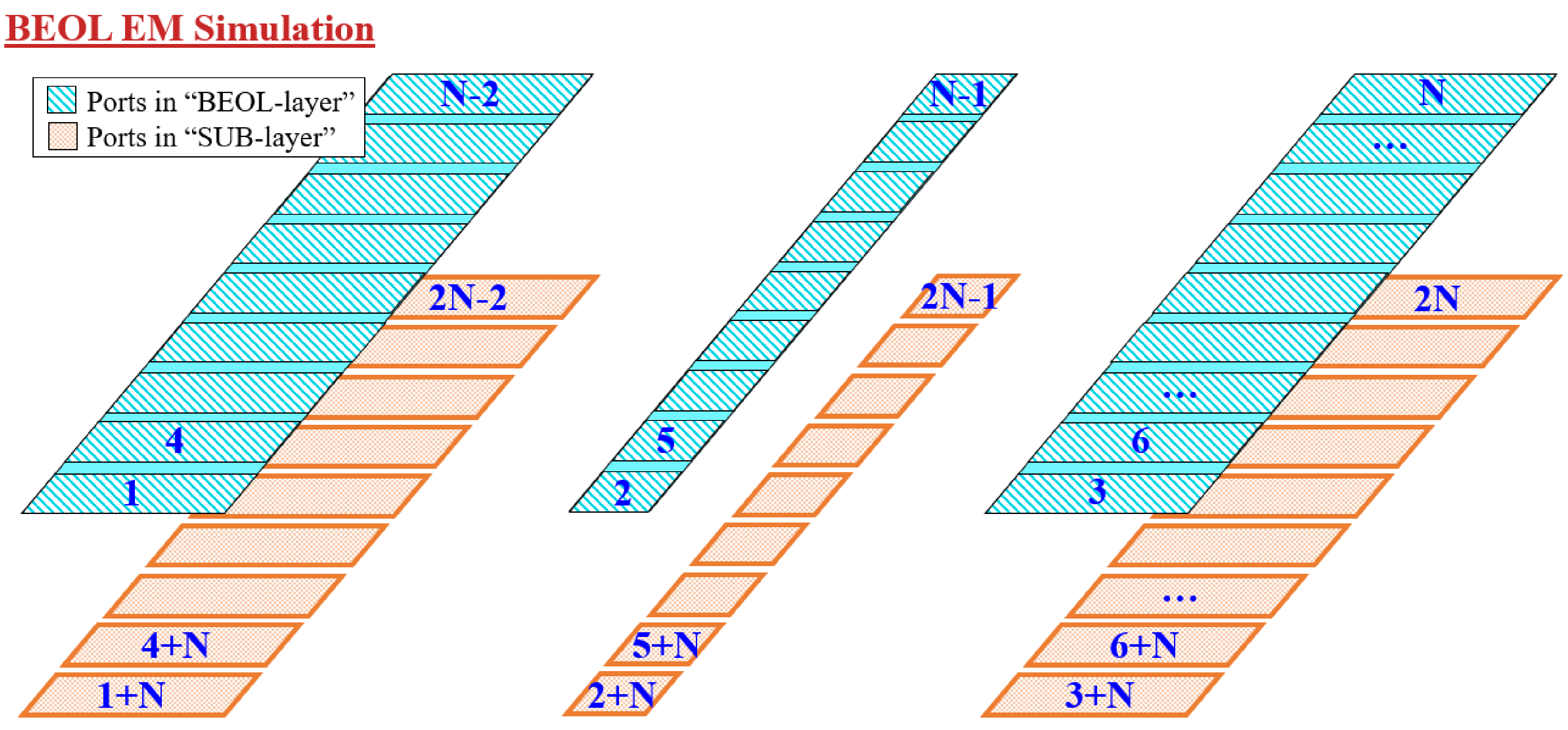




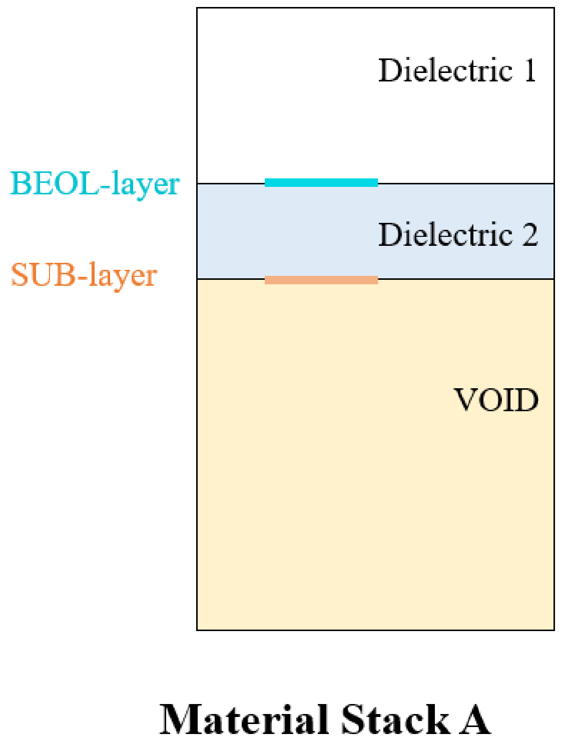
Large-signal simulation methodology combining:

- a 2N-port EM simulation file S_{BEOL}
- an N-port EM simulation file S_{SUB}
- N non-linear dipole admittances $Y_{surf}(V)$

Sim. 1: Linear BEOL



(a)



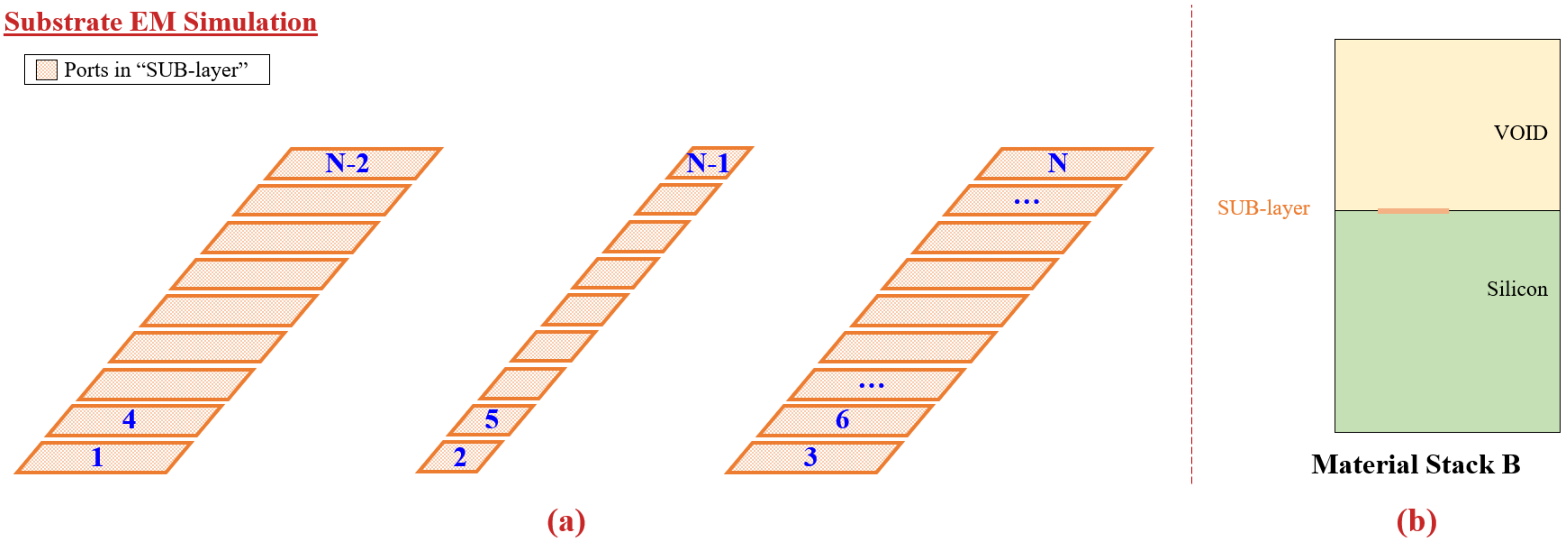
(b)

BEOL EM Simulation.

(a) Layout representation and 2N port definitions.

(b) Material stack used for the BEOL EM layout simulation.

Sim. 2: Linear Si Subtrate Regions



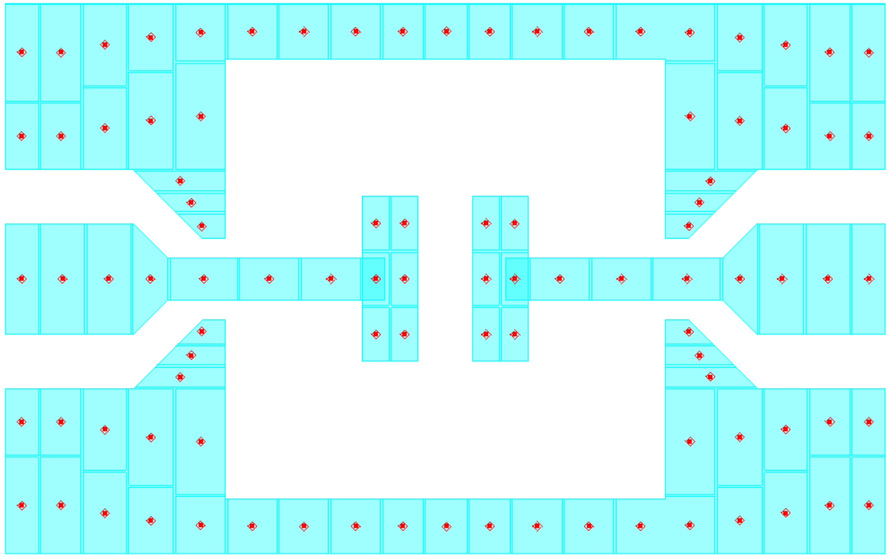
Substrate EM Simulation.

(a) Layout representation and N port definitions.

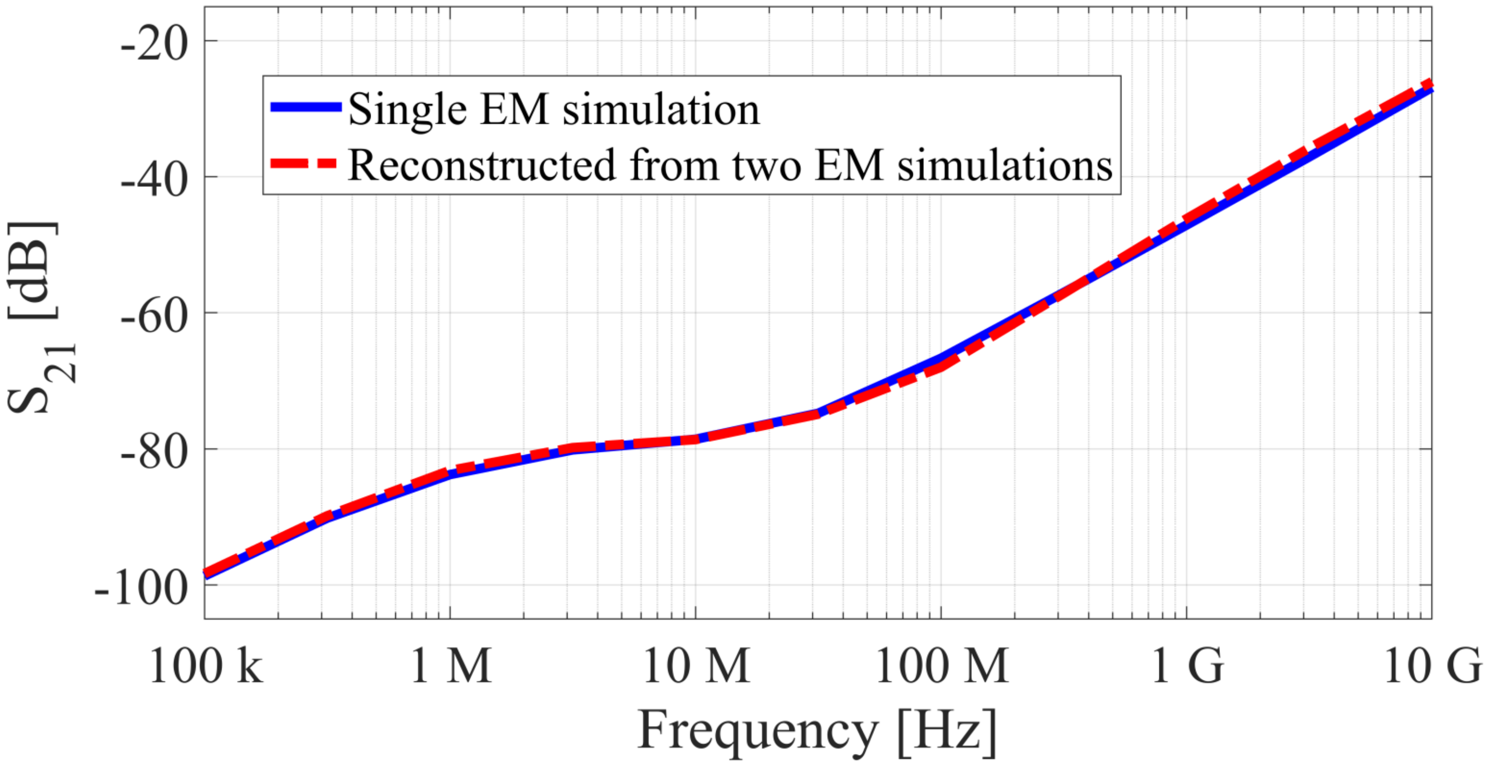
(b) Material stack used for the Substrate EM layout simulation.

Initial validation of the approach

Under small-signal



Two-port crosstalk layout and representation of the EM ports (N = 96).



Simulated S_{21} of the two-port crosstalk structure of using 2 approaches:

1. A single EM simulation and six pins to excite the two GSG ports of the structure.

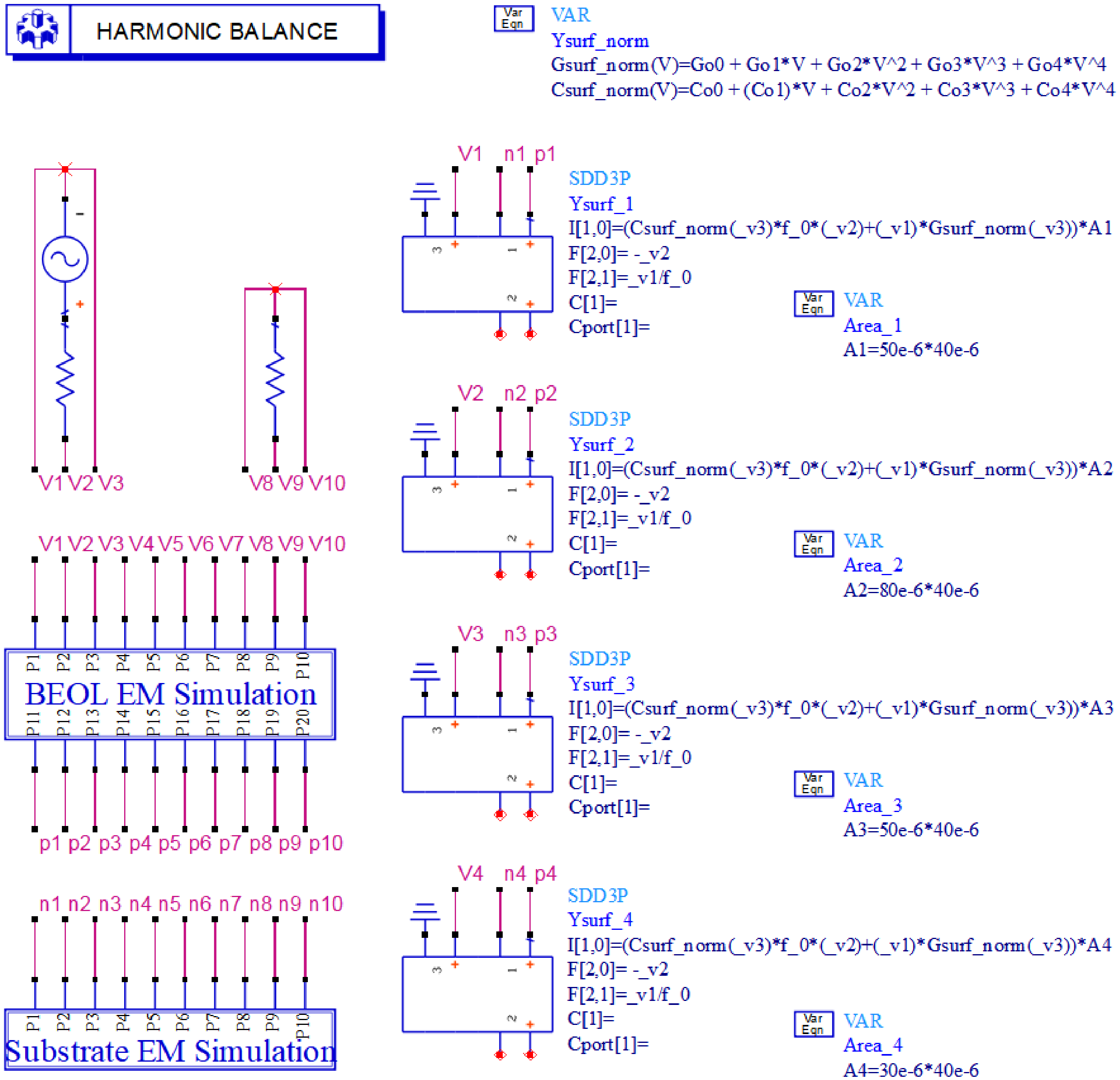
2. Combining two separate EM simulations employing respectively N ports and 2N ports, that are then reconnected together to model the entire layout and materials.

Practical implementation

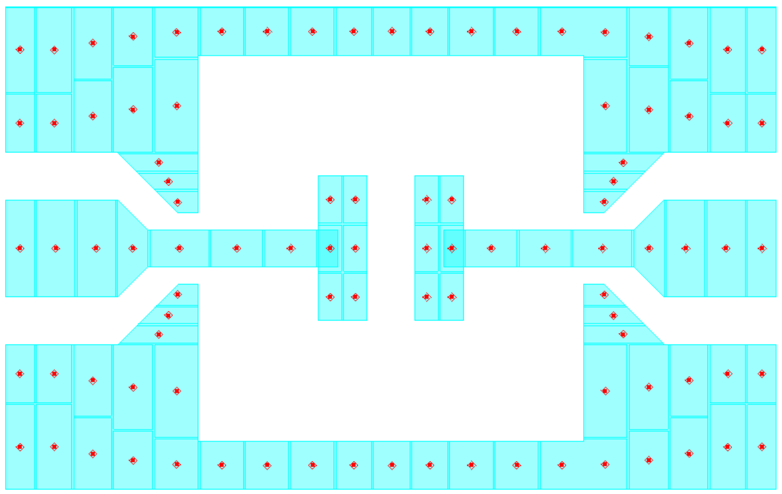
Harmonic Balance

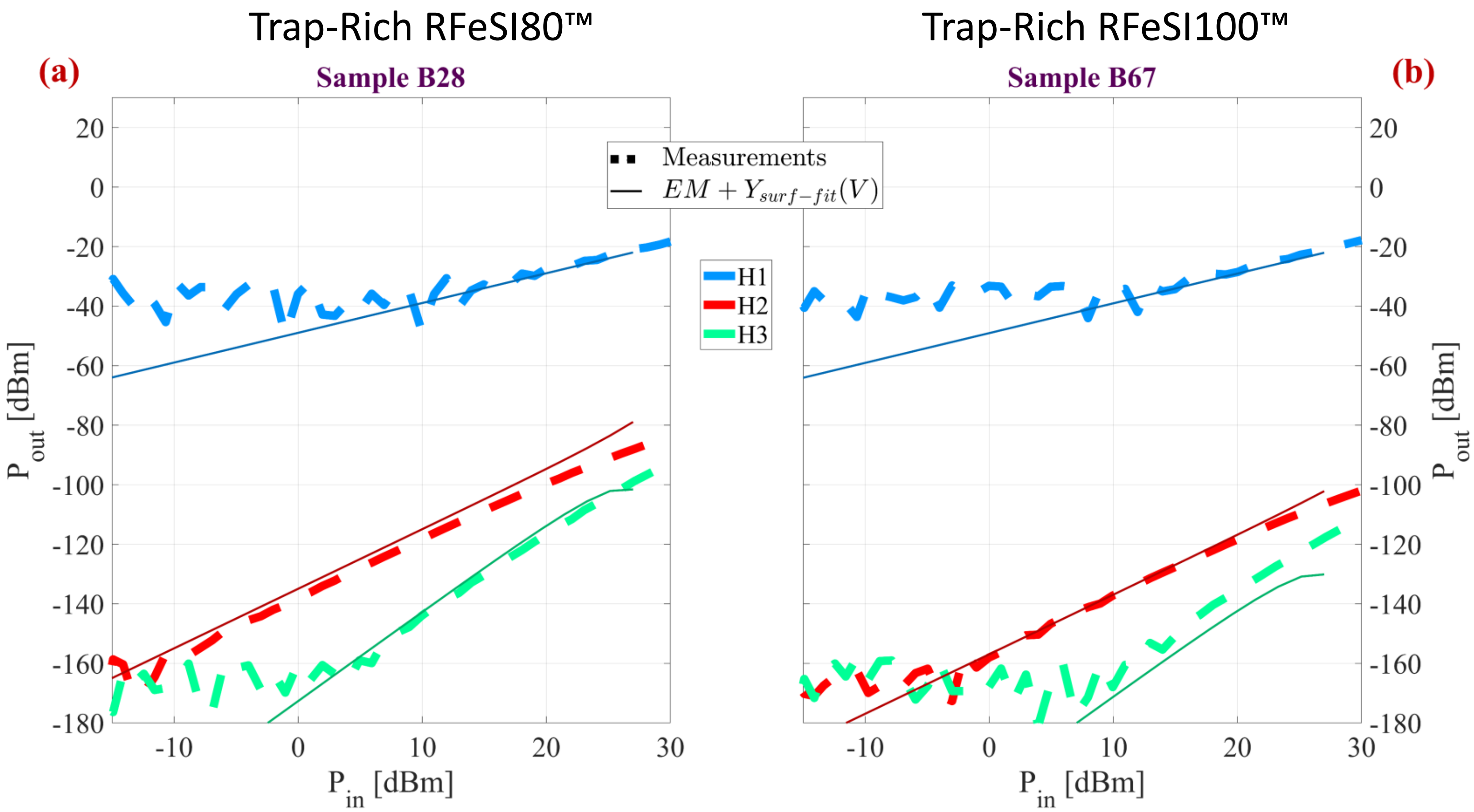
Large-signal simulation approach using ADS harmonic balance combining:

- Two EM S-parameter files (BEOL EM Simulation and Substrate EM Simulation)
- N non-linear surface admittance elements $Y_{surf}(V)$.



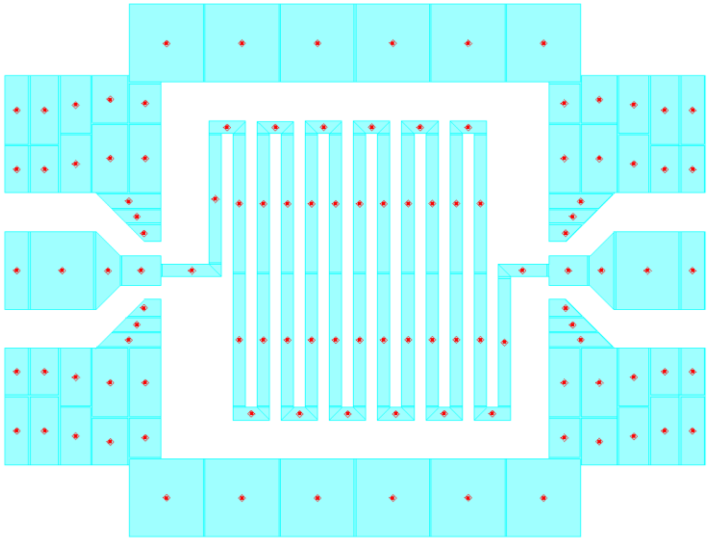
Model on arbitrary layout: *2-port crosstalk structure*



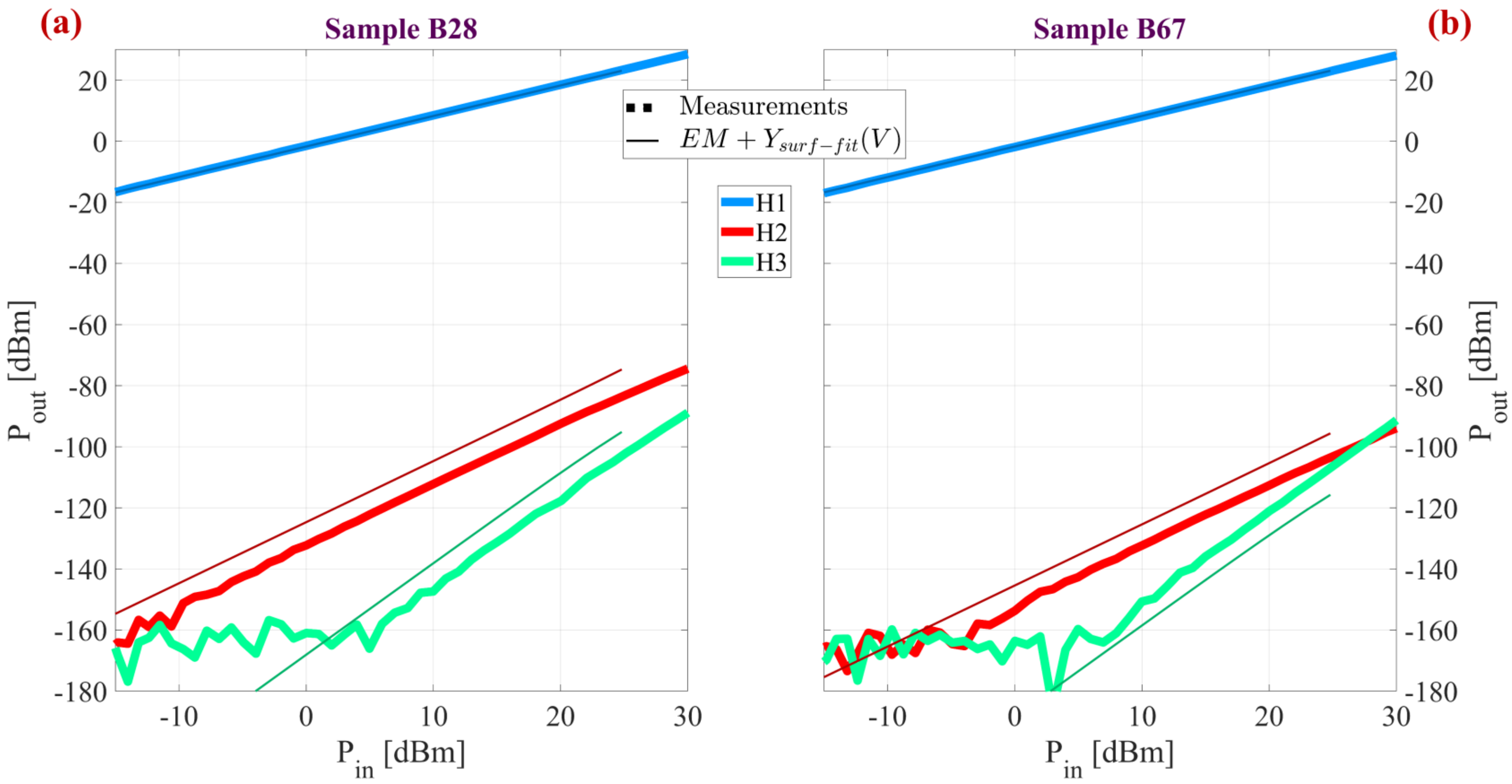


Measured and simulated power of the output components of the **crosstalk structure** on samples **B28** and **B67** for a **900 MHz** input signal of power P_{in}. Low noise floor (-170 dBm) measurements courtesy of ***Incize***.

Model on arbitrary layout: *2-port Meander Line*

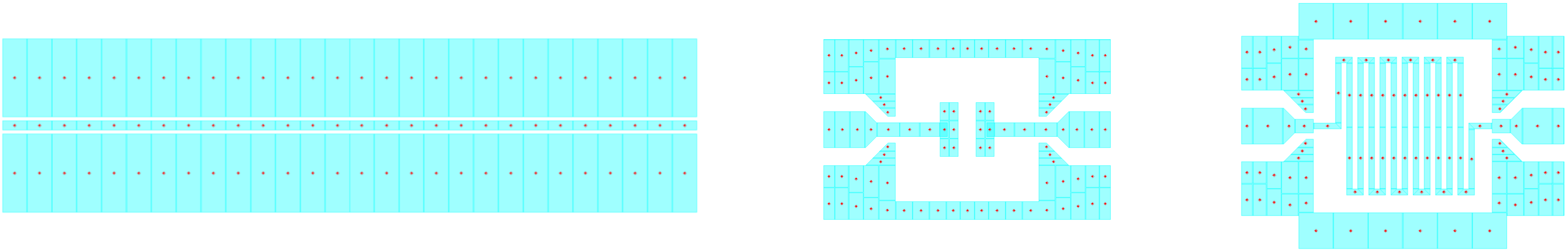


Trap-Rich RFeSI80™ | Trap-Rich RFeSI100™



Measured and simulated power of the output components of the **inductive meander line** on samples **B28** and **B67** for a **900 MHz** input signal of power P_{in}. Low noise floor (-170 dBm) measurements courtesy of ***Incize.***

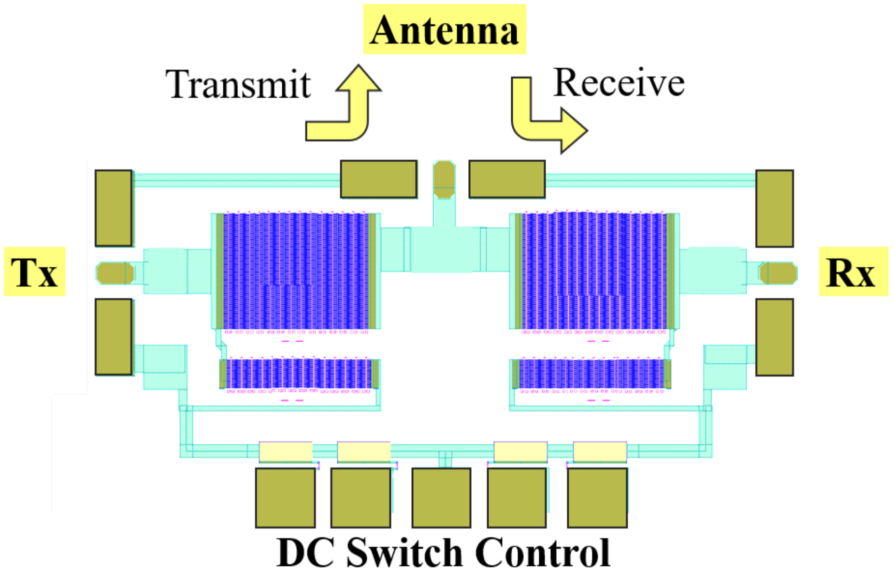
Model to hardware correlation



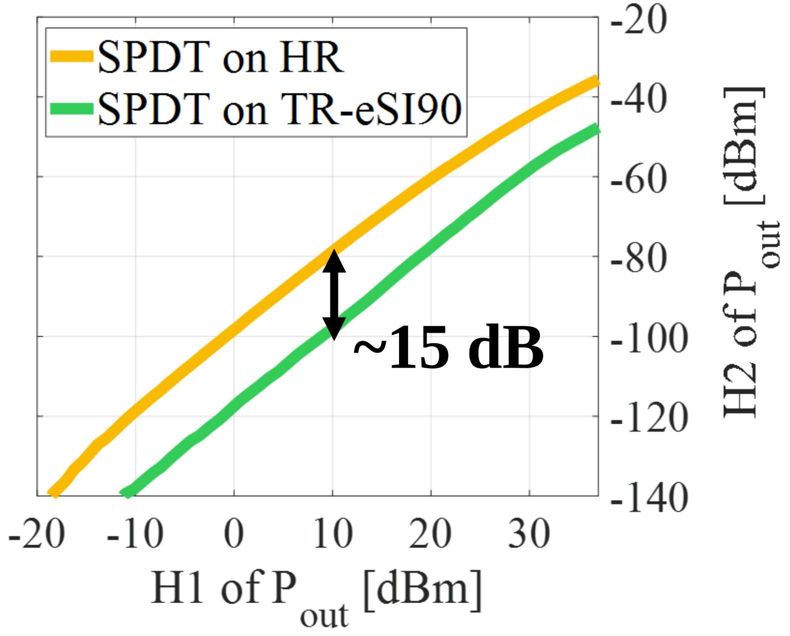
		CPW		Crosstalk		Meander	
		Meas.	Model	Meas.	Model	Meas.	Model
B28	$H1$	+14.6	+14.6	-33.2	-34.0	+13.5	+13.3
	$H2$	-82	-84	-109	-106	-102	-95
	$H3$	-110	-113	-130	-128	-131	-123
B67	$H1$	+14.6	+14.6	-33.3	-34.0	+13.2	+13.3
	$H2$	-102	-104	-128	-127	-122	-116
	$H3$	-138	-141	-150	-155	-135	-142

Table Recap of the model to hardware correlation for the three considered layouts using the $EM + Y_{surf\text{-}fit}(V)$ approach. All data is expressed in dBm and is taken a +15 dBm of fundamental input power at 900 MHz.

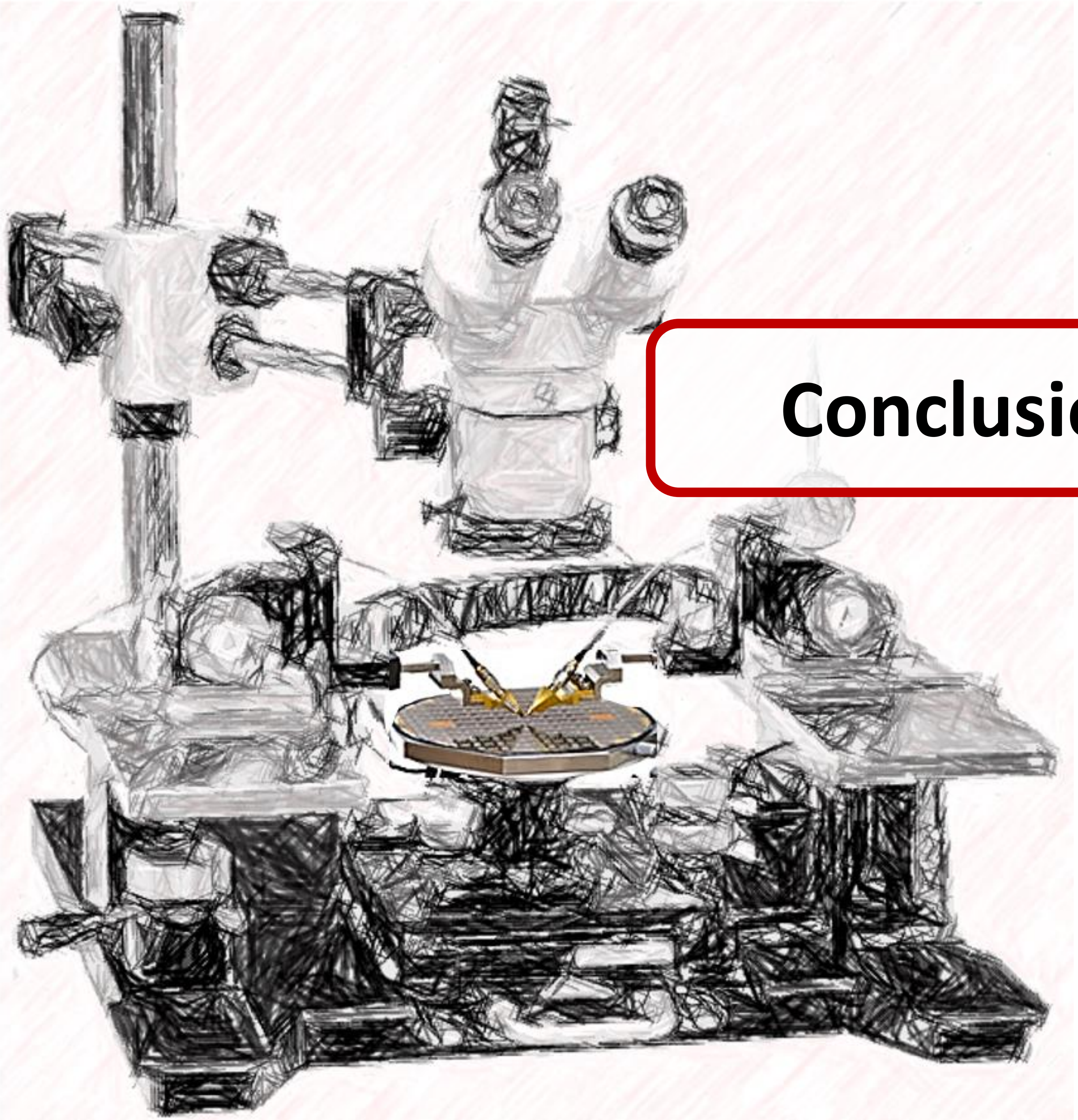
Example of substrate impact:



$f_0 = 900\ MHz$



Next steps: ***Simulate such substrate impact***



Conclusion and Take-Aways

Conclusion

- **Stringent linearity** specification for advanced telecommunications
  - Overall RFIC linearity affected by the substrate

- **Large-signal modelling is a challenge**
  - Account for static and dynamic behaviours of carriers and traps
  - Under non-equilibrium transient RF signal excitations

Dynamic effects and trap/carrier inertia (time constants) were highlighted

The concept of instantaneous substrate impedance out of equilibrium was introduced, accounting for such effects

- **Modelling of arbitrary RF layouts**
  - Combining TCAD transient instantaneous surface impedance descriptions with full EM simulations of linear material regions
  - Promising initial results

Take-Aways

Need for specially optimized/engineered RF substrate solutions

The physical phenomena associated to *Parasitic Surface Conduction* and to trap-rich passivation was reviewed

Large-signal CPW model (2D cross-section coupled with T-line theory) developed in TCAD with good results

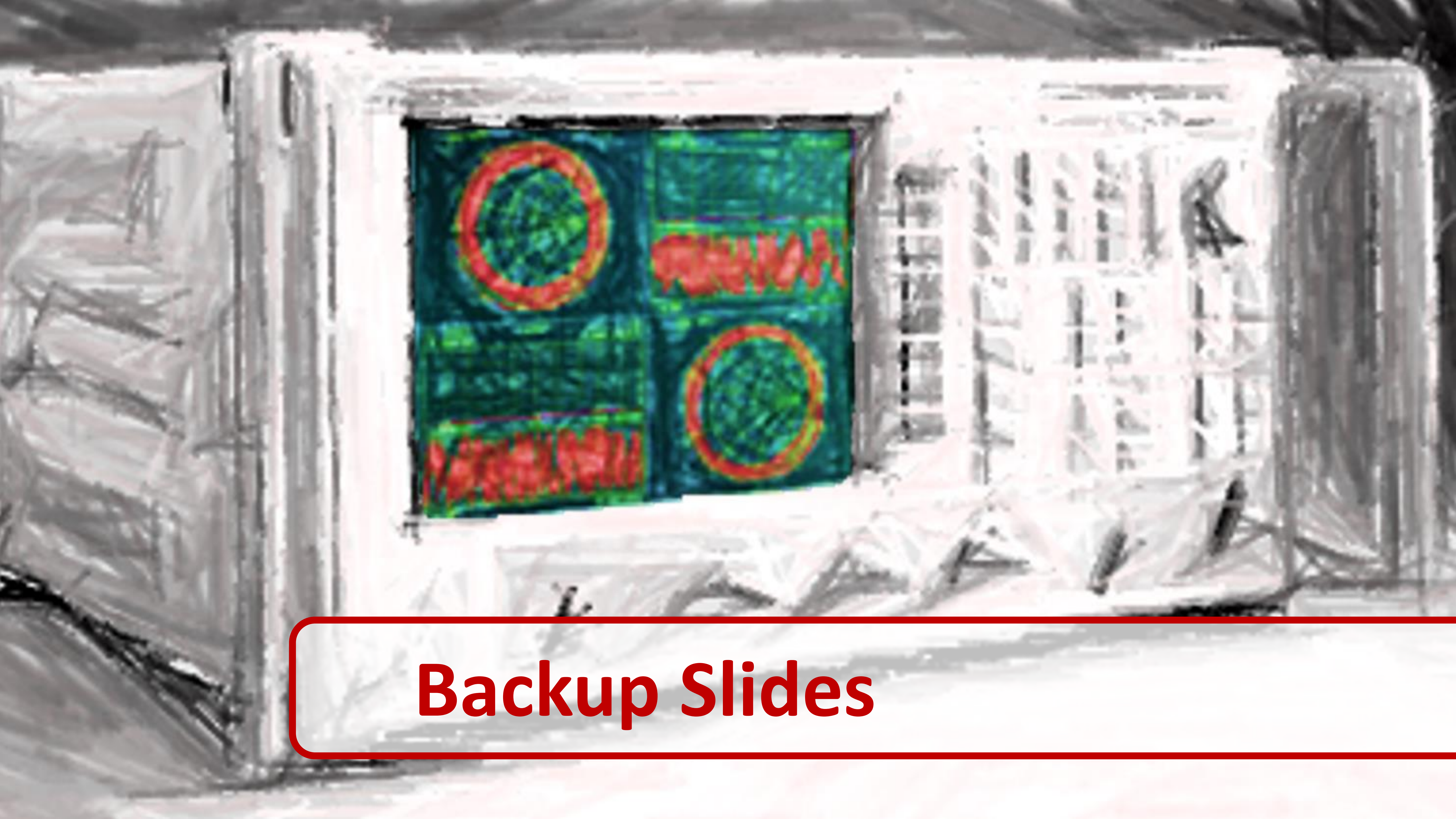
Work starting with an EDA company at the end of 2021

Interest of such Modelling:

1. Support the development of future/novel RF substrate solutions
2. Evaluate the linearity impact of the substrate in an RF module during IC design

Thank you for your attention

Contact: martin.rack@uclouvain.be



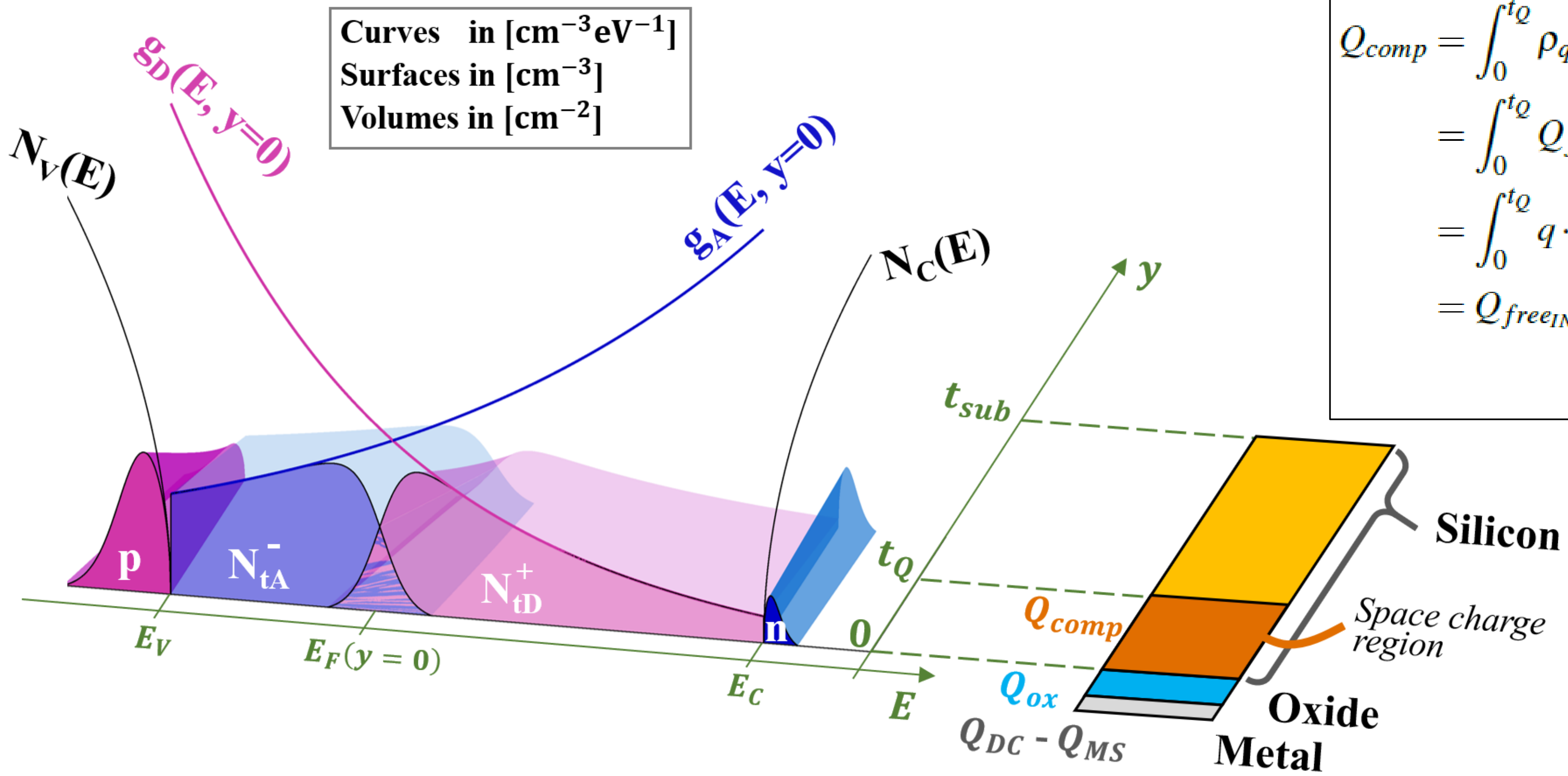
Backup Slides

Quantitative Charge Balance

$$Q_{Applied} = Q_{DC} + Q_{ox} - Q_{MS} \quad [\mathrm{C \cdot cm^{-2}}] \quad \textbf{(3.49)}$$
$$= V_{DC}C_{ox} + Q_{ox} - V_{MS}C_{ox} \quad [\mathrm{C \cdot cm^{-2}}] \quad \textbf{(3.50)}$$

$$Q_{comp} = -Q_{Applied} \quad \text{at equilibrium} \quad [\mathrm{C \cdot cm^{-2}}] \quad \textbf{(3.51)}$$

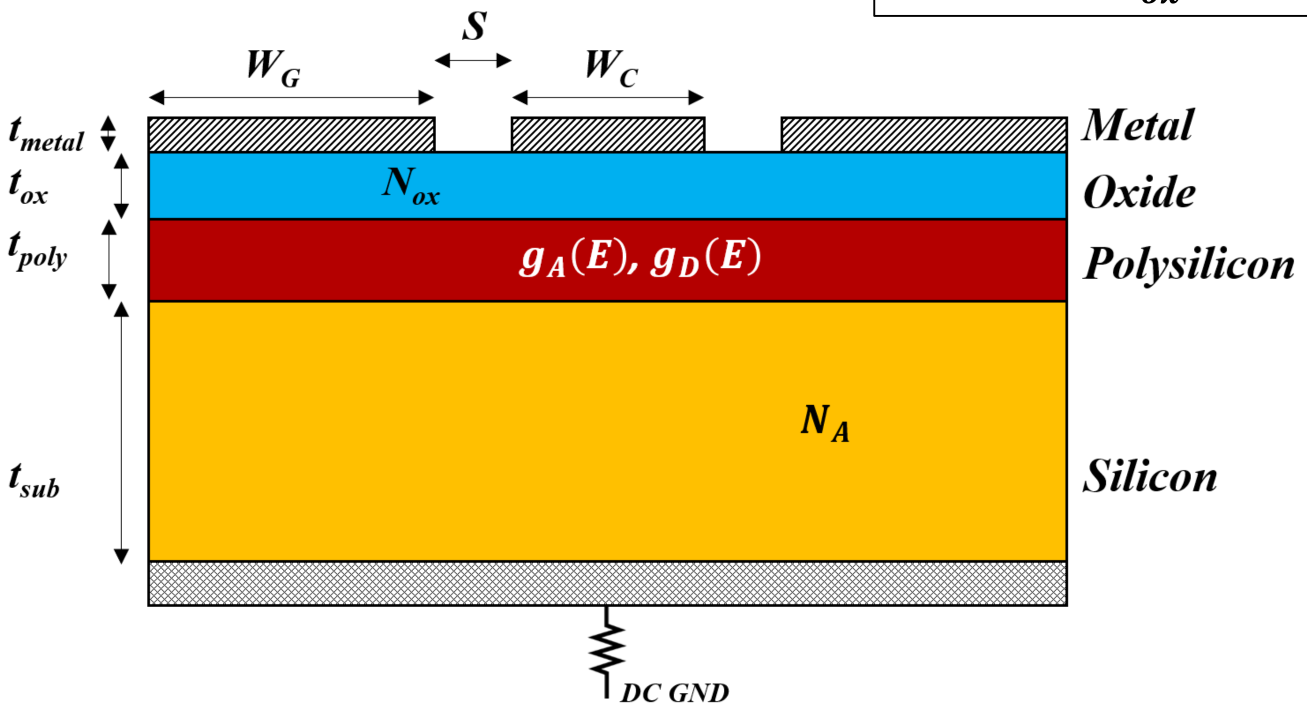
$$\begin{aligned} Q_{comp} &= \int_0^{t_Q} \rho_q \, dy \\ &= \int_0^{t_Q} Q_{free} \, dy + \int_0^{t_Q} Q_{trap} \, dy \\ &= \int_0^{t_Q} q \cdot (p - n) \, dy + \int_0^{t_Q} q \cdot (N_{tD}^{+} - N_{tA}^{-}) \, dy \\ &= Q_{free_{INT}} + Q_{trap_{INT}} \end{aligned} \quad [\mathrm{C \cdot cm^{-2}}] \quad \textbf{(3.52)}$$



free carriers & ionized traps

Traps for RF performance

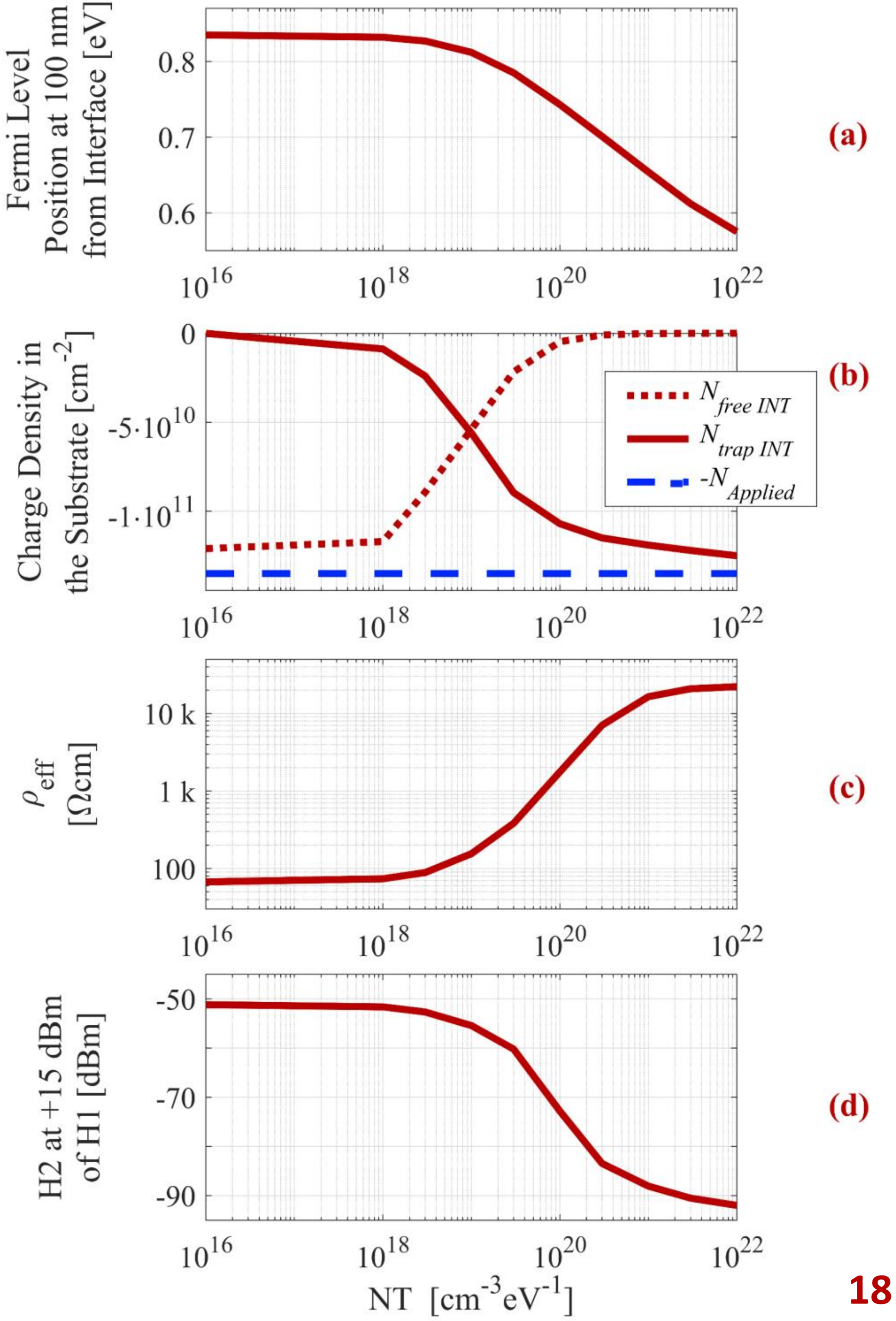
HR bulk & $N_{ox} = 10^{11}\ \text{cm}^{-2}$



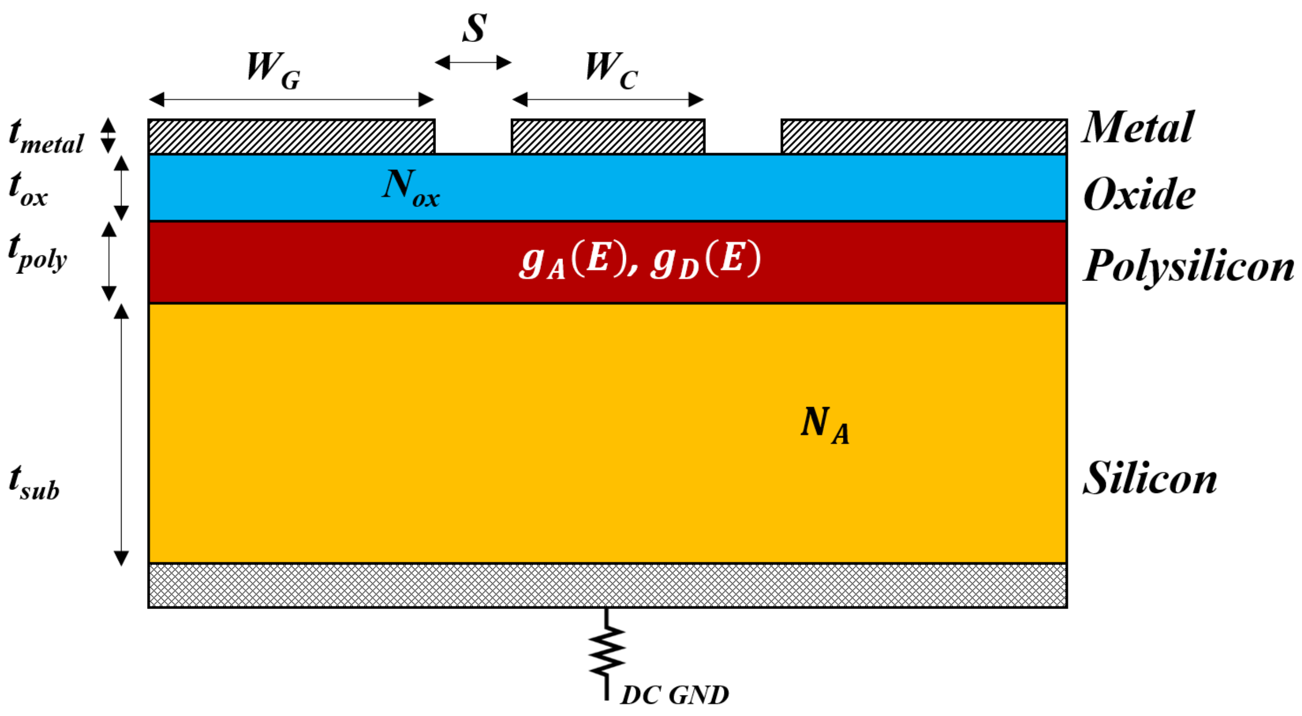
Trap densities $g_A(E)$ and $g_D(E)$ are proportional to parameter NT

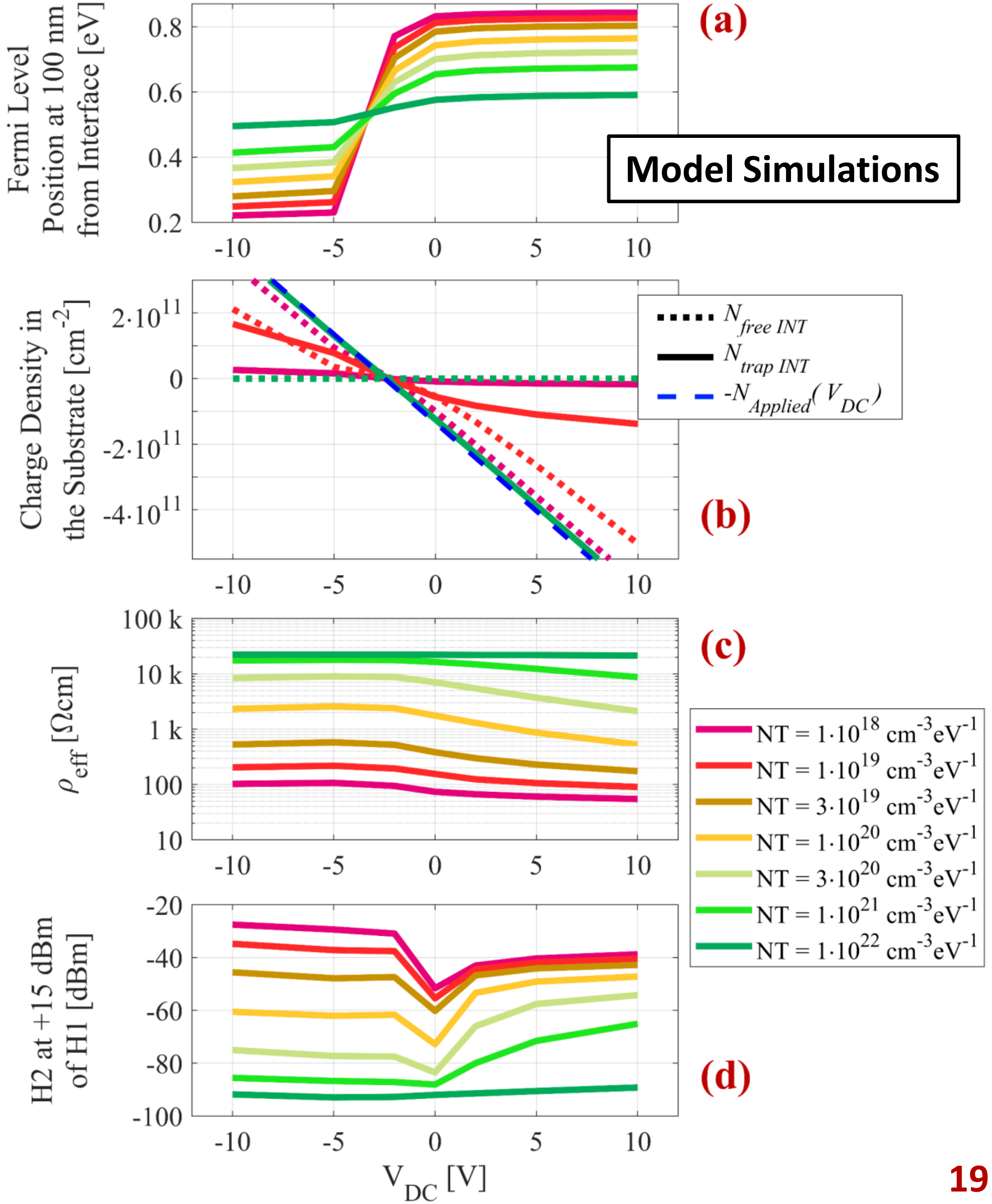
As NT increases:

- Interface **Fermi level** moves deep.
- **Ionized traps** provide the majority of the compensation charge.
- Substrate impedance ρ_{eff} **increases**.
- Substrate becomes **more linear.**



Traps for RF performance – bias dependency





As *NT* increases:

- Interface Fermi level becomes **tightly pinned**.
- Small variation in E_F results in large variations in N_{trap}, and little in N_{free}.
- Substrate impedance $\rho_{eff}(N_{free})$ **becomes bias independent**.
- Substrate linearity also.