PN Junctions Interface Passivation in 22 nm FD-SOI for Low-Loss Passives

L. Nyssens[1], M. Rack[1], M. Nabet[1], C. Schwan[2], Z. Zhao[2], S. Lehmann[2], T. Herrmann[2], D. Henke[2], A. Kondrat[2], C. Soonekindt[2], F. Koch[2], T. Kache[2], D. P. Kini[2], O. Zimmerhackl[2], F. Allibert[3], C. Aulnette[3], D. Lederer[1], J.-P. Raskin[1]

[1] Université catholique de Louvain, Louvain-la-Neuve, Belgium, E-mail: lucas.nyssens@uclouvain.be
[2] GlobalFoundries, Dresden, Germany
[3] Soitec, Bernin, France

***Abstract*— In this paper, GlobalFoundries' 22 nm fully depleted (FD) SOI process was run on standard and high-resistivity wafers with a designed PN junctions interface passivation solution to counter parasitic surface conduction (PSC) effects. Substrate quality is monitored in terms of effective resistivity (ρ_{eff}) and losses based on on-wafer measurements of coplanar waveguides (CPW), fabricated in either bottom or top metal layers. Several PN patterns are examined and they demonstrate effective passivation of the PSC, enabling ρ_{eff} values in the kΩ.cm range. Patterns with intrinsic region separating the P- and N- doping regions show better performance, which can further be improved applying a reverse PN bias to widen the depletion regions. 50 Ω CPW line designed with PN interface passivation achieves 0.15 dB/mm lower propagation losses at 15 GHz than 50 Ω thin-film microstrip line in this technology. Impact of substrate quality on a 5-20 GHz inductor is analyzed by comparing substrates with standard resistivity, high-resistivity with PSC and high-resistivity with PN junction solution, showing an upto 62% improvement in quality factor.**

Keywords*— *FD-SOI, High-Resistivity, Parasitic Surface Conduction, PN junctions, Effective Resistivity, CPW line, TFMS line, Spiral Inductor.

I. Introduction

Nowadays, advanced CMOS nodes are competitive for radio-frequency (RF) and mm-wave applications, featuring f_t and f_{max} in the range of 300 to 400 GHz [1]. The recent CMOS technologies for mm-wave applications typically offer rich back-end-of-line options with several thick metal layers enabling low-loss RF/mm-wave passives and interconnects.

The silicon substrate is part of the electromagnetic environment of such passives and devices and can significantly affect the passives and devices high-frequency behavior. The substrate can be responsible for significant amounts of losses, coupling and non-linear signal distortion [2], particularly if the silicon resistivity is low.

High-resistivity (HR) silicon substrates (with nominal resistivity ρ_{nom} > 1 kΩ.cm) improves these effects compared with standard doped silicon (ρ_{nom} = 10 to 20 Ω.cm), though the benefits are hindered by the *parasitic surface conduction* (PSC) effect. A PSC layer is induced by fixed positive charges at the Si/SiO_2 interface that attract significant amounts of free electrons, forming a thin highly conductive layer [3, 4]. Different interface passivation techniques have been developed to counter the PSC layer, the most widespread of which is the *trap-rich* solution [4]. Despite its strong industrial success in partially depleted (PD) SOI nodes, the transposition to FD-SOI technologies is not straightforward and there are currently no trap-rich options available.

The *PN interface passivation* technique is then particularly of interest for FD-SOI. Implanting alternatively P- and N-type doping creates a chain-series of PN junctions thereby locally interrupting the conductive interface by induced depletion junctions. It has been demonstrated to successfully counter the PSC effect and improve the RF quality of high-resistivity substrates [5-8]. This passivation scheme was first described in [5, 6], then tested in a short-loop process with better lithography (smaller features) resulting in improved RF performance [7]. In [8], the *PN interface passivation* solution is applied within the industrial GlobalFoundries' 22FDX® line run on standard and HR SOI wafers provided by Soitec.

In this paper, we analyze the effect of different PN passivation patterns designed and fabricated in the same run as in [8, 9] on the behavior of coplanar waveguide (CPW) lines and a 5-20 GHz inductor. The improved RF quality of the substrate is demonstrated through substrate losses (described by the effective resistivity, ρ_{eff}) and non-linearity reduction in CPW lines, and increased quality factor of inductors.

II. Fabricated Structures

Several passives and PN passivation patterns were designed. Each passive was replicated several times to include different PN passivation patterns, which were processed on wafers of different resistivities: 10 Ω.cm (std), 620 Ω.cm (HR1) and 985 Ω.cm (HR2).

A. Passive structures

The first set of CPW lines is designed in the last Cu layer "QB" (3 µm-thick and approximately 10 µm away from the Si substrate) and has a signal line width w of 35 µm, and a signal to ground spacing s of 25 µm. The second set of CPW lines is formed in stacked M1 and M2 (combined thickness of 0.17 µm, and approximately 130 nm from the Si substrate) using w = 20 µm and s = 20 µm. Additionally, a set of thin film microstrip lines (TFMS) is designed with the signal line width of 10 µm implemented in QB and ground plane in the 5 thin bottommost metal layers stacked for a combined thickness of ~400 nm at a distance of approximately 9 µm below the signal line. The CPW and TFMS lines dimensions were selected to have a 50 Ω characteristic impedance (Z_c) for a meaningful performance comparison. Lines of multiple lengths (760 µm and 2000 µm) were fabricated, along with dedicated Open and Thru structures, to enable a wideband multi-Through-Reflect-Line (mTRL) calibration and extraction of the line's equivalent RLGC parameters [10].

An inductor for operating frequencies from 5 to 20 GHz is designed on the QB layer. A sketch of the inductors and their geometrical dimensions are presented in the inset of Fig. 3.

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B. PN Interface Passivation Patterns

Two types of PN passivation patterns are considered in this paper: (i) *PNlines* and (ii) *PNgrid*. They are both represented in Fig. 1, and serve to increase the impedance between two terminals through the substrate (for instance the S and G lines of the CPW by hindering the E-field path between these with multiple highly-resistive depletion regions). The *PNlines* patterns include a DC biasing option through on-chip high-valued resistor elements. This allows for the reverse DC biasing of the PN junctions to widen the depletion regions and further increase substrate impedance. Out of the *PNlines* type solution, four different patterns are obtained: (i) different P-/N-doped region widths, (ii) presence of an intrinsic region between the P-/N-doped regions or not. Small dimensions were used to define the patterns in compliance with the process design rules (Fig. 1).

III. RF Performance Results

A. Transmission Lines

The RF performance results of the CPW lines in M1-M2 are summarized in Fig. 2(a) and (b) in terms of effective resistivity, describing the substrate RF losses. As expected, the std substrate ρ_{eff} tends to 10 Ω.cm after the slow-wave mode (~> 20 GHz). The 985 Ω.cm and 620 Ω.cm high-resistivity substrates without any PN pattern suffer from PSC effect, featuring an effective resistivity of, respectively, 49 and 54 Ω.cm (at 15 GHz). The *PNlines* pattern (A) effectively solves the PSC issue and retrieves high values of effective resistivity (290 and 190 Ω.cm for HR1 and HR2, respectively, at 15 GHz). The effectiveness of the PN patterns decreases with frequency due to the frequency-decreasing capacitive impedance in the depletion regions, which translates in a decreasing $\rho_{eff}(f)$. Applying a reverse bias to the P-doped and N-doped regions widens the depletion regions, which further improves the effective resistivity to 520-580 Ω.cm at 15 GHz.

Fig. 2(b) shows the effective resistivity extracted from the M1-M2 CPW lines on the HR 985 Ω.cm substrate with different PN patterns. The *PNgrid* pattern features the lowest substrate losses when no bias is applied, with ρ_{eff} = 440 Ω.cm at 15 GHz. For both pattern widths, the presence of an intrinsic region between the P-/N-doping regions improves the effectiveness of the PN passivation solution by widening the depletion regions. In this run (with fixed implant energy and dose parameters), a width of 350 nm yields the best results. It is also interesting to note that applying a reverse bias to the

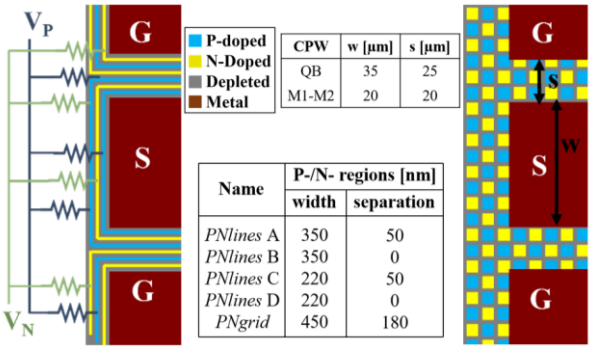

Fig. 1. Sketch and dimensions of designed PN passivation patterns and CPW lines.

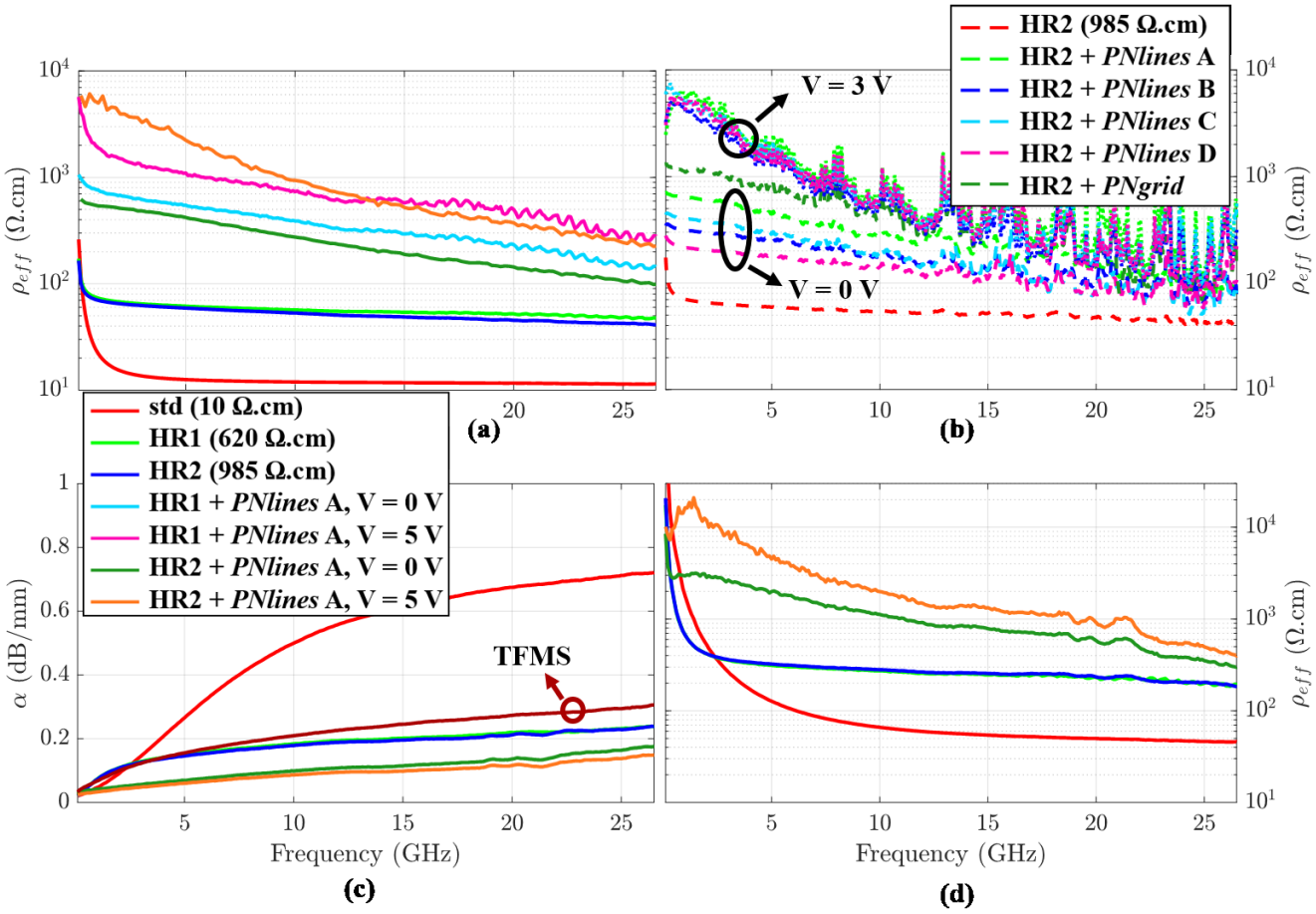

Fig. 2. ρ_{eff} extracted from M1-M2 CPW lines measurements on (a) different substrates and on (b) HR2 with different PN patterns. (c) Line insertion loss (α), and (d) ρ_{eff} extracted from QB CPW lines measured on different substrates.

PN junctions improves the substrate losses resulting in almost the same ρ_{eff} for all *PNlines* patterns.

The total propagation losses (α) and substrate effective resistivity extracted from the CPW lines in QB are shown in Fig. 2(c) and (d). Due to the ~10 µm-thick dielectric stack between the CPW line and substrate, the effective resistivity is averaged out and yields a larger ρ_{eff} compared with the values extracted from the M1-M2 CPW lines. The same trends are observed with respect to the effective resistivity among the various substrates. The propagation losses of the 50 Ω TFMS lines is also reported in Fig. 2(c). TFMS line is usually the prefered topology for transmission line in CMOS technology using std resistivity substrate, as all losses are purely metallic losses. Nevertheless when a quasi-lossless substrate is available, a CPW topology is more interesting, thanks to the additional flexibility of being able to minimize metallic losses while targeting a fixed characteristic impedance. In this work, we demonstrate a 0.15 dB/mm improvement in α at 15 GHz with a 50 Ω CPW line with the reverse biased *PNlines* A on a HR substrate, compared with a 50 Ω TFMS line.

B. *Inductors*

The inductors are measured from 100 MHz to 40 GHz. A 2-step calibration is performed (LRRM calibration on an ISS, followed by an on-wafer mTRL calibration using the TFMS set of lines [11]) to move the reference plane to the DUT vicinity with high accuracy at mm-wave frequencies [12]. The inductance (L) and quality factor (Q) of the inductors are computed as $L = Im(1/Y_{11})/\omega$ and $Q = Im(1/Y_{11})/Re(1/Y_{11})$.

Fig. 3 shows the 1 nH inductance and quality factor of the inductor on several substrates. The quality factor is normalized by the peak value of Q on the standard resistivity substrate ($Q_{peak,std}$ = 16). The RF inductor quality factor is greatly improved as we move from a std substrate to a HR substrate thanks to a much greater bulk resisitivity. Indeed, the peak Q value is around 1.5 times higher (from 16 to 24) and shifted to higher frequencies. Further improvement (from 24 to 26) is achieved thanks to the 3 V reverse biased PN junctions, which significantly increases the substrate resistivity at the interface at high frequency.

The effective resistivity of CPW lines in QB on HR substrate is substantially increased by the use of PN junctions (up to x4 at 20 GHz, see Fig. 2). The gain in propagation losses is also considerable (-0.1 dB/mm at 20 GHz), but is not as large as the one achieved for the CPW lines in M1M2 (-0.5 dB/mm at 20 GHz). As explained above, the signal line in QB is separated from the substrate by a ~10 µm-thick dielectric stack. As a consequence, the overall shunt losses (related to the effective resistivity) are already rather low, because there is a lower concentration of electric field inside the substrate (compared to the CPW lines in M1M2).

The same reasoning explains why the further improvement in the inductor quality factor gained by the use of PN passivation solution on a HR substrate is limited (24 to 26 in peak value). Indeed, since the coil is in QB, the electric field concentration inside the substrate is not as large as if it were in M1M2. Therefore, the overall shunt losses in the substrate are already limited by the sole use of a high-resistivity substrate. And, as demonstrated here, these losses have been further reduced (only by a small extent in absolute since they are already rather small) with the PN patterns. The authors believe the PN passivation solution can lead to a stronger improvement in inductor quality factor if the inductor coil is closer to the substrate (hence being more sensitive to substrate losses). This can be realized either by stacking several metal layers (which will also reduce metallic losses and further increase Q [9]) or by having a thinner back-end of line, i.e. made of fewer metal layers.

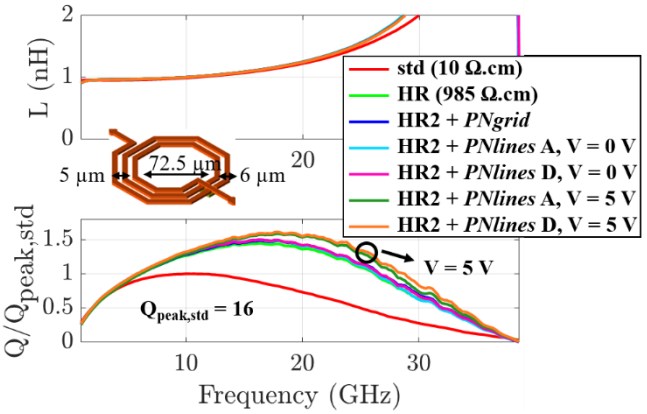

Fig. 3. Inductance (L) and normalized quality factor (Q) of 5-20 GHz inductors on different substrates, with or without interface passivation.

IV. Conclusion

In this paper, several patterns of the PN passivation solution of HR interfaces have been designed and fabricated in an advanced industrial design flow, the 22FDX® node from GlobalFoundries.

Strong improvement in substrate effective resistivity and losses have been observed for CPW lines designed in M1-M2 and QB metal layers: with ρ_{eff} as high as 580 and 1300 Ω.cm at 15 GHz, respectively. QB CPW lines with the PN solution features lower propagation losses than 50 Ω TFMS lines (up to 0.15 dB/mm reduction at 15 GHz).

Several PN patterns with different dimensions are investigated. Among all patterns without applying any bias, the PN grid array presents the lowest substrate losses (still 8 times lower than HR without any interface passivation, i.e. suffering from PSC, at 15 GHz). It also has the advantage of not requiring a co-design with the passive's layout, as it can be patterned as a regular array beneath it. It is also demonstrated that having an intrinsic region between the P-/N-doped regions further enhances the PN passivation effectiveness. Reverse biasing the PN junctions to increase the depletion region width and the substrate impedance is shown to further lower substrate losses. A boost in ρ_{eff} by a factor x2 to x3 with a 5 V bias is observed, achieving ρ_{eff} values in the kΩ.cm-range below 6-8 GHz.

Measurements show a strong improvement (50%) in the quality factor of a 5-20 GHz inductor moving from a standard resistivity to a high-resistivity substrate without interface passivation. Further 8% improvement can be achieved with reverse biased PN interface passivation, thanks to an increased substrate resistivity at the interface.

Overall, the PN passivation offers high quality RF substrate for low-loss passives compatible with an industrial FD-SOI technology.

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