LEAKAGE COMPONENTS IN FULLY-DEPLETED SOI CMOS TECHNOLOGY: IMPLICATIONS ON I_{DDQ} TESTING

B. Iñíguez [(1)], J. P. Raskin [(2)], P. Simon [(2)], D. Flandre [(1)] and J. Segura [(3)]

Microelectronics [(1)] and Microwave [(2)] Laboratories, Université catholique de Louvain (UCL), Place du Levant 3, B-1348 Louvain-la-Neuve, Belgium

[(3)] Physics Department, Universitat de les Illes Balears (UIB), Cra. de Valldemossa, Km. 7.5, Palma de Mallorca, Spain

Abstract

Silicon-On-Insulator (SOI) is emerging as a strong technology candidate for low-power high–performance applications. In this work, based on experimental data, we analyze the fundamental aspects of current leakage in deep-submicron SOI CMOS technologies and we discuss the physical mechanisms and their dependence with bias, temperature and operating frequency. Subsequently, we evaluate the merits of parametric testing techniques based on current monitoring (as I_{DDQ} or I_{DDT} testing) when applied to this technology.

1. Introduction

Deep submicron bulk CMOS technology circuits may consume significant power even when the device is inactive due to current leakage. Such a leakage impacts circuit power consumption and limits the efficiency of parametric test methods based on quiescent current monitoring, such as I_{DDQ}, that have been used to uniquely identify some defect classes [1]. The replacement of bulk CMOS technologies with thin-film SOI CMOS may achieve much smaller channel lengths with still acceptable current leakage values [2], and benefit from parametric testing techniques as I_{DDQ}. A good understanding of the sources of intrinsic current leakage in modern thin film SOI CMOS technologies and their dependences on key parameters (as temperature, channel length, etc.) is required to evaluate the merits of these test methods.

In this paper we analyze the leakage mechanisms in SOI CMOS ICs as a first approach to explore the leakage properties of large SOI CMOS circuits in order to finally predict the validity of test techniques as I_{DDQ}. We report experimental results from transistors fabricated with a LETI 0.25 μm Fully Depleted (FD) SOI CMOS process technology using Si film thickness t_b=40 nm, front gate oxide thickness t_{oxf}=4.5 nm, and back oxide thickness t_{oxb}=380 nm [3] with a supply voltage of V_{DD}=1.25 V.

2. Leakage current sources in SOI MOSFETs

In long-channel devices the off-state current (I_{off}) is dominated by the *pn* junctions leakage. This contribution is drastically reduced in thin-film SOI CMOS circuits, since no well is needed to separate the

p-channel devices from the n-channel devices, and because the area of the drain and source depletion regions is limited by the back oxide (see Fig. 1). Typically, the drain leakage current is 15 to 100 times smaller in SOI than in bulk MOSFETs [2].

In modern deep-submicron technologies, both bulk and SOI CMOS, the weak inversion current becomes the main contribution to I_{off} at room temperature. The dominance of this current in the off-state is due to the low threshold voltage used to maintain performance, and to short-channel effects (mainly drain induced barrier lowering, DIBL, and charge sharing) that decrease the threshold voltage and degrade the subthreshold swing (S) which has a strong impact on I_{off}. The ideal value of S is 59 mV/dec at room temperature. In long-channel thin-film SOI MOSFETs the subthreshold swing can be very close to that ideal value, while in bulk MOSFETs is usually higher than 75 mV/dec. In short-channel devices, the subthreshold swing degradation is lower in FD SOI MOSFETs with respect to bulk MOSFETs thanks to the better control of the channel by the front gate [2]. In advanced bulk CMOS technologies, at room temperature, S is close or higher than 85 mV/dec (for 0.25 μm technologies [5]), while in thin-film SOI MOSFETs, we obtained very acceptable values of S = 70 mV/dec for channel lengths as short as 0.25 μm at room temperature.

Charge sharing reduces the threshold voltage at low drain bias as the channel length is reduced, thus also increasing I_{off}. Similarly to the other effects, the better gate control reduces charge sharing in thin-film SOI MOS with respect to bulk MOS [2,4]. Our measurements showed that the threshold voltage reduction due to charge sharing is about 0.06 V between effective channel lengths of 0.16 and 0.91 μm. A much stronger reduction (more than 0.1 V) is observed in typical 0.25 μm bulk CMOS technologies [5].

DIBL causes a reduction of the threshold voltage as the drain voltage is increased with a consequent increase of the weak inversion current. It becomes more important as the channel length is reduced, thus being an important limiting factor to technology scaling. The stronger gate control of the channel in thin-film SOI MOS devices provides an important reduction of the DIBL effect with respect to bulk MOS transistors of the same channel length [2,4].

Other possible leakage mechanisms, such as GIDL or gate oxide tunneling have been found to be negligible in the reported FD SOI CMOS technology.

For a L_{eff} = 0.26 μm SOI MOSFET we measured I_{off} values of about 2.2 pA/μm, which is about 1 decade lower than conventional bulk CMOS technologies with similar channel lengths where leakage current is of about 20 pA/μm [5]. Figure 2 plots the characteristics of a SOI nMOSFET with L=0.35 μm (L_{eff}=0.26 μm) and W=105.6 μm. The DIBL is observed as a reduction of the threshold voltage for high drain voltage. However, it results to be smaller than in bulk MOS transistors of similar channel length. Fig. 3a plots measurements of the off-state current vs. L_{eff} reporting a high dependence of I_{off} with this parameter, showing the strong influence of the channel length on the weak inversion current.

3. Effect of external parameters

Several techniques have been proposed to reduce current leakage in bulk CMOS ICs and enhance I_{DDQ} testability, as temperature reduction or back-bias [5]. Other methods propose multi-parameter based I_{DDQ} testing taking advantage of the correlation between off-state current and maximum speed.

The off-state current increase with temperature is significant due to several mechanisms: increase of the *pn* thermal generation current, increase of the subthreshold swing, reduction of the threshold voltage, and possible increase of short-channel effects with the temperature.

Temperature reduction (measurement at temperatures lower than room temperature) has been proposed as a useful technique for bulk CMOS ICs to reduce the quiescent current and improve I_{DDQ} results [5]. The I_{off} increase with temperature is smaller in FD SOI CMOS technologies than in bulk CMOS [6] for several reasons: the limited area of the source/drain depletion regions and the absence of well junctions, the better value of the subthreshold swing, the lower dependence of the threshold voltage on the temperature for FD devices, and the reduced short-channel effects. We observed values of S that resulted to be much better than in a 0.35 μm bulk CMOS process (Table I), leading to significantly lower values of I_{off} for the same threshold voltage value. A 0.35 μm gate length bulk MOSFET typically shows an off-state current of 380 pA/μm at 100ºC [5], while our measurements demonstrated I_{off} values of the order of 30 pA/μm for a transistor with L_{eff}=0.26 μm at 100ºC (Fig 4). Therefore, although temperature reduction is effective in lowering the current leakage in SOI technologies, I_{DDQ} testing can be applied to deep-submicron SOI CMOS without the need to reduce this parameter since nominal values at temperatures of about 100ºC are still acceptable. On the other hand, in bulk CMOS technologies, the effectiveness of the temperature reduction technique is reduced from two to one orders of magnitude when scaling from 0.35 μm to 0.18 technologies; this is related to the threshold voltage temperature coefficient decreasing as the gate oxide becomes thinner.

Another technique used to reduce off-state current in bulk CMOS technologies is back gate bias, in which a negative substrate voltage is applied to the circuit to increase the threshold voltage [5]. Although a similar effect can be obtained in SOI CMOS ICs with this technique, it is not required due to the overall better performance obtained in the subthreshold regime. Anyway, backbiasing was shown to be ineffective for 0.18 μm technologies and below [7], probably due to the increase of GIDL and the increase of field across the thin oxide.

An important figure to bin CMOS ICs is the off-state current dependence with f_{max}. If we can tolerate a higher level of I_{off} we can reach a higher f_{max}. In some areas (as in analog applications) a design tradeoff has to be made to balance between the allowed maximum leakage current and the desired maximum operating frequency. Fig. 3b plots the off–state current versus f_{max} measured for the SOI MOS technology under consideration, reporting a considerable higher f_{max} than bulk MOSFETs. These results show sufficiently high values of f_{max} achieved at low values of I_{off}, thus reporting quiescent current levels within acceptable ranges for I_{DDQ} testability.

4. Discussion and conclusions

Measurements on a 0.25 µm FD SOI technology showed that deep-submicron SOI CMOS exhibits much lower off-state current levels with respect to bulk CMOS, with higher performance and better temperature dependence. The background current remains within reasonable margins without the need for high-cost specific techniques used to apply I_{DDQ} in modern submicron bulk CMOS technologies, such as temperature reduction, or back gate bias. Novel SOI technologies, such as double-gate, will decrease even more the off-state current because of the radical reduction of short-channel effects [4].

The measurements conducted in this work at the transistor level can be extrapolated to the overall IC background current, predicting static levels for submicron SOI technologies similar to the quiescent current obtained in the past for micronic bulk CMOS. On the other hand, the impact of bridge and open defects (which are targeted I_{DDQ} testing defects [1]) in SOI circuits is similar to bulk CMOS technologies since they are related to imperfections in lithographic manufacturing processes steps, or caused by in–field operation (oxide wearout, metal electromigration, etc.) and therefore not related to substrate processing [8]. Thus, the defect induced behavior at the circuit level in terms of quiescent current excess is similar in both technologies.

From this analysis it is clear that testing techniques based on monitoring current–related parameters as I_{DDQ} may remain effective for very deep-submicron SOI technologies since the current background limitation is less severe than in bulk CMOS, and its impact in future SOI technologies is not expected to increase significantly.

Acknowledgements

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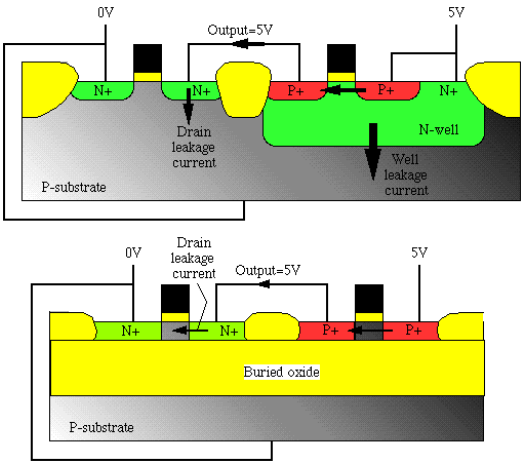


Figure 1. Cross section of bulk CMOS (top) and SOI (bottom) inverters illustrating leakage components

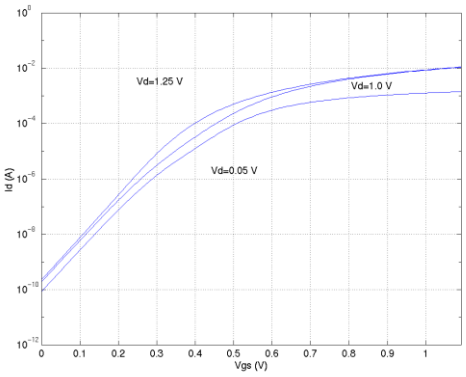
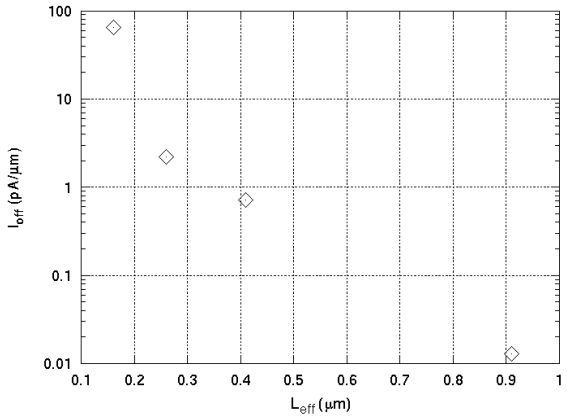
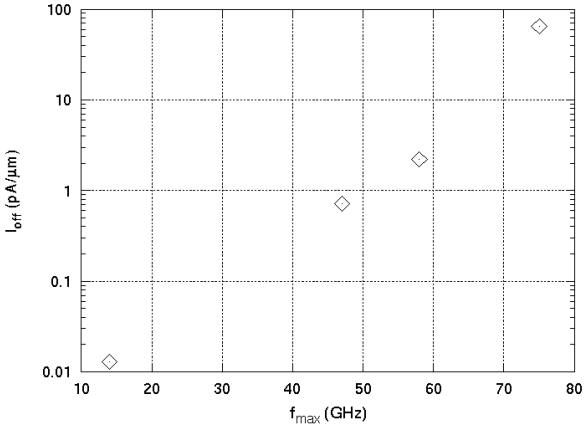


Figure 2**.** Drain current Id vs. Vgs at different drain voltages. SOI nMOSFET with L=0.35 μm (L_{eff}=0.26 μm) and W=105.6 μm.



(a)



(b)

Figure 3. Off-state current, measured at $V_d=V_{DD}=1.25$ V and room temperature, vs. L_{eff} (a) and vs. f_{max} (b) for transistors with Si film thickness $t_b=40$ nm, and front gate oxide thickness $t_{oxf}=4.5$ nm. Effective channel lengths range from 0.16 μm.to 0.91 μm.

Table I: Measured subthreshold slope, S (in mV/dec), for SOI and bulk nMOS transistors with a 0.35 μm gate length

Temperature (ºC)	**S (SOI MOS)**	**S (bulk MOS [5])**
25	64.1	81.9

50	68.5	88.0
75	75.5	96.6
100	86.9	105.8

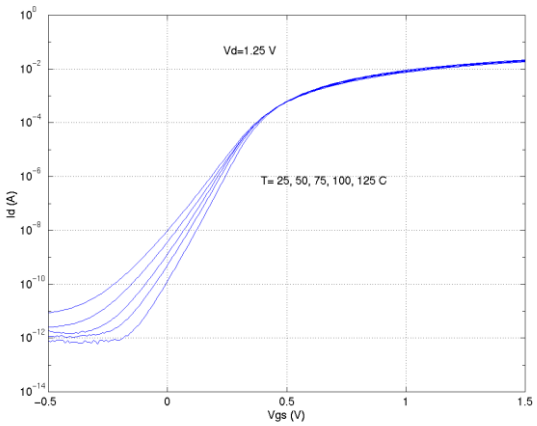


Figure 4. Drain current I_d vs. V_{gs} at different temperatures and V_d=1.25 V. SOI nMOSFET with L=0.35 μm (L_{eff}=0.26 μm) and W=105.6 μm.