TCAD at the heart of innovation in RF SOI technology

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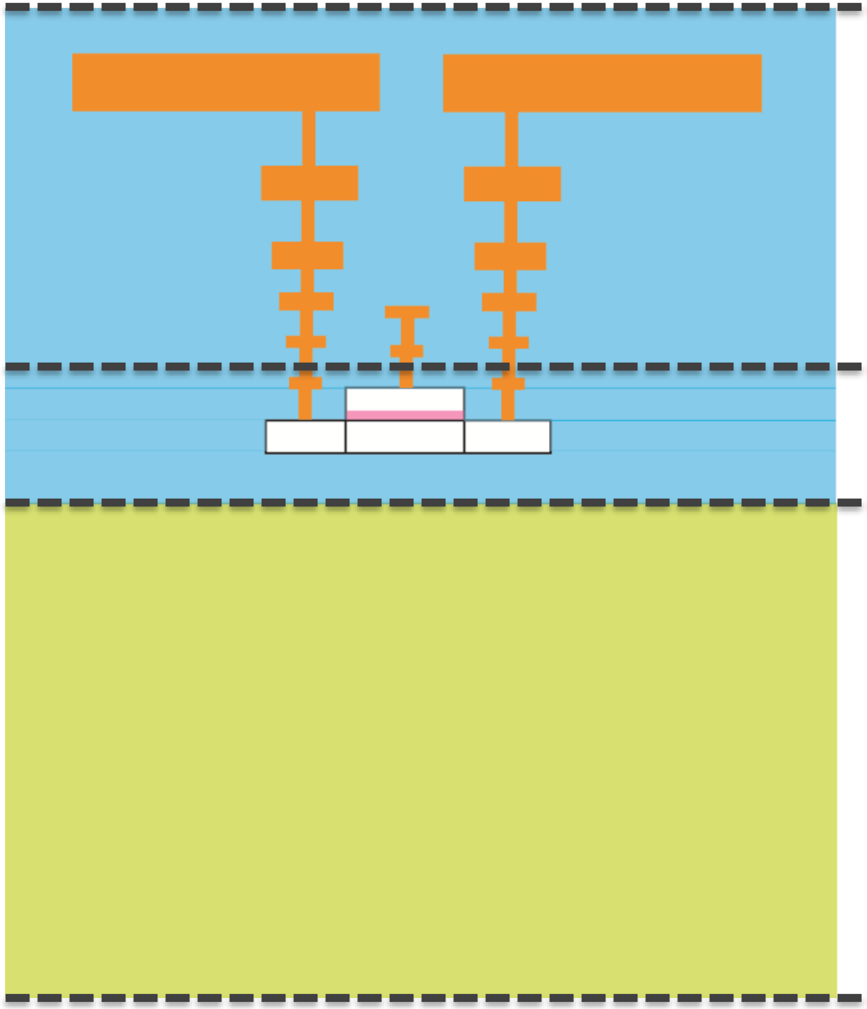
RF SOI CMOS – challenges at different levels …



Back-end

RC parasitics – thick metal, CNTs, low-k

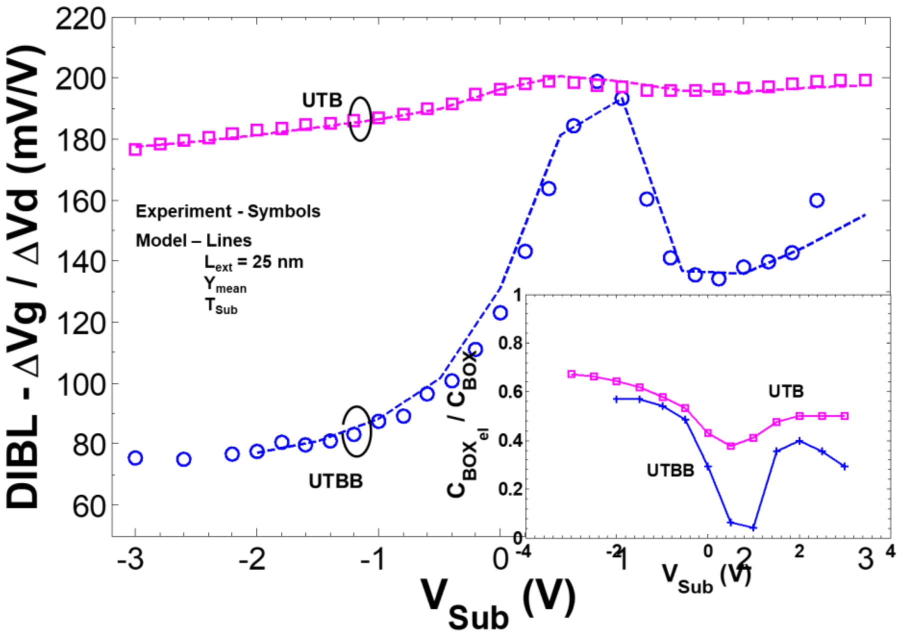
Front-end – new materials, transistors

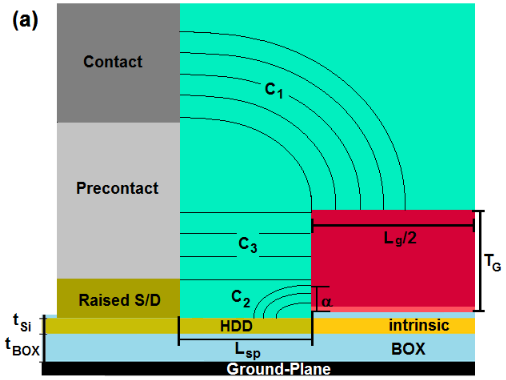
Substrate

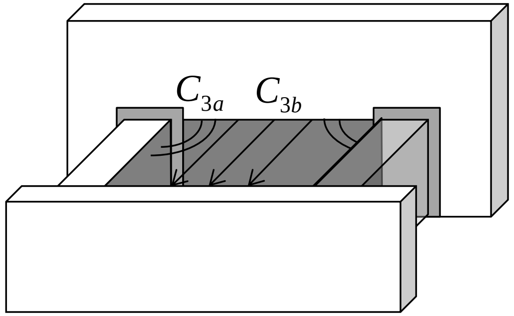
Losses, crosstalk, thermal issues, linearity, …

Silvaco Device simulation tool for RF SOI transistors

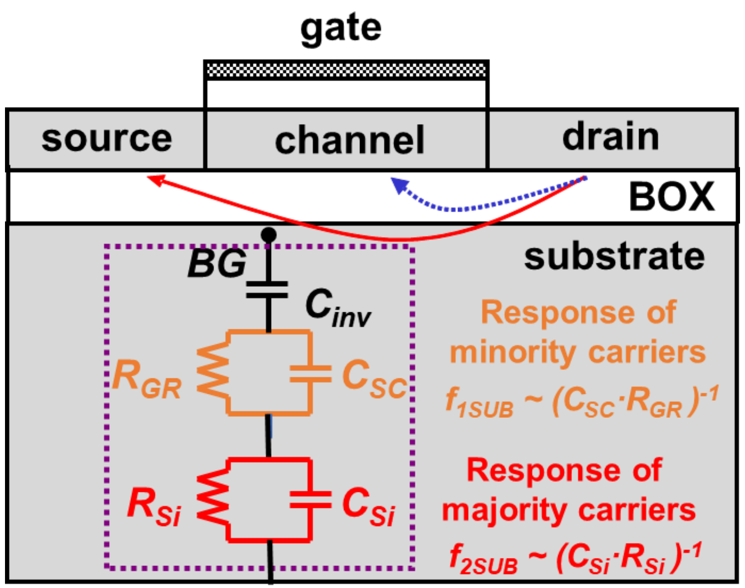
- **Short Channel Effects modelling in FD and multiple-gate SOI transistors**
  - M. K. Md Arshad *et al.*, IEEE TED, January 2012.
  - J.-P. Raskin *et al.*, IEEE TED, May 2006.
- **Development of a threshold voltage extraction method**
  - T. Rudenko *et al.*, IEEE TED, December 2011.
- **Modelling of the parasitic capacitances of FD SOI and FinFET**
  - J. C. Tinoco *et al.*, Semiconductor Science and Technology, January 2018.
  - S. Salas *et al.*, IEEE TED, November 2013.
  - E. E. Solis *et al.*, IEEE TED, July 2016.



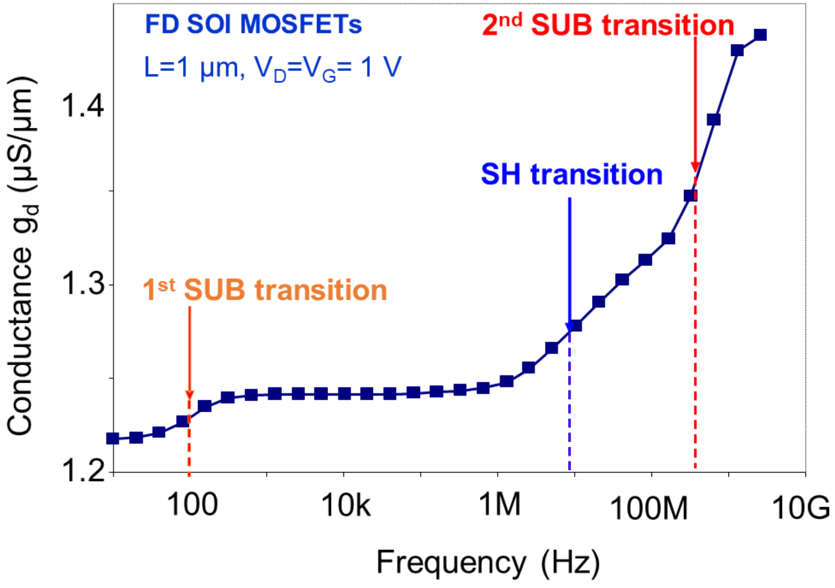




Silvaco Device simulation tool for RF SOI transistors



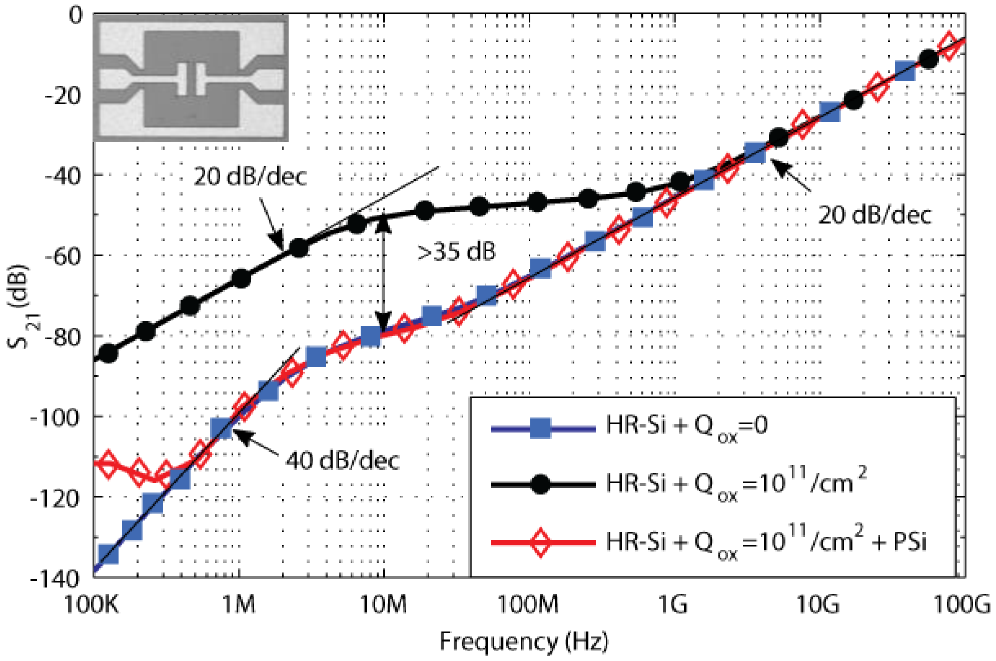
- **Self-heating issues in SOI transistors**
  - V. Kilchytska *et al.*, IEEE EDL, June 2003.
  - S. Makovejev *et al.*, Solid-State Electronics, May 2012.
  - V. Kilchytska *et al.*, Solid-State Electronics, 2007.
  - V. Kilchytska *et al.,* Applied Surface Science, 2008.



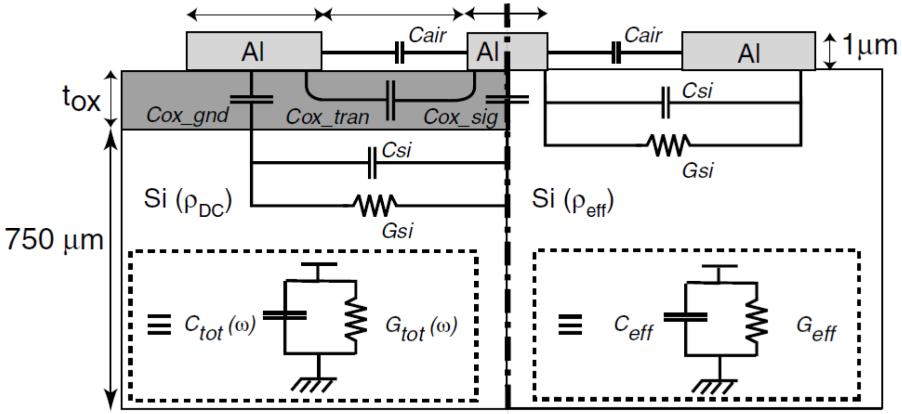
- **Impact of substrate on FD SOI transistors**
  - V. Kilchytska *et al.*, IEEE EDL, June 2003.
  - V. Kilchytska et al., IEEE EDL, May 2007.
  - J.-P. Raskin, Solid-State Electronics, 2007.
  - J.-P. Raskin, Solid-State Electronics, 2016.

Silvaco Device simulation tool for SOI substrates

- **Crosstalk simulation over a wide frequency band**
  - J.-P. Raskin *et al.*, IEEE TED, December 1997.
  - K. Ben Ali *et al.*, IEEE TED, December 2011.



- **Definition of a novel figure of merit: the effective resistivity of semiconductor substrate**
  - D. Lederer and J.-P. Raskin, Solid-State Electronics, 2005.



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Substrate RF non-linear characterization and modelling

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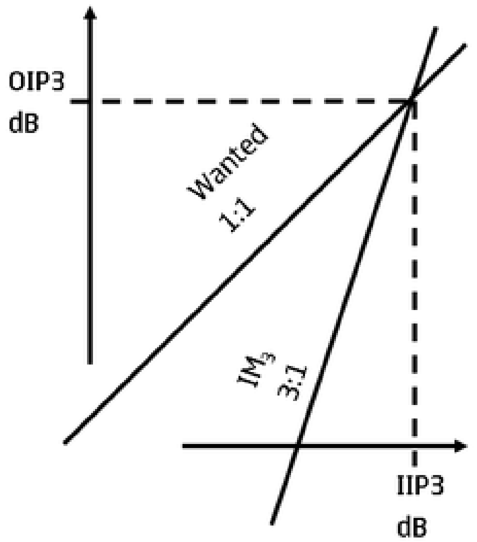
Non-linearity considerations

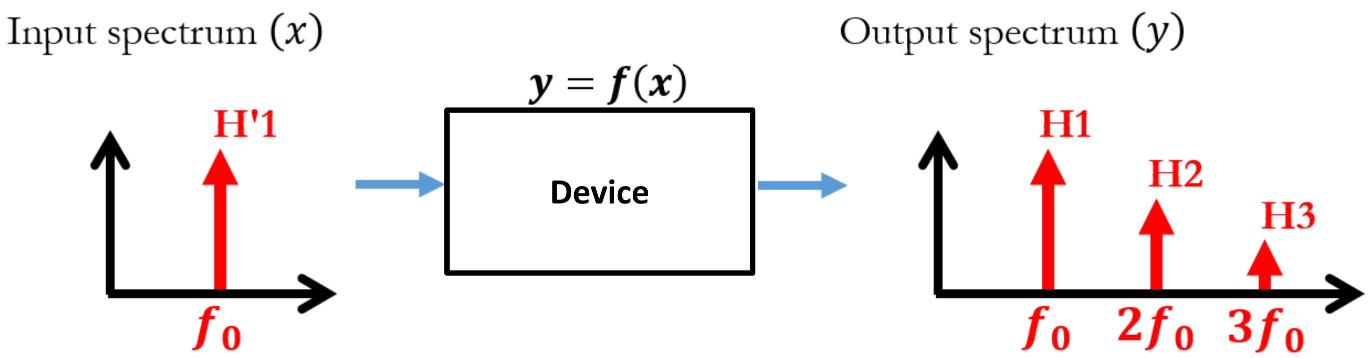
Third-order intercept point



- With each new generation of network standard comes a more **stringent requirement for linearity.**
- Non-linearities come from **active devices**,
- But also from **semiconductor substrates**!

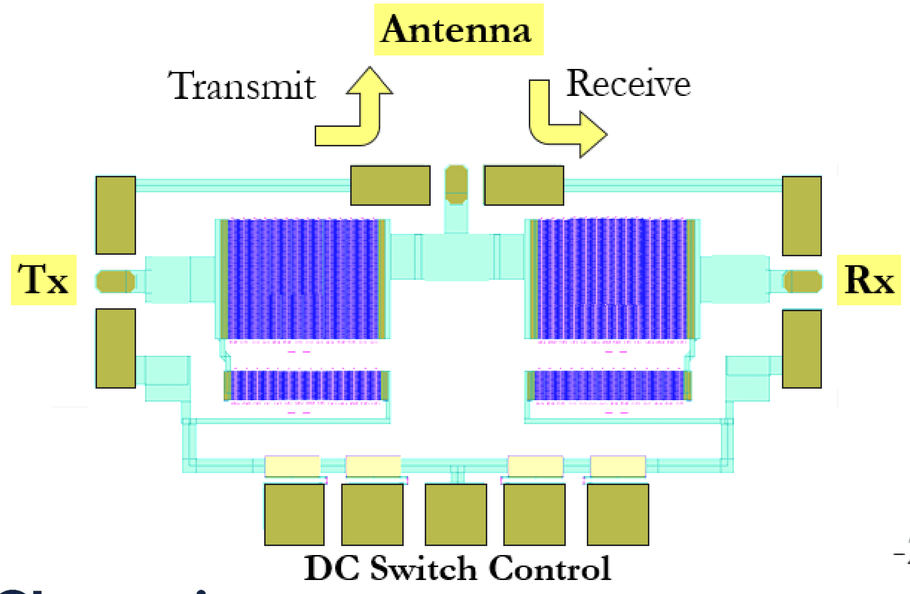
Linearity Requirements by Network Standard	
Network	Linearity IIP3 [dBm]
2G	55
3G	65
4G LTE	72
4G LTE + CA	Up to 90
5G	??

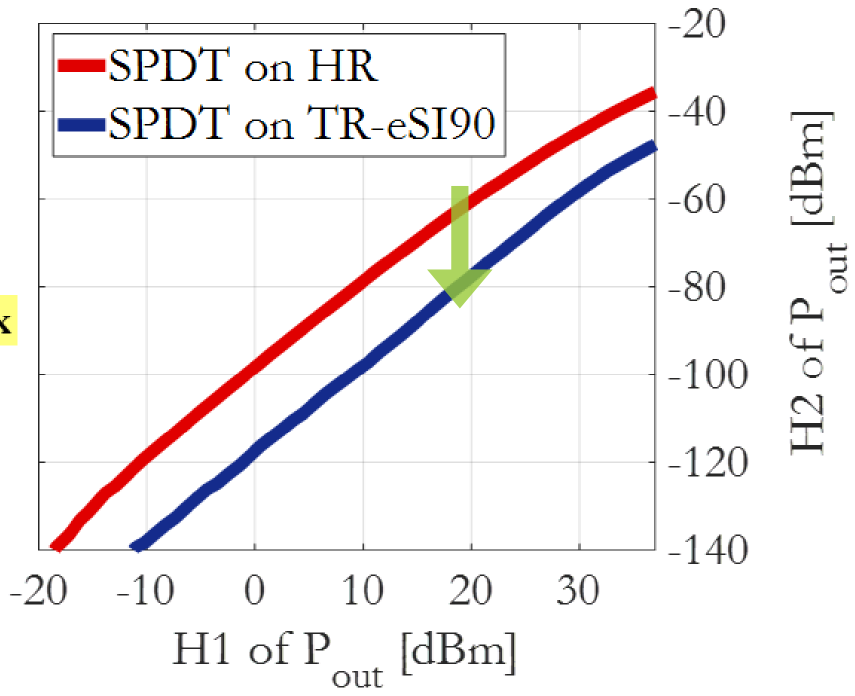
RF switch linearity: Substrate impact example



Ideal linear transfer function: $y = f(x) = a \cdot x$

Real non-linear transfer function: $y = f(x) = a \cdot x + b \cdot x^2 + c \cdot x^3 + \cdots$





Reduced harmonics

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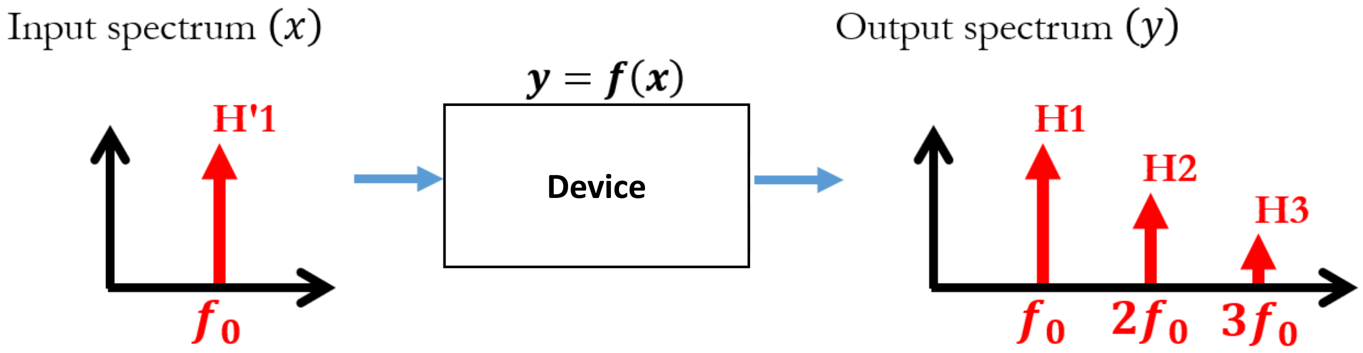
Substrate non-linearities



Ideal linear transfer function: $y = f(x) = a \cdot x$

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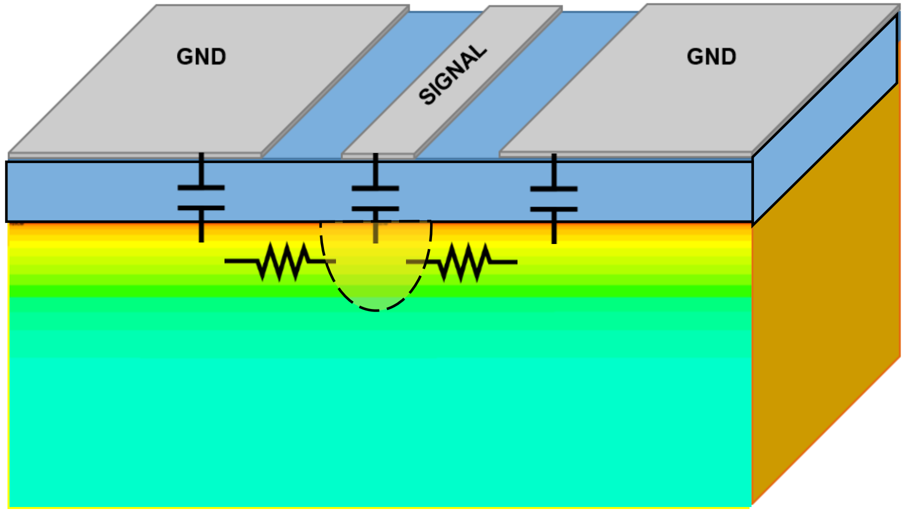
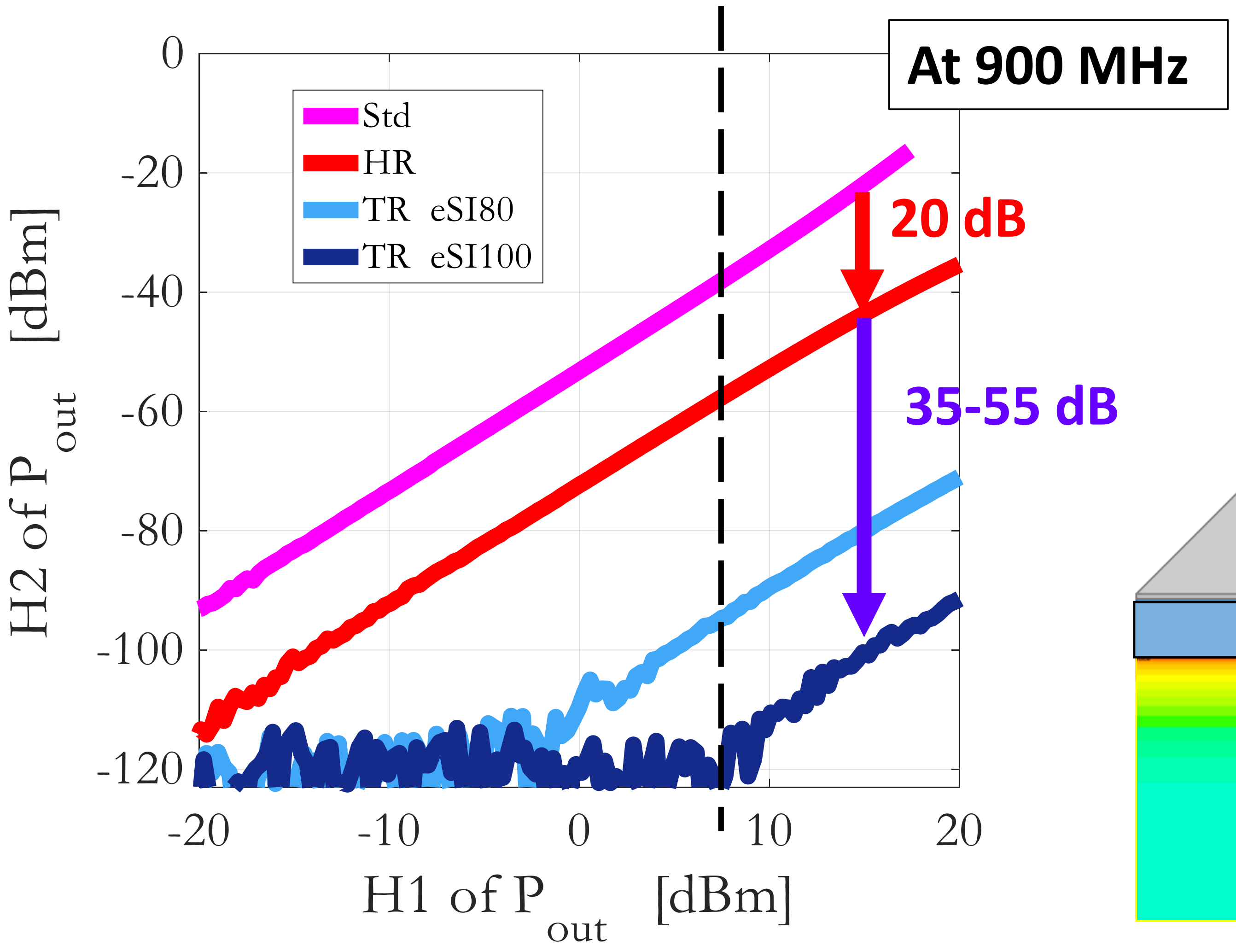
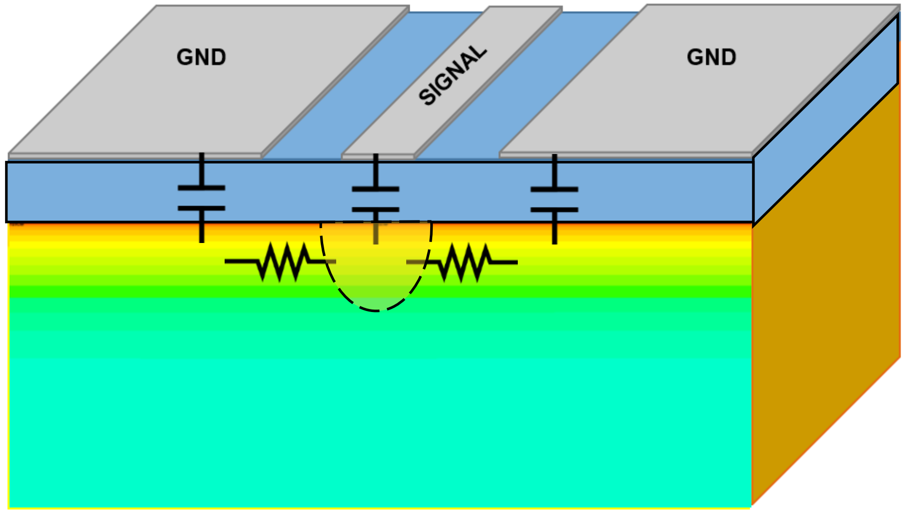
Semiconductors are non-linear by nature (**field-effect**)



Substrate non-linearities





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Substrate non-linearities simulation

- Can we **predict harmonic distortion** of a given materials stack?
- How to model, taking into account all **semiconductor effects**?
- Could we run **sensitivity studies** to gain physical insight into parameter impact on future substrate developments?

Static analysis

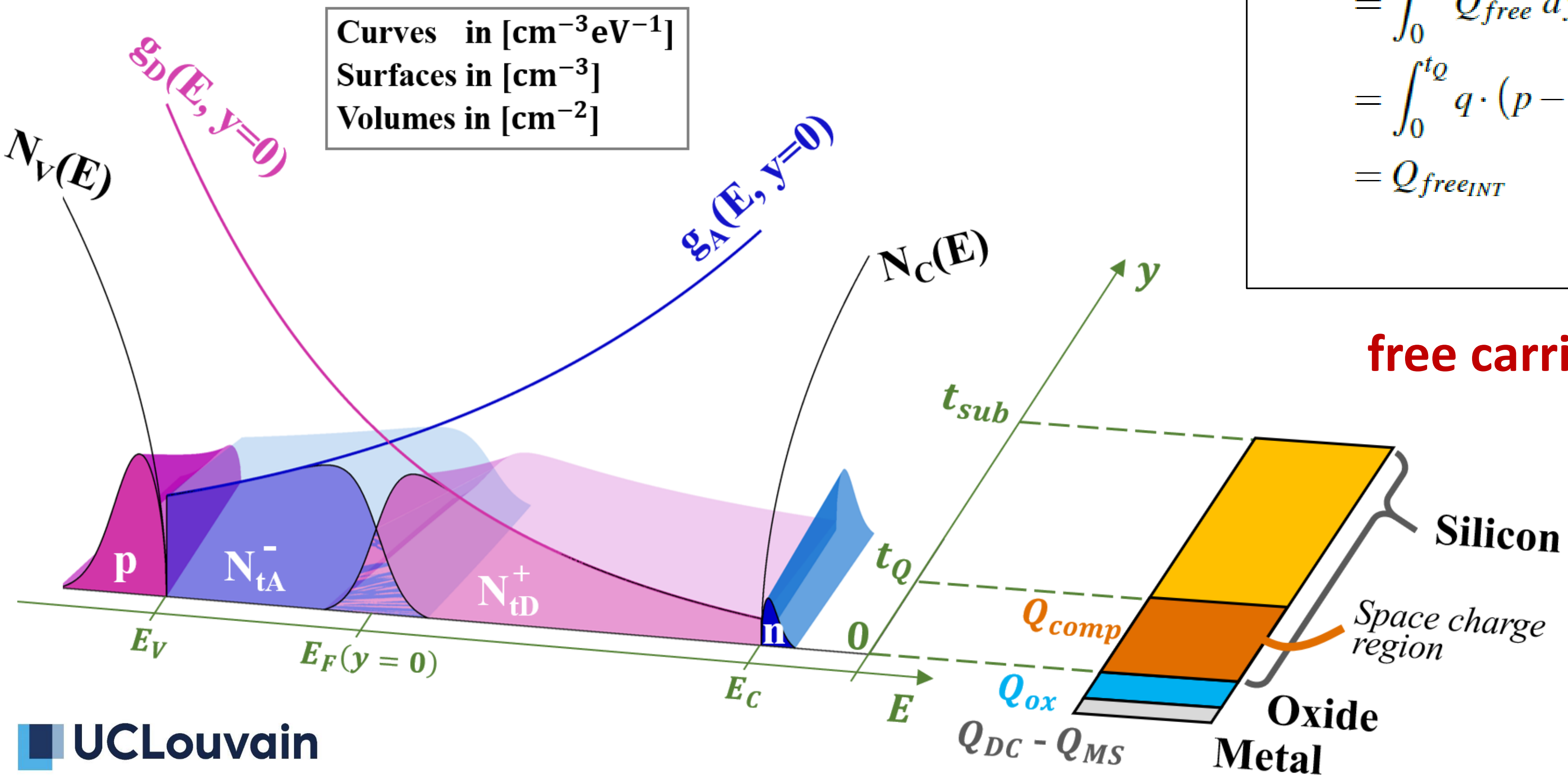
Quantitative Charge Balance

$$Q_{Applied} = Q_{DC} + Q_{ox} - Q_{MS} \quad [\mathrm{C \cdot cm^{-2}}]$$
$$= V_{DC}C_{ox} + Q_{ox} - V_{MS}C_{ox} \quad [\mathrm{C \cdot cm^{-2}}]$$

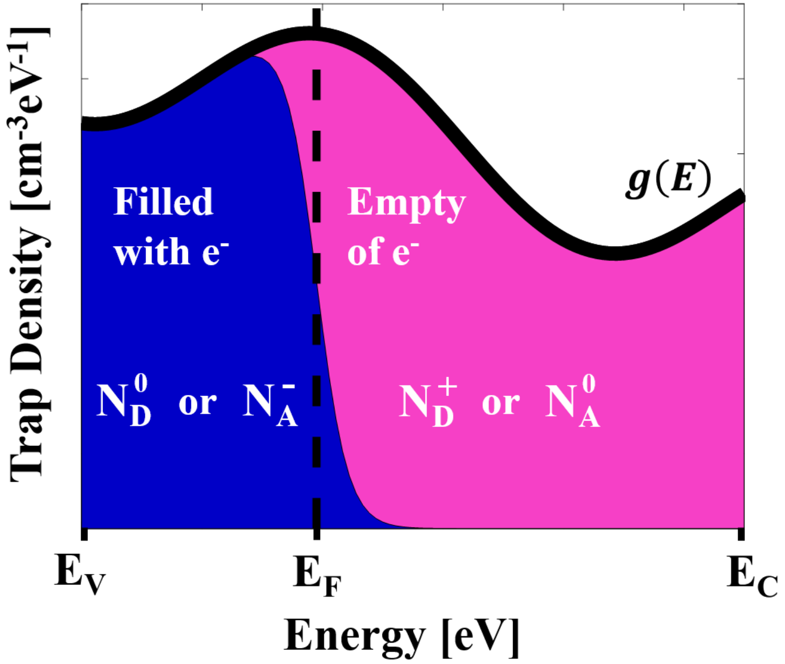
$$Q_{comp} = -Q_{Applied} \quad \text{at equilibrium} \quad [\mathrm{C \cdot cm^{-2}}]$$

$$\begin{aligned} Q_{comp} &= \int_0^{t_Q} \rho_q \, dy \\ &= \int_0^{t_Q} Q_{free} \, dy + \int_0^{t_Q} Q_{trap} \, dy \\ &= \int_0^{t_Q} q \cdot (p - n) \, dy + \int_0^{t_Q} q \cdot (N_{tD}^{+} - N_{tA}^{-}) \, dy \\ &= Q_{free_{INT}} + Q_{trap_{INT}} \end{aligned} \quad [\mathrm{C \cdot cm^{-2}}]$$

free carriers & ionized traps

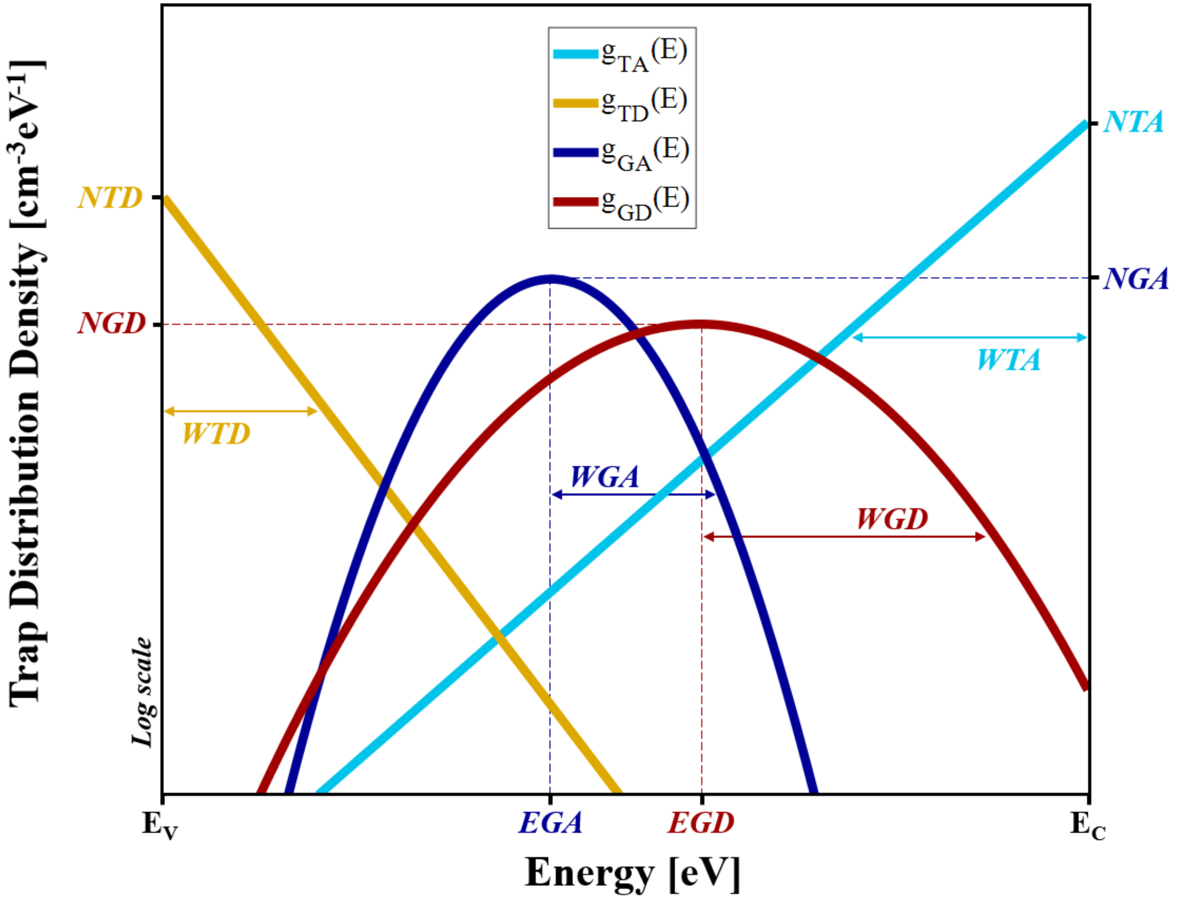


Definition of traps in Si layer



For Acceptor Traps: $Q_{Empty} = 0$, $Q_{Filled} = -q$

For Donor Traps: $Q_{Empty} = +q$, $Q_{Filled} = 0$



Traps in polysilicon:

$$g_{GA}(E) = NGA \cdot \exp\left\{-\left(\frac{EGA - E}{WGA}\right)^2\right\} \quad [\mathrm{cm^{-3} \cdot eV^{-1}}]$$

$$g_{GD}(E) = NGD \cdot \exp\left\{-\left(\frac{EGD - E}{WGD}\right)^2\right\} \quad [\mathrm{cm^{-3} \cdot eV^{-1}}]$$

$$g_{TA}(E) = NTA \cdot \exp\left\{\frac{E - E_C}{WTA}\right\} \quad [\mathrm{cm^{-3} \cdot eV^{-1}}]$$

$$g_{TD}(E) = NTD \cdot \exp\left\{\frac{E_V - E}{WTD}\right\} \quad [\mathrm{cm^{-3} \cdot eV^{-1}}]$$

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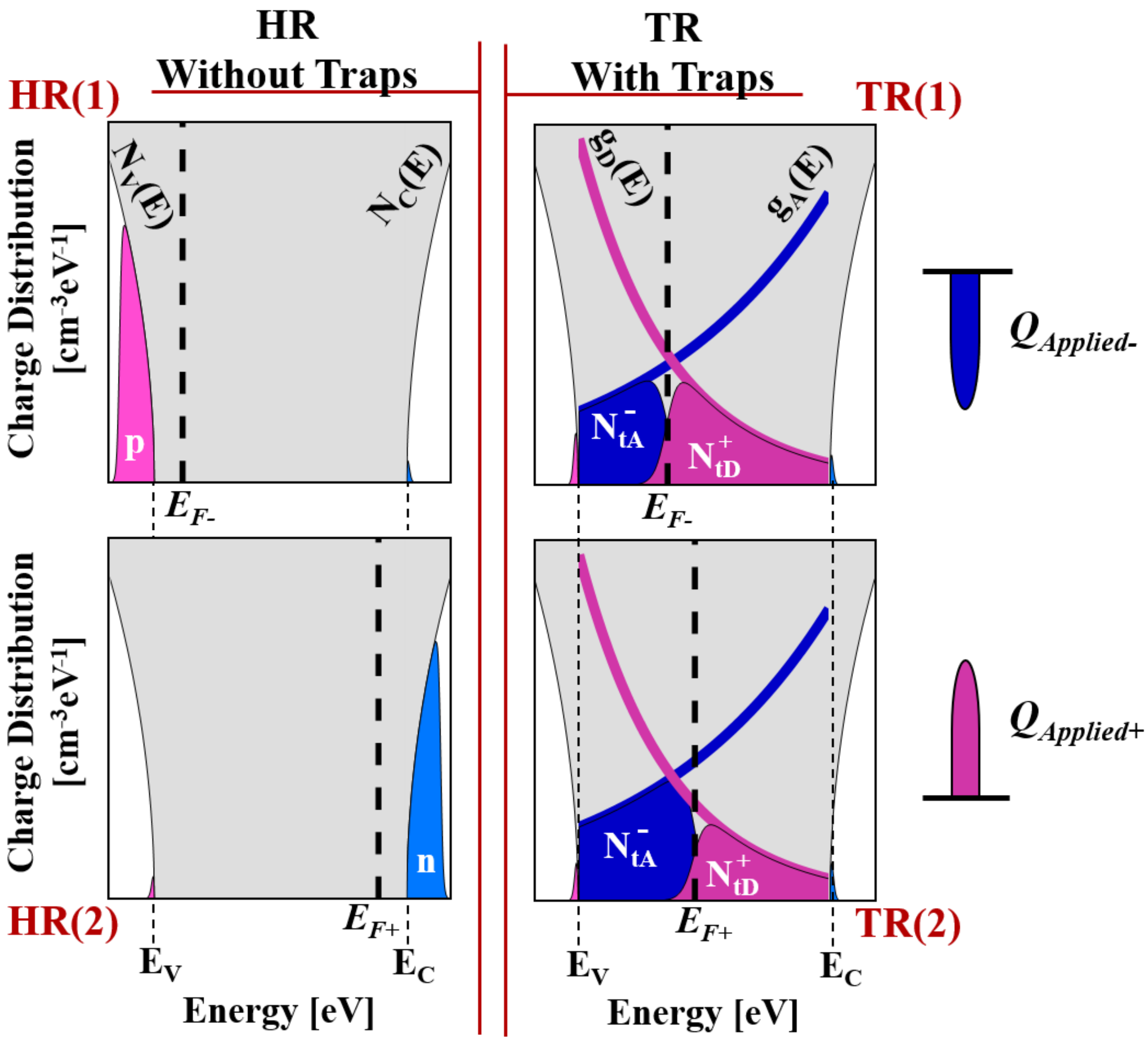
Charge compensation: HR vs. TR



$$N_{free} = \int_0^{t_Q} p(y) - n(y)\,\mathrm{dy} \qquad [\mathrm{cm}^{-2}]$$

$$N_{trap} = \int_0^{t_Q} N_{tD}^{+}(y) - N_{tA}^{-}(y)\,\mathrm{dy} \qquad [\mathrm{cm}^{-2}]$$

$$N_{Applied}(V) = N_{ox} + C_{ox}(V - V_{MS}) \qquad [\mathrm{cm}^{-2}]$$

In all generality:

$$-N_{Applied} = N_{free} + N_{trap}$$

In a HR

$$-N_{Applied} = N_{free}$$

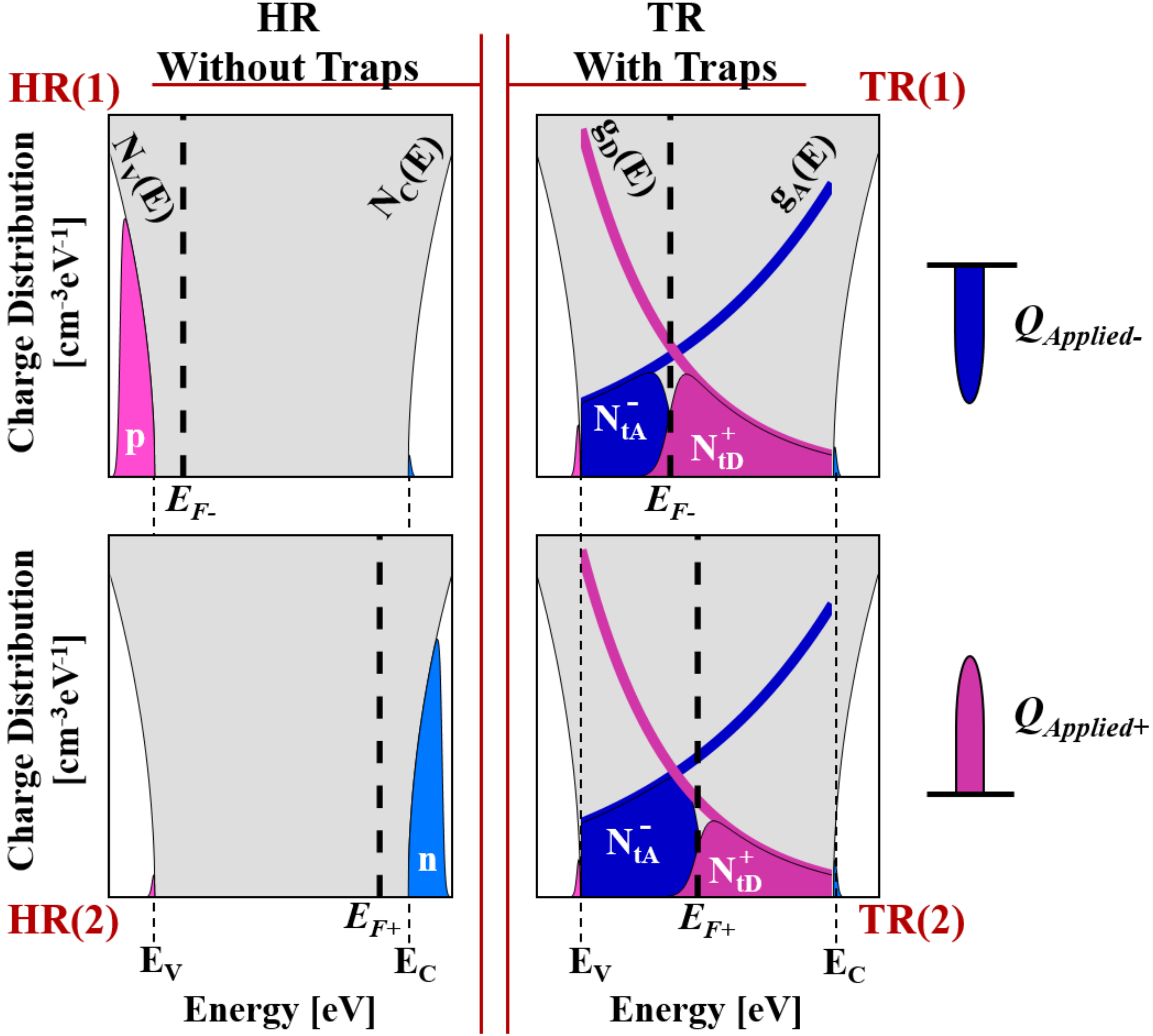
In a « good » TR

$$-N_{Applied} \approx N_{trap}$$

For any usual value of $N_{Applied}(V)$

Static analysis

Charge compensation: HR vs. TR



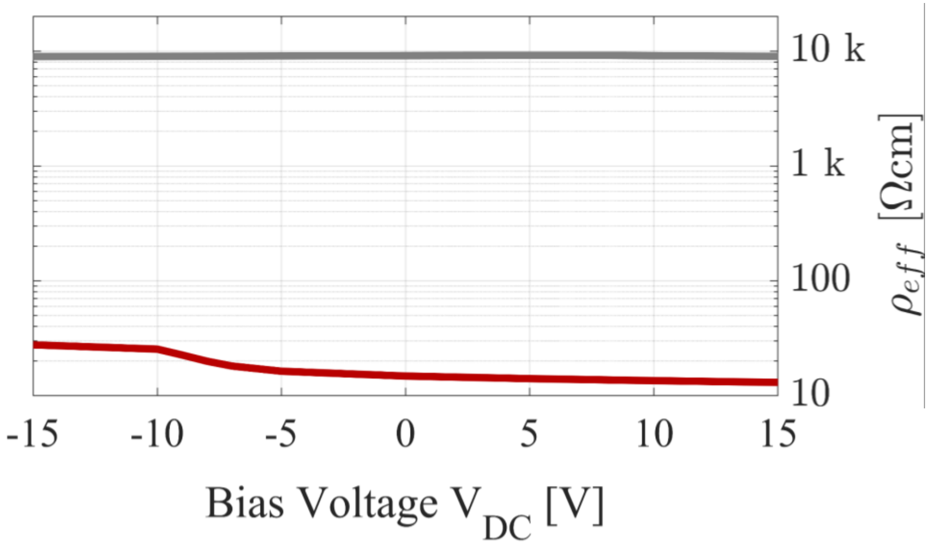
In a HR

n and ***p*** vary strongly with the applied signal $V(t)$

In a « good » TR

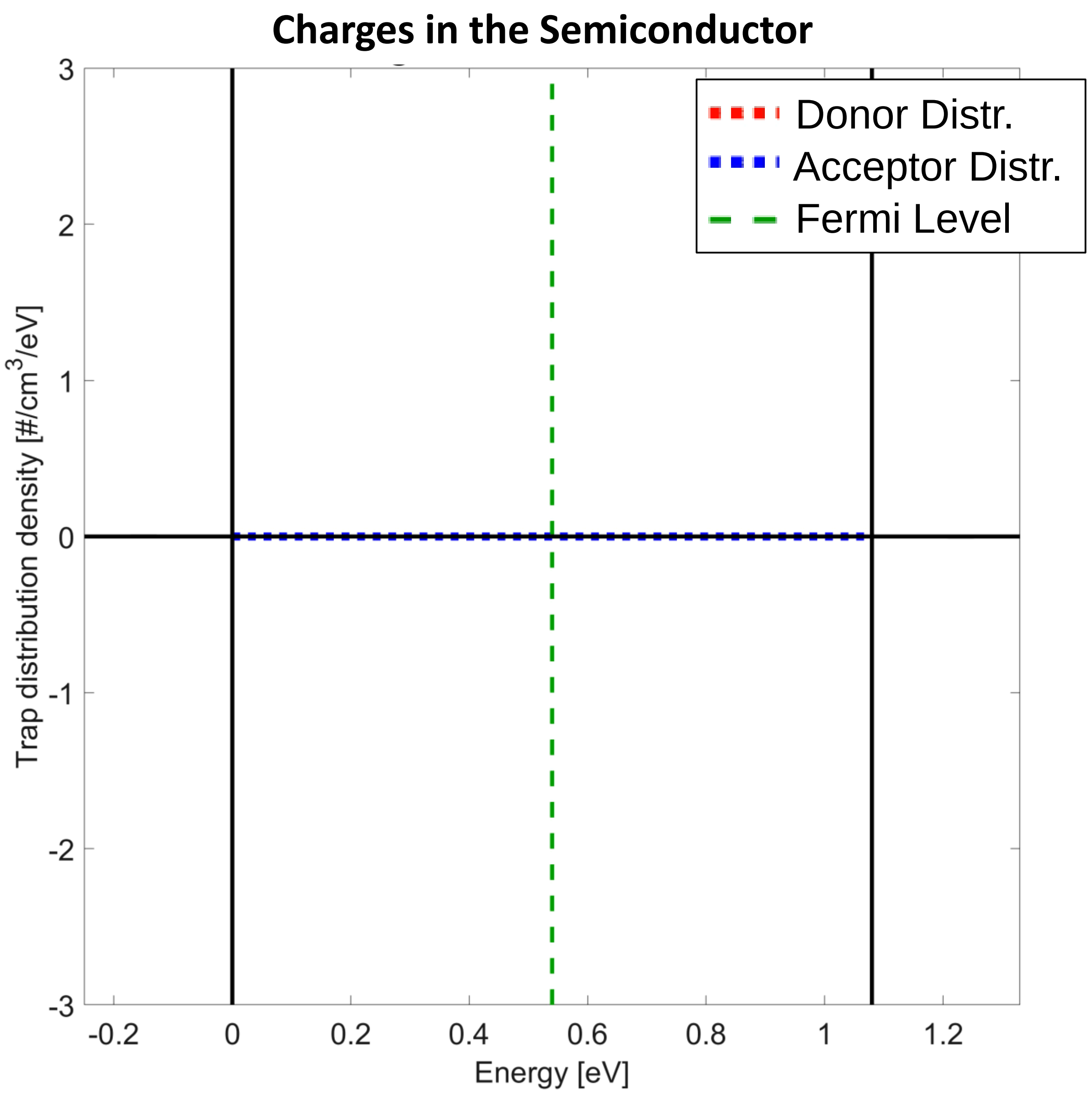
n and ***p*** remain very low for "any" signal $V(t)$

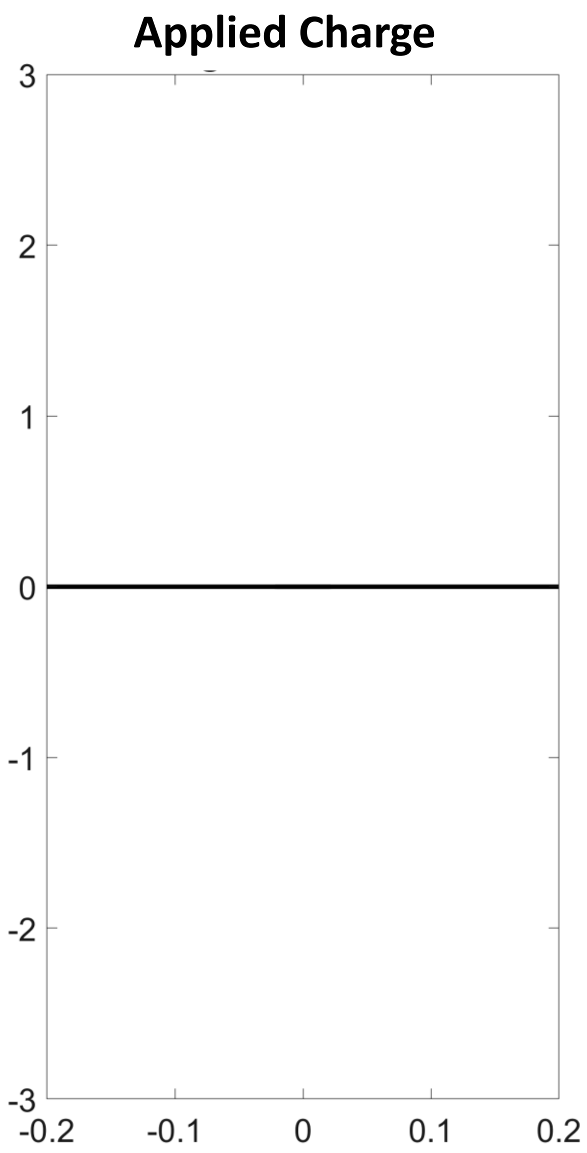
Concept of **Fermi-level pinning**



Static analysis

Charge compensation: HR vs. TR





HR substrate

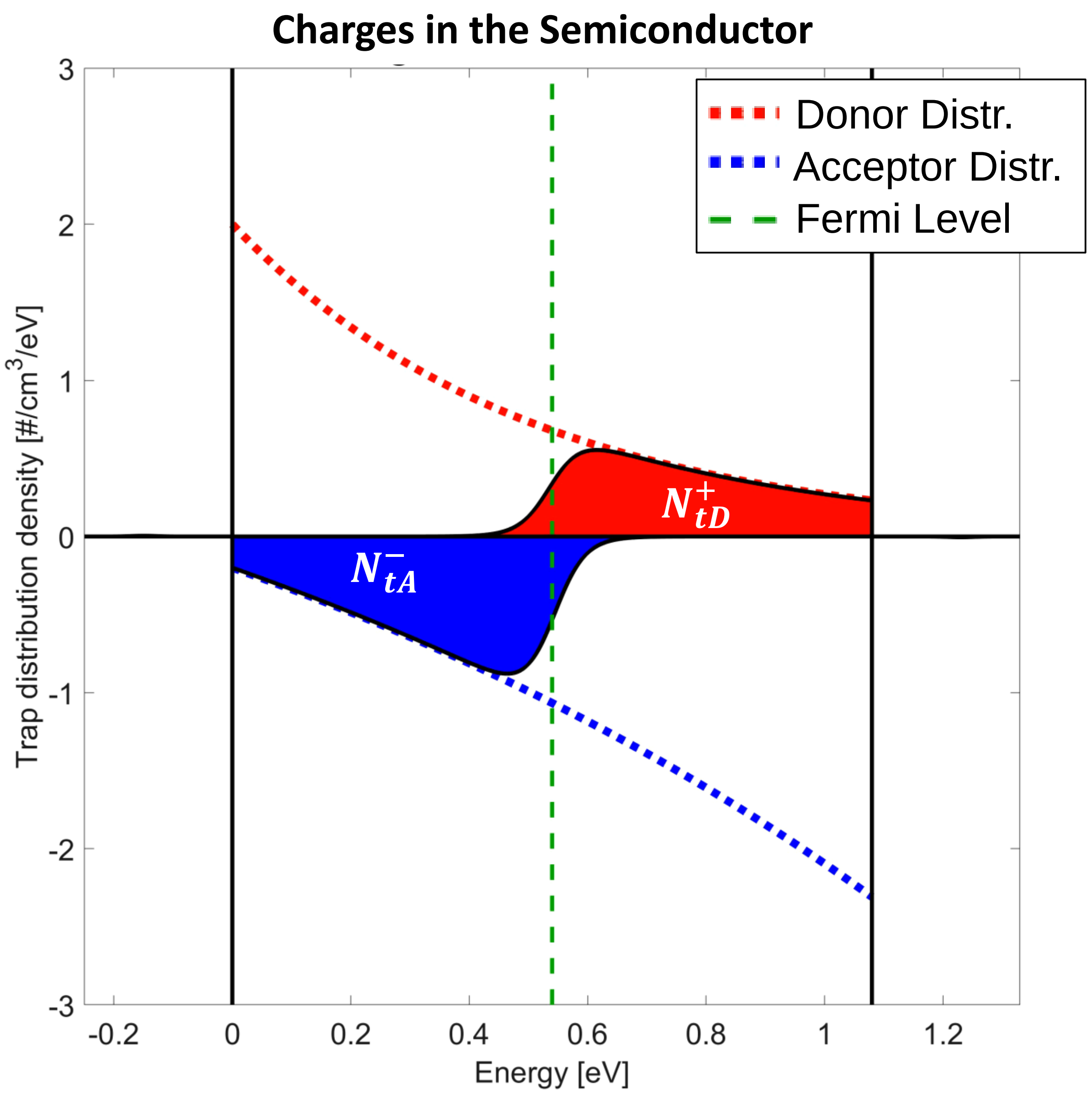
Large variations in n and p

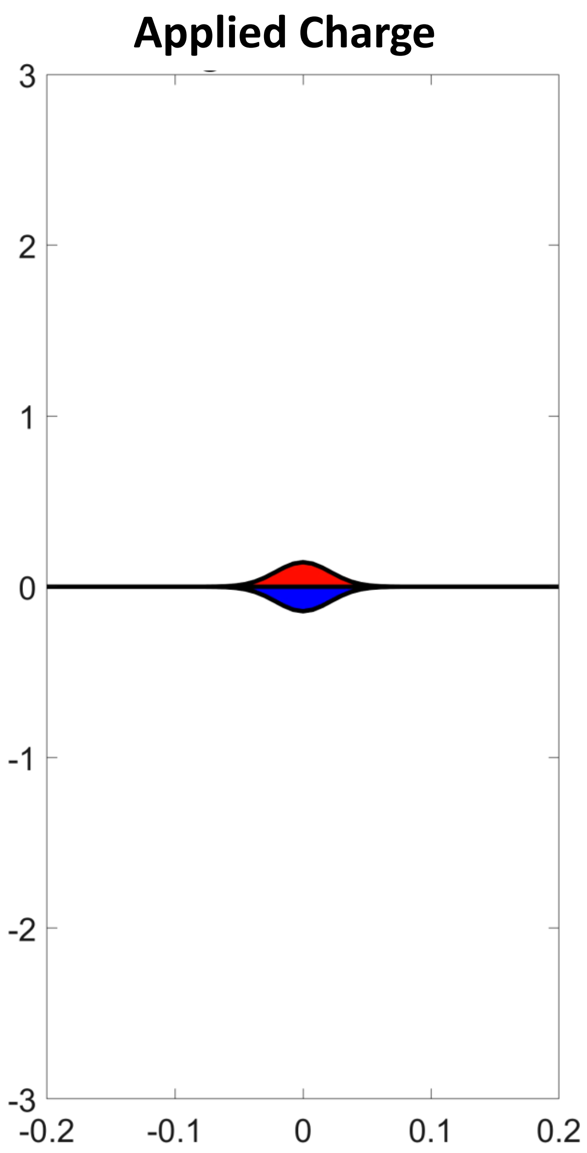
$\Rightarrow$ Large variations in substrate impedance

$\Rightarrow$ Highly voltage-dependent (non-linear)

Quasi-static analysis (DC or low-freq)

Charge compensation: HR vs. TR





TR substrate

Small variations in n and p

$\Rightarrow$ Small variations in substrate impedance

$\Rightarrow$ Little voltage-dependency (at low freq. !)

Quasi-static analysis (DC or low-freq)

At RF, full description involves E_{QFn}, E_{QFp}, $E_{QFtrap1}$, $E_{QFtrap2}$, etc.

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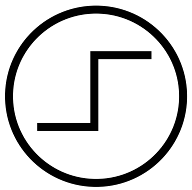
Non-Equilibrium Dynamics

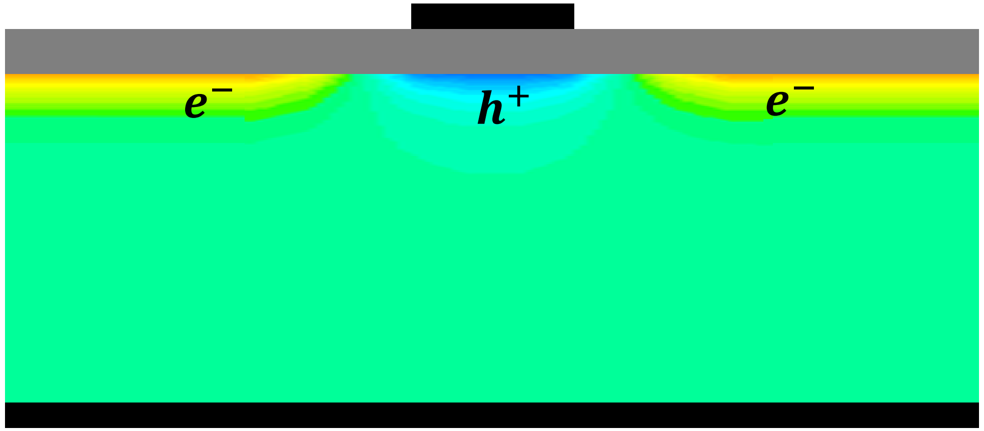
Voltage step applied to MOS device

$N_{ox} = 10^{11}\ \ cm^{-2}$

$V(t)$

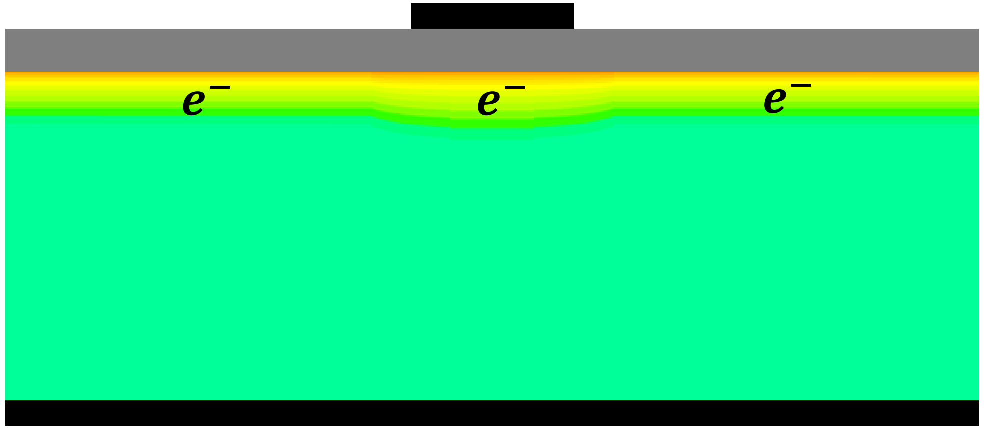


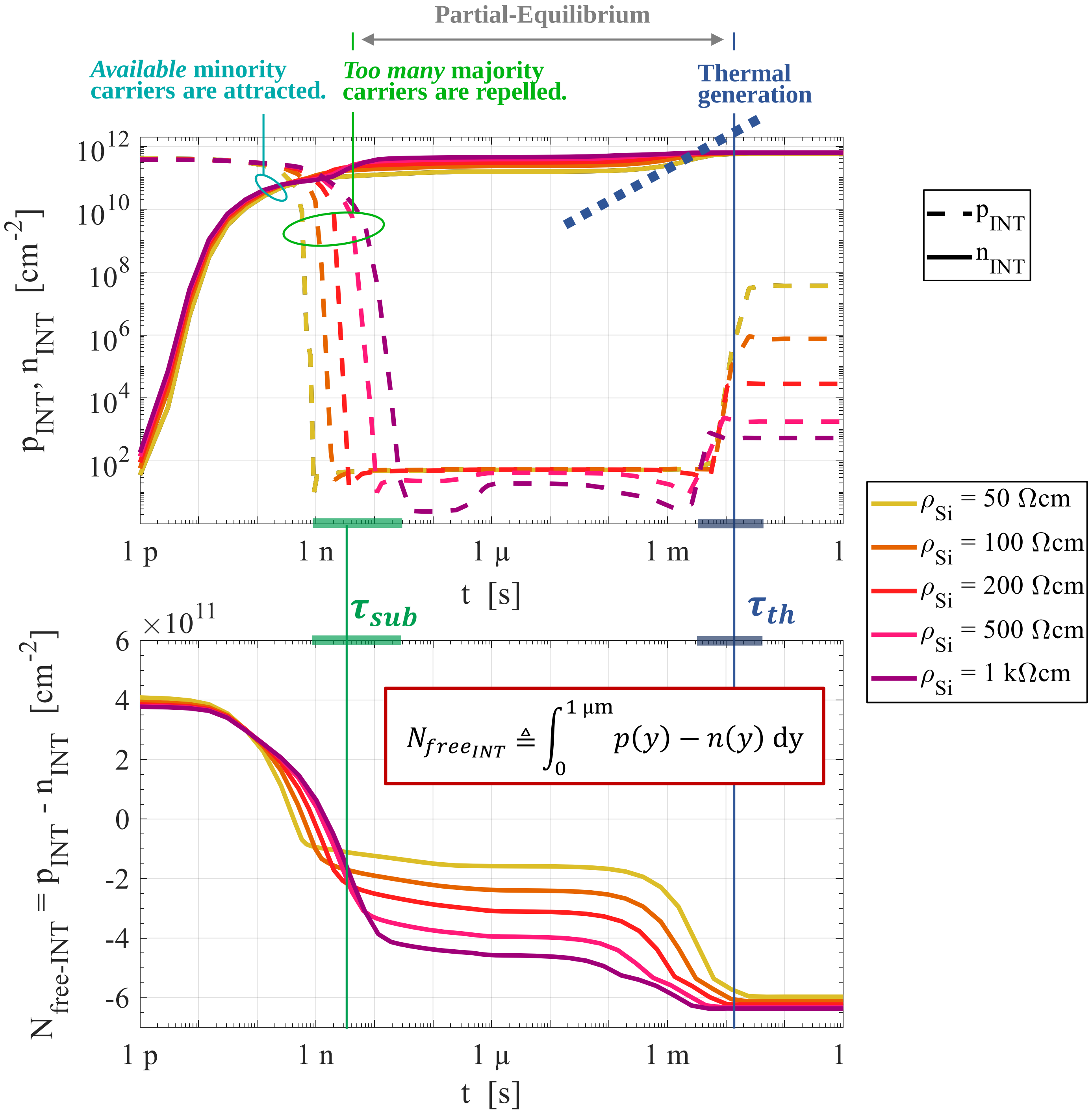
$V(t = 0^-) = -10\ V$



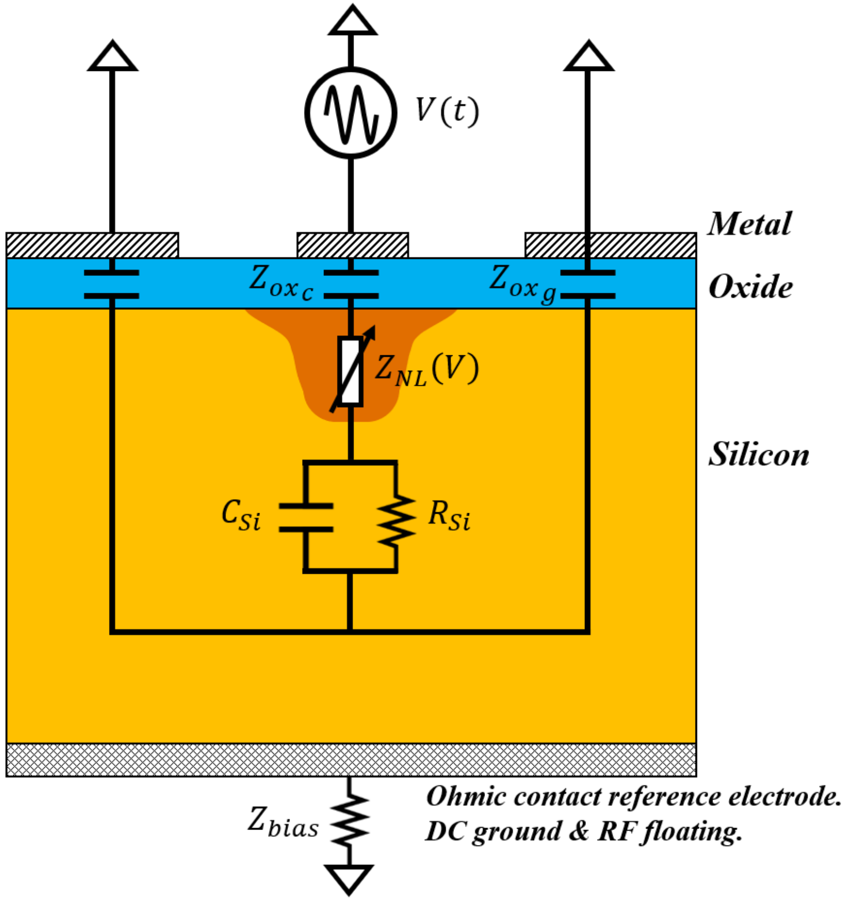
Color map
$n(x, y)$

$V(t = +\infty) = +10\ V$

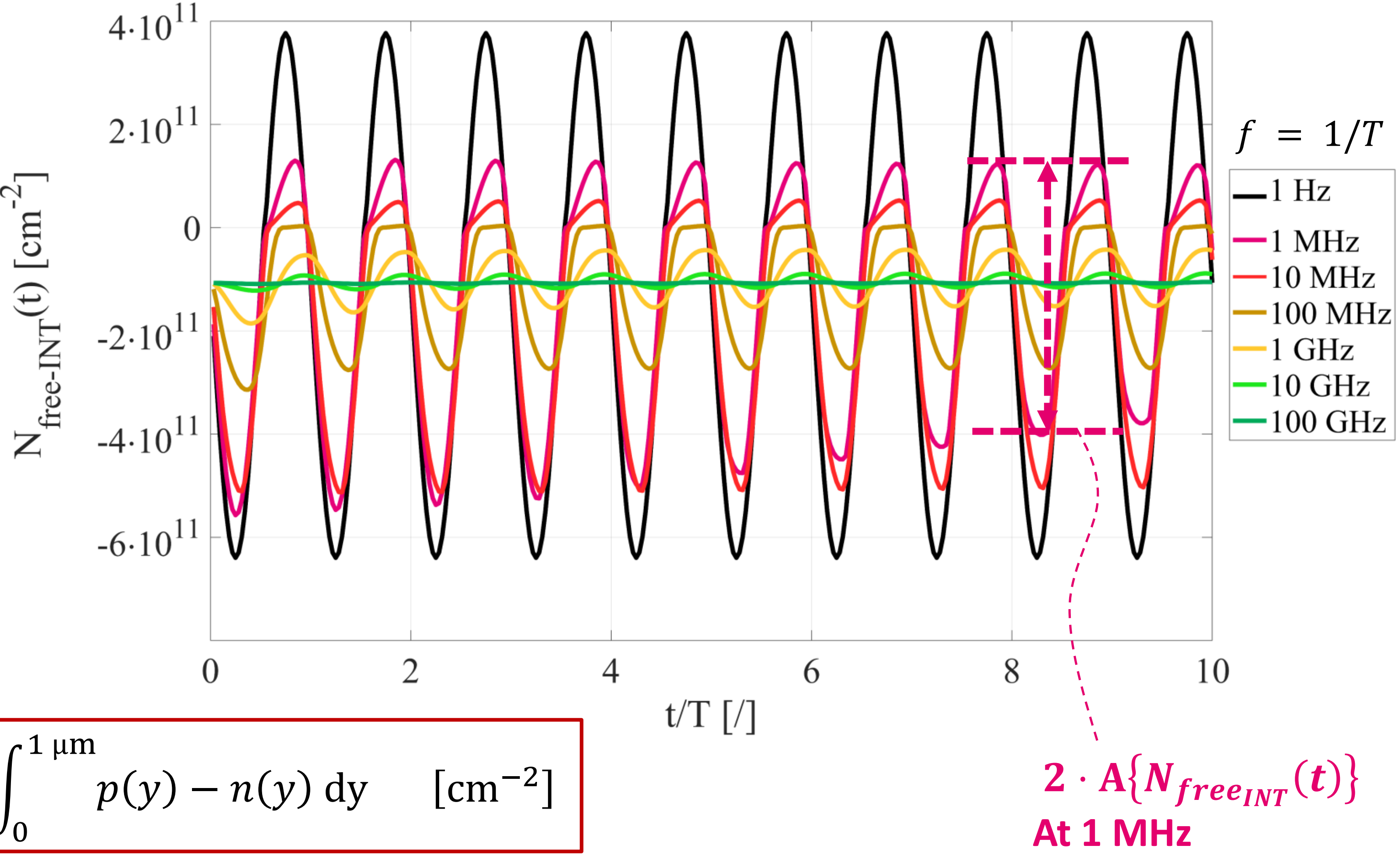




Non-Equilibrium Dynamics   Sinusoidal $V(t)$ - RF analysis



HR $\rho_{Si} = 1$ kΩcm (P-type),
$t_{ox} = 400$ nm, $N_{ox} = 10^{11}$ cm^{-2}

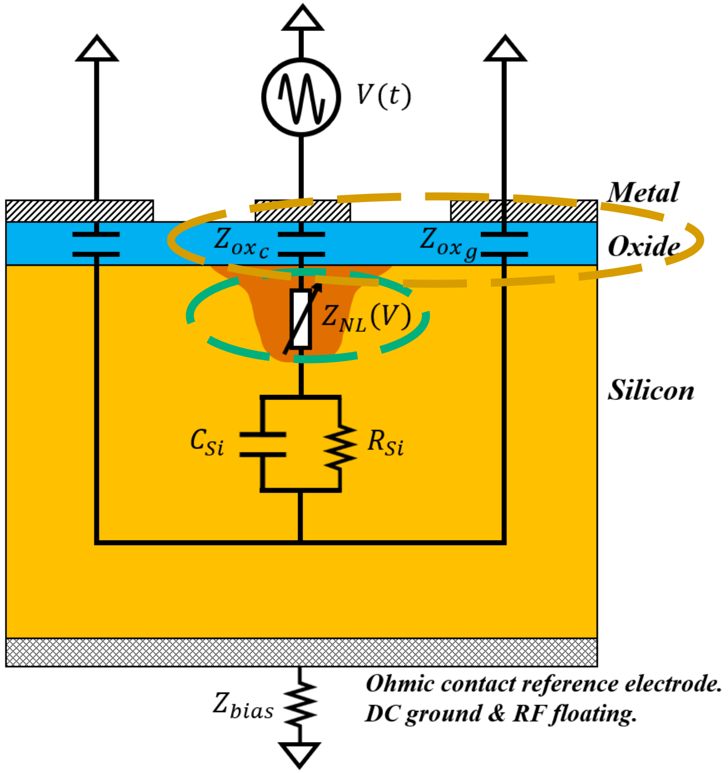


$$N_{free_{INT}} \triangleq \int_0^{1\,\mu m} p(y) - n(y)\,dy \qquad [\text{cm}^{-2}]$$

As f increases: only a spatial rearrangement of existing *available carriers through time*
no (significant) generation/recombination

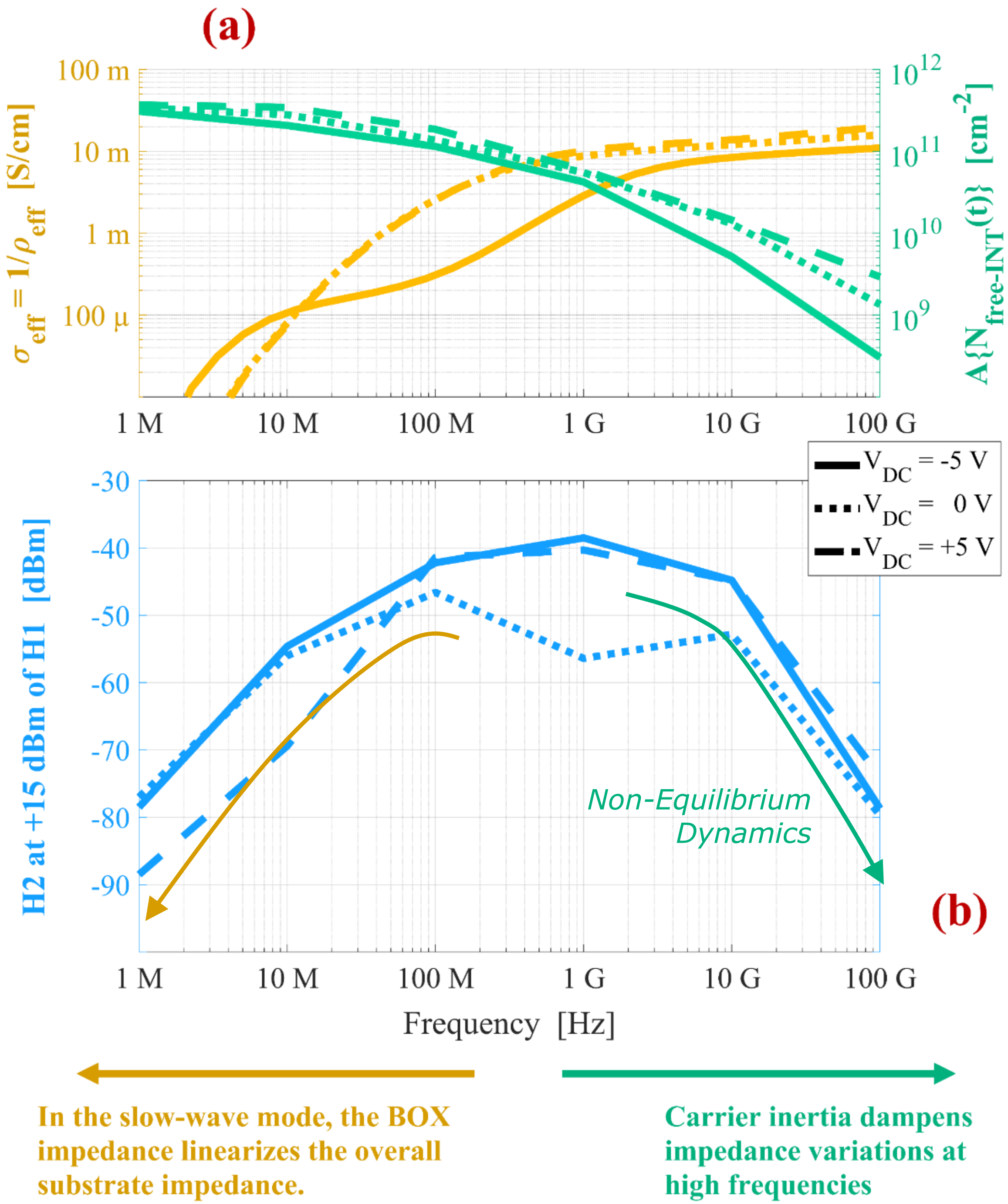
Substrate non-linearities

Impact of frequency - Modelling



HD is maximum just after the end of the slow-wave mode f_{SW}

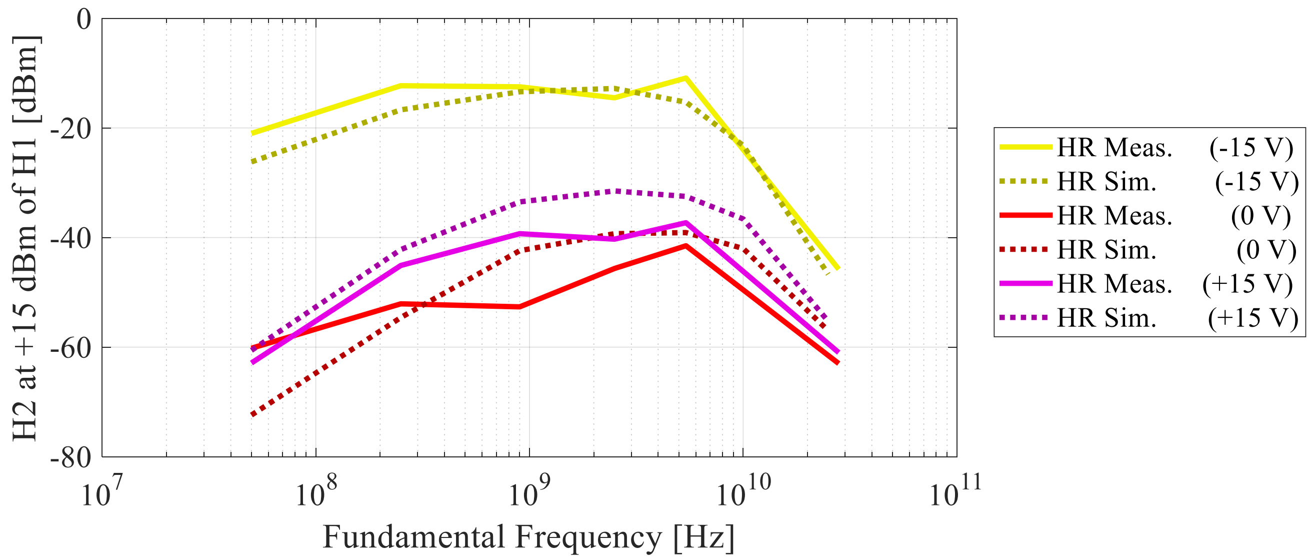
	ρ_{eff} [Ωcm]	f_{SW}
Standard Si	~10	5 - 15 GHz
HR with strong PSC	< 50	5 - 15 GHz
HR with weak PSC	50 – 200	1 - 5 GHz
TR	10k	10 - 50 MHz



Substrate non-linearities

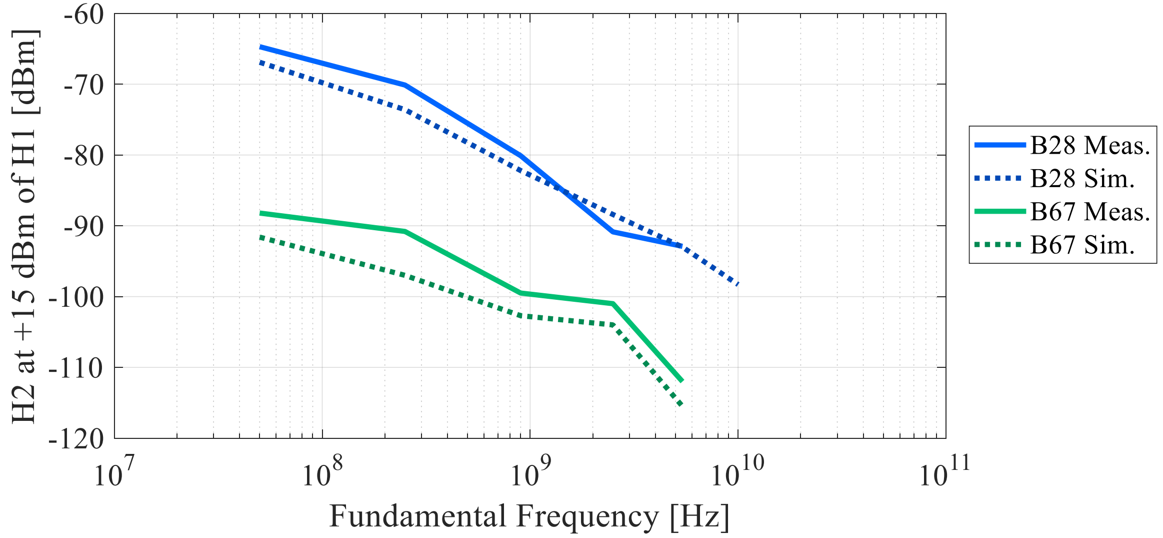
Impact of frequency - Measurements

HR becomes more linear above the slow-wave mode transition frequency due to **finite carrier inertia**



TR samples H2 at 28 GHz is in noise floor

=> Lower than -100 or -110 dBm on the setup that was implemented.



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Conclusions

- Silvaco Device simulation tool simulates properly **a wide variety of physical phenomena;**
- **Time domain (transient mode) simulations** have been conducted to study the non-linear behaviour of various types of SOI substrates;
- Silvaco Device simulation tool simulates accurately the **different semiconductor relaxation time constants;**
- It is a fantastic tool to **understand the physical behaviour of semiconductor devices** under static or dynamic electrical signal of small or large amplitude;
- To explore the performance of **innovative Si-based substrates for RF and mmW applications.**

Main references

M. Rack, F. Allibert, J.-P. Raskin, “RF modelling of trap-rich passivated semiconductor substrates: Part I - Static and dynamic physics of carriers and traps”, *IEEE Transactions on Electron Devices*, vol. 68, no. 9, pp. 4598-4605, September 2021, doi: 10.1109/TED.2021.3096777.

M. Rack, F. Allibert, J.-P. Raskin, “RF modelling of trap-rich passivated semiconductor substrates: Part II – Parameter impact on harmonic distortion”, *IEEE Transactions on Electron Devices*, vol. 68, no. 9, pp. 4606-4613, September 2021, doi: 10.1109/TED.2021.3096781.