Impact of Device Position within the Silicon Active Area on Self-Heating and Thermal Coupling in FD-SOI Transistors

N.Sahebghalam[1*], M.Vanbrabant[1], L. Lucci[2], Y. Zhang Fu[2], J-P. Raskin[1], V. Kilchytska[1]

[1]*Université catholique de Louvain, Louvain-la-Neuve, Belgium*

[2] *Université Grenoble Alpes, CEA, Leti, F-38000 Grenoble, France*

Abstract — This work investigates self-heating (SH) and thermal coupling (TC) in fully depleted silicon-on-insulator (FD-SOI) transistors, focusing on their location within the silicon active area (SAA). The gate resistance thermometry technique [1] is used to extract thermal resistance, and the resulting temperature rise in operating MOSFET ("heater") and nearby "sensors" at different distances from the "heater". A temperature rise (ΔT) of ~45 °C above ambient is observed for the "heater" and rapidly decreases with distance. Moreover, the device located near the SAA edge exhibits a ~6 °C higher temperature rise than the centrally located device, with no significant impact on the electrical figures of merit (FoMs). **Introduction**- Thermal effects, particularly self-heating, are significant in FD-SOI transistors due to the low thermal conductivity of the surrounding oxides, which limits heat dissipation and results in a rise of device temperature. This affects device performance through threshold voltage shift, mobility degradation and raise reliability concerns [2]. Therefore, understanding heat generation and dissipation is essential for accurate device modeling and optimization. In this study, the impact of transistor location within the silicon active area (SA and SB (Fig. 1)) on SH and TC behavior is investigated. **Measured Device-** The FD-SOI transistors, early stage prototypes within the FAMES 10nm FD-SOI Pilot Line [3] were processed in CEA Leti and are featuring a Back-oxide of 25nm a Silicon channel thickness of 7.5 nm and minimum physical gate length of 28 nm. The HiK metal gate stack has 1.8 nm HfO_2 on SiO_2 interlayer, followed by 6.5 nm TiN for a total height of 43 nm, with SiN spacers. Device is also featuring raised (~25 nm) S/D with in-situ doping. Specific test structure was designed to study SH and TC effects (Fig. 1). It is composed of one active gate finger (W = 5 µm, L = 30 nm) acting as a "heater" and four dummy fingers used as temperature sensors, positioned at 96, 222, 348, and 600 nm from the heater. Studied devices are only different in their location within the SAA. The "edge" device features SA = 0.076 µm and SB = 3.982 µm, whereas the "central" one has SA = 1.84 µm and SB = 2.218 µm. Moreover, both devices display an identical threshold voltage ($V_{th} = 0.41\,V$), extracted from the linear Id-Vg characteristics (Fig. 2), using 2nd derivative method. **Methodology-** The Gate resistance thermometry technique used to estimate the device temperature rise consists of two-steps: (1) calibration and (2) SH and TC extraction (Fig.3). During calibration step, the heater is turned off and gate resistances of the "heater" and "sensors" (R_G, R_{sen}) are extracted by applying a small current to the gate, while varying the chuck temperature. In the SH/TC extraction step, the "heater" is turned on at different biases (and hence dissipated power ($P = I_d \times V_d$)) and the resistances are measured using the same procedure, but the temperature rise (and corresponding resistance change) is now induced by device/"heater" operation while the chuck temperature remains at ambient. By comparing R_G, R_{sen} (T_{chuck}) and R_G, R_{sen} (P) plots, the device temperature due SH/TC is obtained. Thermal resistance is extracted from the slope of device temperature vs power curve. **Discussion-** Fig. 4 shows R_{th} and temperature rise ($\Delta T = T_{device} - T_{ambient}$) in the "heater" and "sensors" located at different distances from it. ΔT reaches about 45°C in the "heater" of "edge" device and decreases rapidly with distance becoming ~15°C and <5°C at 100 and 600 nm, respectively. The values exhibited by "edge" devices agree well with previously reported results for 28 nm FD-SOI technology [4] (Fig.4). Next to that, our experiments reveal that the "central" device exhibits lower R_{th} and, hence, a smaller ΔT than "edge" device. This is suggested to be due to larger silicon active area on the source side, which facilitates heat dissipation in "central" devices. The difference in ΔT between the "edge" and "central" devices is ~6 °C. Such a difference is expected to impact carrier mobility by ~2-3% (according to the power-law mobility µ(T) model [5]), thus leading to correspondingly lower drain

* Corresponding author: nika.sahebghalam@uclouvain.be

current and transconductance in the “edge” device. However, such small expected reduction could not be clearly evidenced in our experiments, as it is comparable to the variability in 10-15 measured dies (Fig. 2). Additional measurements may be required to further confirm the link between ΔT difference and electrical FoMs. **Conclusion**- SH and TC in advanced FD-SOI devices have been investigated. The impact of transistor location within the silicon active area is experimentally evidenced for the first time, to the best of authors’ knowledge. Thermal resistance, and consequently temperature rise, are ~10% lower in a “central” device thanks to larger silicon surrounding area which facilitates heats evacuation. While there is no clear evidence of the impact on the transistor FoMs, this difference, nevertheless, should be considered from a reliability perspective, as the “edge” device may experience enhanced aging and reduced lifetime compared to centrally located transistors.

References

[1] T. Takahashi *et al.,* IEEE J. Electron Devices Soc., vol. 4, no. 5, pp. 365–373, Sep. 2016.
[2] M. Cassé *et al.*, *2025 IEEE International Reliability Physics Symposium (IRPS)*, Monterey, CA, USA, 2025.
[3] C. Fenouillet-Beranger *et al., Solid-State Electronics*, vol. 231, p. 109264, 2026.
[4] F. E. Bergamaschi *et al.,* in IEEE Transactions on Electron Devices, vol. 71, no. 4, April 2024.
[5] T.-H. Shim *et al.*, *Journal of Applied Physics*, vol. 103, no. 9, p. 094522, 2008.

Acknowledgement- The research work presented in this abstract was carried out in the framework of the FAMES Pilot Line of the Chips JU, funded by Horizon Europe grant 101182279 and the ANR NextGen project ANR-22-NEXTG-001 of the France 2030 initiative.

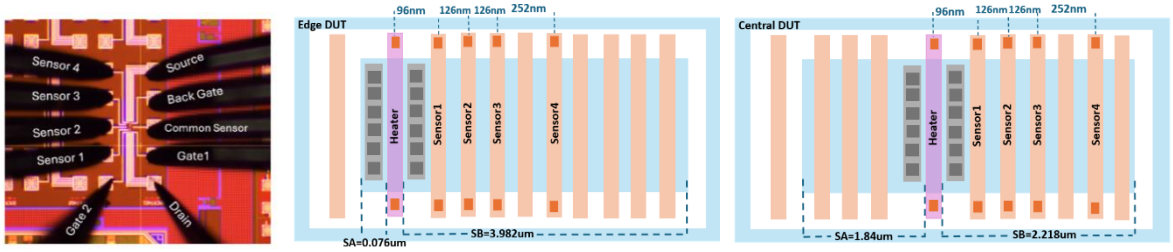

Figure 1. Thermal coupling structure.

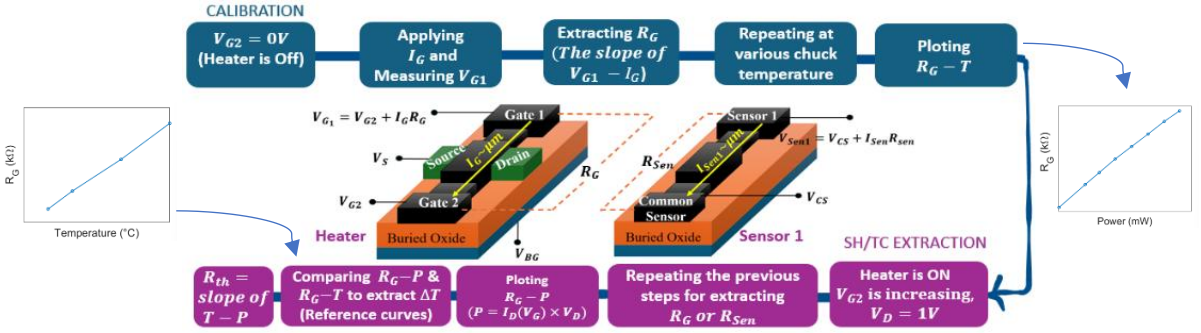

Figure 3. Measurement Methodology Overview

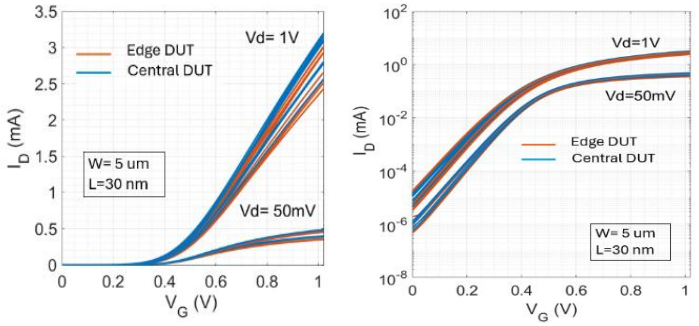

Figure 2. I_d-V_g characteristics of “edge” and “central” devices in linear and saturation regime in linear and semi-logarithmic scale.

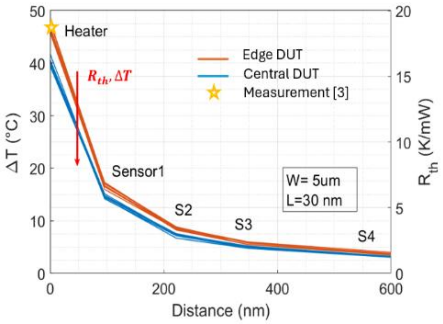

Figure 4. R_{th} and ΔT in different devices (V_g = 0.8 V, V_d = 1 V, P = 2.5 mW/m).