Harmonic Distortion in Symmetric and Asymmetric Self-Cascodes of UTBB FD SOI Planar MOSFETs

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***Abstract*— This paper presents an analysis of the harmonic distortion extracted from simulated results of symmetric and asymmetric self-cascode devices (S-SC and A-SC, respectively) composed by ultra-thin body and BOX fully depleted silicon-on-insulator planar MOSFETs 28 nm technological node. The results show that the A-SC effectively increases the operating drain current range for lower distortion. Comparisons with the literature show that the A-SC structures are a promising option for enhancing the circuit design flexibility for advanced MOSFETs.**

Keywords*— *UTBB; Asymmetric Self-Cascode; Composite Transistor; Harmonic Distortion; Analog Figures of Merit; SPICE Simulation.

I. Introduction

Ultra-thin body and buried oxide (BOX) (UTBB) technology is a promising variation of the planar fully-depleted (FD) SOI technology where the enhancement of the electrostatic control of the gate bias over the channel of the device due to the very thin front gate effective oxide, active layer and BOX thicknesses manages to further reduce the technological node [1]. The advantages of UTBB include improved short-channel effects [2], variability [3], parasitic resistances and capacitances and analog figures of merit [4].

One way to further improve the analog characteristics is the use of self-cascode (SC) structure [5], schematically shown in Fig. 1, where V_G, V_D and V_S are the gate, drain and source biases, respectively, and MS and MD are the transistors close to the source and close to the drain, respectively. Studies of self-cascode applications on other SOI technologies have shown further improvements on the output conductance and, therefore, the intrinsic voltage gain, without compromising other FoMs such as the cutoff frequency [5]. For the symmetric self-cascode (S-SC), where both transistors feature the same threshold voltage, V_T, the advantages regarding the output conductance are obtained due to the reduction of the channel length modulation effect caused by the presence of transistor of MD for a certain range of V_{DS}. The asymmetric self-cascode (A-SC) showcases transistors with different V_T, being $V_{T,MD} < V_{T,MS}$. For this case, the benefits are further enhanced due to diminishing the electric field peak close to the drain-channel junction and the impact ionization carriers generation [6].

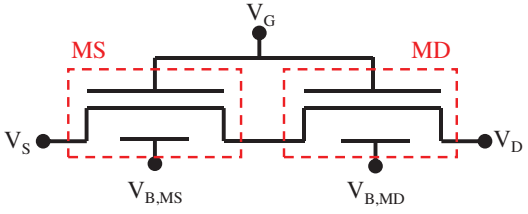

Fig. 1. Schematic representation of a self-cascode structure.

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The A-SC structure can take advantage of the V_T control by the back gate bias offered by the UTBB technologies [3]. SPICE simulation results reported in [7] have shown that the back-gate tuning combined with the SC structure can provide a promising alternative for analog circuit design.

The non-linearity is an intrinsic characteristic of MOSFETs that can be measured through the total harmonic distortion and third harmonic obtained from devices I-V characteristics. So far, works investigating the harmonic distortion on self-cascodes have been limited to standard planar FD SOI MOSFETs, being this the first reports of it for UTBB technologies, which are of importance for the potential use of this structure in RF applications.

II. Device Characteristics and Methodology

This work is based on SPICE simulations of transistors from 28 nm technological node from ST-Microelectronics [3]. In these technology transistors showcase a BOX thickness of 25 nm, active layer thickness of 7 nm and front gate EOT of 1.3 nm. The results were obtained through simulations performed using the software Eldo by Mentor Graphics [8] and the model referenced in [9], [10]. The simulated devices are 1 μm wide, with length (L) of 30 and 110 nm. The threshold voltage values (extracted by the second derivative method) of simulated single transistors are shown in Table I for different back-gate biases (V_{BS}).

The drain current (I_{DS}) curves as a function of gate-to-source voltage (V_{GS}) are presented in Fig. 2(A) for single transistors biased at drain-to-source voltage (V_{DS}) of 1V. The g_m/I_{DS}, which is a parameter that correlates the gain of current to a given current bias, is also presented. Fig. 2(B) shows the transconductance ($g_m = dI_{DS}/dV_{GS}$) as a function of the drain current. As expected, the increase of V_{BS} reduces transistors threshold voltage. Also, for a given drain current level, one can observe a small g_m increase with V_{BS} reduction.

These single devices were used to configure different SC structure. For all SC structures, the back bias of MD transistor ($V_{BS,MD}$) has been kept equal to 2V, whereas $V_{BS,MS}$ has been varied as shown in Table II. It is worth noting that symmetric self-cascode devices are obtained when $V_{BS,MS} = V_{BS,MD}$. As shown by these results, the threshold voltage of the composite structure is close to the V_T of the MS device for the self-cascodes. The small differences noted in the A-SC device are caused by the lower charges controlled by the gate-to-source

TABLE I. Threshold Voltage of Single Transistors Used to Form Self-Cascode Structures.

Length [nm]	V_T @ V_{BS}= -2V	V_T @ V_{BS}= 0V	V_T @ V_{BS}= 2V
30	0.56	0.44	0.32
110	0.59	0.47	0.32

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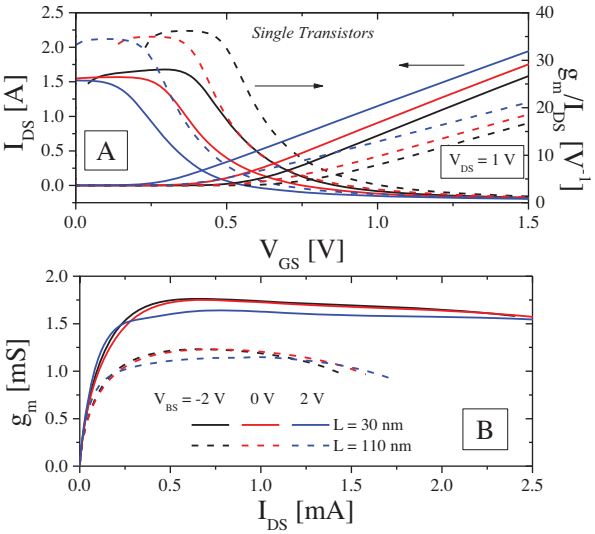

Fig. 2. (A) Drain current and tranconductance-to-current ratio as a function of gate-to- source voltage and (B) transconductance as a function of drain-to-source current for devices biased at V_{DS}=1V and various V_{BS}.

TABLE II. SELF-CASCODE STRUCTURES THRESHOLD VOLTAGE.

Self-Cascode ($V_{BS,MD}$=2V)			
$V_{BS,MS}$	L_{MS}=30nm L_{MD}=30nm	L_{MS}=30nm L_{MD}=110nm	L_{MS}=110nm L_{MD}=110nm
-2V	0.54 V	0.53 V	0.57 V
0V	0.42 V	0.41 V	0.47 V
2V	0.32 V	0.32 V	0.32 V

voltage when compared to the S-SC, because of the differences in the V_T of the two devices.

III. CHARACTERISTIC CURVES

Fig. 3 presents the drain current curves as a function of the gate-to-source voltage for the nine SC structures described in Table II biased at V_{DS} = 1V. The transconductance as a function of drain current is presented in Fig. 4. As can be seen by the comparison of S-SC (blue lines) and A-SC (black and red lines) with similar L_S and L_D, the increase of difference between $V_{T,MS}$ and $V_{T,MD}$ promotes an increase of g_m for low current levels, indicating the suitability of these structures for low voltage applications. For an A-SC with fixed L_S (solid and dashed lines), the increase of L_D reduces both I_{DS} and g_m. When L_D is kept constant (dashed and dot-dashed lines), the reduction of L_S increases the current. This behavior is in accordance with results reported for FD SOI devices with thicker Si and BOX layers [5], and shows that MS acts as a main transistor, whereas MD as a load, that reduces $V_{D,MD}$ variation.

The drain current curves as a function of V_{DS} were also simulated and used to extract the output conductance (g_D = dI_{DS}/dV_{DS}) at different gate voltage overdrive voltages (V_{GT} = $V_{GS} - V_T$). The g_D curves as a function of g_m/I_{DS} ratio are shown in Fig. 5. Apart from the increase of I_{DS} observed in I_{DS}-V_{GS} curves, the increase of $V_{T,MS} - V_{T,MD}$ difference is responsible for reducing channel length modulation effect, resulting in improved (smaller) output conductance.

By combining the results of g_m and g_D, the intrinsic voltage gain (A_V = g_m/g_D) has been obtained and is depicted in Fig. 6 as a function of g_m/I_{DS}. The A-SC associations will consistently display a higher A_V than single transistors and the associations where the two transistors were biased oppositely present even further enhancement, both due to larger g_m and

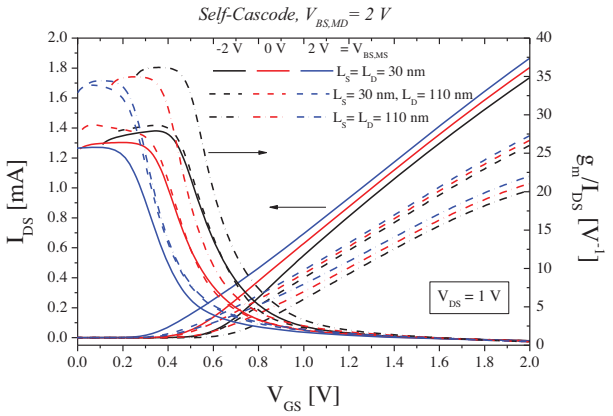

Fig. 3. Drain current and tranconductance-to-current ratio as a function of gate-to-source voltage for S-SC and A-SC devices biased at V_{DS}=1V.

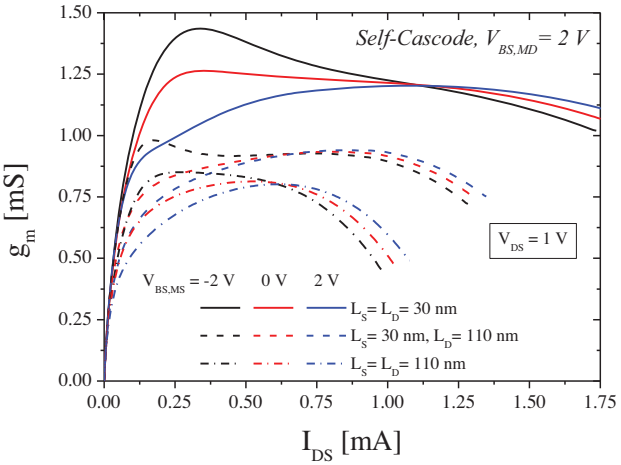

Fig. 4. Transconductance as a function of drain-to-source current for S-SC and A-SC devices biased at V_{DS}=1V.

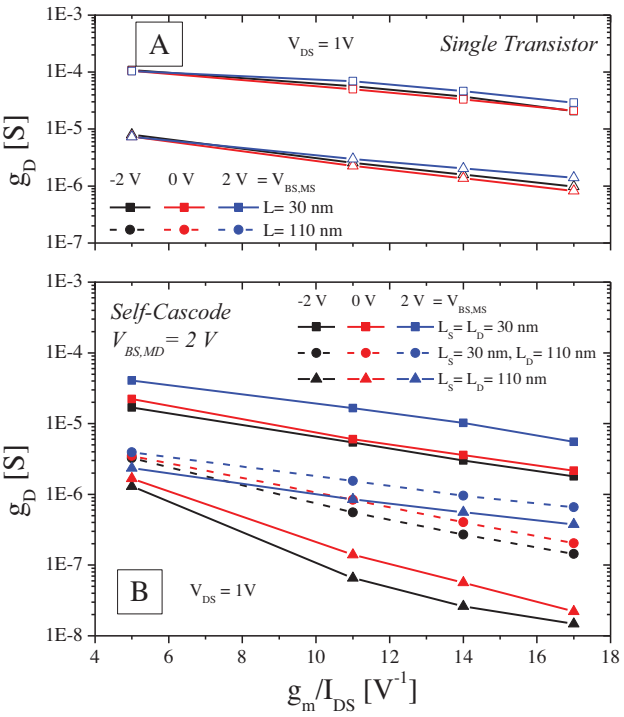

Fig. 5. Outuput conductance for Single Transistor (A) and for various S-SC and A-SC devices (B) as a function of transconductance over drain-to-source current biased at V_{DS}=1V.

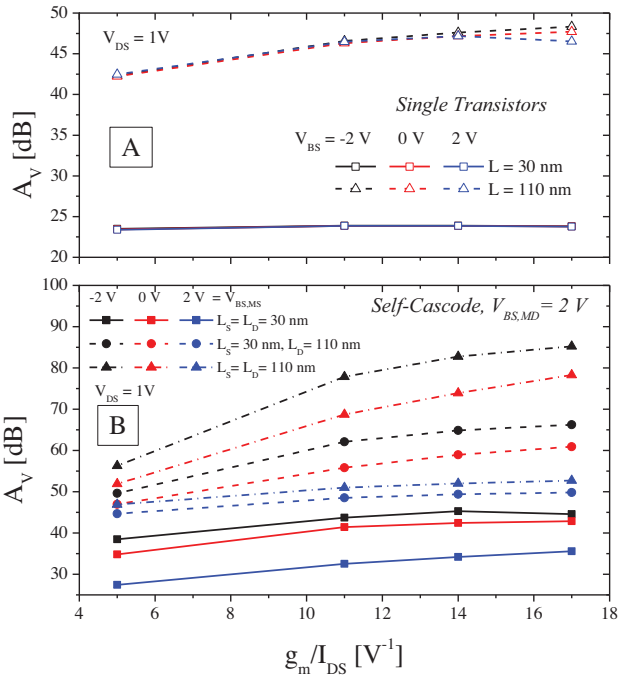

Fig. 6. Intrinsic voltage gain as a function transconductance over drain-to-source current ratio for (A) Single Transistors and (B) various S-SC and A-SC devices biased at V_{DS}=1V.

reduced g_D. It also can be seen that the best A_V values can be found for the associations showcasing a longer L_S and L_D.

IV. Harmonic Distortion

The results of harmonic distortion were obtained from DC I-V simulations of the transistors using the Integral Function Method [11], which allows for obtaining the total harmonic distortion, as well as the second and third order harmonics without the need of AC characterization. Fig. 7 compares the second harmonic (HD2), which is the main component of the total harmonic distortion, and the third harmonic (HD3), normalized by the intrinsic voltage gain, A_V (g_m/g_D), of self-cascode devices composed by MS and MD of different channel lengths and MS back-gate biases, as a function of the I_{DS}, considering a constant input amplitude (V_a) of 50 mV. These results were obtained considering different DC input bias points. When comparing the S-SC and A-SC composed by transistors of similar dimensions, it can be noticed that the larger difference between the two transistors V_T will provide an improved (reduced) distortion profile. Longer composite transistors enhance HD2/A_V and HD3/A_V and, for larger I_{DS}, the best values of HD2 can be found for the longer S-SC.

Using HD2 and HD3 equations described in [12], one can write equations 1 and 2 [12]. In order to correlate the obtained results to these equations, g_m and its first and second derivatives (dg_m/dV_G and d^2g_m/dV_G^2) are presented as a function of the I_{DS} on Fig. 8 and 9.

$$\frac{HD2}{A_V} = \frac{V_a \cdot \frac{dg_m}{dV_G}}{g_m{}^2} \cdot g_D \quad (1)$$

$$\frac{HD3}{A_V} = \frac{3}{2}\frac{V_a^2 \cdot \frac{d^2g_m}{dV_G^2}}{g_m{}^2} \cdot g_D \quad (2)$$

As it can be seen, for higher currents, dg_m/dV_G and d^2g_m/dV_G^2 are very close for all the combined transistors. Therefore, HD2/A_V improvement seen for the A-SC devices might be attributed to the higher g_m and reduced g_D, previously shown in Fig. 4 and 5. For HD3/A_V, at lower I_{DS} levels, dg_m/dV_G and d^2g_m/dV_G^2 trends compensate each other. However, the reduced g_D of A-SC once again reduces the distortion in comparison to single transistors.

Fig. 10 presents the harmonic distortion normalized by the gain at a fixed DC input bias ($V_{GS} - V_T$) of 400 mV and V_{DS} of 1 V, applying a variation on the input signal amplitude. From these results, one can see that HD2/A_V displays better (lower) results for the A-SC structures with largest difference between back-gate biases between the transistors. It can be also seen that, for a fixed distortion, A-SC structures allows for

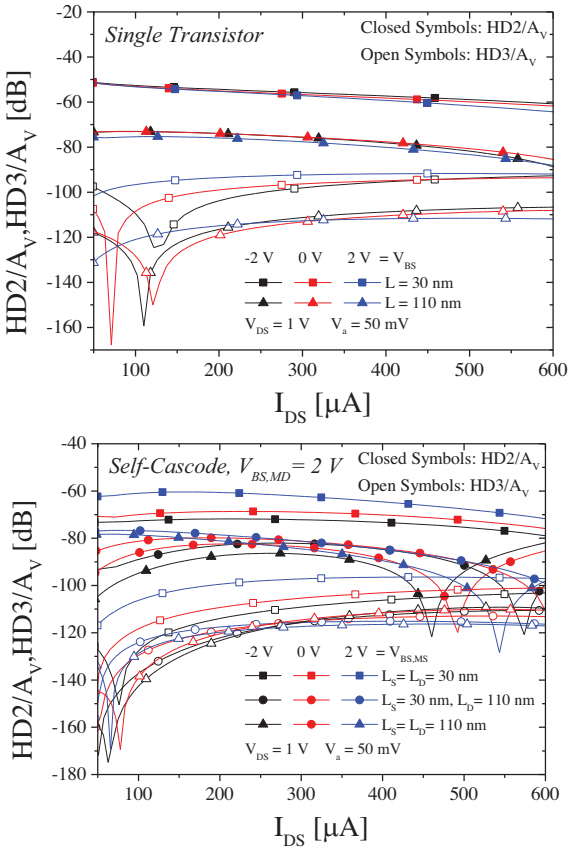

Fig. 7. 2nd and 3rd order harminics normalized by the intrinsic voltage gain as a function of the drain current biased at V_{DS}=1V and V_a = 50mV.

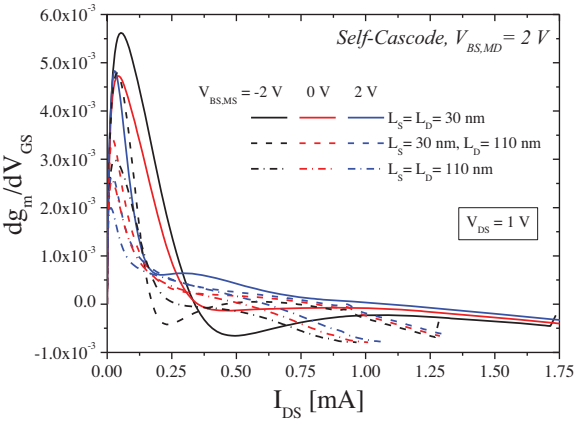

Fig. 8. First derivatives of the transconductance as a function of the drain current (I_{DS}) biased at V_{DS}=1V.

larger input signal. For instance, by picking a maximum -70dB of allowed HD2/A_V for the shortest composite transistor, an acceptable V_a range would be of 22 mV, 51 mV and 84 mV for, respectively, $V_{BS,MS}$ of 2 V, 0 V and -2 V, being the later more flexible for circuit design. Similarly, when comparing the other associations with $V_{BS,MS}$ of -2 V, a V_a of 192 mV and larger than 300 mV can be allowed for the associations with L_{MS} of 30 nm and 110 nm, respectively.

V. Conclusion

This paper showed an analysis of the harmonic distortion for symmetric and asymmetric self-cascode composite transistors combining UTBB nMOSFET, focusing on the variation of the back bias on MS. The results indicate that the A-SC structure can provide a reduced harmonic distortion. The A-SC also improves the flexibility of the circuit design for limited harmonic distortion applications, especially when considering the one formed by the longest individual transistors.

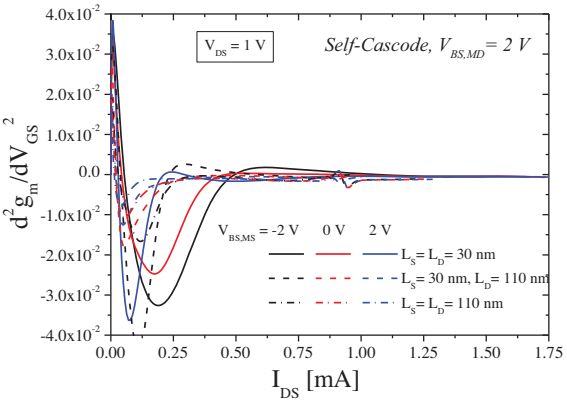

Fig. 9. Second derivatives of the transconductance as a function of the drain current (I_{DS}) biased at V_{DS}=1V.

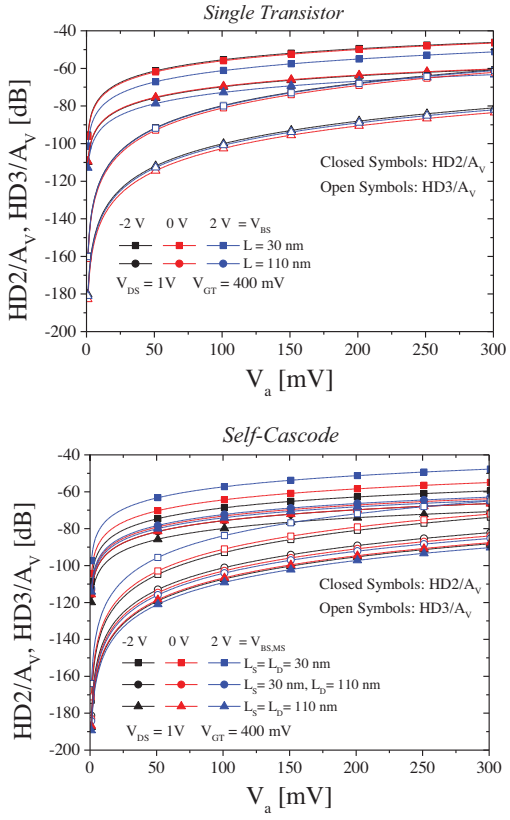

Fig. 10. 2nd and 3rd order harmonics normalized by the intrinsic voltage gain as a function of the input signal amplitude biased at V_{DS}=1V and V_{GS} - V_T = 400mV.

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