FinFET versus UTBB SOI - a RF perspective

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***Abstract*— FinFET and Ultra Thin Body and BOX (UTBB) Silicon-on-Insulator (SOI) MOSFETs are the most promising advanced devices to fulfill the International Technology Roadmap for Semiconductors (ITRS) requirements. Both devices have been intensively studied these last years. Most of the reported data concern their digital performance. In this paper, their analog/RF behavior is described and compared. Both show pretty similar characteristics in terms of transconductance, Early voltage, voltage gain, self-heating issue but UTBB outperforms FinFET in terms of cutoff frequencies thanks to their relatively lower fringing parasitic capacitances.**

Keywords—FinFET; UTBB; Silicon-on-Insulator; Analog/RF performance; Cutoff frequency; Mutiple gate MOSFET.

I. INTRODUCTION

Over the last decades silicon technology has been driven by downscaling dictated by the need of highly-integrated digital circuits. However, further reduction of device dimensions is problematic due to intrinsic physical limitations such as short channel effects, high current leakage through gate dielectrics, high series resistances, low mobility due to interface effects and high doping levels, and so on. The most common strategies to address these challenges include the introduction of new materials such as germanium, high-k gate dielectrics and metal gates, low-k for the backend dielectrics, Silicon-on-Insulator (SOI) technology, strain engineering and alternative device architectures (multiple gate, i.e. FinFET, tunnel FET, etc.).

Fully Depleted (FD) electronic regime is a promising approach to continue scaling of silicon metal–oxide–semiconductor field effect transistors (MOSFETs). Scaling the thickness of the silicon body is proposed in the case of FinFET and ultra-thin body and BOX (UTBB) technologies in order to control short channel effects [1, 2].

Good DC figures of merit (FoM) of FinFET and FD planar SOI devices were previously reported in [2, 3], respectively. However, analog/RF FoM for both advanced devices have not been widely reported. In this paper, the transconductance, the Early voltage, the voltage gain, the cutoff frequencies as well as the self-heating issue of FinFET and UTBB are presented and compared.

II. EXPERIMENTAL DEVICES

UTBB, called also 28 FD-SOI, were fabricated at ST-Microelectronics and FinFET at IMEC. UTBB presents a BOX, a Si body and an equivalent gate oxide thicknesses of 25 nm, 7 nm and 1.3 nm, respectively. The channel is strained and rotated by 45° from the (100) plane. The ground-plane implantation introduced under the BOX is well-type. The gate lengths of the measured devices range from 26 nm to 1 µm. More details about the process can be found in [3].

40 nm-long n-channel FinFETs were fabricated on Silicon-on-Insulator (SOI) wafers with 145 nm-thick BOX. Fin patterning (resulting in a 60 nm fin height) is followed by gate stack (HfO_2 dielectric + TiN gate) deposition, spacer formation, highly doped drain (HDD) implant, Ni silicidation and Cu Back-End-of-Line (BEOL). The background doping of the silicon fins is 10^{15} cm^{-3}, and no additional fin doping, threshold voltage adjust implants or halo (pocket) implants are used. FinFETs are composed of parallel gate fingers, each finger containing an array of parallel fins in order to design devices with appropriate channel width/length ratios, fin widths varying from 12 to 82 nm, numbers of fins per finger ranging from 5 to 20 and fin spacings between 228 and 528 nm. More details about the FinFET structures and technology can be found in [4, 5].

III. ANALOG PERFORMANCE

Fig. 1 benchmarks the studied 28 nm node UTBB against other technologies. Selected bias conditions are those that are typically used for analog applications and thus the data for other technologies are available [6, 7]. Variation of g_m with Av is chosen as a figure of merit. The benchmarked technologies include SOI FinFETs [6], planar MOSFETs [6] and UTBB MOSFETs [7]. The 28 nm node FDSOI devices outperform their counterparts and allow achievement of higher g_m and Av values. The 28 nm technology devices feature larger g_m than the UTBB devices due to strain in the channel while showing only a slight reduction of Av.

g_m–Av analog metric in Fig. 1 is obtained at DC, however, due to frequency dependence of self-heating and substrate effects [8], DC techniques do not provide fair assessment of analog FoM of devices aimed at high frequency operation. Therefore, RF characterization method was used. Fig. 2 shows

g_m–Av in the frequency range from 100 kHz to 1 GHz for UTBB. An increase of g_m and a reduction of Av with increasing frequency are observed. It is worth noting that the Av variation with frequency is dominated by strong g_d frequency dependence. Indeed, depending on the gate length, g_d increases by 25–70% due to self-heating and substrate coupling whereas g_m increases only by 1–10%. As a result Av decreases with frequency [9].

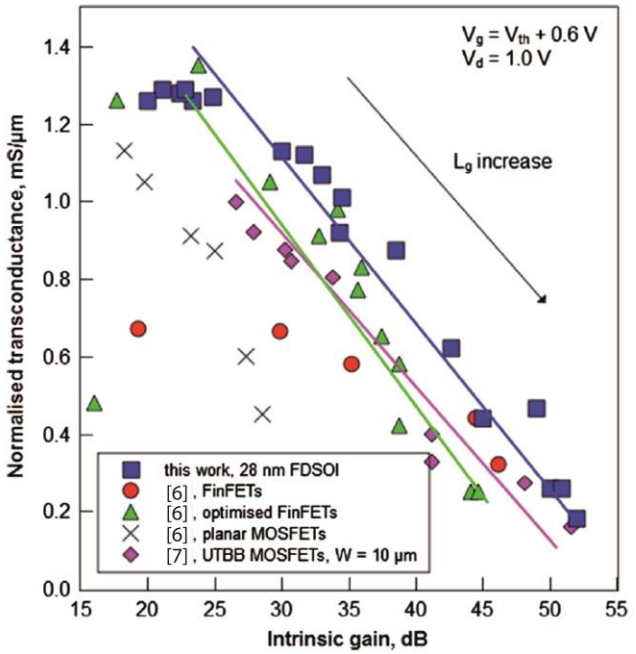


Fig. 1. Transconductance variation with Av in various FD SOI technologies at DC conditions [9].

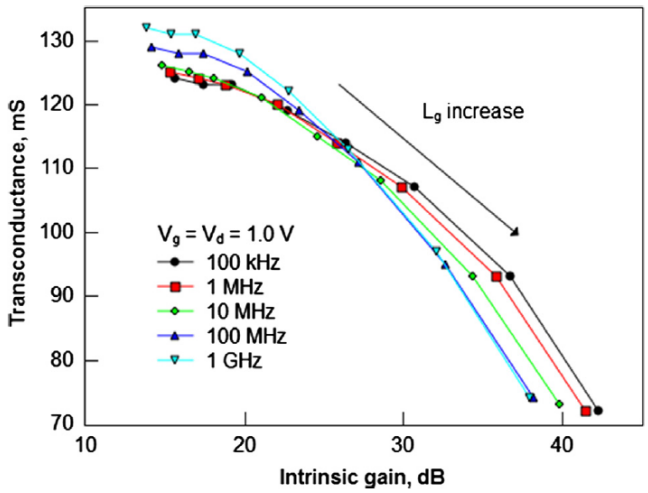


Fig. 2. Variation of g_m with Av extracted at various frequencies for UTBB at $V_g = V_d = 1$ V [9].

IV. Self-Heating Issues

Self-heating was evaluated using the RF extraction method described in [10]. The method relies on proportionality of the thermal resistance to g_d difference at high (isothermal) and low frequencies. RF thermal characterization is required as the isothermal frequencies of the advanced devices enter the gigahertz region [5, 11]. Indeed, the silicon volume of the advanced MOS devices being so much reduced the thermal time constant is today in the range of a few tens of ns.

The temperature rise is a product of the thermal resistance, the drain current and the drain voltage. Fig. 3 presents the temperature rise in the device active region of FinFETs above ambient (fixed at 300 K) for different fin widths. The temperature rise is obtained at a constant power of 50 mW. The temperature is smaller in the devices with wider fins and a higher number of parallel fins (not shown here) due to the reduced thermal resistance as expected. Fig. 4 shows the average temperature variation for UTBB with the gate length at $V_g = V_d = 1.0$ V. For the same channel length, UTBB and FinFET present similar self-heating behavior. Both devices are characterized by a quite thin and narrow silicon channel and the main thermal path from the channel is the source and drain contacts to the back-end metallic lines.

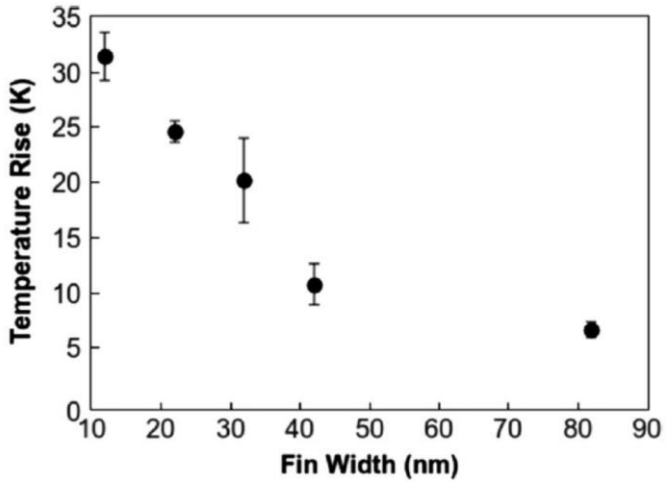


Fig. 3. Temperature rise above ambient in the channel of FinFETs with varying fin widths at constant power (50 mW) [5].

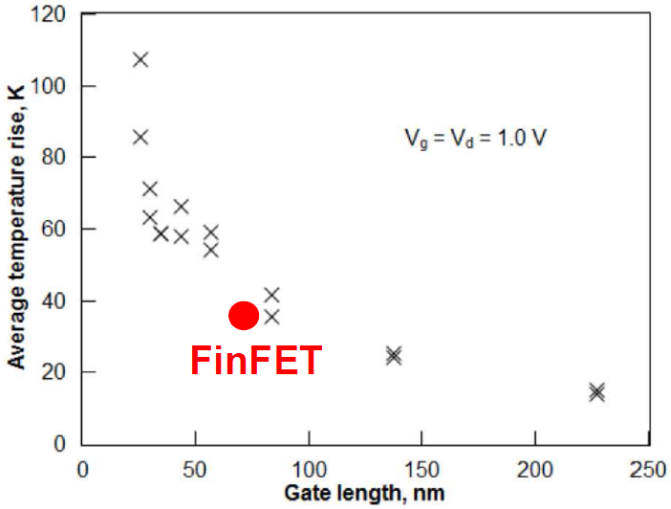


Fig. 4. Average temperature rise due to self-heating in UTBB devices with various gate lengths at $V_g = V_d = 1.0$ V [9].

V. CUTOFF FREQUENCIES

MOSFET frequency performance is evaluated by two major figures of merit, i.e. the maximum oscillation frequency, f_{max}, and the current gain cutoff frequency, f_T.

Fig. 5 shows the f_T and f_{max} variations versus with the channel length L_g. Both f_T and f_{max} increase with L_g scaling down but f_T follows a $1/L_g$ trend (and an even weaker one in shortest devices) i.e. attenuated comparing with ideally predicted $1/L_g^2$. This is due to carrier velocity saturation, parasitic source and drain resistances R_s, R_d and extrinsic total gate capacitance C_{gge}. It is important to point out that in case of devices shorter than 90 nm, f_{max} becomes smaller than f_T. This is due to the increase of gate resistance R_g with L_g reduction.

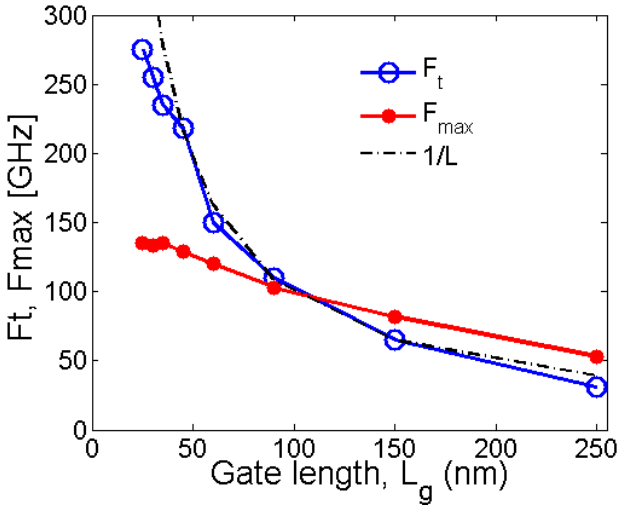


Fig. 5. f_T and f_{max} versus gate lengths (L_g) for UTBB with W_f = 2 µm and N_f = 10 [12].

Fig. 6 shows the comparison between the extracted cut-off frequency for FinFETs including the whole parasitic effects (f_{Te}), the cut-off frequency with the extrinsic series resistances removed (f_{TR}) and the intrinsic cut-off frequency, i.e. after withdrawing the parasitic resistances and capacitances (f_{Ti}) as a function of the FinFET channel length. First of all, comparing the current gain cutoff frequency of UTBB (Fig. 5) and FinFET (Fig. 6) of similar channel length we see that UTBB outperforms FinFET by at least 50%. In Fig. 6, we can also observe only a marginal improvement of f_T after the removal of the series resistances for FinFET. On the contrary, after withdrawing the total parasitic gate capacitance C_{gge}, intrinsic cut-off frequency reaches nearly 400 GHz for a 60 nm-long FinFET.

Fig. 7 compares the extracted extrinsic and intrinsic total gate capacitances (C_{gge} and C_{ggi}) for the measured L_g-array FinFETs. The capacitances are normalized by the total gate oxide capacitance (C_{ox}). As can be seen, for relatively long channel FinFETs (L_g = 500 nm), the extrinsic capacitances are much lower compared with the intrinsic counterparts. However, for short channel devices ($L_g \leq 120$ nm) C_{gge} is even greater than C_{ggi}. This effect is more noticeable as the channel length is decreased.

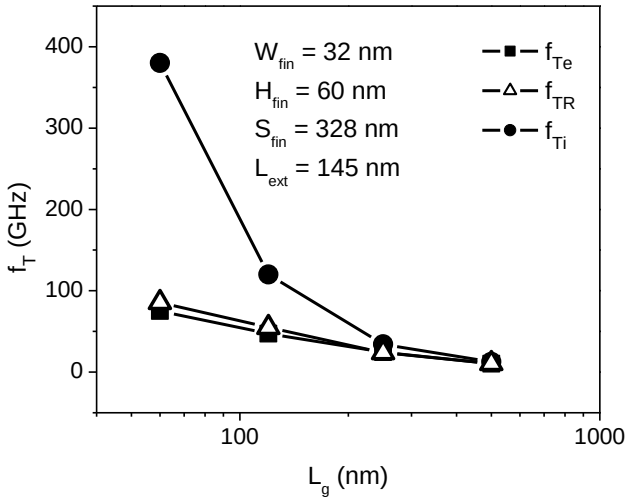


Fig. 6. Measured cut-off frequencies versus FinFET channel length [13].

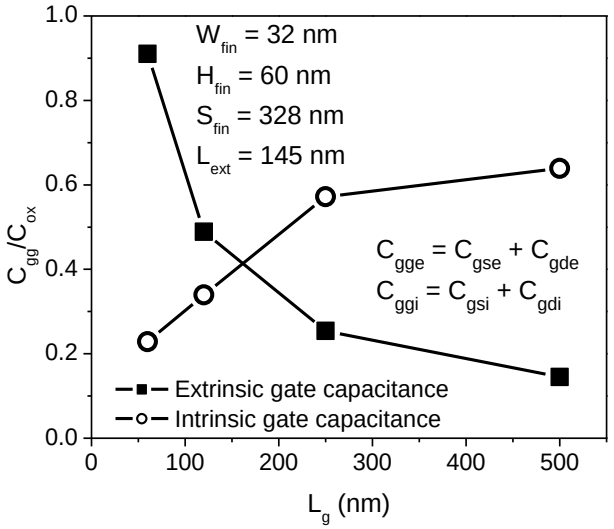


Fig. 7. Comparison between the C_{gge}/C_{ox} and C_{ggi}/C_{ox} ratios for measured FinFETs with different channel lengths. C_{ggi} are extracted at V_d = 1.1 V and V_g at maximum gate transconductance [13].

The origin of the additional parasitic capacitance in the case of FinFET (and multiple gate devices in general) is directly related to the metal or polysilicon interconnection between each fin. The parasitic capacitance value depends on the proximity between the gate and S/D electrodes, and it will be more and more important as L_{ext} is comparable or even shorter than S_{fin}. For very short L_{ext}, direct electrical coupling exists between both electrodes, and thus a parallel-plate like capacitor (C_{3b}) must be considered between the gate electrode and the S/D electrodes, as presented in Fig. 8. Thus, the C_3 component has to be split-off in two parts: (i) C_{3a} which corresponds to the fringing component as was indicated in the Wu's model [14], and (ii) C_{3b} a parallel-plate like component.

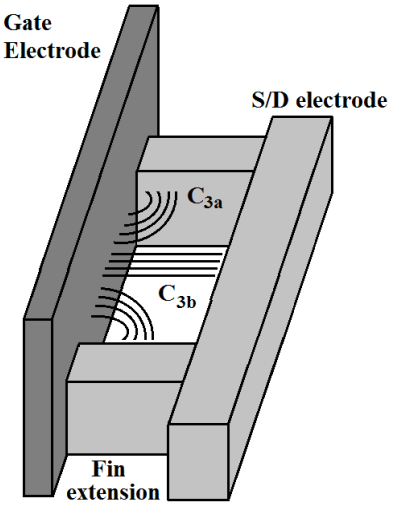


Fig. 8. Three-dimensional view of two fins half-FinFET to highlight the capacitance components C3a and C3b which correspond, respectively, to the fringing component as was indicated in the Wu's model [14] and a parallel-plate like component between the sides of the gate electrode and the S/D contact regions [13].

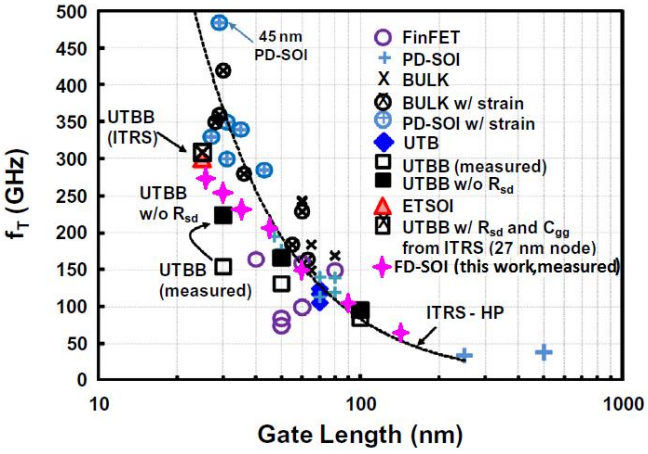
In [13], measurements and numerical 3-D simulations clearly demonstrate the improvement achieved by reducing the fin spacing, the S/D fin extension as well as by increasing the fin aspect ratio.

VI. BENCHMARKING WITH STATE-OF-THE ART DEVICES

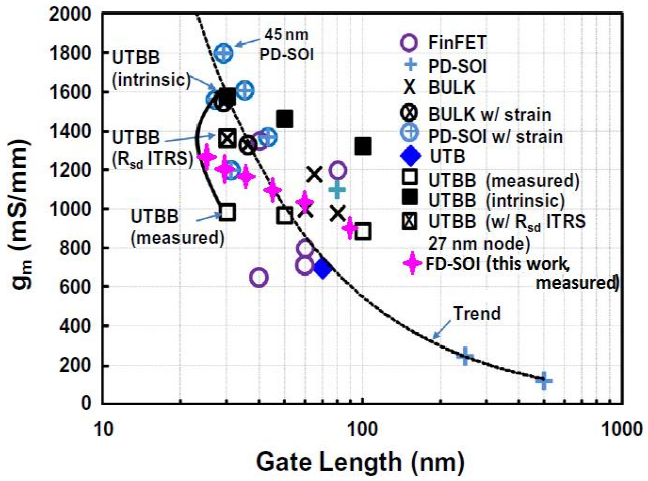
The benchmarking of f_T and g_m for the UTBB and other state-of-the art technologies are shown in Fig. 9. As can be seen, the highest g_m and f_T of 1,800 mS/mm and 480 GHz, respectively, is reported for 45 nm-node CMOS technology based on PD-SOI MOSFET with strained technique [15]. Fig. 9a and 9b show the direct correlation between $g_{m\text{-}max}$ and f_T. Our benchmarking illustrates that the performance of the studied UTBB 28 FD-SOI is much better than previous reported in [16] and is comparable with other technologies reported before i.e. UTB, PD-SOI, FinFET and Bulk for similar gate lengths. Besides the mobility boosters, an efficient improvement is achievable by optimization of process and architecture targeting reduction of parasitic series resistances and capacitances.

VII. CONCLUSION

FinFET and UTBB SOI MOSFETs are the promising advanced devices to fulfill the ITRS requirements. Efforts must be made on the reduction of the parasitic resistances and capacitances, especially in the case FinFET, to still get high-speed and high-frequency behavior improvements with the transistor channel length downscaling.



(a)



(b)

Fig. 9. Benchmarking of (a) f_T and (b) $g_{m\text{-}max}$ of state-of-the art MOSFETs versus gate length, L_g (nm).

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