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Effect of Heat Sink in Back-End of Line on Self-Heating in 22 nm FDSOI MOSFETs

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***Abstract*—This work studies the effect of heat sink in the back-end of line on the self-heating (SH) parameters. The RF characterization technique, which involves S-parameter measurements over a wide frequency range, is used to evaluate SH parameters. Two types of sink configurations in the back-end of line (BEOL) are considered; one connected to the gate and the other left floating. We experimentally demonstrate that gate-connected heat sink allows for a reduced self-heating in 22 nm FDSOI devices. Around 15% to 20% reduction in thermal resistance is observed for the gate-connected heat sink in comparison to the floating sink.**

Keywords-FDSOI; UTBB; Self-Heating Effect, BEOL, Heat Sink, S-Parameters

I. Introduction

The downscaling of CMOS technology has been crucial for the improvement of device performance and reduction of manufacturing costs [1]. The aggressive scaling of gate lengths and equivalent oxide thicknesses has helped in achieving lower intrinsic switching delay (CV/I) in high performance transistors [2]. Reduced gate length is highly beneficial for the MOSFET frequency performance increasing the current gain cutoff frequency f_T and maximum oscillation frequency f_{max} [3]. However, lower device dimensions result in higher current and power densities, which potentially increases the concerns associated with self-heating (SH) effect. As a consequence of higher device temperatures caused by SH, undesirable effects like mobility reduction, threshold voltage shift, lower output current and reduced reliability are encountered [3].

Aiding the dissipation of this heat generated in the channel would ameliorate the issues arising from SH. Removal of the heat generated in the channel can take place through the substrate, gate and drain regions and the back-end of line (BEOL) above. Previously, the prospect of using thermal shunts in the BEOL to suppress SH was studied in [4] by simulations. Out of the aforementioned possible heat evacuation paths, the BEOL path above the MOSFET is of interest in this work. Our work addresses heat evacuation through the BEOL using various heat sink configurations by experimental analysis.

The 22 nm Fully depleted Silicon-on-Insulator (FDSOI) technology from GlobalFoundries, one of the most advanced nodes that caters to the tremendous requirements in upcoming mobile, RF and Internet-of-Things (IoT) applications [5], is used in this study. The BEOL consisting of 11 metal layers in the technology provided ample scope of realization of heat sinks to facilitate heat dissipation. Knowing that FDSOI is more prone to SH issues because of the presence of the buried oxide (BOX) layer under the channel, our approach was tested on this technology [6].

In this paper, potential techniques of reducing SHE are explored experimentally using dedicated heat sinks for the devices implemented in the process' BEOL. Additionally, the effect of the presence of the heat sinks on performance of the devices is studied.

II. Experimental Details and Approach

The devices used in this study originate from the 22 nm FDSOI technology from GlobalFoundries [5]. The gate length is 20 nm, total width is 30 µm for each of these devices composed by 60 fingers of 0.5 µm finger width. In this work, two identical FETs but with two different heat sink configurations are considered. One of them is connected to a heat sink through the gate (called "gate-connected sink"), while the other one includes the same heat sink, which is left floating (called "floating sink").

The heat sink, introduced in the BEOL, consists of a metallic pad right above the FET over which the passivation layer is removed. With the BEOL consisting of 11 metal layers, a metal plate of 234 µm by 114 µm is used on the uppermost metal layer, connected down with vias to the fifth metal layer. Fig. 1 and Fig. 2 schematically

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illustrate the gate-connected sink and the floating sink configurations used respectively. The floating sink is left electrically and thermally floating above the fingers of the FET in the fifth metal layer and consists of metal rectangles that continue to stack up to the metal plate in the topmost layer. The gate-connected sink comprises of a similar metal plate in the top metal layer, however, it is connected by vias to the gate above the gate accesses. The main difference between these two kinds of sinks is the electric and thermal connection to the gate with metal vias above the fifth metal layer (labelled as connected vias "Vx" in Fig. 1). The absence of these vias in case of the floating sink can also be perceived clearly in Fig. 2.

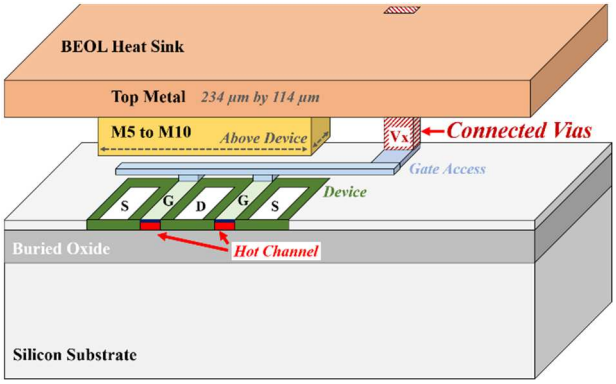

Fig. 1. Schematic of the gate-connected sink

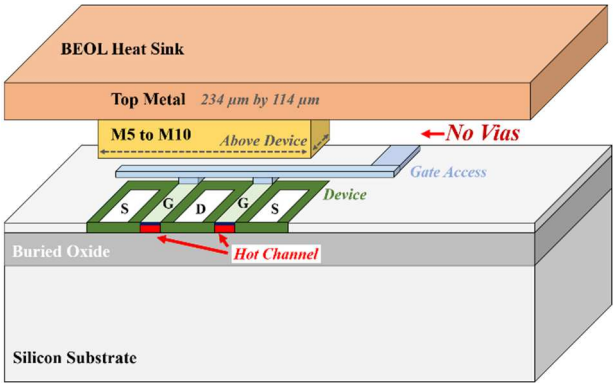

Fig. 2. Schematic of the floating sink

To assess self-heating features we use in this work the RF characterization technique, a frequency domain method. RF technique was recently shown to be the most suitable for SH characterization in the most advanced deeply down-sized state-of-the-art devices [7], because frequencies up to a few gigahertz need to be reached to attain dynamic self-heating-free conditions in these devices. In this context, it is important to look into the thermal resistance R_{th} and thermal capacitance C_{th}. An RC thermal circuit consisting of R_{th} and C_{th} can then be used to model the complex thermal impedance as described in [8]. R_{th} refers to the resistance offered to heat flow and is linked to the temperature rise ΔT and power P as

$$\Delta T = R_{th} \cdot P \quad (1)$$

While R_{th} depends on the surface area available for heat evacuation, C_{th} depends on the volume available to store heat [7]. With technology scaling down, the thermal capacitance C_{th} related to the device volume reduces, reducing the thermal time constant τ_{th} which is the product of R_{th} and C_{th}. The thermal frequency ($f_{th} = 1/(2\pi\tau_{th})$) that is inversely proportional to τ_{th}, is thereby shifted to higher values. Alternative techniques for SH characterization have shown distinct limitations especially for devices in the most advanced technology nodes. For example, the AC conductance technique is limited in frequency to a few megahertz [7] due to which accurate estimation of SH parameters in advanced devices with a high thermal frequency is not possible. The Pulsed IV technique, on the other hand, uses pulse widths that are not sufficiently low for advanced devices with low thermal time constants. For this reason, the RF technique was preferred over other characterization techniques for the devices studied in the 22 nm FDSOI technology.

For the RF characterization, S-parameters are measured in a frequency range from 100 kHz to 3 GHz and converted to Y parameters. An ENA vector network analyser and two RF |Z| probes of 100 µm pitch are used for these measurements. SOLT (Short-open-load-thru) method is used for calibration at room temperature. The output conductance (g_d) is computed as the real part of Y_{dd}, transconductance (g_m) is the real part of Y_{dg}.

The impact of SH causes a transition from low frequency to the high frequency in Y_{dd} which can be seen in (2) [11].

$$Y_{dd,HF} - Y_{dd,LF} = Z_{th} \frac{\partial I_d}{\partial T} (I_d + V_d Y_{dd}) \quad (2)$$

From the real part of (2) above, the g_d versus frequency curve shows a transition due to SH, which allows to assess SH-related features (as e.g. R_{th}). In a similar way, a transition from the imaginary part of the Y_{dd} in (2) can be alternatively used to evaluate SH. In this work, it is the g_d versus frequency transition from the real part of (2) that has been used to extract R_{th}. The transition due to source and drain coupling through the substrate is suppressed by the doped back gate in our devices [9]. The thermal resistance R_{th} can be extracted using the equation (3) given below:

$$R_{th} = \frac{\Delta g_d}{(I_d + V_d g_{d,LF}) \partial I_d / \partial T} \quad (3)$$

where Δg_d is the difference between $g_{d,LF}$ and $g_{d,HF}$ the output conductance g_d at low and high frequencies

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respectively, I_d is the DC drain current, $g_{d,LF}$ is the output conductance g_d at low frequency and $\partial I_d/\partial T$ is the slope of the I_d versus temperature plot extracted from I_d-V_g curves measured in a temperature range from 300 up to 400 K. This has been achieved by a Thermochuck from Temptronic that allows heating up the devices to the desired temperature points with good temperature control and stabilization. The extractions have been made in saturation at a V_g and V_d of 0.9 V. Though the nominal V_d of this technology is 0.8 V, a value of 0.9 V has been used here to increase the power in the channel and thereby stimulate higher SH. The back gate was grounded during measurements.

III. Results and Discussion

Fig. 3 shows the I_d-V_g and the g_m-V_g curves for both types of devices in saturation at V_d = 0.9 V. The fact that the gate connection of the sink does not affect the DC device performance is observed from the almost overlapping curves. The same threshold voltage V_{th} of 0.34 V is obtained for both types of devices from the second derivative method in the linear regime.

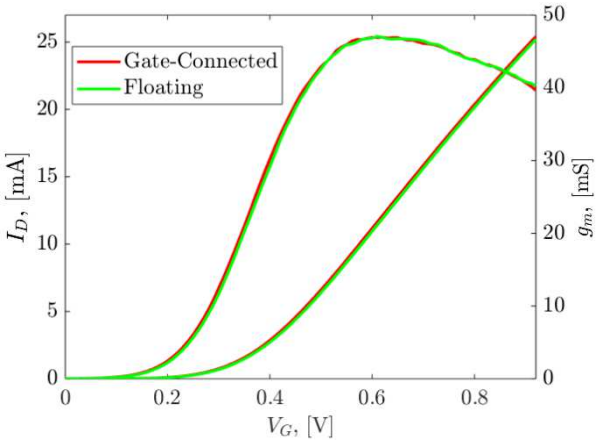

Fig. 3. Drain current I_d and transconductance g_m vs gate voltage V_g for the "gate connected" and "floating" sinks recorded in saturation at V_d = 0.9 V.

One can expect greater capacitive coupling in the case of gate-connected sink and thus degradation of the short circuit current gain H_{21}. We have verified that in our case measured H_{21} degradation is limited to ~1.5 dB at 1 GHz and a 28% increase in total gate capacitance is observed.

Fig. 4 shows the I_d-V_d curves for both types of devices for V_g = 0.9 V. While it is observed that the curves are mostly overlapping, the I_d and its slope (i.e. g_d) for the gate-connected sink are a bit larger than that for the floating sink in saturation suggesting weaker SH in the gate-connected sink device.

Fig. 5 shows the variation of output conductance g_d with frequency and from this plot, $g_{d,LF}$ (g_d at low frequency of 10 kHz), $g_{d,HF}$ (g_d at high frequency of 1 GHz) and Δg_d (the difference between $g_{d,HF}$ and $g_{d,LF}$) are extracted. The values of g_d at low and high frequencies represent the cases where dynamic self heating is present and removed, respectively. Higher value of g_{d_LF} obtained for the gate-connected sink agree with conclusions drawn from I_d-V_d plots above and demonstrate the fact that it is less affected by SH compared to the floating sink.

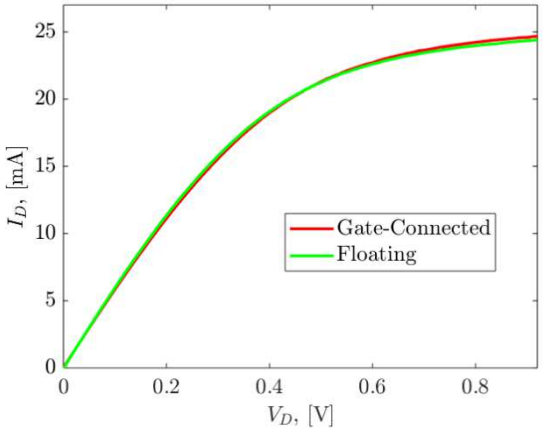

Fig. 4. Drain current I_d vs drain voltage V_d for the "gate connected" and "floating" sinks recorded at V_g = 0.9 V.

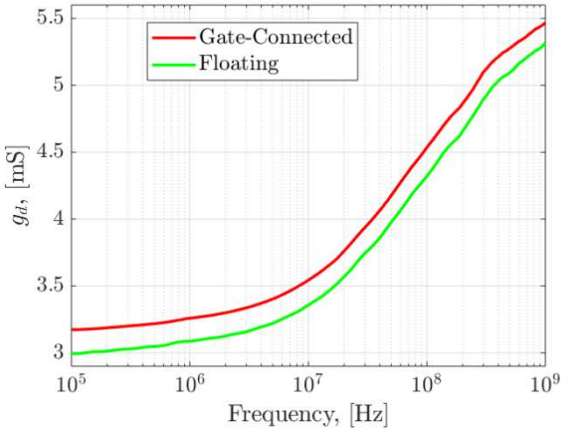

Fig. 5. Output conductance g_d vs frequency for the "gate connected" and "floating" sinks at V_g = V_d = 0.9 V.

Table I summarizes the comparison of the devices with gate-connected sink and floating sink not only in terms of normalized values of R_{th}, but also various parameters of Eq. 1, such as output conductance g_d at low frequency $g_{d,LF}$ and the difference between g_d at high and low frequencies Δg_d and $\partial I_d/\partial T$. Higher value of $g_{d,LF}$ and lower Δg_d are obtained for the gate-connected sink demonstrating lower SH there. The absolute value of $\partial I_d/\partial T$ is found to be higher for the gate-connected sink confirming weaker SH in this case. Combination of the above parameters results in a lower value of R_{th} for the gate-connected sink. It is observed that the normalized R_{th} in the case of gate-connected sink is around 20 % lesser than for the floating sink case. Measurements on multiple dies confirm these

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trend of lower normalized R_{th} and lower $g_{d,LF}$ in the case of gate-connected sink.

Theoretically, the absence of the metal vias above the fifth layer of the BEOL in the case of the floating sink results in a greater R_{th} of that part. This stems from the fact that the thermal conductivity of dielectric SiO_2 is two orders of magnitude lower than that of bulk Silicon and even lower w.r.t metal [10]. On the other hand, in case of the gate-connected sink, connections from the FET to the heat sink in the topmost layer is expected to allow easier heat evacuation, resulting in a lower overall R_{th}. The results obtained experimentally validate the idea.

TABLE I. SELF-HEATING PARAMETERS. VG=VD=0.9 V.

Sink Type	$g_{d,LF}$ *(mS)*	Δg_d *(mS)*	dI_d/dT *(μA/K)*	*Rth Normalized (Kμm/mW)*
Connected	3.17	2.29	-9.85	254
Floating	3	2.31	-8.17	313

IV. CONCLUSION

The prospect of using a BEOL heat-evacuator in order to alleviate self-heating in advanced devices has been studied in this work. The reduction of thermal resistance (and hence temperature rise) in the case of a sink connected to the gate in comparison to it being left floating with respect to the gate has been experimentally verified. The fact that the performance of the two types of devices are similar in order to make a fair comparison with respect to SH parameters has been verified. With the present configuration, we have achieved ~15-20% of the SH parameters reduction. Thus, the possibility of using a gate-connected sink to reduce self-heating has been put forth here as a proof of concept. To enhance the efficiency of the heat removal by the sink and minimize the parasitic capacitance added by it, further optimization of the sink configuration is envisaged. Prospect of future work includes extraction at other bias conditions and usage of an alternate SH extraction technique from the transition in the imaginary part of Y_{dd} to supplement the results obtained in this work.

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