This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JSEN.2017.2647848, IEEE Sensors Journal

Quantum Efficiency Improvement of SOI PIN Lateral Diodes Operating as UV Detectors at High Temperatures

C Novo[1], R Bühler[1], J Baptista[1], R Giacomini[1], A Afzalian[2] and D Flandre[2]
[1]*Centro Universitário da FEI, São Bernardo do Campo, Brazil*
[2]*ICTEAM Institute, UC Louvain, Louvain-la-Neuve, Belgium.*

***Abstract*— Thin-film lateral SOI PIN diodes can be used as photodetectors especially in the wavelength range of blue and UV radiation. Unlike vertical devices, lateral diodes can have depletion regions very close to the device surface, where the absorption of low-wavelengths radiation takes place. Due to this proximity to the surface, a MOS back-gate can control the charge density inside this region, allowing quantum efficiency improvement. This work reports experimental results of SOI PIN photodetectors with different intrinsic lengths in the 300K to 500 K range, simultaneously considering back-gate bias and temperature influences. Indeed, the back-gate bias becomes very effective in terms of quantum efficiency control with up to 52.4% for LI=1µm at T=500K in inversion mode, while in accumulation, the resulting efficiency was 48.2% at T=500K for the device with LI=10µm at UV. These variations are related to the behavior of dark current and recombination rate of the devices.**

***Index Terms*—photodiode, quantum efficiency, PIN, intrinsic length, dark current, photosensitive.**

I. Introduction

Optical detection at short wavelengths in the ultra-violet (UV) spectral range from 10 nm to 400 nm is widely used in many applications that can be found in medical imaging and optical communication market (280 nm – 400 nm) [1,2], protein analysis and DNA sequencing (240 nm – 300 nm) [3,4], forensic analysis (250 nm – 300 nm) [5], disinfection and decontamination (240 nm – 280 nm) [6] and space observation (Vacuum and Extreme UV ranges from 10 to 200 nm) [7,8]. The devices used in such applications can operate at temperatures of up to 500K, and require fast response, low dark current levels, high quantum efficiency and signal to noise ratio (SNR) [9]. An efficient alternative to absorb short wavelengths with Si-based devices is to implement photodetectors in thin silicon layers based on SOI wafers [10], in which the presence of the buried oxide below the active silicon film promotes isolation from the carriers generated in the substrate. The SOI PIN photodiodes studied here consist of highly doped P and N regions separated by an intrinsic region (with light P-type residual doping) with length L_I (Fig. 1a). In such lateral devices, carriers generated by light radiation at short wavelength can be collected more efficiently, because a depletion region can be formed from the surface to the depth of the silicon film in addition to the standard junction depletion regions. This fact is important since the light penetration depth in semiconductor varies according to the wavelength [11], therefore the lower the wavelength, the lower the penetration depth. The thickness of the SOI intrinsic region has to be thick enough to absorb the target wavelength range (e.g. 70nm of Si for 400nm light), but thin enough to allow full depletion and limit the junction leakage current and capacitance [10]. Furthermore, the hole-electron pairs must not recombine, and have to be quickly separated by the horizontal electric field present in the depletion region. Therefore, the intrinsic region length must be a compromise between being long enough to allow the absorption of a significant number of photons, but sufficiently short to guarantee that the entire intrinsic region is depleted and the photogenerated carriers are drifted by the horizontal electric field before they are recombined [12]. Thus, the size of the intrinsic region is a trade-off between speed of response and sensitivity.

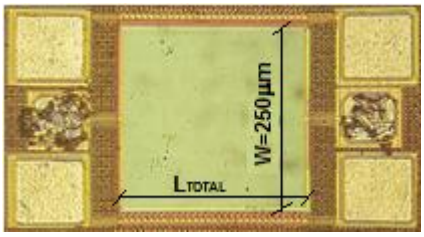
The devices analyzed in this work were fabricated on the ST 0.13µm SOI CMOS technology described in [14]. They consist of five PIN diodes with different intrinsic lengths (L_I), obtained by changing the numbers of parallel fingers (m), but keeping the same total surface area (A_{TOTAL}) of 0.0625mm^2. Fig. 1 (a) presents a photograph of one of the experimental photodiodes used in this work. Fig. 1b shows a 3D schematic view of the studied PIN SOI photodiode which have a doping profile of P+/P-/N+ and t_{SI}=150nm (active silicon region), t_{BOX}=390nm, L_P=L_N=1.36µm and t_{OX}=300nm. The parallel multifinger configuration consists of a number m of P+/P-/N+ structure placed side by side where the N+ region of one funger is connected to the N+ region of the adjacent finger and so on. This is a very important configuration to photosensors devices since there can be a reduction in the chip area. Table I and Table II summarize the main dimensions and parameters of the 5 devices (PIN 1 to 5), respectively.

This paragraph of the first footnote will contain the date on which you submitted your paper for review.

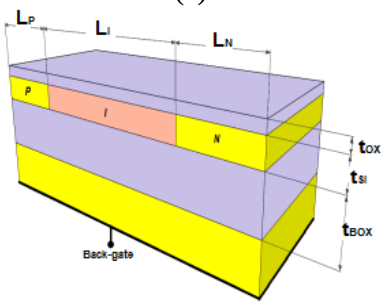
This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JSEN.2017.2647848, IEEE Sensors Journal

Table I: Lateral SOI PIN technological dimensions

PIN ID:	PIN – 1	PIN – 2	PIN – 3	PIN – 4	PIN – 5
L_I (µm)	1	2	5	10	100
m	105	75	39	22	2
W (µm)	250	250	250	250	250
Ltotal (µm)	249.16	250	249.4	251.28	204.08



(a)



(b)

Fig 1: PIN SOI Photodiode: a) Picture of one studied device b) 3D Schematic view of the studied PIN SOI photodiode.

Table II: Lateral SOI PIN technological parameters.

Parameter	*Value*
Silicon Thickness (t_{Si})	150nm
Buried Oxide Thickness (t_{oxb})	390nm
Passivation Oxide Thickness (t_{ox})	300nm
P^- Doping Concentration (N_I)	$1x10^{15}$ cm^{-3}
High Doped Regions N^+ (N_D) and P^+ (N_A)	$1x10^{20}$ cm^{-3}

The main parameters that define the photodiode`s behavior are the responsivity (from the relation between the photocurrent and the optical power), the total active area (responsible to absorb the light), the dark current (the current in the dark condition, generated by background radiation and saturation current from pn diode junction under reverse bias), the bandwidth (the diode capacitance influence on the rise and fall time of the photocurrent, impacting the speed of the photodiode) [13] and quantum efficiency (that is the relation between the current generated by light and the maximum current that would be generated without any kind of loss.

In fact, the aim of this paper is to present a deep analysis of total quantum efficiency in order to improve it. This goal will be achieved including the analysis of the parameters that directly influences the quantum efficiency of PIN diodes: temperature, back-gate bias, and intrinsic length variation.

II. Temperature Effect

In order to evaluate the performance of PIN photodiodes as photodetectors, the devices were measured for temperatures (T) ranging from 300 K to 500 K. The Variable Temperature Micro Probe System K20, from MM Technologies, has been used to control the range of temperatures. For electrical characterization, the measurements were conducted with Agilent 4156C Semiconductor Parameter Analyzer, considering the dark condition (absence of light) and the illuminated condition, with the photodiode exposed to different wavelengths ranging from 376nm to 401nm with incident optical power of 0.63µW.

The influence of back-gate voltage (V_{BG}) is very important in the performance of photodiodes, controlling the condition of the active silicon layer, which can be inversion, accumulation or depletion [15]. In Fig. 2a and Fig. 2b, the total diode current (I_{TOTAL}) normalized by the number of fingers is presented as a function of V_{BG}, for temperatures of 500K and 300K, respectively, with the incidence of UV light and incident optical power of 0.63µW. As can be seen, the current level is higher at 500K (Fig. 2a), independently of L_I since it is composed mainly by the leakage current. With the temperature raise, an increase in the number of electrons with sufficient thermal energy to pass into the conduction band occurs. The intrinsic concentration of carriers, n_i, presents a raise for higher temperatures while E_g (band-gap energy) suffers a moderate decrease. Therefore, the value of the junction internal potential (V_{bi}) will suffer changes with temperature variation. All these effects explain the change in the generation/recombination rate, which affects specially the dark current of the device, which in turn, will affect the total.

The accumulation in the bottom of the photodiode occurs for V_{BG} around -7.9V, where there is a decrease of the current, related to the decrease of electron mobility and the increase of recombination, due to higher hole concentration. The depletion occurs when increasing V_{BG} with an abrupt rise of the electric current, meaning smaller carriers' recombination. This behaviour which gives rise to a peak in the current level in the depletion mode has been studied for gated diodes in [16] and has been also detected in this work. The inversion is achieved for V_{BG} > 3.2V, condition where an effective P+/N-/N+ like doping profile is created, instead of P+/P-/N+ [14]. The minority carriers that dictate the recombination in the intrinsic region are now the holes and not the electrons. This behaviour is observed for all devices, but as devices with longer L_I presents larger photosensitive surface area (with fewer fingers), they have higher total electric current when compared to smaller devices (that can be seen when comparing curves of devices with L_I = 10µm and L_I = 1µm). We can also check that higher V_D (anode bias) leads to higher electric currents, since it increases the lateral depletion region of cathode and anode interface junctions, until their maximum thicknesses with V_D of -3V (determined by the technology). The values for the maximum depletion region achieved in the diodes were 2.31µm for T=300K and 2.13µm for T=500K.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JSEN.2017.2647848, IEEE Sensors Journal

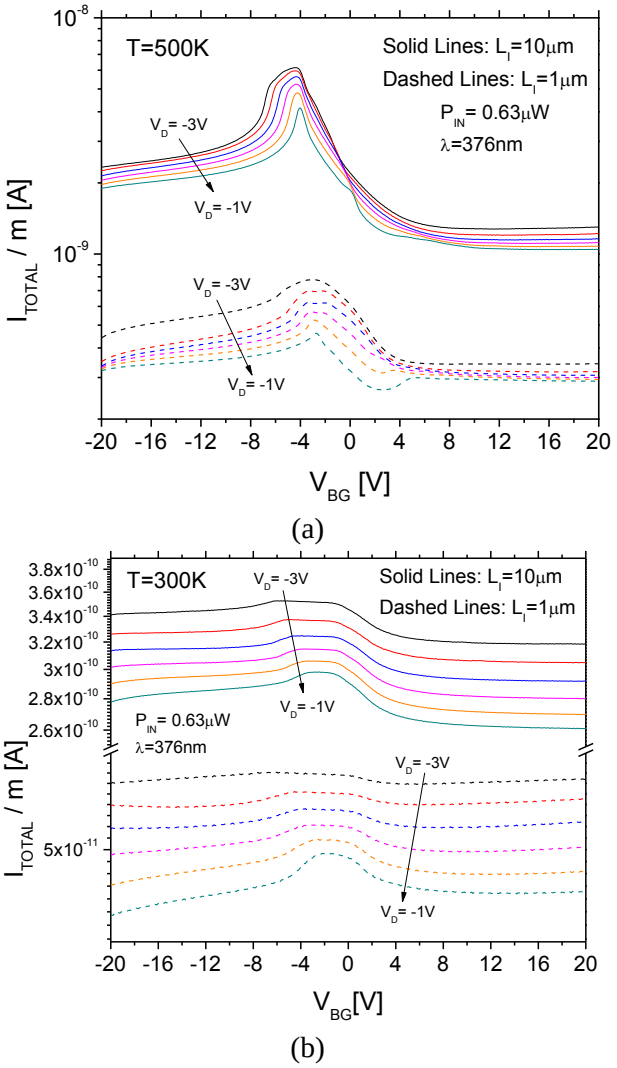


Fig. 2: Measured I_{TOTAL} normalized by the number of fingers with P_{IN}=0.63μW and λ=376nm, as a function of back-gate (V_{BG}) and junction reverse biases for: a) T=500K and b) T=300K

As the device is reversely biased, for T = 500K (Fig. 2a), the generation of carriers, rather than the recombination of excess carriers, will dominate, since $p*n < n_i^2$ (being p and n the total hole and electrons concentration, respectively) [17]. This behavior leads to the fact that the electric current in accumulation will be higher than the inversion one. On the other hand, for T = 300K (Fig 2b), two different behaviors can be seen: one for longer devices (L_I = 10μm), that present the same trend as already explained, and other for shorter devices (L_I = 1μm). These phenomena will be understood through numerical simulation as follows.

In order to make this comparison more quantitative, Fig. 3 shows the ratio of the electrical current in inversion with respect to the accumulation, as a function of L_I. Thus, it is possible to notice that for ratios above 1.0, carriers' recombination will dominate, since the electrical current in inversion will be higher than in accumulation, which happens specially for smaller devices at room temperature, while, for ratios below 1.0, carriers' generation will prevail [18]. As mentioned previously, in some applications the photodiodes are exposed to high temperatures, which affect their performance. For instance, at T = 300K, the photodiode with L_I = 1μm showed an increase in inversion current of 11% for V_D = -0.25V, while the device with L_I = 10μm, showed an increase around 1.5%. But for T = 500K, the increase of electric current in accumulation was 51% and 33% for the same devices respectively, what demonstrates that the temperature plays an important role when comparing the inversion and accumulation ratios [19].

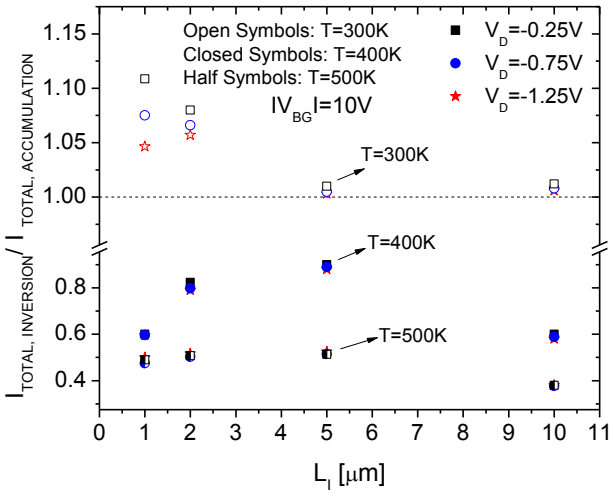


Fig. 3: Ratio of measured I_{TOTAL} between inversion and accumulation as a function of L_I at different temperatures and diode reverse biases

As previously discussed, the design of a PIN photodiode is always a trade-off with regards to the size of the intrinsic length and responsivity. On one hand, a large intrinsic length will enlarge the photosensitive area and increase the photogeneration. On the other hand, a large intrinsic length could increase the generated electrons-holes recombination. As referred in [17], it would be possible to optimize the responsivity of the device by increasing the ratio of the photosensitive area (S) (that is percentage of the area of the device that is effectively photoactive). This is illustrated in Fig. 4-a where is shown the photosensitive area [17] as a function of L_I given by (1):

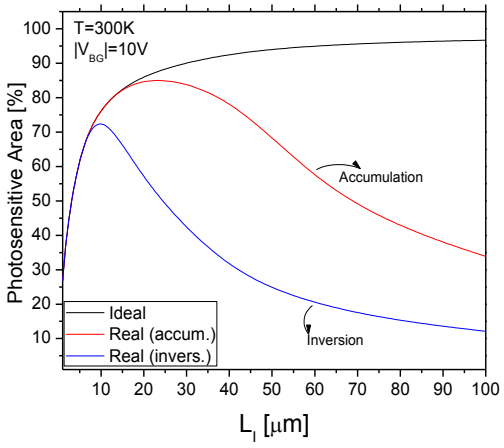
$$S\,(\%) = \frac{m\,.\,\min(L_I, L_{dif})}{m\,.\,(L_N + L_P + L_I) + L_N}\,.100 \quad (1)$$

Where m is the number of fingers, L_N, L_P and L_I are the lengths of cathode, anode and intrinsic regions, respectively, and L_{dif} is the diffusion length. It is important to notice that independent of the intrinsic length and number of fingers, all the diodes have fixed total area of 0.0625mm^2.

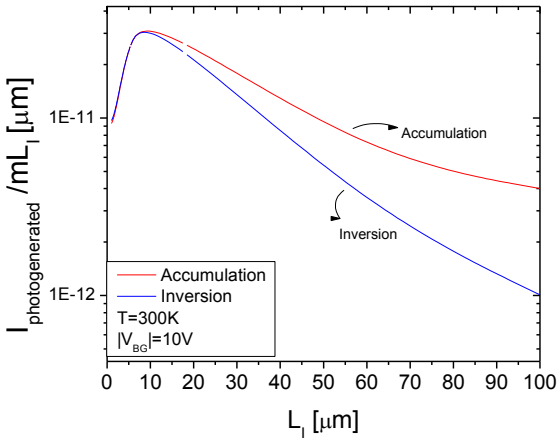
As can be seen in this figure, if the device is ideal, the ratio of the photosensitive area would always increase with the raise in intrinsic length. However, in real cases, there is a maximum value of photosensitive area, from where the current photocurrent generated starts to decay. This happens because the carriers transport in intrinsic area is limited by the lateral

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JSEN.2017.2647848, IEEE Sensors Journal

diffusion length, that, for this technology is $L_{dif\ (ACCUM)}$= 35µm and $L_{dif\ (INVER.)}$= 12.5µm [17]. It means that for the devices where $L_I > L_{dif}$, a saturation effect occurs and the photogenerated current has a strong dependence on the recombination process. This fact can be clearly seen in Fig. 4-b where the maximum measured photogenerated current is present for the devices with L_I=10µm and then starts to decrease differently for the accumulation and inversion modes due to the difference in L_{dif}.



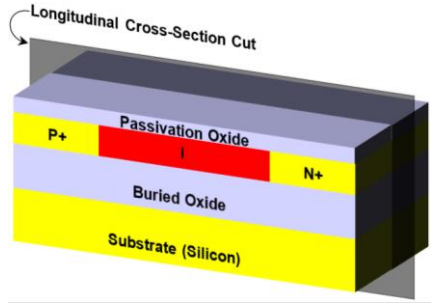
(a)



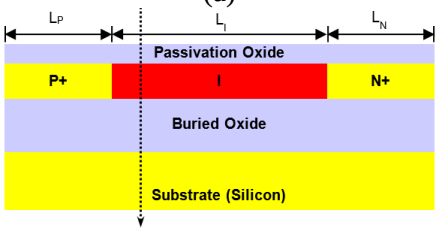
(b)

Fig 4: a) Calculated photosensitive area as a function of intrinsic length for accumulation, inversion and ideal cases. B) Measured photogenerated current normalized by the number of fingers and L_I as a function of intrinsic length. Both for T=300K, V_{BG}=|10|V, V_D= -1V and λ=376nm

Aiming to investigate the physical phenomena related to the observed experimental results, numerical simulations of thin-film SOI PIN photodiodes were performed with TCAD (Atlas numerical simulator, from Silvaco Inc. [21]). All devices were simulated considering the same technological parameters as in the experimental samples. Fig. 5 shows the complete SOI PIN photodiode structure with the longitudinal cross-section cut in Fig. 5 (b). From top to bottom is the passivation oxide layer, the active layer next to the buried oxide (BOX) layer and then the silicon substrate. A MOS capacitor is formed between the active region and the substrate contact.



(a)

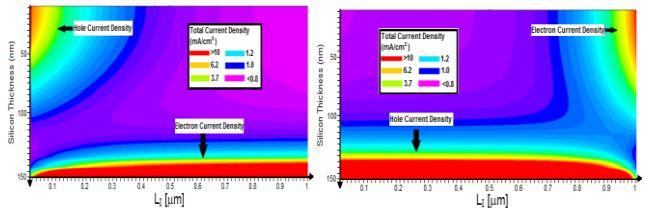


(b)

Fig 5: Complete (a) SOI PIN photodiode structure with the (b) longitudinal cross-section cut.

At this point, it is possible to say that the difference in the electric current level between accumulation and inversion can be attributed to a significant change in the carriers' generation/recombination rate when comparing these two operating modes. Furthermore, the generation/recombination rate is closely related to the composition of the total device electric current (electrons and holes) [22, 23]. In this way, Fig. 6a and Fig. 6b show the total current density without illumination at T = 500K for the device with L_I = 1µm, and the interface with the BOX mainly composed by electrons when V_{BG} = + 10V (Fig 6a) and the interface with the BOX predominantly populated by holes when V_{BG} = -10V (Fig. 6b).

At room temperature, there was a significant increase in the hole current density in inversion regime, as can be seen in Fig. 6c, while the same effect occurs in accumulation mode, where there is a hole current density increase (Fig. 6d). In both cases, it had been found that the electric current density of minority carriers increases, while the current density of majority carriers tends to decrease. This opposite behavior occurs only for shorter devices at room temperature, due to the decreased thermal generation of carriers. Therefore, there is the predominance of the recombination phenomenon, what causes a significant impact on the total device current, depending on the mode of operation [24].



(a) (b)

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JSEN.2017.2647848, IEEE Sensors Journal

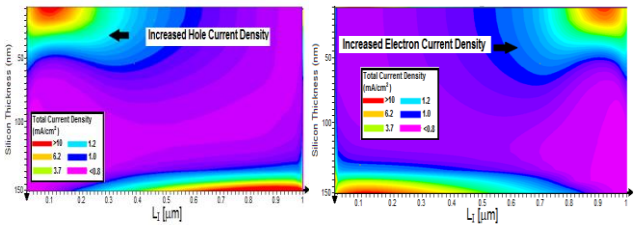


Fig. 6: Simulated Total Current Density for the device with L_I = 1µm for: a) Inversion at T = 500K; b) Accumulation at T = 500K; c) Inversion at T = 300K and d) Accumulation at T = 300K. (V_{BG}=|10|V and V_D= -1V).

III. Back-gate bias effect

It is well known that the dark current of a PIN photodiode is directly proportional to the length of the depletion region [25], due to thermal generation of carriers [26]. These carriers can recombine in the device and then do not contribute to the dark current. On the other side, if the depletion region is very large, the chance for them to recombine reduces a lot, since the depletion region is a spatial charge region where the recombination rate is very low. That is what can be seen in Fig. 7, for V_{BG} between 0V and -6.8V, where there is a maximum vertical depletion region produced by the back-gate bias, depending on the temperature. Besides this, it is possible to see that, as for the illuminated current, the dark current shows three different modes of operation, and as expected, the higher the temperature, the higher the dark current as well. As the temperature increases, the depletion region moves toward higher V_{BG} (right side of the figure). It occurs due to the increase of the intrinsic concentration (n_i), which in turn will reduce the internal potential of the junction V_{BI}, reducing back-gate depletion width, which requires higher V_{BG} for full depletion [27]. Although this figure only shows the dark current for the device with L_I=1µm, the same behavior was observed for the other devices. The anode voltage also influences the dark current, because it produces a lateral depletion region when it is reversely biased, as shown in Fig. 7 for V_D= -1.5V.

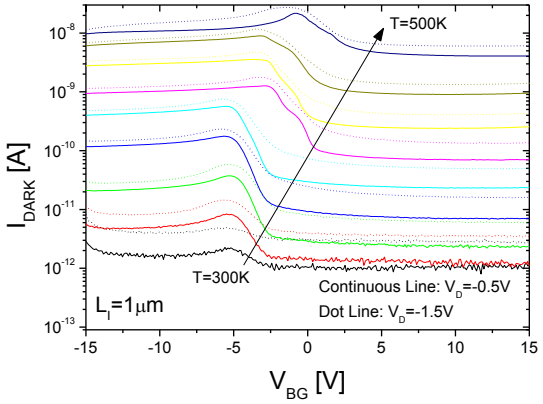


Fig 7: Measured Dark current as a function of back-gate bias for two V_D values at T=300 to T=500K.

To get further insight in the investigation and analysis of the experimental dark current, we performed numerical simulation to evaluate the lateral and vertical depletion layers. Fig. 8 presents the simulated depletion conditions in the I-region at temperature of 300K for the device with L_I = 10µm, where the red lines represent the depletion region obtained from the electric potential distribution as in [28]. It is possible to see the presence of a lateral depletion region produced by V_D of -1.5V and a vertical depletion region produced by V_{BG} of -6.5V.

Fig 8: Simulated Depletion Region Edge with V_D = -1.5V and V_{BG} = -6.5V.

This interdependence of anode and back-gate bias can be more clearly seen in Fig. 9 where the dark current as a function of the anode voltage is presented for the device operating with the active region/BOX interface in accumulation (V_{BG} = -10V) and inversion (V_{BG} = + 10V) regimes. As already mentioned, the dark current of a PIN photodiode is directly proportional to the size of the depletion region [29]. That is the reason why for positive back-gate voltage (for both devices: L_I=1µm and 100µm), the dark current is directly proportional to the reverse voltage V_D, which produces a current raise when V_D is more negative for T=500K. This increase in dark current can achieve 316% for the device with L_I = 1µm, comparing V_D of -0.5 and -1.5V. However, for negative back-gate bias (again for both devices: L_I=1µm and 100µm), this dependence becomes much less evident and the increase in dark current produced by the reverse V_D raise achieves only 58% for the same L_I = 1µm.

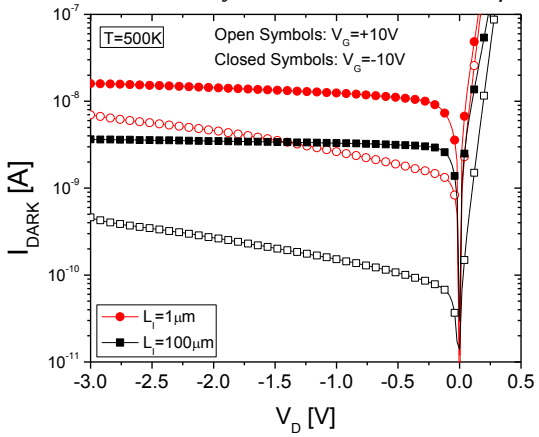


Fig. 9: Measured dark Current as a function of anode bias for V_{BG} of +10V and -10V for two devices with L_I=1µm and L_I=100µm.

In order to explain the fact that the dark current suffers less variation with V_D for negative back-gate voltages, an electrical model was developed based on [30] in which the intrinsic region with its control gate can be approximated to a MOSFET (in our case the control gate is actually the back-gate). This transistor is in series with a junction diode and presents a series resistance that differently affects the dark current, as shown in Fig. 10. It is important to note that the diode is represented in the P+ (anode) side of the intrinsic region or in the N+ (cathode)

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JSEN.2017.2647848, IEEE Sensors Journal

side, depending on the back-gate bias. This occurs because the intrinsic region can behave as P- or N- depending on the the V_{BG} applied, which changes the place where the maximum electric field is presented [31].

With large enough positive V_{BG} voltage (10V) (Fig. 10-A), the intrinsic region operates as a N-type region, therefore the metallurgical junction is located between P+ (anode) and the intrinsic region. That is why the transistor is a NMOS type. If we consider that most of the reverse voltage V_D will drop across the diode, we can say that the source of the transistor (lower potential) will have zero voltage. Thus, the V_{GS} bias depend only on the substrate voltage. Therefore, in the case of a positive V_{BG}, we have: $V_{GS} = V_{BG}$ (since the voltage at the source is zero), and the series resistance does not depend on V_D. In this way, the dark current will be only affected by the size variation of the depletion region produced by V_D and not for the series resistance. This result will make the dark current dependent on V_D bias in a way that will increase to more reverse V_D.

On the other hand, for negative gate bias (Fig. 10-B), the intrinsic region will be in accumulation mode and the metallurgical junction will be located between the N + region and the intrinsic region, moreover, the transistor is PMOS. Again, we consider that the reverse voltage will drop across the diode, and that in the source terminal of the transistor will be the V_D bias. Therefore, the V_{GS} bias depend both on V_G and V_D since $V_{GS} = V_{BG}$-V_D. Thus, V_D bias will have an effect on the carrier concentration in the intrinsic region that influences the series resistance of this region. The higher the reverse voltage V_D, the higher the carrier concentration, which decreases the carrier's mobility [32].

That is why there is a concurrent effect on the V_D voltage: firstly, the increase of the reverse voltage V_D should cause an increase in dark current in the way that there will be an enlargement of the depletion region, while on the other hand, the effect of increasing the series resistance caused by the increase of the reverse voltage will cause a reduction in dark current. Thus, as there are two competing effects on the increase in reverse voltage V_D, its effect on dark current level will be diminished.

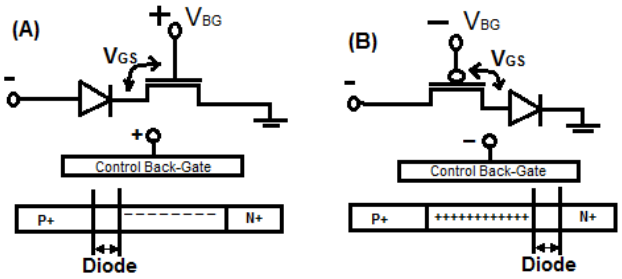


Fig. 10: Electrical Equivalent Model for: A) Positive gate bias and B) Negative Gate Bias

IV. Intrinsic Length Effect

The dark current can also be affected by the size of the intrinsic region of the photodiodes (L_I), since I_{DARK} is proportional to the junction area and the size of the depletion region [33]. It is possible to see this effect by observing Fig. 11, which shows the dark current as a function of the intrinsic length for accumulation and inversion at different temperatures. The PIN diode have fixed total area with different number of fingers. This fact is possible by changing the intrinsic lengths as already shown in Table I. Thus, when the film is in accumulation, the dark current will decrease with increased intrinsic region, since there will be a decrease in the number of fingers. On the other hand, when the film is in inversion, the dark current increases with the increase of L_I, since there is a difference in the diffusion length concerning the mode of operation, as already mentioned. In addition, thermal generation is more pronounced in the depletion layer, where there is a smaller carrier recombination owing to the presence of fixed charges [11]. The same behavior was observed for other temperatures.

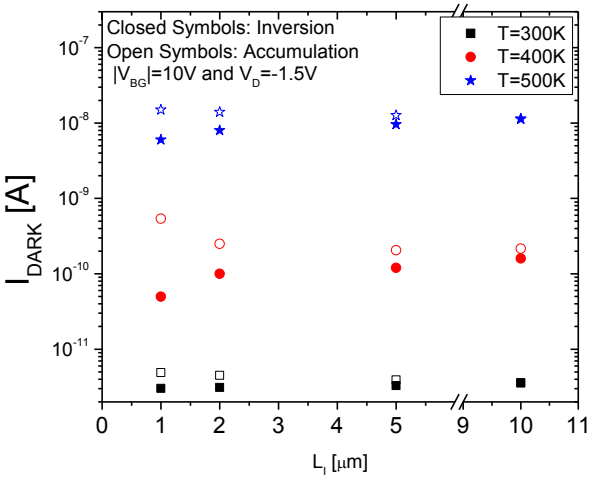


Fig 11: Measured dark current as a function of L_I for three temperatures in accumulation and inversion.

V. Total Quantum Efficiency

Considering that the three mentioned parameters: back-gate bias, temperature and number of fingers affect the performance of the PIN diodes, there will be a significant change with respect to the total quantum efficiency of the device, since it is linked to the amount of generated photocurrent and the dark current.

In order to investigate the consequence of the photodiode efficiency under different operating modes, Fig. 12 shows the measured total quantum efficiency (QE_T) as a function of L_I for three different temperatures in inversion and accumulation modes of operation.

The QE_T is defined as the ratio between the photogenerated current (that is the total diode current minus the dark current) and the maximum current that would be generated if there was no kind of loss, like the recombination of photogenerated carriers before reaching the anode and cathode terminals, the non-photosensitive area (metal covered and interconnections) and reflection [2]. The QE_T was calculated based on the responsivity [14] as demonstrated in (2).

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JSEN.2017.2647848, IEEE Sensors Journal

$$QE_T = \frac{h\,c\,R}{\lambda\,q} \quad (2)$$

Where R is the responsivity defined as the relationship between the photocurrent and the incident optical power, h is the Planck constant, c is the light velocity in the vacuum and q, the elementary charge of electron.

As it can be seen in figure 12, the total quantum efficiency is higher for T = 500K, followed by T = 400K and then T = 300K. This is due to the increase of generated photocurrent at higher temperatures apart from V_{BG} bias. This behavior suggests that there is an increase in the amount of absorbed incident optical power that could be related either to a reduction of the absorption length, or to a kind of avalanche or charge multiplication effect related to the increase of carrier`s thermal energy at high temperatures as explained in [10].

In accumulation mode, the quantum efficiency increases, as the intrinsic length is higher due to the decrease of the dark current. On the other hand, in inversion mode, the opposite effect is observed, because as L_I increases, I_{DARK} raises its value, lowering QE_T. The maximum value of the QE_T of 52.4% was achieved for L_I = 1um at T = 500K in inversion mode, while in accumulation, the largest value was 48.2% at T = 500K for the device with L_I = 10µm. In the depletion case, although not showed by Fig. 12, QE_T is higher than accumulation and inversion due to the increased photocurrent.

Another valid observation is that for the entire range of temperatures, the inversion mode showed to have higher quantum efficiency, due to the fact that it presented larger photocurrent than in accumulation, which means that it had lower recombination rate.

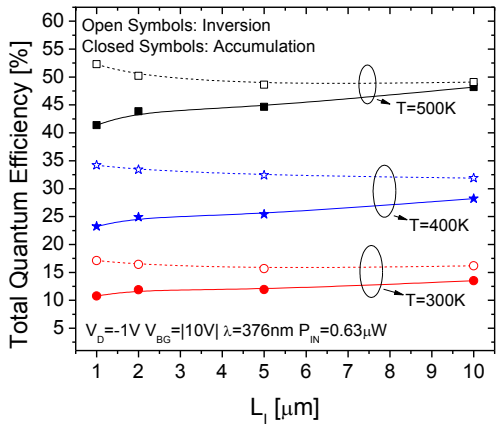


Fig. 12: Total Quantum Efficiency as a function of L_I for T=300K, 400K and 500K in inversion and accumulation modes of operation

In order to make this issue clearer and quantitative, Table III brings the comparative values of dark current and quantum efficiency for P_{IN} of 0.63µW. The difference in QE_T between inversion and accumulation shows a strong relationship compared to the dark current ratio. It can be seen that the difference in QE_T for T=400K is the highest one and can achieve 10.97 for L_I=1µm. This is specially related to the lower ratio in dark current that is 0.15 when comparing inversion to accumulation. This decrease of dark current ratio in T=400K can be explained by the mobility degradation caused by the temperature increase [26]. On the other hand, by raising the temperature beyond 400K, the effect of lifetime dependence with temperature and the high level of generated carriers overlap this effect and current ratio raises.

Table III. Ratios of ($QE_{T\ +15V}$/ $QE_{T\ -15V}$) and ($I_{DARK\ +15V}$/$I_{DARK\ -15V}$) for V_D= -1.5V, λ=376nm and P_{IN}=0.63µW.

L_I	$QE_{T\ +10V}$/ $QE_{T\ -10V}$			$I_{DARK\ +10V}$/$I_{DARK\ -10V}$		
µm	300K	400K	500K	300K	400K	500K
1	6.34	10.97	10.93	0.62	0.15	0.41
2	4.56	8.50	6.35	0.69	0.42	0.58
5	3.75	7.01	3.96	0.77	0.61	0.76
10	2.67	3.68	0.88	0.91	0.75	0.99

VI. Conclusions

In this work, the influence of back-gate bias on the performance of lateral SOI PIN photodiodes at high temperatures was presented. Experimental results demonstrated that the operation mode of the photodiodes is affected by back-gate bias, modifying the dark currents, which presents its maximum value when the silicon film is laterally depleted, indicating minimal carrier`s recombination. It was also shown that the dark current tendency is changed by the mode of operation when comparing devices with different number of fingers. In accumulation, the dark current decreases with increased intrinsic region, while, in inversion, there is a dark current raise with the increase of L_I. These results lead to an improvement in total quantum efficiency of the device for L_I=1µm in inversion reaching 52.4% at T=500K. On the hand, in accumulation, the largest efficiency was achieved for the device with L_I=10µm with 48.2% under UV radiation.

References

[1] Grundfest W 1999 Overview of medical applications and cardiovascular intervention *Proc. Quantum Electron* (Laser Sci. Conf. 1999) pp 23–28

[2] Zhengyuan X *et al*. 2007 Experimental performance evaluation of non-line-of-sight ultraviolet communication systems *Proc. of SPIE* vol. 6709 (San Francisco, CA) pp 1-12

[3] Karczemska A and Sokolowska A 2001 Materials for DNA sequencing chip *Proc. Int. Conf. Novel Appl. Wide Bandgap Layer* (Zakopane) vol 3 (Poland) p 176

[4] Bulteel O and Flandre D 2009 Optimization of blue/UV sensors using p-i-n photodiodes in thin-film SOI technology *ECS Transactions* **19** (4) 175-180

[5] Smith W A and Lam K P 2010 Exploratory analysis of UVvis absorption spectra *Proc. Int. Congr. Image Signal Process* pp 3359–3363

[6] Knight G 2004 Monitoring of ultraviolet light sources

for water disinfection *Proc. IEEE Ind. Applicat. Conf* vol 39 IAS Annu. Meet. pp 1016–1018

[7] Malinowski P E *et al.* 2010 10 μm pixel-to-pixel pitch hybrid backside illuminated AlGaNon- Si imagers for solar blind EUV radiation detection *Proc. IEEE Int. Electron Dev. Meet.* (San Francisco, CA) pp 348–351

[8] International Technology Roadmap for Semiconductors: Lithography [Online]. Available: http://www.itrs.net

[9] Shi L and Nihtianov S 2012 Comparative study of silicon-based ultraviolet photodetectors *IEEE Sensors Journal* **12** (7) 2453-2459

[10] Afzalian A and Flandre D 2005 Physical modelling and design of thin-film SOI lateral p-i-n photodiodes *IEEE Trans. On Electron Device* **52** (6) 1116-1122

[11] Ohta J 2007 *Smart CMOS Image Sensors and Applications* vol 2, ed Taylor & Francis (New York) pp 11-53

[12] Streetman B G and Banerjee S 2000 *Solid state electronic device* (New York: Prentice Hall) pp 384-385

[13] Monroy E, Omnès F, and Calle F 2003 Wide-bandgap semiconductor ultraviolet photodetectors *Semiconductor Science and Technology* **18** (4) R33–R51

[14] Afzalian A and Flandre D 2007 Characterization of quantum efficiency, effective lifetime and mobility in thin film ungated SOI lateral PIN Photodiodes *Solid-State Electronics* **51** (2) 337-342

[15] Lee C, Lederer D, Afzalian A, Yan R, Dehdashti N, Xiong W and Colinge J 2008 Comparison of contact resistance between accumulation-mode and inversion-mode multigate FETs *Solid-State Electronics* **52** (11) 1815-1820

[16] Rudenko T, Rudenko A, Kilchytska V, Cristoloveanu S, Ernst T, Colinge J P, Dessard V and Flandre D 2004 Determination of film and surface recombination in thin-film SOI devices using gated-diode technique *Solid State Electronics* **48 (**3) 389-399

[17] Colinge J P and Colinge C A *Physics of semiconductor devices* (New York: Kluwer Academic) pp 73-89

[18] Galeti M, Martino J A, Simoen E and Claeys C 2008 Improved generation lifetime model for the electrical characterization of single and double-gate SOI nMOSFETs *Semiconductor Science and Technology* **23** (12) 125011

[19] Souza M, Bulteel O, Flandre D and Pavanello M 2010 Analysis of lateral SOI PIN diodes for the detection of blue and UV wavelengths in a wide temperature range *ECS Transactions* **31 (**1) 199-206

[20] Bulteel O, Afzalian A and Flandre D 2010 Fully Integrated blue/UV SOI CMOS photosensor for biomedical and environmental applications *Analog Integrated Circuits and Signal Processing* **65** (3) 399-405

[21] ATLAS User's Manual 2010, SILVACO

[22] Li G, Zeng Y, Hu W and Xia Y 2014 Analysis and simulation for current-voltage models of thin-film gated SOI lateral PIN photodetectors *Optik Optics* **125** 540-544

[23] Novo C, Giacomini R, Doria R, Afzalian A and Flandre 2014 Illuminated to dark ratio improvement in lateral SOI PIN photodiodes at high temperatures *Semiconductor Science and Technology* **29** (7) 01–09

[24] Novo C, Giacomini R, Doria R, Afzalian A and Flandre D 2013 Back-gate bias influence on the operation of lateral SOI PIN photodiodes at high temperatures *Proc. of 9th. Workshop of Thematic on SOI Technology, Devices and Circuits,* EuroSOI (Paris)

[25] Li G, André N, Poncelet O, Gérard P, Zeeshan S, Udrea F, Francis L, Zeng Y, and Flandre D 2016 Silicon-on-Insulator Photodiode on Micro-Hotplate Platform With Improved Responsivity and High-Temperature Application *IEEE Sensors Journal* **16** (9) 3017-3024

[26] Souza M, Bulteel O, Flandre D and Pavanello M 2011 Temperature and silicon film thickness influence on the operation of lateral SOI PIN photodiodes for detection of short wavelengths *JICS* **6** (2) 107-113

[27] Novo C, Giacomini R, Afzalian A and Flandre D 2013 Operation of lateral SOI PIN photodiodes with back-gate bias and intrinsic length variation *Proc. of 223rd Electrochemical Society Meeting* (Toronto) vol 53 pp 121-126

[28] Alirezaei I and Burte E 2016 Modeling and simulation of a 3D- CMOS silicon photodetector for low-intensity light detection *Proc. of SPIE* volume 9742 pp 1-10

[29] Zimmermann H, Muller B, Hammer A, Herzog K and Seegebrecht P 2002 Large-area lateral p-i-n photodiode on SOI *IEEE Trans. On Electron Devices* **49** (2) 334-336

[30] Stewart M and Miltiadis H 2000 High Performance Gated Lateral Polysilicon PIN diodes *Solid-State Electronics* **44** (2000) 1613-1619

[31] Schmidt A, Dreiner S, Vogt H, Paschen U 2015 Thin Film SOI PIN Diode Leakage Current Dependence on Back-Gate Potential and HCl Traps *Proc. of ESSDERC* 290-293

[32] Abid Kamran, Khokhar A and Rahman F 2011 High responsivity silicon MOS phototransistors *Sensors and Actuators A: Physical* **172** 434-439

[32] Augendre E *et al.* 2005 On the scalability of source/drain current enhancement in thin film SOI *Proc. of ESSDERC* pp 301-304