A nA-Range Area-Efficient Sub-100-ppm/°C Peaking Current Reference Using Forward Body Biasing in 0.11-μm Bulk and 22-nm FD-SOI

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***Abstract*—In recent years, the development of the Internet of Things (IoT) has prompted the search for nA-range current references that are simultaneously constrained to a small area and robust to process, voltage and temperature variations. Yet, such references have remained elusive, as existing architectures fail to reach a low temperature coefficient (TC) while minimizing silicon area. In this work, we propose a nA-range constant-with-temperature (CWT) peaking current reference, in which a resistor is biased by the threshold voltage difference between two transistors in weak inversion. This bias voltage is lower than in conventional architectures to cut down the silicon area occupied by the resistor, and is obtained by forward body biasing one of the two transistors with an ultra-low-power voltage reference so as to reduce its threshold voltage. In addition, the proposed reference includes a circuit to suppress the leakage of parasitic diodes at high temperature, and two simple trimming mechanisms for the reference current and its TC. As the proposed design relies on the body effect, it has been validated in both 0.11-μm bulk and 22-nm fully-depleted silicon-on-insulator, to demonstrate feasibility across different technology types. In post-layout simulation, the 0.11-μm design generates a 5-nA current with a 65-ppm/°C TC and a 2.84-%/V line sensitivity (LS), while in measurement, the 22-nm design achieves a 1.5-nA current with an 89-ppm/°C TC and a 0.51-%/V LS. As a result of the low resistor bias voltage, the proposed references occupy a silicon area of 0.00954 mm^2 in 0.11 μm (resp. 0.00214 mm^2 in 22 nm) at least 1.8× (resp. 8.2×) smaller than fabricated nA-range CWT references, but with a TC improved by 6.1× (resp. 4.4×).**

***Index Terms*—Peaking current reference, temperature coefficient (TC), temperature-independent, constant-with-temperature (CWT), forward body biasing (FBB).**

I. Introduction

THE last decade has seen the development of numerous ultra-low-power (ULP) sensor nodes embedding intelligence at the edge, fostered by the growth of Internet-of-Things (IoT) applications. As is the case for most integrated circuits, the analog blocks constituting these sensor nodes need to be biased by a current, commonly generated by on-chip current references. Nonetheless, designing such sensor nodes poses three main challenges listed in Fig. 1(a), which result in specific requirements for the current references they embed. First, the power consumption of these sensor nodes is greatly constrained by the fact that they operate from limited-capacity batteries or energy harvesting. The typical average power consumption is thus comprised between 0.1 and 100 μW [1], albeit this value largely varies from one application to another. A reference current in the nA range is thus desirable to bias always-on circuit blocks operating in sleep mode, and to ensure an ultra-low power consumption while providing sufficient performance in active mode. Then, silicon area must be minimized to limit the production cost and the associated direct environmental footprint, typically comprised between 1 and 4 kgCO_2-eq/cm^2 [2], [3], given the large production volumes projected for the IoT [4]. Therefore, the area occupied by current references should also be limited to leave more space for circuits providing useful functionalities, especially in the case of IoT nodes using small silicon dies. Finally, sensor nodes must be able to cope with a wide range of operating conditions due to the diversity of possible deployment scenarios. Hence, current references need to be robust to process, voltage and temperature (PVT) variations, to avoid degrading the performance of analog blocks such as real-time

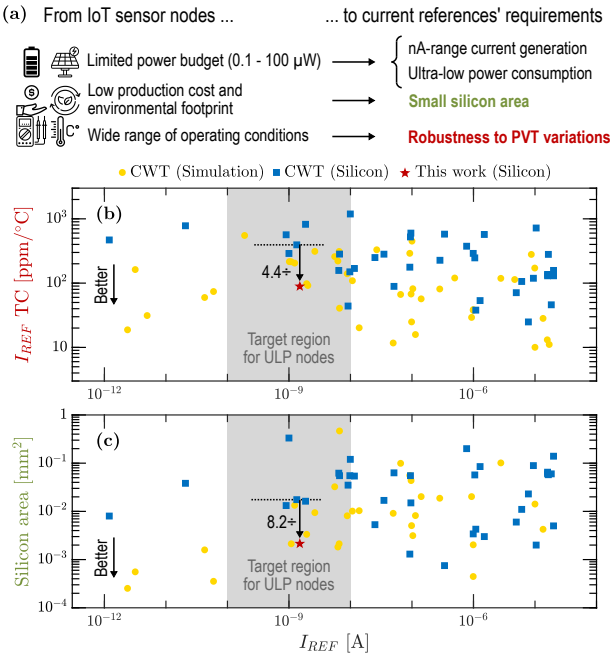

Fig. 1. (a) Requirements of current references in the context of the IoT, and landscape of existing CWT current references in terms of (b) temperature coefficient (TC) and (c) silicon area, highlighting the absence of both temperature-independent and area-efficient architectures in the nA range.

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clock generators [5], [6] and temperature sensors [7], [8].

As already observed in [9], the landscape of existing current references [Figs. 1(b) and (c)] reveals the absence of fabricated references that are simultaneously robust to temperature variations and area-efficient in the nA range, while such references are ideally suited to the needs of IoT sensor nodes [1]. A common way to generate a current from a voltage is to use a voltage-to-current (V-to-I) converter. First, resistor-based references [10], [11], [12] rely on a resistor biased by the threshold voltage (V_T) difference between two transistors of different V_T types. Hence, they offer a good TC thanks to the relatively linear temperature characteristics of the resistance, at the cost of a large area necessary to reach the nA range, as it is constituted of several segments in series. Second, references based on gate-leakage transistors [13] offer a similar trade-off, except that the large area originates from the necessity to connect numerous gate-leakage devices in parallel. Finally, references based on a self-cascode MOSFET (SCM) [14], [9] present a significantly reduced area compared to the two previous categories, but generally feature a poorer TC because of the nonlinear I-V characteristics of the SCM, and the difficulty to bias it with a voltage leading to a constant-with-temperature (CWT) current.

This work proposes a nA-range CWT peaking current reference (PCR), in which the threshold voltage difference between two subthreshold transistors of the same V_T type, denoted as ΔV_T, biases a resistor. This ΔV_T results from the forward body biasing (FBB) of one of the transistors by a two-transistor (2T) ULP voltage reference, leading to a reduced bias voltage and thus, to a reduced resistance and area. The proposed design includes a leakage suppression circuit to mitigate the impact of parasitic diodes at high temperature, as well as trimming mechanisms for the reference current and its TC to maintain performance across process corners. As the proposed reference relies on the body effect, it has been validated with post-layout simulations in 0.11-μm bulk and 22-nm fully-depleted silicon-on-insulator (FD-SOI) technologies to demonstrate feasibility in these two technology types. In addition, the proposed reference has been fabricated in 22-nm FD-SOI, yielding a 1.5-nA current with an 89-ppm/°C TC and a 0.51-%/V line sensitivity (LS), while consuming 2.87 nW at 0.75 V and occupying a record silicon area of 0.00214 mm^2. This paper is organized as follows. First, Section II presents the operation principle of the proposed reference and discusses its sizing. Section III details architectural optimizations, while Sections IV and V respectively present simulation and measurement results. Finally, Section VI compares this work to the state of the art, while Section VII offers perspectives for future works.

II. Operation Principle and Sizing

The main objective of this section is to respectively remind the operation principle of the conventional proportional-to-absolute-temperature (PTAT) PCR, and explain the one of the proposed CWT PCR, based on their governing equations in Sections II-A and II-B. Then, Section II-C discusses the design and sizing methodology of the proposed CWT PCR in 0.11-μm bulk and 22-nm FD-SOI technologies.

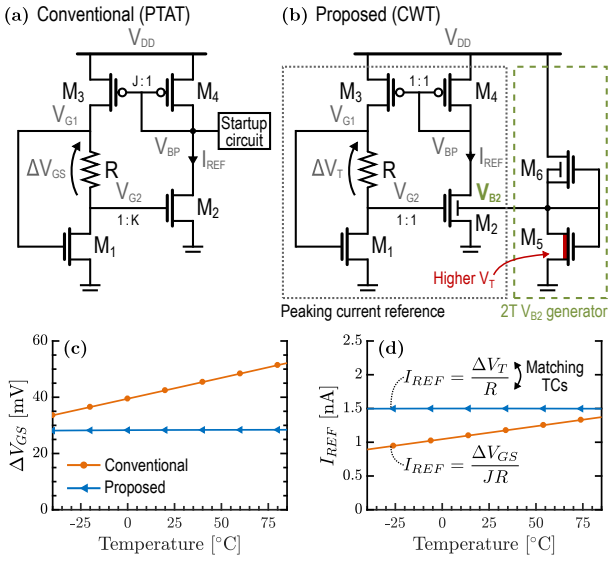

Fig. 2. Schematic of (a) the conventional PTAT peaking current reference and (b) the simplified proposed CWT one, which relies on the threshold voltage difference ΔV_T between M_{1-2}, obtained by forward body biasing M_2 with a 2T voltage reference (M_{5-6}). Operation principle illustrated with pre-layout simulations of (c) ΔV_{GS} and (d) I_{REF} in 22-nm FD-SOI, for the conventional design with $J = K = 2$, and the proposed one.

Before getting into the heart of the governing equations, we need to remind two important concepts. First, the drain-to-source current in subthreshold is given by

$$I_{DS} = I_{SQ} S \exp\left(\frac{V_{GS} - V_T}{nU_T}\right), \tag{1}$$

for $V_{DS} > 4U_T$, with $I_{SQ} = \mu C'_{ox}(n-1)U_T^2$ the specific sheet current, μ the carrier mobility, C'_{ox} the gate oxide capacitance per unit area, n the subthreshold slope factor, U_T the thermal voltage, $S = W/L$ the transistor's aspect ratio, and V_T the threshold voltage at any V_{BS}, as opposed to V_{T0}, which refers to the threshold voltage at zero V_{BS}. Consequently, the gate-to-source voltage is described by

$$V_{GS} = V_T + nU_T \ln\left(\frac{I_{DS}}{I_{SQ} S}\right). \tag{2}$$

The second important concept to be introduced is the the body effect, which is captured by

$$\begin{aligned}\Delta V_T = V_T - V_{T0} &= \gamma_b\left(\sqrt{2\phi_{fp} - V_{BS}} - \sqrt{2\phi_{fp}}\right) \\ &\approx -\gamma_b^* V_{BS}\end{aligned} \tag{3}$$

in a bulk technology, where ϕ_{fp} denotes Fermi's potential, γ_b the body factor, γ_b^* its linearization around V_{BS} = 0, and by

$$\Delta V_T = V_T - V_{T0} = -\gamma_b^* V_{BS} \tag{4}$$

in an FD-SOI technology. γ_b^* is temperature-dependent in bulk, and CWT at first order in FD-SOI [15].

A. Conventional PTAT Peaking Current Reference

In the conventional PTAT architecture [Fig. 2(a)], we consider that M_{1-2} have the same technological parameters and do not use any kind of body biasing, i.e., $V_{T01} = V_{T02} = V_T$ and $n_1 = n_2 = n$, excluding mismatch. In addition, the current mirror ratios J and/or K need to be larger than one, to have a positive voltage drop across resistor R. This results in

$$\Delta V_{GS} = V_{GS1} - V_{GS2} = nU_T \ln(JK) \tag{5}$$

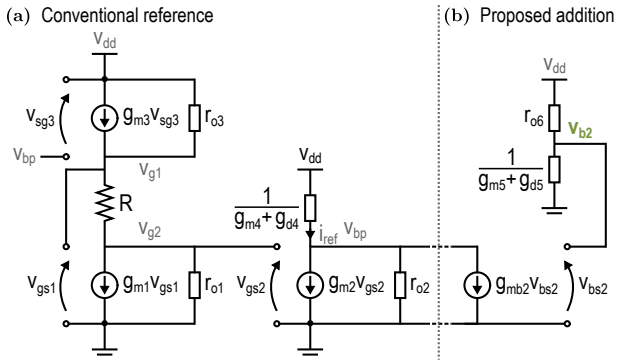

Fig. 3. Small-signal schematic of (a) the conventional PTAT PCR and (b) the proposed FBB addition to obtain a CWT reference current.

using (2), and

$$I_{REF} = \frac{\Delta V_{GS}}{JR} = \frac{nU_T \ln(JK)}{JR}. \quad (6)$$

The TC of I_{REF} at a given temperature can be computed as

$$\text{TC} = \frac{1}{I_{REF}}\frac{dI_{REF}}{dT} = -\frac{1}{R}\frac{dR}{dT} + \frac{1}{T}. \quad (7)$$

Eq. (7) shows that the TC of I_{REF} cannot be equal to zero unless the temperature coefficient of resistance (TCR) is equal to $1/T$. But in practice, the TCR is always smaller than $1/T$ and the TC of I_{REF} is thus positive. In Figs. 2(c) and (d), we observe that the PTAT behavior of ΔV_{GS} results in a PTAT behavior of I_{REF}, which is consistent with the positive TC.

Another quantity of interest is the LS of I_{REF}, which can be computed from a small-signal analysis of the PCR. Based on the small-signal schematic in Fig. 3(a), we find that

$$v_{bp} = \frac{(g_{m4}+g_{d4})v_{dd} - g_{m2}v_{g2}}{g_{m4}+g_{d4}+g_{d2}} \approx v_{dd} - \left(\frac{g_{m2}}{g_{m4}}\right)v_{g2} \quad (8)$$

with the simplification $g_m \gg g_d$, and we can thus compute the LS of I_{REF} as

$$\frac{i_{ref}}{v_{dd}} = \frac{1}{J}\frac{g_{d3}}{g_{m1}}\left(\frac{1}{R} - g_{m1}\right) + g_{d2} \approx g_{d2}, \quad (9)$$

to be evaluated around the operation point of the current reference. Interestingly, the LS is predominantly related to the output conductance of M_2.

B. Proposed CWT Peaking Current Reference

In the proposed CWT PCR [Fig. 2(b)], M_1 has its body connected to its source and is therefore not impacted by the body effect, hence $V_{T1} = V_{T01}$, while M_2 is biased with $V_{BS2} > 0$ and undergoes a forward body biasing lowering its threshold voltage, i.e., $V_{T2} < V_{T1}$. In addition, unitary current mirror ratios $J = K = 1$ are used. In this architecture, the body voltage of M_2 is generated by the 2T voltage reference formed by M_{5-6}, in which the equilibrium of subthreshold currents $I_{DS5} = I_{DS6}$, given by (1), leads to

$$V_{B2} = \left(V_{T05} - \frac{n_5}{n_6}V_{T06}\right) + n_5 U_T \ln\left(\frac{I_{SQ6}S_6}{I_{SQ5}S_5}\right). \quad (10)$$

The voltage drop across resistor R is therefore equal to the difference of threshold voltages between M_1 and M_2 expressed by (3) or (4), i.e.,

$$\Delta V_{GS} = \Delta V_T = V_{T01} - V_{T2} \approx \gamma_b^* V_{B2}, \quad (11)$$

TABLE I
RESISTOR PROPERTIES IN 0.11-μM BULK AND 22-NM FD-SOI TECHNOLOGIES. THE DENSITY IS MEASURED AT 25°C AND THE TCR IS CHARACTERIZED FROM -40 TO 85°C, AND BOTH CHARACTERISTICS ARE NORMALIZED TO THE LOWEST OBTAINED VALUE. ALL THE RESISTORS HAVE A WIDTH AND LENGTH OF 0.5 μM AND 1 μM IN 0.11 μM, AND 0.36 μM AND 0.4 μM IN 22 NM.

Techno.	Properties	N+			P+		
		diff.	poly.	poly. (high res.)	diff.	poly.	poly. (high res.)
0.11 μm	Normalized density	**1**	1.28	-	1.06	2.88	**4.12**
	Normalized TCR	**14.98***	1.69*	-	7.87*	**1***	5.34†
22 nm	Normalized density	1.13	2.51	3.98/**4.07**	**1**	-	-
	Normalized TCR	5.55*	**1***	1.36†/1.12†	**5.72***	-	-

* Positive TCR. † Negative TCR.

and results in a reference current

$$I_{REF} = \frac{\Delta V_T}{R} = \frac{\gamma_b^* V_{B2}}{R}. \quad (12)$$

The TC of I_{REF} at a given temperature can be computed as

$$\text{TC} = \frac{1}{I_{REF}}\frac{dI_{REF}}{dT} = -\frac{1}{R}\frac{dR}{dT} + \frac{1}{\gamma_b^*}\frac{d\gamma_b^*}{dT} + \frac{1}{V_{B2}}\frac{dV_{B2}}{dT}. \quad (13)$$

Contrary to (7), in which there is no tuning knob to set the TC of I_{REF}, the proposed architecture allows to zero out the TC by properly selecting the TC of V_{B2}, which will compensate for the temperature dependence of R and γ_b^*. V_{B2} TC can indeed be tuned by changing the ratio of aspect ratios S_6/S_5 in (10). This will be the basis for the TC trimming circuit later discussed in Section III-B, which allows to mitigate the impact of V_{B2} process variations on I_{REF} TC. In Figs. 2(c) and (d), we notice that a close-to-CWT ΔV_{GS} gives a CWT I_{REF}, by matching the TC of ΔV_{GS} with the TCR. Hence, the operation principle of the proposed reference is to bias the resistor with the ΔV_T between two subthreshold transistors of the same V_T type, one of them being forward body biased to create a V_T imbalance. Interestingly, no startup circuit is required as the proposed reference is unstable at zero I_{REF}. The 2T voltage reference indeed generates a positive voltage V_{B2} even if the rest of the reference is stuck at zero. This leads to a non-zero I_{DS2} which starts the reference. Other CWT PCRs employing slightly different ideas exist in the literature, such as [16], [17], biasing the resistor with the ΔV_T between transistors of the same V_T type but different lengths, and [18], making use of an additional degeneration resistor to achieve temperature compensation. Yet, these works are either limited to simulations and/or generate a larger I_{REF}.

Similarly to the conventional PCR, the LS can be obtained from a small-signal analysis. Based on the small-signal schematic in Figs. 3(a) and (b), we first find

$$v_{b2} = \frac{g_{d6}}{g_{m5}+g_{d5}+g_{d6}}v_{dd} \approx \left(\frac{g_{d6}}{g_{m5}}\right)v_{dd}, \quad (14)$$

and consequently,

$$\frac{i_{ref}}{v_{dd}} = \frac{g_{d3}}{g_{m1}}\left(\frac{1}{R} - g_{m1}\right) + g_{d2} + g_{mb2}\left(\frac{g_{d6}}{g_{m5}}\right), \quad (15)$$

$$\approx g_{d2} + g_{mb2}\left(\frac{g_{d6}}{g_{m5}}\right). \quad (16)$$

The 2T bias generator thus affects the LS of I_{REF} through the second term of (16).

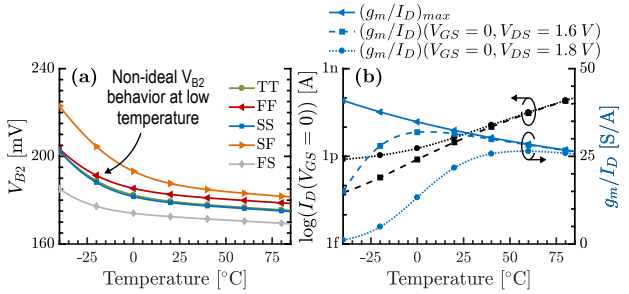

Fig. 4. **The 2T voltage reference presents a nonideal behavior at low temperature, due to gate leakage, or to GIDL at high V_{DS}.** All figures correspond to 22-nm FD-SOI. Temperature dependence of (a) V_{B2} in all process corners for a 2T voltage reference supplied at 1.8 V and implemented with 1-μm-long I/O nMOS, and (b) $\log(I_D)$ and (g_m/I_D) at V_{GS} = 0, and $(g_m/I_D)_{\text{max}}$, for two different V_{DS} and for an I/O SLVT nMOS with W = 3.89 μm and L = 1 μm in the SS process corner.

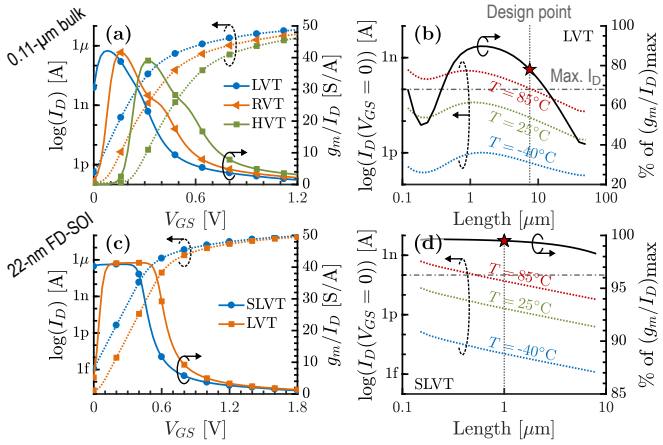

Fig. 5. All figures correspond to the SS process corner with a fixed $V_{DS} = V_{GS,\text{max}}/2$. $\log(I_D)$, g_m/I_D vs. V_{GS} curves at -40°C (a) in 0.11 μm for core LVT, RVT and HVT nMOS with W = 0.5 μm and L = 10.45 μm, and (c) in 22 nm for I/O SLVT and LVT nMOS with W = 2 μm and L = 8 μm. $\log(I_D)$ at V_{GS} = 0 and -40, 25 and 85°C, and g_m/I_D at V_{GS} = 0 and -40°C as a percentage of $(g_m/I_D)_{\text{max}}$ (b) in 0.11 μm for a core LVT nMOS with W = 0.5 μm and L ranging from 0.12 to 50 μm, and (d) in 22 nm for an I/O SLVT nMOS with W = 2 μm and L ranging from 0.15 to 8 μm.

C. Design and Sizing Methodology

In what follows, the LS and TC are computed using the conventional box method, as is done in [9]. The design and sizing methodology of the proposed CWT PCR can be brought down to three main steps:

1) The selection of the resistor, based on its density in $\Omega/\square$ and its TCR in ppm/°C.
2) The sizing of the 2T body bias generator, which consists in selecting the transistor type and dimensions for M_{5-6}.
3) The sizing of all remaining transistors M_{1-4}, focusing on maintaining these transistors saturated in all PVT corners, and keeping mismatch-induced variability under an acceptable threshold.

First, step 1) relies on Table I to select an appropriate resistor type. We notice that diffusion resistors are typically a poor choice for nA-range CWT current references, as they present both a low density and a large TCR. High-resistivity (high-res.) polysilicon (poly) resistors are a better fit as they usually have a large density and a low TCR. In 22-nm FD-SOI, the high-res. poly resistor can even have its width narrowed down to 150 and 40 nm, thereby effectively increasing its

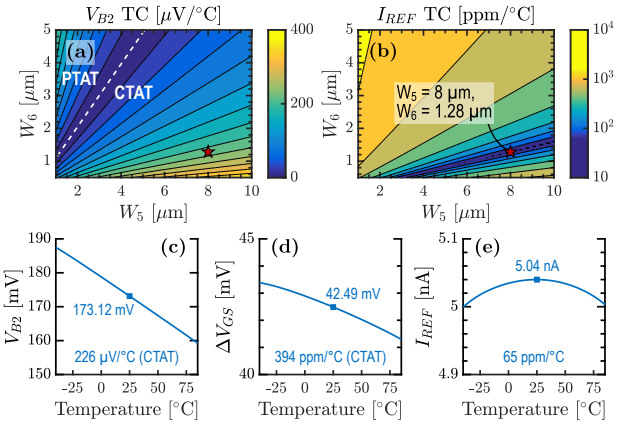

Fig. 6. **In bulk technologies such as 0.11-μm, a CTAT V_{B2} is required to achieve a CWT I_{REF} due to the temperature dependence of the linearized body factor γ_b^*.** Temperature coefficient of (a) V_{B2} and (b) I_{REF}, as a function of transistor widths W_5 and W_6. Temperature dependence of (c) V_{B2}, (d) ΔV_{GS} and (e) I_{REF} at the chosen design point.

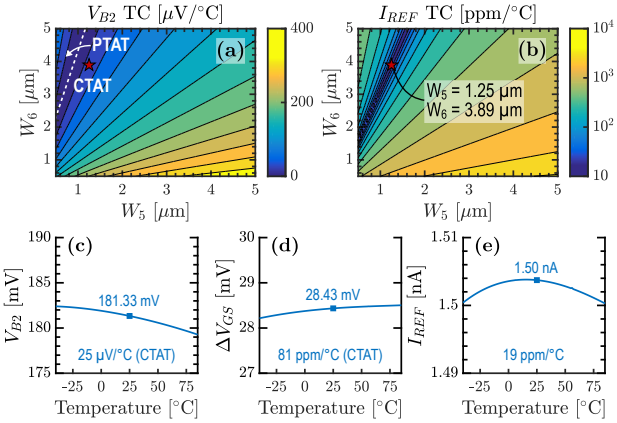

Fig. 7. **In FD-SOI technologies such as 22-nm, a close-to-CWT V_{B2} is required to achieve a CWT I_{REF} due to the first-order temperature independence of the linearized body factor γ_b^*.** Temperature coefficient of (a) V_{B2} and (b) I_{REF}, as a function of transistor widths W_5 and W_6. Temperature dependence of (c) V_{B2}, (d) ΔV_{GS} and (e) I_{REF} at the chosen design point.

density by 2.4 and 9× compared to the values shown in Table I. In 0.11 μm, a P+ high-res. poly resistor is selected, while in 22 nm, an N+ high-res. narrow poly resistor is chosen. Because this work focuses on area reduction, we select the resistor with the highest density, but a better TC could potentially be attained by selecting the resistor with the lowest TCR. Section IV however demonstrates that a sub-100-ppm/°C TC can be reached with the proposed choice.

Next, step 2) is presented in Figs. 4 to 7. The main problem that can appear in an inappropriately-sized 2T body bias generator is a divergence of the generated V_{B2} from its ideal behavior at low temperature, as depicted in Fig. 4(a). This discrepancy either stems from gate leakage, or from gate-induced drain leakage (GIDL), whose relative impact is exacerbated at low temperature due to an increased V_T. In the considered technologies, gate leakage is unlikely as 0.11-μm core devices still have a relatively thick oxide, and the devices used in 22 nm are I/O ones. Fig. 4(b) reveals that, at low temperature, I_{DS} at V_{GS} = 0 flattens instead of decreasing exponentially, while (g_m/I_D) at V_{GS} = 0, i.e., the slope of the $\log(I_D)$ vs. V_{GS} curve at V_{GS} = 0, plummets. This sharp

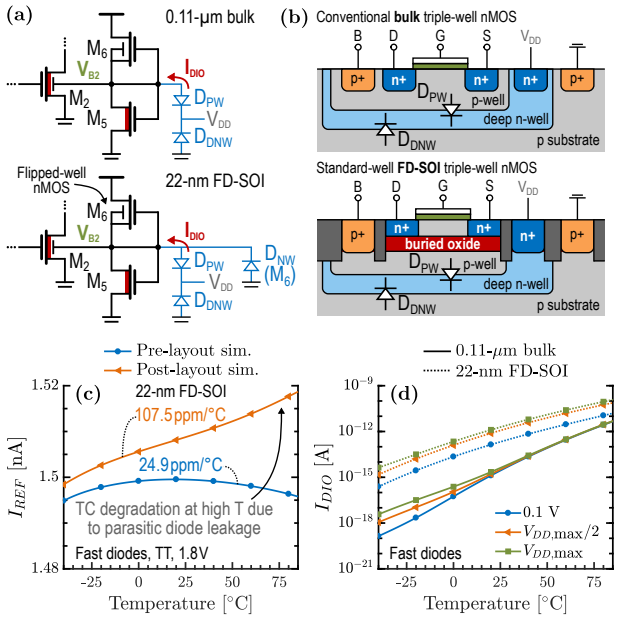

Fig. 8. **I_{REF} TC is degraded by the leakage of the parasitic p-well/deep n-well diode D_{PW}.** All figures are for 0.11-μm and 22-nm technologies except for (c). (a) Schematic of the 2T body bias generator with parasitic diodes. (b) Cross-section of triple-well nMOS devices. (c) Temperature dependence of I_{REF} in TT 1.8 V and fast diodes, based on pre- and post-layout simulations in 22-nm. (d) p-well/deep n-well diode leakage in a fast corner, as a function of temperature, for different reverse voltages, and for a diode area of 968 μm^2 in 0.11 μm (resp. 370 μm^2 in 22 nm).

drop is even more pronounced for a high V_{DS}, which is consistent with the fact that GIDL is exacerbated at high V_{DS}. This issue can nevertheless be alleviated by properly selecting the transistor type and length of the transistors used in the 2T body bias generator, as shown in Fig. 5. In 0.11 μm, a low-V_T (LVT) transistor is preferable to a regular- or high-V_T (RVT or HVT) one, as these latter types present a strong degradation of (g_m/I_D) at V_{GS} = 0 [Fig. 5(a)]. Regarding the transistor length, L = 7.5 μm is selected, thereby yielding a (g_m/I_D) at V_{GS} = 0 equal to 78.1 % of $(g_m/I_D)_{\max}$ in the SS -40°C corner, and a 107.9-pA leakage per transistor in the SS 85°C corner which is close to the selected 100-pA target [Fig. 5(b)]. In 22 nm, super-low-V_T (SLVT) I/O transistors are selected as they feature a nearly-perfect behavior at V_{GS} = 0 [Fig. 5(c)]. A length of 1 μm is chosen, leading to a (g_m/I_D) at V_{GS} = 0 equal to 99.5 % of $(g_m/I_D)_{\max}$ in SS -40°C, and a 50.7-pA leakage per transistor in SS 85°C. Note that, as the supply voltage can go up to 1.8 V thanks to the use of I/O devices, an additional zero-V_{GS} transistor M_7 identical of M_6 is added on top of it in Fig. 10(b) to reduce the V_{DS} to values similar to Fig. 5, thereby limiting the impact of GIDL while simultaneously improving LS. Now that the transistor types and lengths have been selected, a two-dimensional sweep of W_{5-6} allows to determine the ratio S_6/S_5 leading to a CWT I_{REF}, as represented in Figs. 6 and 7 for the 0.11-μm and 22-nm designs, respectively. In 0.11 μm, a complementary-to-absolute-temperature (CTAT) V_{B2} is required to compensate the temperature dependence of γ_b^* in bulk [Fig. 6(a)]. The chosen design point corresponds to W_5 = 8 μm and W_6 = 1.28 μm [Fig. 6(b)], and leads to a 226-μV/°C CTAT slope for V_{B2} [Fig. 6(c)] and a 65-ppm/°C TC for I_{REF} [Fig. 6(e)]. In 22 nm, a close-to-CWT V_{B2} is required because of the first-order temperature independence of γ_b^* in FD-SOI [15] [Fig. 7(a)]. The chosen design point corresponds to W_5 = 1.25 μm and W_6 = 3.89 μm [Fig. 7(b)], and leads to a 25-μV/°C CTAT slope for V_{B2} [Fig. 7(c)] compensating the CTAT TCR of the chosen high-res. N+ poly. resistor, and a 19-ppm/°C TC for I_{REF} [Fig. 7(e)].

Finally, step 3) must ensure that M_{1-4} remain saturated across PVT corners, and that variability constraints are met. On the one hand, M_{1-2} are operated in weak inversion and their aspect ratio S_{1-2} must be chosen so that $V_{GS2} = V_{DS1} > 4U_T$ in the FF 85°C corner. M_{3-4} should be biased in moderate inversion to minimize the current mirror mismatch within a reasonable silicon area, and their aspect ratio S_{3-4} must be such that $V_{GS4} = V_{DS4} > 4U_T$. In practice, this limit on V_{GS4} should be larger than $4U_T$ because of the operation in moderate inversion. On the other hand, variability considerations can also come into play, but this requires to establish an analytical expression linking the variability of I_{REF} to the transistor dimensions. Eq. (20), developed in Appendix A, informs us that the variability of I_{REF} stems from the V_T mismatch between the transistor pairs M_{1-2} and M_{5-6}, as well as the current imbalance between M_{3-4}, the latter being the dominant source of mismatch as later discussed in Section IV. Special care must therefore be taken in sizing the pMOS current mirror.

III. Architectural Optimizations

This section details the features added to the simplified design in Fig. 2(b), namely a circuit to mitigate the impact of parasitic diode leakage in Section III-A, and another to trim I_{REF} and its TC in Section III-B. Then, all the details regarding the final implementation of the proposed PCR in 0.11-μm bulk and 22-nm FD-SOI are provided in Section III-C.

A. Parasitic Diode Leakage Mitigation

The remaining issue with the 2T voltage reference is related to parasitic diode leakage, which becomes significant at high temperature and leads to a distortion of V_{B2}, consequently impacting the TC of I_{REF}. It stems from the fact that the 2T voltage reference biases the body of the nMOS transistor M_2 with a voltage $V_{B2} > 0$ [Fig. 8(a)]. Therefore, M_2 needs to be implemented as a triple-well device, whose cross-section is represented for bulk and FD-SOI technologies in Fig. 8(b). Its p-well is biased at $V_{B2} > 0$, while its deep n-well and p-substrate are respectively connected to V_{DD} and ground. The connections of the parasitic diodes resulting from this triple-well implantation are shown in Fig. 8(a), and these parasitic diodes are located in the cross-section in Fig. 8(b). The leakage of the parasitic p-well/deep n-well diode leads to a current I_{DIO} flowing from V_{DD} to V_{B2}. Fig. 8(c) displays the degradation of I_{REF} TC from 107.5 to 24.9 ppm/°C between pre- and post-layout simulations in 22-nm FD-SOI. Furthermore, Fig. 8(d) reveals that this leakage increases exponentially with temperature and is also impacted by the reverse voltage drop V_D across the diode, with a higher V_D inducing a higher leakage. At 85°C, for a p-well

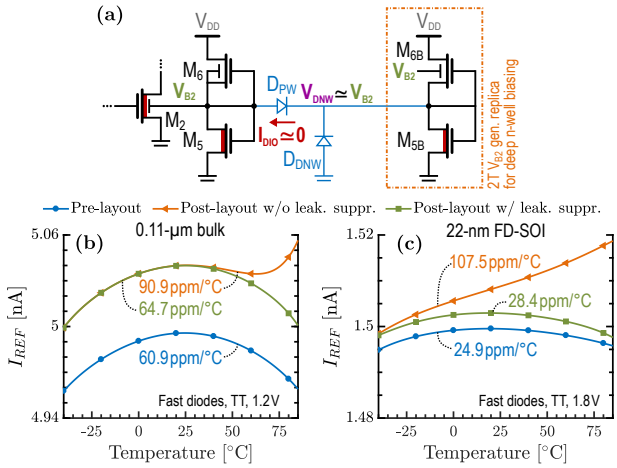

Fig. 9. ***I_{REF}* TC degradation is mitigated by leakage suppression, relying on a replica of the 2T body bias generator to bias the deep n-well.** (a) Schematic of the 2T body bias generator with parasitic diodes and a replica for leakage suppression. Temperature dependence of I_{REF}, based on pre-layout simulations, and post-layout simulations without and with leakage suppression, (b) in 0.11-μm bulk, with a 100-$\times$ scaling factor on the p-well/deep n-well diode leakage, and (c) in 22-nm FD-SOI.

corresponding to the dimensions of M_2 with its surrounding dummies, I_{DIO} is around 4.8 pA in 0.11 μm, and ranges from 15.4 to 120.4 pA in 22 nm. These results suggest that I_{DIO} is largely underestimated in 0.11-μm models, as at 25°C and V_D = 0.1 V, the leakage per unit area is 2.83 aA/μm^2 in 0.11 μm compared to 565.96 aA/μm^2 in 22 nm, so a 200-$\times$ difference. At 85°C, this difference narrows down to 8.9$\times$, with a leakage per unit area worth 4.70 fA/μm^2 in 0.11 μm and 41.73 fA/μm^2 in 22 nm. If we compare the leakage in 0.11 μm bulk to the dark current of a P+/n-well photodiode in 0.18 μm bulk at 25°C [19], the measured value is 7.16 fA for a 20$\times$20-μm^2 diode, corresponding to a 17.9-aA/μm^2 leakage per unit area 6.3$\times$ larger than the simulated value in Fig. 8(d).

The proposed solution to mitigate the impact of this leakage, referred to as *leakage suppression*, consists in zeroing out the leakage by biasing the parasitic p-well/deep n-well diode with a reverse voltage V_D close to zero. This is achieved by biasing the deep n-well with a voltage V_{DNW} close to V_{B2}, generated by a replica of the 2T body bias generator, as shown in Fig. 9(a). This replica has the same S_6/S_5 ratio as the body bias generator, but not necessarily the same widths W_{5-6}, thereby allowing to adjust its power consumption. Note that, to increase the temperature range up to 125°C, a larger S_6/S_5 in the replica compared to the body bias generator might be needed, to ensure that the parasitic p-well/deep n-well diode remains reverse-biased and that its leakage current remains negligible. The leakage suppression technique was initially proposed in the context of voltage references [20], and used to generate a CTAT 191-nA current reference in [21], with both works providing measurement results in bulk technologies. For the 0.11-μm design, because the parasitic diode model underestimates the leakage, we observe no significant degradation of I_{REF} TC between pre- and post-layout simulations. However, when we apply a 100-$\times$ scaling factor to this leakage as in Fig. 9(b), I_{REF} TC increases from 60.9 to 90.9 ppm/°C, and the leakage suppression circuit cuts down this degradation to 64.7 ppm/°C. For the 22-nm design in Fig. 9(c), I_{REF} TC

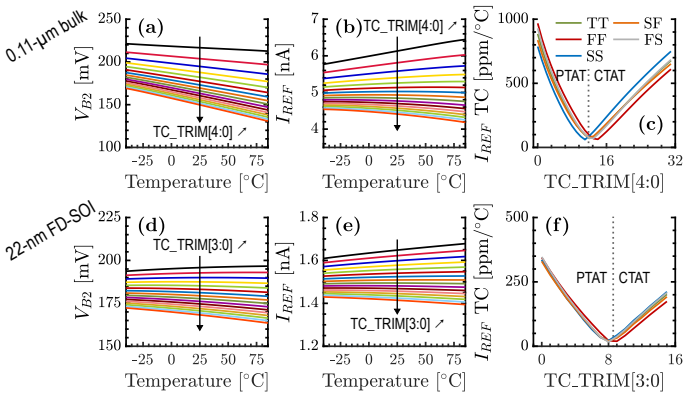

Fig. 11. ***I_{REF}* TC is trimmed by changing the effective width of M_5 in the 2T body bias generator.** In TT 1.2 V (resp. 1.8 V), temperature dependence of V_{B2} [(a) and (d)] and I_{REF} [(b) and (e)] as a function of the trimming code in 0.11 μm (resp. 22 nm). (c)(f) I_{REF} TC as a function of the trimming code in conventional process corners.

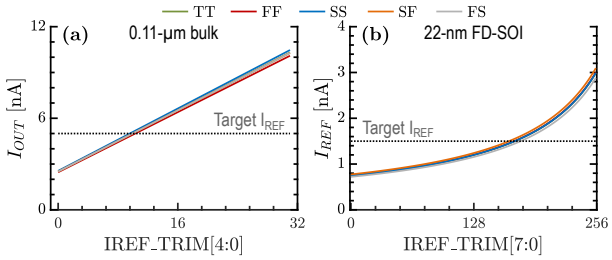

Fig. 12. ***I_{OUT}* is trimmed by means of a binary-weighted current mirror in bulk, and *I_{REF}* by a trimmable binary-weighted resistance in FD-SOI.** At 1.2 V (resp. 1.8 V), trimmed current at 25°C as a function of the trimming code in (a) 0.11 μm and (b) 22 nm.

is degraded from 24.9 to 107.5 ppm/°C due to the parasitic diode leakage, but this degradation is nearly entirely recovered by the leakage suppression circuit, leading to a post-layout 28.4-ppm/°C TC. In the complete schematic in Fig. 10, the careful reader may notice that in 0.11-μm bulk, M_{6-6B} have their body connected to V_{B2} [Fig. 10(a)] and are located in the same p-well as M_2. On the contrary, in 22-nm FD-SOI, M_{6-6B} have their body connected to V_{DNW} [Fig. 10(b)], because they are implemented with SLVT flipped-well devices required to have a lower V_T than M_{5-5B}. They are thus located in an n-well, which is biased by the replica to keep the leakage of diode D_{NW} [Fig. 8(a)] from impacting V_{B2}.

B. Temperature Coefficient and Reference Current Trimming

Depending on the application, it might be necessary to calibrate the TC of I_{REF} and/or I_{REF} itself, to maintain performance across process corners. The proposed design includes two trimming circuits fulfilling this function. First, the TC trimming circuit is presented in Fig. 10 and relies on a change of S_6/S_5 in (10) to tune the TC of V_{B2}, and therefore, the TC of I_{REF}. It is implemented by changing the effective width of M_5 using binary-weighted branches connected in parallel. The switches are either located on top of or below transistors M_{5Vi}. We find more effective to place switches below M_{5Vi} in technologies with a large n as it results in a low I_{on}/I_{off} ratio. This switch arrangement alleviates the problem by providing a larger V_{GS} and therefore I_{DS} when the switch is on. Figs. 11(a) to (c) illustrate the effect of

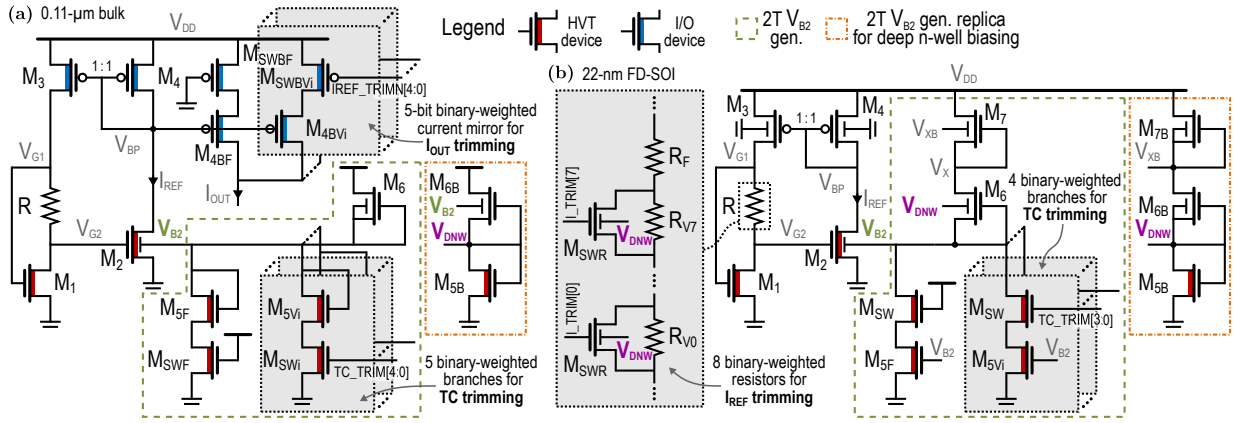

Fig. 10. Complete schematic of the proposed nA-range CWT reference in (a) 0.11-μm bulk and (b) 22-nm FD-SOI. The schematic includes trimming circuits for TC and I_{REF}, as well as a replica of the 2T body bias generator to suppress the leakage of the parasitic p-well/deep n-well diode.

TABLE II
SIZING OF THE PROPOSED NA-RANGE CWT CURRENT REFERENCES.

	0.11-μm bulk*							22-nm FD-SOI					
	w/o trimming			w/ TC and I_{REF} trimming				w/o trimming			w/ TC and I_{REF} trimming		
	Type*	W [μm]	L [μm]	Type*	W [μm]	L [μm]		Type*	W [μm]	L [μm]	Type*	W [μm]	L [μm]
M_{1-2}	LL	2×8	4×5	LL	2×8	4×5	M_{1-2}	LVT	8	4×8	LVT	8	4×8
M_{3-4}	HS	2×2	2×25	I/O	20×2.5	5	M_{3-4}	SLVT	0.32	10×8	SLVT	0.32	10×8
M_5	LL	16×4	7.5	-	-	-	M_5	LVT	8×1.25	1	-	-	-
M_{6-7}	HS	8×1.28	7.5	HS	8×1.28	7.5	M_{6-7}	SLVT	8×3.89	1	SLVT	8×3.9	1
M_{5B}	LL	4×4	7.5	LL	4×4	7.5	M_{5B}	LVT	8×1.25	1	LVT	16×0.625	1
M_{6B-7B}	HS	2×1.28	7.5	HS	2×1.28	7.5	M_{6B-7B}	SLVT	8×3.89	1	SLVT	8×3.9	1
R	P+ poly (high res.)	0.5	256×15.565	P+ poly (high res.)	0.5	212×18.705	R	N+ poly (high res.)	0.04	100×9.765	-	-	-
M_{5F}	-	-	-	LL	4×4	7.5	M_{5F}	-	-	-	LVT	8×0.625	1
M_{5Vi}	-	-	-	LL	1 to 16×4	7.5	M_{5Vi}	-	-	-	LVT	1 to 8×0.625	1
M_{SWF}	-	-	-	LL	4×0.25	2	M_{SW}	-	-	-	LVT	0.16	8
M_{SWVi}	-	-	-	LL	1 to 16×0.25	2	M_{SWR}	-	-	-	SLVT	10	0.15
M_{4BF}	-	-	-	I/O	10×2.5	5	R_F	-	-	-	N+ poly (high res.)	0.04	85×5.634
M_{4BVi}	-	-	-	I/O	1 to 16×2.5	5							
M_{SWBF}	-	-	-	I/O	10×0.25	1.25	R_{Vi}	-	-	-	N+ poly (high res.)	0.04	1 to 128×5.634
M_{SWBVi}	-	-	-	I/O	1 to 16×0.25	1.25							

* Dimensions reported for 0.11-μm bulk are pre-shrink ones, and must be scaled by a factor 0.9× to obtain silicon dimensions. * In 0.11 μm, HS refers to high-speed, i.e., LVT, and LL to low-leakage, i.e., HVT. In 22 nm, SLVT refers to super-low-V_T, and LVT to low-V_T.

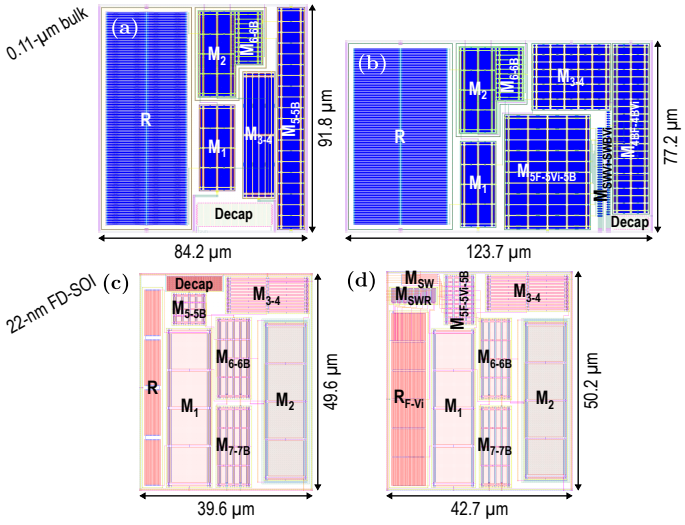

Fig. 13. Layout of the proposed reference (a)(c) without and (b)(d) with TC and I_{REF} trimming, in 0.11-μm bulk and 22-nm FD-SOI.

TABLE III
SUMMARY OF THE SIMULATED AND MEASURED PERFORMANCE OF THE PROPOSED NA-RANGE CWT REFERENCES.

	0.11-μm bulk		22-nm FD-SOI		
	w/o trimming Sim.	w/ trimming Sim.	w/o trimming Sim.	w/ trimming Sim.	**Meas.**
I_{REF} [nA]	5.04	5.03	1.50	1.50	1.21/1.50†
Power [nW]	5.03 @0.45V	13.88 @0.85V	2.04 @0.65V	2.35 @0.75V	2.87 @0.75V
Area [mm^2]	0.00773	0.00954	0.00197	0.00214	
Supply range [V]	0.45 – 1.2	0.85 – 1.2	0.65 – 1.8	0.75 – 1.8	
LS [%/V]	2.22	2.84	0.44	0.41	0.51
PSRR* [dB]	-35.4	-35.8	-38.4	-35.9	N/A
Temp. range [°C]	-40 – 85	-40 – 85	-40 – 85	-40 – 85	
TC [ppm/°C]	121.3	64.3	52.2	21.7	168.0/89.2†
I_{REF} var. (process) [%]	11.60	9.05	10.48	9.88	4.10/0.61†
I_{REF} var. (mismatch) [%]	0.71	1.32	2.55	2.98	
t_{start} [ms]	0.65	1.82	0.96	1.05	11.96

† Before and after trimming. * PSRR = $20\log_{10}\left[(i_{ref}/v_{dd})/(I_{REF}/V_{DD})\right]$ is characterized at 10 Hz and $V_{DD,\min}$, with a 1-pF capacitor between V_{BP} and V_{DD}.

this trimming circuit in 0.11 μm, whereas Figs. 11(d) to (f) depict it in 22 nm. We observe in Figs. 11(a) and (d) that the change in V_{B2} TC allows to make I_{REF} either PTAT or CTAT [Figs. 11(b) and (e)] across the trimming range, and that the minimum I_{REF} TC is easily reached in the five conventional process corners [Figs. 11(c) and (f)]. Section IV-A will later highlight that skewed process corners, i.e., different process corners for the devices of different V_T types used for M_5 and M_6, are more critical and should be adequately considered when defining the trimming range.

Moreover, a trimming of I_{REF} can be required in applications relying on an accurate value of I_{REF}. In 0.11 μm, this trimming is performed by a 5-bit binary-weighted current mirror [Fig. 10(a)], allowing for a linear control of the output current I_{OUT} [Fig. 12(a)]. Besides, 3.3-V I/O devices are used for the mirror formed by M_3, M_4 and $M_{4BF-4BVi}$, and for the switches $M_{SWBF-SWBVi}$, as they feature a lower I_{off}

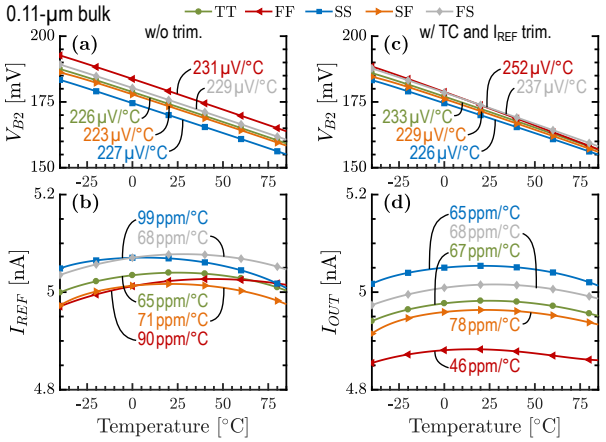

Fig. 14. In 0.11-μm bulk, post-layout simulation of the temperature dependence of V_{B2} and I_{REF}, in all process corners and at 1.2 V, without trimming [(a) and (b)], and with TC and I_{REF} trimming [(c) and (d)].

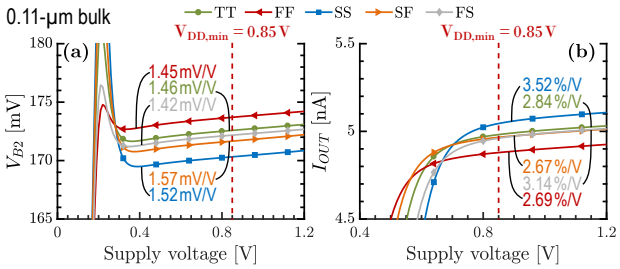

Fig. 15. In 0.11-μm bulk, post-layout simulation of the supply voltage dependence of V_{B2} and I_{REF} in all process corners and at 25°C, with TC and I_{REF} trimming.

than core devices. In 22 nm, the I_{REF} trimming circuit is integrated inside the reference, and is implemented by eight binary-weighted resistors which can be shorted by nMOS switches [Fig. 10(b)]. This trimming scheme is possible as the I_{on}/I_{off} ratio is larger in 22 nm than in 0.11 μm thanks to a lower n, and is also more power-efficient as it avoids the overhead associated with I_{OUT}. In addition, it enables a finer trimming resolution, but leads to a nonlinear relationship between the calibration code and I_{REF} as it changes the value of resistor R in (12) [Fig. 12(b)].

C. Final Implementation

Two current references, respectively without trimming, and with TC and I_{REF} trimming, have been implemented in each of the 0.11-μm bulk and 22-nm FD-SOI technologies. The complete schematic of the proposed reference with leakage suppression, and TC and I_{REF} trimming, is presented in Fig. 10, while the layout and sizing of the four proposed references can be found in Fig. 13 and Table II, respectively. Interestingly, Fig. 13 reveals that the area overhead of the trimming circuit, with respect to the area of the reference without trimming, corresponds to 23.5 % in 0.11 μm and can be attributed equally to the TC and I_{REF} trimming circuits, while it is only 9.1 % in 22 nm and is predominantly due to the binary-weighted resistors used to trim I_{REF}.

IV. Post-Layout Simulation Results

In this section, we discuss the post-layout simulation results of the four references introduced in Section III-C. More

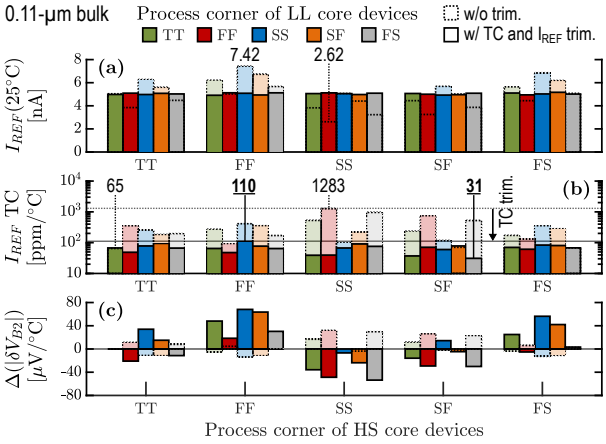

Fig. 16. In 0.11-μm bulk and at 1.2 V, post-layout simulation of (a) I_{REF} at 25°C, (b) I_{REF} TC from -40 to 85°C, and (c) the change in CTAT slope of V_{B2}, denoted as δV_{B2}, with respect to its nominal value, without trimming, and with TC and I_{REF} trimming.

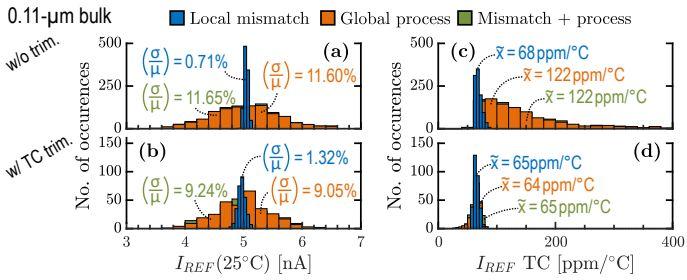

Fig. 17. In 0.11-μm bulk, for post-layout MC simulations (10^3 without trimming, and 3×10^2 with TC trimming) in TT at 1.2 V, histograms of I_{REF} at 25°C [(a) and (b)] and of I_{REF} TC from -40 to 85°C [(c) and (d)], without trimming [(a) and (c)], and with TC trimming [(b) and (d)]. $\tilde{x}$ denotes the median of the distribution.

specifically, the temperature dependence is discussed in conventional and skewed process corners, and for Monte-Carlo (MC) simulations. The interest of this section is thus to demonstrate the performance of the proposed references and the robustness of the trimming mechanisms under the impact of local mismatch and global process variations, which cannot be as extensively and thoroughly covered in measurement. Additionally, for the design with TC and I_{REF} trimming, we characterize the supply voltage dependence and startup. Table III summarizes the performance of the designs.

A. Designs in 0.11-μm Bulk CMOS Technology

The temperature dependence of V_{B2} and I_{REF} is shown in Fig. 14. In the design without trimming, there is a slight change of V_{B2} [Fig. 14(a)], hence deteriorating I_{REF} TC in FF and SS to 90 and 99 ppm/°C, compared to 65 ppm/°C in TT [Fig. 14(b)]. Trimming the TC and I_{REF} modifies the CTAT slope of V_{B2} [Fig. 14(c)], and thereby reduces the TC to at most 78 ppm/°C in SF [Fig. 14(d)]. While the trimming mechanism in Fig. 14 may not yield obvious benefits in conventional process corners, its interest in dealing with different process corners for the two V_T types employed for M_{5-6} is paramount, as will be discussed herebelow in relation to Fig. 16. Next, the supply voltage dependence is depicted in Fig. 15, with the minimum supply voltage given by

$$V_{DD,\min} \approx 4U_T + \max\left(V_{GS1}, V_{SG4}, V_{B2}\right). \qquad (17)$$

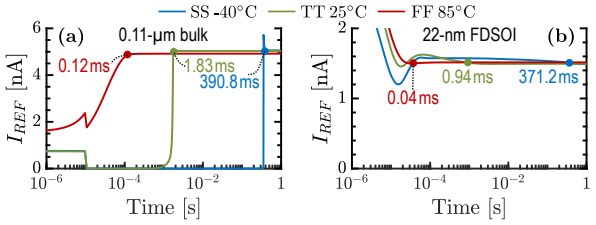

Fig. 18. Post-layout startup waveforms of the reference with TC and I_{REF} trimming, in the fastest (FF 85°C), typical (TT 25°C), and slowest (SS -40°C) corners, (a) at 1.2 V in 0.11-μm bulk and (b) at 1.8 V in 22-nm FDSOI, using a voltage source with a 100-μs rise time.

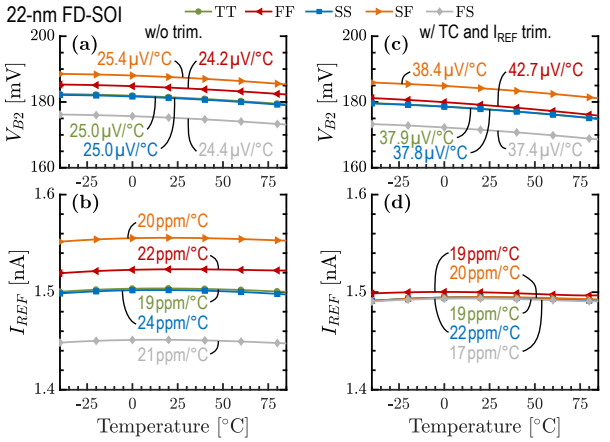

Fig. 19. In 22-nm FD-SOI, post-layout simulation of the temperature dependence of V_{B2} and I_{REF}, in all process corners and at 1.8 V, without trimming [(a) and (b)], and with TC and I_{REF} trimming [(c) and (d)].

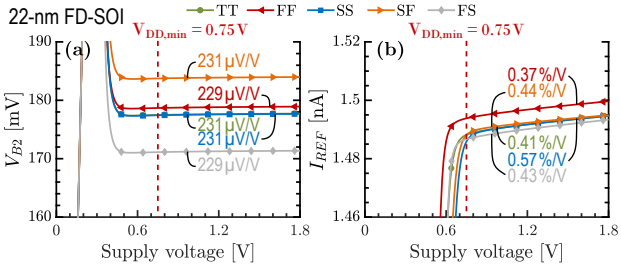

Fig. 20. In 22-nm FD-SOI, post-layout simulation of the supply voltage dependence of V_{B2} and I_{REF} in all process corners and at 25°C, with TC and I_{REF} trimming.

For this design, $V_{DD,\text{min}}$ is limited to 0.85 V by the large V_{SG4} due to the use of I/O devices in the pMOS current mirror. Yet, the 2T body bias generator already produces a valid V_{B2} above 0.4 V, explaining why the design without trimming can operate down to 0.45 V in Table III. V_{B2} LS is comprised between 1.42 and 1.57 mV/V from 0.85 to 1.2 V [Fig. 15(a)], while I_{REF} LS ranges from 2.67 to 3.52 %/V [Fig. 15(b)]. Eq. (9) indicates that this LS predominantly stems from the variation of M_2 V_{DS}. In addition, Fig. 16 considers the impact of HS/LL skewed process corners, i.e., different process corners for the high-speed (HS) and low-leakage (LL) core devices used for M_{5-6}. Fig. 16(a) shows that, without trimming, I_{REF} ranges from 7.42 nA in (FF, SS) down to 2.62 nA in (SS, FF), resulting in process variations of +47.2% / -48.0%. The remaining variations after trimming are +3.6%/-1.4%, related to the finite resolution of the trimming circuit. Regarding I_{REF} TC [Fig. 16(b)], it lies between 65 and 1283 ppm/°C without trimming, and is reduced to a range from 31 to 110 ppm/°C

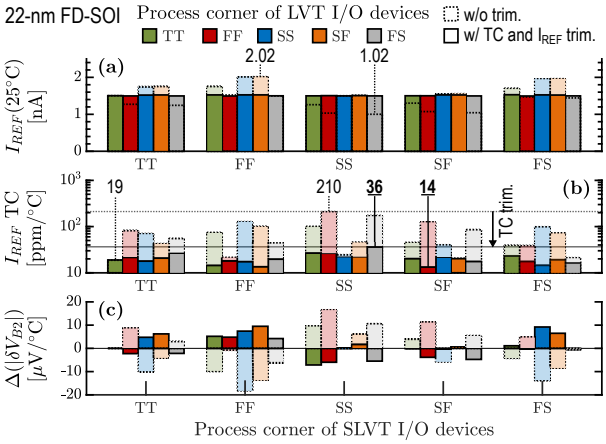

Fig. 21. In 22-nm FD-SOI and at 1.8 V, post-layout simulation of (a) I_{REF} at 25°C, (b) I_{REF} TC from -40 to 85°C, and (c) the change in CTAT slope of V_{B2}, denoted as δV_{B2}, with respect to its nominal value, without trimming, and with TC and I_{REF} trimming.

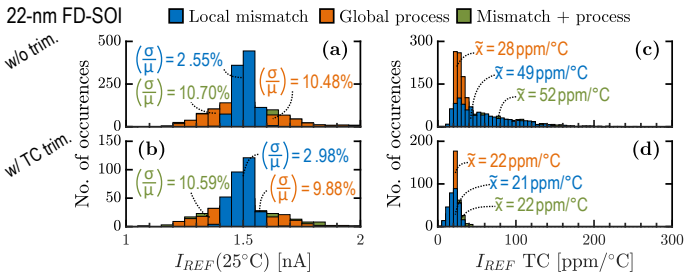

Fig. 22. In 22-nm FD-SOI, for post-layout MC simulations (10^3 without trimming, and 3×10^2 with TC trimming) in TT at 1.8 V, histograms of I_{REF} at 25°C [(a) and (b)] and of I_{REF} TC from -40 to 85°C [(c) and (d)], without trimming [(a) and (c)], and with TC and I_{REF} trimming [(b) and (d)]. $\tilde{x}$ denotes the median of the distribution.

after trimming. Moreover, I_{REF} TC is below 100 ppm/°C in all process corners except (FF, SS), which would necessitate a slightly larger TC trimming range. The effect of the TC trimming scheme is to increase the CTAT slope of V_{B2} in fast nMOS HS corners, and to diminish it in slow ones, on top of smaller variations related to the LL corner [Fig. 16(c)]. Then, MC simulations highlight that, without trimming [Fig. 17(a)], the impact of mismatch is limited, with a (σ/μ) of 0.71 %.This value is relatively close to the 1.18 % predicted by (20), from which 1% can be attributed to the mismatch of the pMOS mirror. The impact of process variations is more significant, with a (σ/μ) of 11.60 %, as a result of the process variations of M_{5-6} but more critically, of the resistance. In Fig. 17(b), the distribution of the TC due to local mismatch presents a 68-ppm/°C median and an 84-ppm/°C 99th percentile, while global process and combined effects both have a 122-ppm/°C median, with 99th percentiles at 422 and 446 ppm/°C. With TC trimming and no I_{REF} trimming, I_{REF} (σ/μ) slightly rises to 1.32 % with mismatch and shrinks to 9.05 % with process variations [Fig. 17(c)], due to a different sizing and to the trimming itself. In terms of TC, the median is cut down to 65 ppm/°C, with a 99th percentile at 75 ppm/°C for mismatch, and 80 ppm/°C for process and combined effects [Fig. 17(d)]. Finally, the x-% startup time corresponds to the time at which I_{REF} remains within (100-x) % of its steady-state value. The nominal 99-% startup time is equal to 1.83 ms in Fig. 18(a), and ranges from 0.12 to 390.8 ms in the best- and worst-case

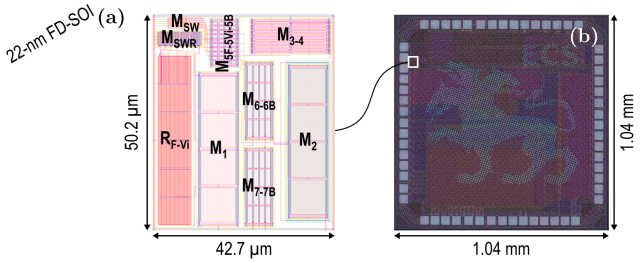

Fig. 23. In 22-nm FD-SOI, (a) layout of the proposed nA-range CWT current reference and (b) chip microphotograph with overlaid layout of the 1.08-mm^2 CERBERUS MCU.

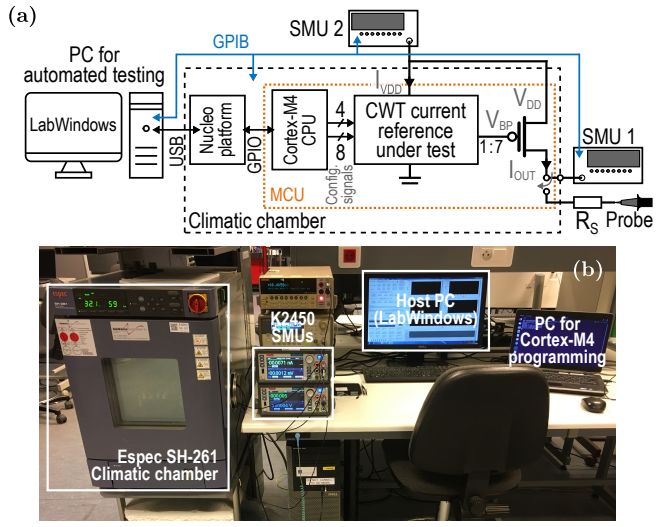

Fig. 24. Measurement testbench for the characterization of the dependence to supply voltage and temperature, as well as the startup time.

corners, respectively FF 85°C and SS -40°C.

B. Designs in 22-nm FD-SOI CMOS Technology

In Fig. 19, depicting the temperature dependence of I_{REF}, the design without trimming shows slim variations of V_{B2} CTAT slope between 24.4 and 25.4 μV/°C [Fig. 19(a)], translating into negligible variations of I_{REF} TC from 19 to 24 ppm/°C [Fig. 19(b)]. After trimming, V_{B2} and its TC are slightly different [Fig. 19(c)], yet I_{REF} TC remains in a range similar to the design without trimming, comprised between 17 and 22 ppm/°C, while a clear effect of the I_{REF} trimming can be observed [Fig. 19(d)]. Then, regarding the supply voltage dependence in Fig. 20, $V_{DD,\text{min}}$ is equal to 0.75 V and is not dominated by V_{SG4} as in 0.11 μm, but rather by the minimum V_{DD} required by the switches in the I_{REF} trimming circuit to avoid distortion. Fig. 20(a) reveals that V_{B2} is generated at 0.5 V, and presents an LS around 230 μV/V. In Fig. 20(b), I_{REF} features an LS between 0.37 and 0.57 %/V, which is a reduction of nearly 6× compared to the 0.11-μm design, thanks to the larger (g_m/g_d) in FD-SOI. Moreover, Fig. 21 illustrates the variations in SLVT/LVT skewed process corners, i.e., different process corners for the SLVT and LVT I/O devices used for M_{5-6}. Fig. 21(a) displays that I_{REF} spans from 2.02 nA in (FF, SF) to 1.02 nA in (SS, FS) without trimming, leading to process variations of +34.1% / -33.4%. However, trimming reduces variations to +0.2% / -0.3%, approximately 10× better than in 0.11 μm, which is consistent with the fact that the 22-nm design uses three additional calibration bits for I_{REF}. Adding more bits to the 0.11-μm design would be possible, but only at the expense of significant area overhead for the binary-weighted current mirror. Then, regarding the TC, it ranges from 19 to 210 ppm/°C without trimming, and is reduced from 14 to 36 ppm/°C after it, while being below 50 ppm/°C in all corners [Fig. 21(b)]. The effect of the TC trimming is to bring V_{B2} CTAT slope closer to its value in the SLVT TT corner, with slightly larger (resp. lower) values in the fast (resp. slow) nMOS LVT corners [Fig. 21(c)]. Next, considering MC simulations, without trimming, mismatch leads to a (σ/μ) of 2.55 % which is 3× larger than in 0.11 μm due to the smaller dimensions of the pMOS current mirror. Eq. (20) indeed predicts a variability of 3.78 % from which 3.65 % come from the mirror mismatch. Process variations lead to a (σ/μ) of 10.70 % similar to 0.11 μm [Fig. 22(a)]. I_{REF} TC suffers most from mismatch, with a 49-ppm/°C median and a 172-ppm/°C 99th percentile, than from process variations, with a 28-ppm/°C median and a 62-ppm/°C 99th percentile [Fig. 22(c)]. After TC trimming and no I_{REF} trimming, I_{REF} (σ/μ) slightly increases while process variations are reduced, in the same fashion as in 0.11 μm [Fig. 22(b)]. The TC now has a median around 22 ppm/°C in all simulation types, with 99th percentiles at 33, 28, and 42 ppm/°C, for mismatch, process, and combined effects. Lastly, Fig. 18(b) highlights a nominal 99-% startup time of 0.94 ms, which spans from 0.04 and 371.2 ms in extreme corners.

V. Measurement Results

A. Measurement Testbench

Out of the four designs in Section III-C, the 22-nm design with TC and I_{REF} trimming has been fabricated as part of the CERBERUS microcontroller unit (MCU) [Fig. 23(b)]. Eleven dies have been measured, using the setup shown in Fig. 24. It consists of a host PC controlling an Espec SH-261 climatic chamber for the temperature sweep, and two Keithley K2540 source measure units (SMUs) for the supply voltage sweep. On the one hand, SMU 1 measures $I_{OUT} = 7I_{REF}$ with V_{SD} = 0.9 V, and the current mirror producing I_{OUT} only slightly increases I_{REF} (σ/μ) by 0.36 %. Besides, the leakage of the electrostatic discharge (ESD) protection diodes in the analog pad is at most 8.12 pA at 85°C, i.e., only 0.077 % of I_{OUT}. On the other hand, SMU 2 measures the sum of I_{OUT} and the supply current I_{VDD}. Besides, the calibration bits are managed by an on-chip Cortex-M4, interacting through GPIO with a Nucleo-64 platform piloted by the host PC. To measure the startup time, SMU 1 is replaced by an 82-MΩ resistance R_S, in series with the 1-MΩ input resistance of the probe.

B. Measurement of the 22-nm FD-SOI Design

Fig. 25(a) illustrates that the temperature dependence of I_{REF}, with I_{REF} already trimmed, changes from PTAT to CTAT for different TC trimming codes. Figs. 25(b) and (c) show the histogram of the optimal code before and after I_{REF} trimming, revealing only marginal changes and thereby confirming that trimming I_{REF} does not impact its TC. This

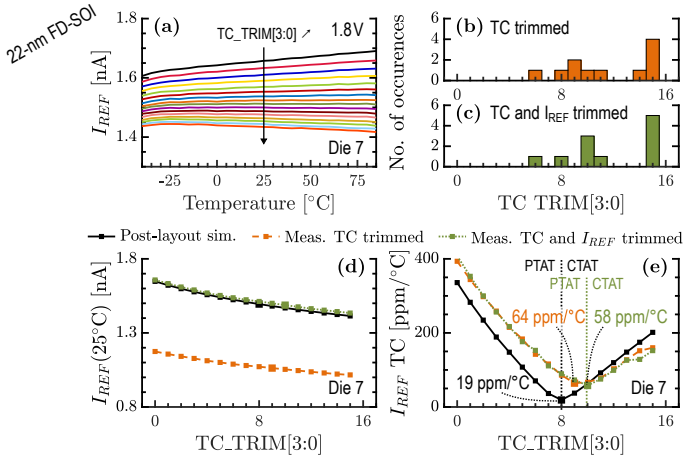

Fig. 25. In 22-nm FD-SOI, (a) measured temperature dependence of I_{REF} at 1.8 V for all trimming codes, with I_{REF} already trimmed. Histograms of the trimming code giving the minimum TC (b) before and (c) after I_{REF} trimming. Impact of the TC trimming (d) on I_{REF} at 25°C and (e) on I_{REF} TC. (b)(c) are for the 11 dies while (a)(d)(e) are for die 7.

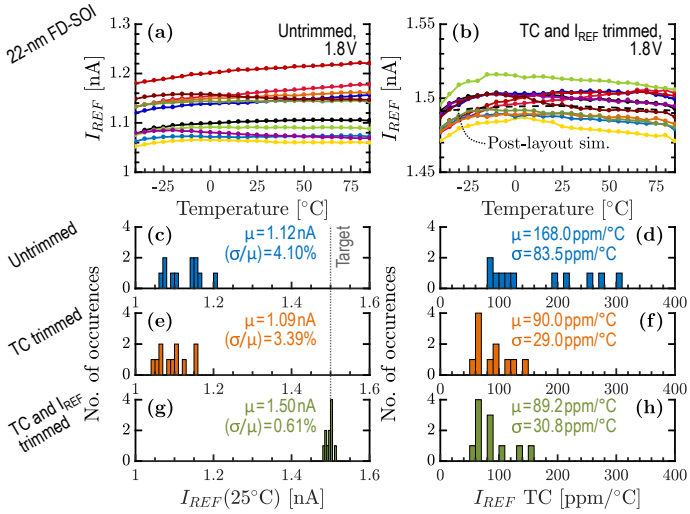

Fig. 26. In 22-nm FD-SOI and at 1.8 V, measured temperature dependence of I_{REF} (a) without trimming, and (b) with TC and I_{REF} trimming. Measured histograms of I_{REF} at 25°C [(c), (e) and (g)] and of I_{REF} TC from -40 to 85°C [(d), (f) and (h)], for the reference without trimming, with TC trimming, and with TC and I_{REF} trimming.

intuitively makes sense, as the TC of I_{REF} depends on the TCR, and on the TCs of V_{B2} and γ_b^*, but is not impacted by the change of resistance employed to trim I_{REF}. However, trimming the TC slightly modifies I_{REF} [Fig. 25(d)] due to a change of V_{B2}. The TC should thus be trimmed first, and I_{REF} consequently adjusted to reach the target value. For the die showing the best TC, a minimum TC of 58 ppm/°C is reached for a code of 0xA, compared to 19 ppm/°C for 0x8 in the TT post-layout simulation [Fig. 25(e)]. This gap originates from the behavior of I_{REF} below -20°C, as shown in Fig. 26(b). Next, the temperature dependence of I_{REF} is studied in Fig. 26 at the three stages of the trimming process, with Figs. 26(a) and (b) representing the I_{REF} vs. T curves for the 11 dies without and with trimming, respectively. Before any trimming, I_{REF} is 1.12 nA on average, with a (σ/μ) of 4.1 % and a TC of 168 ppm/°C [Figs. 26(c) and (d)], suggesting that the dies might originate from a slow SLVT and fast LVT nMOS process corner [Fig. 22(a)]. After

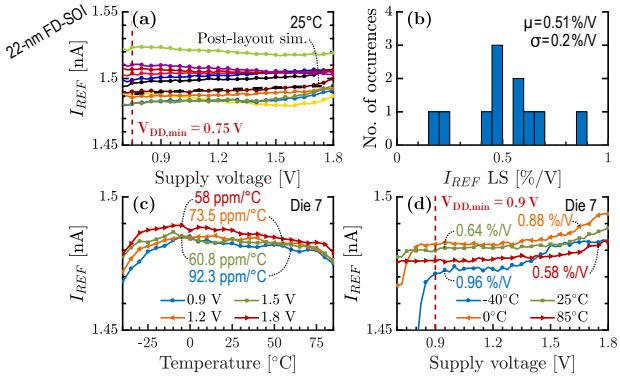

Fig. 27. In 22-nm FD-SOI and with TC and I_{REF} trimmed, (a) measured supply voltage dependence at 25°C and (b) histogram of LS from 0.75 to 1.8 V. For die 7, measured (c) temperature dependence at different supply voltages and (d) supply voltage dependence at different temperatures.

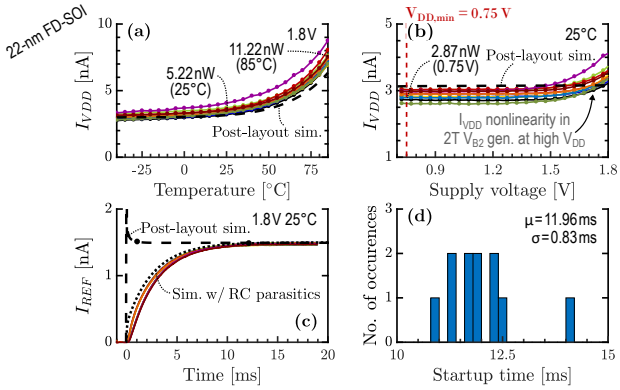

Fig. 28. In 22-nm FD-SOI, measured dependence of the supply current (a) to temperature at 1.8 V, and (b) to supply voltage at 25°C. (c) Measured startup waveforms and (d) histogram of the 99-% startup time at 1.8 V 25°C.

trimming the TC, (σ/μ) diminishes to 3.39 % while the TC decreases to 90 ppm/°C, with a standard deviation cut from 83.5 to 29 ppm/°C [Figs. 26(e) and (f)]. Finally, after complete trimming, I_{REF} is close to the 1.5-nA design point, with a (σ/μ) reduced to 0.61 % and an 89.2-ppm/°C average TC [Figs. 26(g) and (h)]. These results correspond to a trimming based on the complete temperature profile from -40 to 85°C, but a two-point trimming at -35 and 65°C gives similar results as it only marginally increases the mean TC from 89.2 to 89.4 ppm/°C. In both cases, we see a clear improvement compared to the 168-ppm/°C TC of the untrimmed reference, which could be even larger in other process corners, as suggested in Fig. 21(b). The TC differs from post-layout simulations due to the decrease of I_{REF} below -20°C, which is most likely due to the nMOS switches in the TC trimming circuit limiting the current flowing through M_{5Vi}. Moreover, Fig. 27(a) shows the supply voltage dependence of I_{REF} for the 11 trimmed dies, with $V_{DD,\text{min}}$ = 0.75 V and a 0.51-%/V average LS [Fig. 27(b)] in line with the 0.41-%/V simulated value. Then, I_{REF} temperature dependence is characterized at various supply voltages, revealing a consistent behavior, albeit the TC is slightly degraded from 58 to 92.3 ppm/°C as V_{DD} is reduced from 1.8 to 0.9 V [Fig. 27(c)]. Additionally, Fig. 27(d) characterizes the supply voltage dependence of I_{REF} at different temperatures, and indicates that a $V_{DD,\text{min}}$ of 0.9 V would be required to operate down to -40°C, but also that the LS deteriorates from 0.58 to 0.96 %/V as temperature

TABLE IV
COMPARISON TABLE OF TEMPERATURE-INDEPENDENT NA-RANGE CURRENT REFERENCES.

	Far [22]	Cordova [23]	Santamaria [24]	Agarwal [25]	Aminzadeh [26]	Mahmoudi [27]	Bruni [28]	Huang [29]	Yang [30]	De Vita [31]	Dong [32]	Ji [10]	Wang [14]	Wang [11]	Huang [12]	Lee [33]	Chang [13]	Shetty [34]	Lefebvre [9]	**Lefebvre This work**
Publication	ROPEC	ISCAS	ISCAS	TCAS-II	AEU		CAE	AEU	AEU	ISCAS	ESSCIRC	ISSCC	VLSI-DAT	TCAS-I	TCAS-II	JSSC	JJAP	TCAS-I	JSSC	JSSC
Year	2015	2017	2019	2022	2022	2022	2023	2023	2023	2007	2017	2017	2019	2019	2020	2020	2022	2022	2023	2024
Type of work	**Simulations**									**Silicon measurements**										Sim. / Meas.
Samples	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	20	16	10	10	16	10	10	3	10	20	N/A / 11
Technology	0.18μm	0.18μm	0.18μm	0.18μm	0.18μm	0.13μm	0.18μm	0.18μm	0.18μm	0.35μm	0.18μm	0.18μm	0.18μm	0.18μm	0.18μm	0.18μm	90nm	0.13μm	22nm	0.11μm / 22nm
I_{REF} [nA]	14	10.9	2.7	5.6	6.7	6.6	6.3	8.9	1.96	9.1	35	6.7	6.5	9.8	11.6	1	1.3	1.9	1.25/0.9*	5.03 / 1.12/1.50†
Power [nW]	150	30.5	26	9.5	51	3.7	3.3	0.05	9.2	54.8	1.02	9.3	15.8	28	48.6	4.5/14	8.6	10.2	7.8/5.8*	13.88 / 2.87
	@1V	@0.9V	@2V	@0.55V	@1V	@0.4V	@0.6V	@0.8V	@0.55V	@1.5V	@1.5V	@N/A	@0.85V	@0.7V	@0.8V	@1.5V	@0.75V	@0.85V	@0.9V	@0.85V / @0.75V
Area [mm^2]	**0.0102**	**0.01**	**0.0093**	0.032	**0.46**	**0.0021**	**0.0018**	**0.008**	**0.0033**	0.035	0.0169	**0.055**	**0.062**	**0.055**	**0.054**	**0.332**	0.0175	0.0163	0.0132	**0.00954** / **0.00214**
Supply range [V]	1 – 3.3	0.9 – 1.8	2 – 3.63$^\diamond$	0.55 – 1.9	1.1 – 1.8	0.4 – 1.6	0.6 – 1.8	0.8 – 1.8	0.55 – 1.8	1.5 – 4	1.5 – 2.5	1.3 – 1.8	0.85 – 2	0.7 – 1.2	0.8 – 2	1.5 – 2	0.75 – 1.55	0.85 – 2	0.9 – 1.8	0.85 – 1.2 / 0.75 – 1.8
LS [%/V]	**0.1**	**0.54**	**8.9**$^\diamond$	**0.022**	**0.03**	2.7	**12.1**	1.39	**0.2**	**0.57**	3	1.16	4.15	**0.6**	1.08	1.4	**0.15**	4	**0.26/0.39***	2.84 / **0.51**
Temp. range [°C]	0 – 70	-20 – 120	-40 – 125	-30 – 70	-40 – 120	-40 – 120	-40 – 120	0 – 125	0 – 100	0 – 80	-40 – 120	0 – 110	-10 – 100	-40 – 125	-40 – 120	-20 – 80	0 – 120	-40 – 120	-40 – 85	-40 – 85 / -40 – 85
TC [ppm/°C]	**20**	**108**	309	256	**40.3**	308	219	**139**	**96.8**	**44**	282	**680**/283†	**157**	**150**	**169**	289/265$^\triangleright$	**53**/394*	530/**822***	**203**/565*	**65** / 168/**89**†
TC type	Typ.	μ	μ	μ	μ	μ	Typ.	μ	μ	μ	μ	μ	μ	μ	μ	μ	μ	μ	μ	$\tilde{x}$ / μ
I_{REF} var. (process) [%]	N/A	15.8 / 11.6†	N/A	+55.4 / -28.5$^\diamond$	N/A	N/A	+129.1 / -61.8$^\diamond$	+2.8 / -13.9$^\diamond$	8.7	2.16	±4.7	N/A	N/A	+11.7 / -8.7$^\diamond$	+17.6 / -10.3$^\diamond$	N/A	21.1	N/A	+9.9 / -9.5	+3.64 / -1.41$^\triangleleft$ / +0.21 / -0.54$^\triangleleft$
I_{REF} var. (mismatch) [%]	5.8	N/A	**20.3**	**10.4**	**0.7**	**6.1**	N/A	2.6	1.7		1.6	4.07/1.19*	3.33	1.6	4.3	1.26/**0.25**†		**15.6**	**6.39/9.20***	1.32 / 4.10/**0.61**†
Trimming	No	TC (6b)	No	No	No	TC (12b)	No	TC (6b)	No	No	No	I_{REF}	No	TC (5b)	TC (4b)	I_{REF}	I_{REF} (4b)	I_{REF} (4b)	No	TC (5b), I_{REF} (5b) / TC (4b), I_{REF} (8b)
Spec. components	No	**ZVT**	No	Res.	Res., **BJT**	LVT, HVT	**ZVT**	**ZVT**, HVT	No	No	No	Res., **BJT**	No	Res., I/O	Res.	HVT	**ZVT**, HVT	Res., HVT	HVT	Res., HVT, I/O / Res., LVT
FoM$_1$ [ppm/°C^2×mm^2]	**0.0029**	**0.0077**	0.0174	0.0819	0.1159	**0.0040**	**0.0025**	**0.0089**	**0.0032**	0.0193	0.0298	0.1415	0.0887	0.0499	0.0570	0.9595	0.0575	0.0835	0.0597	**0.0050** / **0.0015**
FoM$_2$‡ [ppm/°C^2]	3.061	2.398	9.017	7.896	**1.917**	2.698	**1.195**	**0.0078**	8.261	2.208	**0.034**	3.571	4.082	3.711	5.532	**24.733**	**28.961**	**32.447**	**32.365**	**1.688** / **1.816**

* Simulated and measured values. † Before and after trimming. $^\diamond$ Estimated from figures. $^\triangleright$ For 25 and 2.5 minutes between two calibrations. $^\triangleleft$ After trimming. ‡ FoM$_2$ $= \frac{\text{TC}}{(T_{\max}-T_{\min})} \times \frac{I_{VDD}}{I_{REF}}$, as used in [17].

decreases from 85 to -40°C. These curves highlight an increase of I_{REF} above 1.5 V, which could be linked to drain-induced barrier lowering (DIBL). Moreover, the current consumption I_{VDD} in Fig. 28(a) is $2I_{REF}$ = 3 nA at low temperature as it is dominated by the PCR, consisting of two branches drawing the same current, but increases exponentially with temperature when the 2T body bias generator and its replica start to prevail, leading to a 2.1-× increase from 25 to 85°C. The dependence of I_{VDD} to the supply voltage in Fig. 28(b) presents a sharper increase at high V_{DD} compared to I_{REF}, likely originating from the 2T body bias generator. An average power consumption of 2.87 nW is reached at 0.75 V and 25°C. At last, regarding the 99-% startup time, an average value of 11.96 ms 11.4× larger than the simulated value is obtained [Fig. 28(d)]. In simulation, when considering a 33-pF capacitance at the drain of the pMOS transistor generating I_{OUT}, in parallel with the 82-MΩ resistance of R_S, a startup time of 12.15 ms is reached [Fig. 28(c)], confirming that PCB parasitics are the source of the observed discrepancy.

VI. COMPARISON TO THE STATE OF THE ART

In this section, we compare our work to the state of the art of simulated and fabricated nA-range CWT current references, detailed in Table IV and illustrated in Fig. 29. To better understand the performance of existing current references, we introduce a figure of merit (FoM) combining the temperature dependence of the current with the area occupied by the reference, i.e.,

$$\text{FoM}_1 = \frac{\text{TC}}{(T_{\max}-T_{\min})} \times \text{Area} \quad [\text{ppm/°C}^2 \times \text{mm}^2]. \quad (18)$$

It shares strong similarities with the one used in [35], [34], but puts less emphasis on the temperature range and does not include power consumption. In addition, it does not normalize performance, as the tradeoff between TC and silicon area is complex to model and depends on many factors. In our comparison, we focus on fabricated current references, and hence limit our discussion to the proposed 22-nm design. Besides, we do not normalize the silicon area to the technology

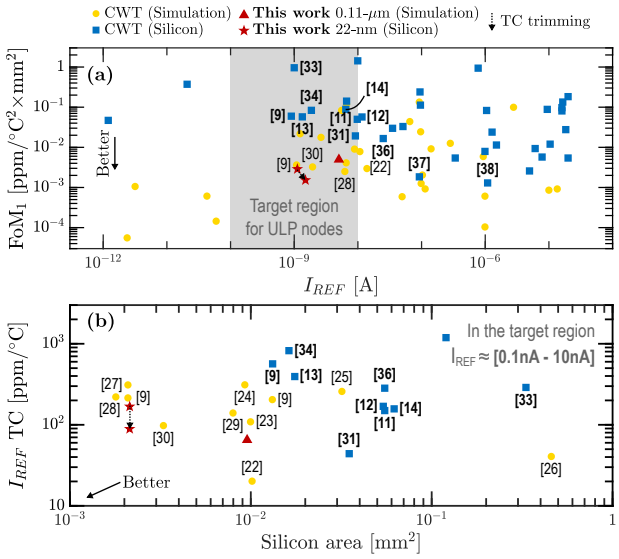

Fig. 29. (a) Figure of merit combining temperature dependence and silicon area as a function of I_{REF}, and (b) trade-off between TC and area in the target region, based on the state of the art of current references.

node as a fair normalization is not straightforward for analog circuits. First, Fig. 29(a) indicates that trimming the TC of I_{REF} improves the FoM of our 22-nm design by 1.9× thanks to a TC reduction from 168 to 89 ppm/°C. Compared to the closest fabricated competitor [31], our design offers a 12.9× FoM reduction explained by a 16.4× area reduction and an increased temperature range, despite a 2× larger TC. Moreover, [14], [11], [12] achieve an acceptable TC around 150 ppm/°C within a silicon area above 0.05 mm^2, due to the use of large subthreshold transistors [14] or resistors [11], [12]. [13], [34], [9] exhibit areas between 0.01 and 0.02 mm^2, dominated by gate-leakage transistors [13], resistors [34], or a subthreshold β-multiplier [9]. Nevertheless, their area efficiency is counterbalanced by their relatively large TC above 400 ppm/°C. [36] uses a pMOS with a V_G tracking V_T, and a source degeneration resistor to achieve temperature compensation. It occupies a 0.0053-mm^2 area but consumes 28.5 μW,

thereby limiting its interest. [33] employs a current DAC periodically trimmed by a high-precision duty-cycled current reference. It achieves a 265 ppm/°C TC, but at the expense of a significant 0.332-mm^2 silicon footprint. Finally, [37] and [38] are interesting architectures in terms of TC and area which lie outside of the target region. [37] relies on a β-multiplier with a triode transistor as V-to-I converter, and produces a 92.2-nA current with a 177-ppm/°C TC and 0.0013-mm^2 silicon area, but suffers from a large 6.1-% variability due to mismatch. [38] biases a resistor with the threshold voltage difference between two transistors of different V_T types, thereby generating a 1.1-μA 38-ppm/°C current within a 0.0043-mm^2 silicon area. However, the limited area is achieved thanks to the fact that resistors are well suited to the generation of a μA current.

VII. Conclusion

In this work, we presented a nA-range CWT peaking current reference, biasing a resistor with the ΔV_T between two subhtreshold transistors, one of them being forward body biased to decrease its V_T. The body bias is generated by a 2T voltage reference, with a replica to suppress the leakage of parasitic diodes at high temperature. In addition, the proposed reference does not require a startup circuit, and includes two simple mechanisms to trim I_{REF} and its TC, so as to maintain performance across process corners. It requires high-density polysilicon resistors and transistors of two different V_T types, which are common features of most technology nodes today. Then, we proposed a thorough sizing methodology and validated the reference with post-layout simulations in a bulk and an FD-SOI technology, to demonstrate that the body effect can indeed be employed in both of these technologies. Finally, we fabricated the proposed reference in 22-nm FD-SOI, and measured a 1.5-nA current across 11 dies with average TC and LS of 89 ppm/°C and 0.51 %/V, respectively. It consumes 2.87 nW at 0.75 V and occupies an area of 0.00214 mm^2. This results in a 12.9× FoM improvement compared to the closest fabricated competitor in the nA range. Further work could focus on extending the temperature range to 125°C while avoiding a sharp increase of the power consumed by the 2T voltage reference.

Appendix A
Analytical Expression of I_{REF} Variability

To establish an analytical expression linking the variability of I_{REF} to the transistor dimensions, we can rely on Pelgrom's law [39], and, under the assumption that the dominant source of mismatch is the threshold voltage, which is a common assumption in weak/moderate inversion [40], on the I_{DS} mismatch between two transistors taken from [41]. To compute the variability of I_{REF} due to mismatch, we employ the following expression

$$I_{REF} = \frac{(V_{T01} - V_{T02}) + \gamma_b^* V_{B2} + nU_T \ln\left(1 + \frac{\Delta I_{DS}}{I_{DS}}\right)}{R}, \tag{19}$$

which is a more accurate version of (12) taking into account the difference of V_{T0} and the current imbalance between M_{1-2}. Considering R, γ_b^*, n and U_T as constants, the variance of I_{REF} in the proposed CWT PCR can be computed as

$$\sigma^2(I_{REF}) = \frac{\sigma^2\left(\Delta V_{T0,1-2}\right)}{R^2} + \left(\frac{\gamma_b^*}{R}\right)^2 \sigma^2\left(V_{B2}\right) + \left(\frac{nU_T}{R}\right)^2 \sigma^2\left(\ln\left(1 + \frac{\Delta I}{I}\right)\right), \tag{20}$$

with

$$\sigma^2(\Delta V_{T0,1-2}) = \frac{2A_{V_{Tn}}}{W_1 L_1}, \tag{21}$$

$$\sigma^2(V_{B2}) = A_{V_{Tn}}\left[\frac{1}{W_5 L_5} + \left(\frac{n_5}{n_6}\right)^2 \frac{1}{W_6 L_6}\right]. \tag{22}$$

The random variable $X = \left(1 + \frac{\Delta I}{I}\right)$ has a normal distribution with an expected value of one and a variance $\sigma^2_{\Delta I/I}$ given by [41]. The third term in (20) can thus be obtained as the variance of a log-normal distribution expressed as

$$\sigma^2\left(\ln\left(X\right)\right) = \left[\exp\left(\sigma^2_{\Delta I/I}\right) - 1\right]\exp\left(2 + \sigma^2_{\Delta I/I}\right), \tag{23}$$

using the common expression linking $\sigma^2\left(\ln\left(X\right)\right)$ to the parameters of the normal distribution X, and simplifies to

$$\sigma^2\left(\ln\left(X\right)\right) \approx \sigma^2_{\Delta I/I}\exp(2) \tag{24}$$

as $\sigma^2_{\Delta I/I} \ll 1$.

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