Characterization of heat transfer in 3D CMOS structures using Sideband Scanning Thermal Wave Microscopy

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Abstract

Efficient thermal management is critical for cryogenic CMOS circuits, where local heating can compromise device performance and qubit coherence. Understanding heat flow at the nanoscale in these multilayer architectures requires localized, high-resolution thermal probing techniques capable of accessing buried structures.

Here, we introduce a sideband thermal wave detection scheme for Scanning Thermal Microscopy, S-STWM, to probe deeply buried heater structures within CMOS dies. By extracting the phase of propagating thermal waves, this method provides spatially resolved insight into heat dissipation pathways through complex multilayer structures. Our approach enables quantitative evaluation of thermal management strategies, informs the design of cryo-CMOS circuits, and establishes a foundation for *in situ* thermal characterization under cryogenic operating conditions.

1 Introduction

Quantum computers hold the promise of solving computational problems intractable for classical computers. Recent advancements have pushed the number of physical qubits in a single system beyond the one-thousand mark [1] but have also highlighted significant challenges in scalability, integration, and thermal management. In particular, connecting each qubit to room-temperature equipment via individual cables would result in thermal loads and space requirements exceeding the capacity of current commercially available dilution refrigerators

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— the so-called I/O bottleneck of quantum computing. A promising approach to mitigate this issue is to position certain measurement and control electronics at cryogenic temperatures (e.g. cryo-CMOS) in close proximity to the qubits such that the I/O count of cabling up to higher-temperature stages is greatly reduced [2, 3, 4, 5].

However, this proximity necessitates the development of efficient thermal management solutions with minimal spatial footprint as operating cryo-CMOS circuits within dilution refrigerators can lead to significantly elevated temperatures relative to their ultra-cold surroundings [6, 7, 8]. These temperature gradients induced on thermally coupled systems result in reduced coherence times for neighbouring qubits [9]. Addressing this issue will demand the development of advanced packaging and integration strategies along with thermally aware design and layout of cryo-CMOS circuits, potentially even allowing for co-integration of CMOS circuitry on the same chip as the physical qubits. Knowledge of deep-cryogenic material properties, especially in the sub-4 K temperature range, is extremely limited. Even if some bulk properties of relevant materials are known for the temperature range of interest, commercial CMOS foundries often do not fully reveal all materials, thicknesses, and semiconductor doping concentrations used in their process to their customers or Process Design Kit (PDK) users. Therefore, the effective thermal properties of cryo-CMOS integrated circuits must be determined empirically.

To enable this *in situ* cryogenic thermal characterization of CMOS technologies and devices at their base operating temperatures, further development of cryo-capable, localized characterization tools is necessary [10]. While integrated on-chip heater and thermometer devices in the front-end-of-line (FEOL) allow for characterization of local device self-heating and intra-chip inter-device heating [7], the back-end-of-line (BEOL) remains largely uncharacterized for deep-cryogenic conditions and presents an increasingly important aspect as dense packaging and 2.5D/3D integration become required to achieve quantum systems of larger scale. In particular, the thermal pathways between chip surface metal (e.g. pads, bumps) and buried devices must be characterized [11]. The thermal behaviors of these pathways are challenging to predict due to a complex multi-layer structure consisting of thermal conductivities with cubic temperature relationships (e.g. Si [12], amorphous SiO_2 [13], and Si-Cu boundaries [14]) and linear temperature relationships (e.g. metals such as Cu and Al [15]). Extreme power densities [16] and generally much lower thermal conductivities compared to room temperature [12] act to generate self heating in transistors which can exceed 90 K at a 6.5 K base temperature [17] and consequently induce massive on-chip temperature gradients [18]. Added dimensional effects (e.g. when the silicon dimension approaches the phonon mean free path length [19]) compound this challenge, as BEOL structures can span from nanometer- to millimeter-scale.

Characterizing and modeling these thermal pathways will facilitate the evaluation and optimization of traditional thermal management strategies such as deep thermal through-silicon vias (TSV) [20] and BEOL heat sinks [21] for the cryogenic environment. This will also enable more sophisticated design and development of cryo-specific thermal management approaches, e.g. making use of superconducting interconnects [22].

Among the most promising techniques for enabling this characterization is Scanning Thermal Microscopy (SThM) due to its versatility, compatibility with rough surfaces, ability to measure thermal conductivities, and potential for operation at cryogenic temperatures [10, 23, 24]. SThM is a variant of contact-mode Atomic Force Microscopy (AFM) in which a temperature-sensing element is integrated at the apex of the AFM probe. A feedback mechanism – such as laser reflection on a photodiode or phase modulation of a tuning fork – is used to control the force applied by the cantilever during scanning. As the probe is scanned over the sample surface, minute changes in the resistance of the integrated thermometer provide spatially resolved information on thermal conductance and/or local temperature. This technique enables researchers to investigate nanoscale heating and heat diffusion phenomena. As a result, SThM has been widely employed to study hot spots in active devices [25, 26, 27, 28, 29, 30], as well as to analyze device failure mechanisms [31, 32, 33]. However, accurately probing surface heating from deeply buried heater structures in a CMOS chip poses an experimental challenge that extends beyond simply maximizing the sensitivity of the measurement scheme.

In this work, we address this challenge by introducing a sideband thermal wave detection scheme for SThM (see Figure 1). This approach builds on previously developed AC-SThM techniques for quantitative surface thermometry, which mitigate the influence of local variations in thermal contact resistance between probe and sample [34, 35]. By detecting sidebands, we gain access to the phase information of the propagating thermal wave. This phase response encodes the out-of-equilibrium thermal dynamics within the sample. Such knowledge is essential for understanding heat dissipation pathways in complex device architectures and for guiding the design of next-generation low-power electronic technologies.

2 Methodology and Sample Description

In our Sideband Scanning Thermal Wave microscopy (S-STWM), an on-sample heating element is modulated at a low frequency $f_{\mathrm{mod}} = 1$ kHz while the SThM probe is monitored at a higher carrier frequency $f_{\mathrm{car}} = 91$ kHz. The on-sample heater thus induces a low-frequency variation in the surface temperature, which in turn amplitude-modulates the high-frequency signal detected by the probe, as illustrated in Fig. 1a. This mixing process produces sidebands that encode the local temperature oscillations induced by the heating element. The amplitude of the resulting sideband signal is proportional to the local temperature oscillations while the phase is linked to the propagation time of the heat wave from the heating element to the SThM probe's sensor.

In prior work [35], tandem demodulation was used to obtain amplitude and phase of such temperature oscillations, where the f_{car} signal is demodulated at f_{mod}. While effective, this approach has two drawbacks: (i) if the first-stage bandwidth is narrower than f_{mod}, the modulation signal may be attenuated or lost, especially given the long integration times typical for thermal signals; (ii) the recovered amplitude depends on the relative phase of the two demodulators, requiring additional post-processing to obtain the true sideband amplitude.

To overcome the limitations of tandem demodulation, we implement a parallel synchronized demodulation scheme. In this approach, the raw signal is simultaneously fed into three phase-locked demodulators operating at f_{car}, $f_{\mathrm{car}} - f_{\mathrm{mod}}$, and $f_{\mathrm{car}} + f_{\mathrm{mod}}$. Phase locking ensures immunity to phase-dependent artifacts that arise in successive demodulation stages. Moreover, because demodulation occurs in parallel, the method is not limited by the bandwidth of low-pass filters, which typically constrain thermal imaging [36, 37]. As a result, sideband SThM enables faster acquisition of low-frequency thermal signals with enhanced signal-to-noise ratio (SNR). Importantly, this approach is broadly applicable to samples containing active heat sources, whether located at the surface or deeply buried.

Furthermore, the phase of the detected thermal signal reveals the time delay associated with heat propagation from the active device to the SThM probe as illustrated at Fig. 1b. Applied to buried structures, this phase-based approach is known as Scanning Thermal Wave Microscopy (STWM) [38], which enables non-invasive thermal characterization of the environment surrounding self-heating devices embedded deep within a circuit. The measured phase lag can be converted into an apparent heat-wave velocity, determined by the material's thermal diffusivity α, the geometry, and the presence of thermal interfaces along the propagation path, as illustrated at Fig. 1b. This provides valuable insight into heat transport mechanisms in complex commercial device architectures. More details about the equipment and experimental parameters can be found in Supplementary Information 1.

In this work, the enhanced SNR and increased scanning speed enabled by the sideband SThM technique were leveraged to image surface heating and heat propagation due to a deeply buried heater device in the GlobalFoundries 22-nm FDSOI process. The buried heater device used in this work was a diode-triggered silicon-controlled rectifier (DTSCR) operated in the forward blocking mode such that the effective heating element was a string of 3 vertical silicon diodes connected in series as shown in Fig. 2a. The pad noted in Fig. 2a is located outside the visible window of Fig. 3a, and the electrical connection to the DTSCR is made through routing on buried metal layers.

Careful excitation is required to heat the diode string without triggering the SCR or causing avalanche breakdown. For this purpose, a unipolar sinusoidal signal (0–3 V) was applied, with its maximum set between the diode string's turn-on voltage and the SCR breakover voltage (Fig. 2b). This turn-on voltage was confirmed using the diode's self-heating at Supplementary Information 2.

The unipolar sinusoidal excitation of a purely resistive Ohmic element gives rise to a thermal response comprising a DC component, as well as first and second harmonics. Additional harmonics result from the non-Ohmic resistance of the diode string as shown in Fig. 2c and d, but these additional higher-order harmonics are non-dominant due to their smaller magnitude and the material attenuation of high-frequency components and are therefore ignored in this analysis. Since the resistance of the SThM probe is monitored at f_{car}, this thermal modulation results in four major amplitude-modulated sidebands, appearing at frequency offsets of $\pm f_{\mathrm{mod}}$ and $\pm 2f_{\mathrm{mod}}$ from the carrier frequency f_{car}. The demodulated signal at f_{car} reflects changes in the DC temperature component of the surface. More details about the model can be found in Supplementary Information 3.

Fig. 3a presents an optical micrograph of the sample. The surface is predominantly covered by an insulating passivation layer, with the exception of the large Al pads, which remain unpassivated except for a narrow band bordering their perimeters. The measured topography at the boundary between passivated and unpassivated regions of the pads reveals the passivation layer thickness to be apx. 1 µm. The region between the Al pads is fully passivated and contains smaller, floating square metallic islands, also formed from the same Al top metal layer (apx. 3 µm thick based on measured surface height differential at pad/island edges). The DTSCR (highlighted by the blue rectangle) is buried at a depth of at least 6.9 µm below the passivation layer where there is no Al top metal [39]. The region between the Al/passivation top layers and the DTSCR consists of several layers of copper routing and insulating dielectric material (see Supporting Information 4 for more information). Owing to the mirror symmetry of the device, only half of the region above the DTSCR was scanned. This approach is advantageous given the limited scanning window of the SThM system, indicated by the green rectangle in Fig. 3a.

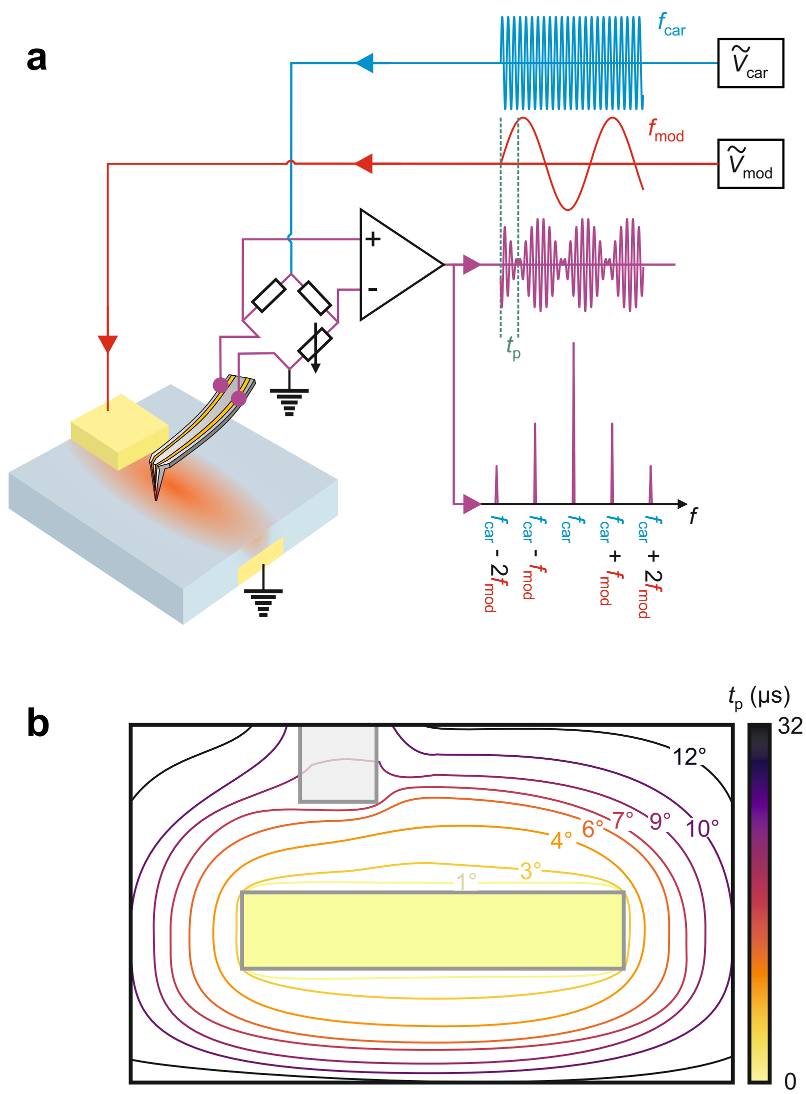

Figure 1: **a** Schematic of the sideband-SThM setup used in this work. A high-frequency carrier signal f_{car} probes the resistance of the thermometer embedded in a Wheatstone bridge, while a low-frequency excitation f_{mod} is applied to a heater buried beneath the sample surface. The resulting SThM signal at the Wheatstone bridge is an amplitude-modulated f_{car}, which can be demodulated to extract the sideband signals. Input and output signals are shown schematically and are not to scale. **b** Isophase curves for the heat waves propagating around a buried heating element. Another material with a different thermal diffusivity is shown in grey. The added colorbar shows the conversion from phase to propagation time of the heat wave. Color scale indicates the conversion to a propagation time.

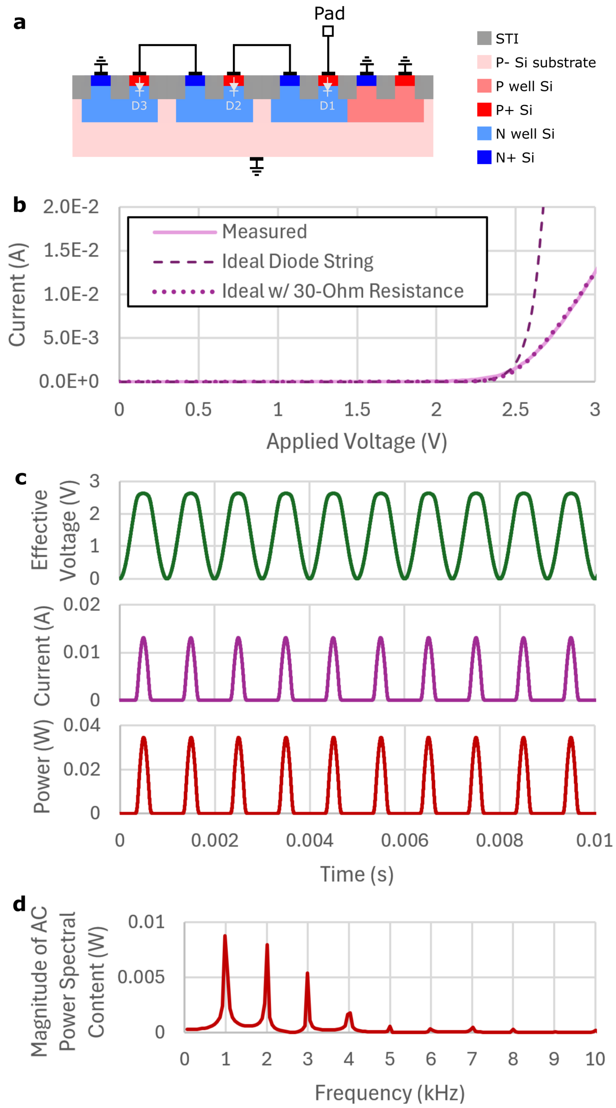

Figure 2: **a** Simplified cross-sectional diagram of buried DTSCR heater structure (not to scale) showing diodes D1, D2, and D3. **b** Measured DC I-V response of the diode string, which can be modeled as an ideal diode string with 30 Ω inline series resistance (reducing the effective voltage across the diode string at high bias compared to the sourced voltage). **c** Modeled transient waveforms for effective voltage, current, and dissipated power at the diode string. **d** Resulting modeled spectral content of power dissipation in the diode string. The fundamental frequency and 2nd harmonic are dominant, though the 3rd harmonic is also significant.

3 Results and Analysis

Fig. 3b presents the relative AFM topography of this region, while Fig. 3c displays the corresponding DC response of the SThM probe. The strongest DC temperature response is

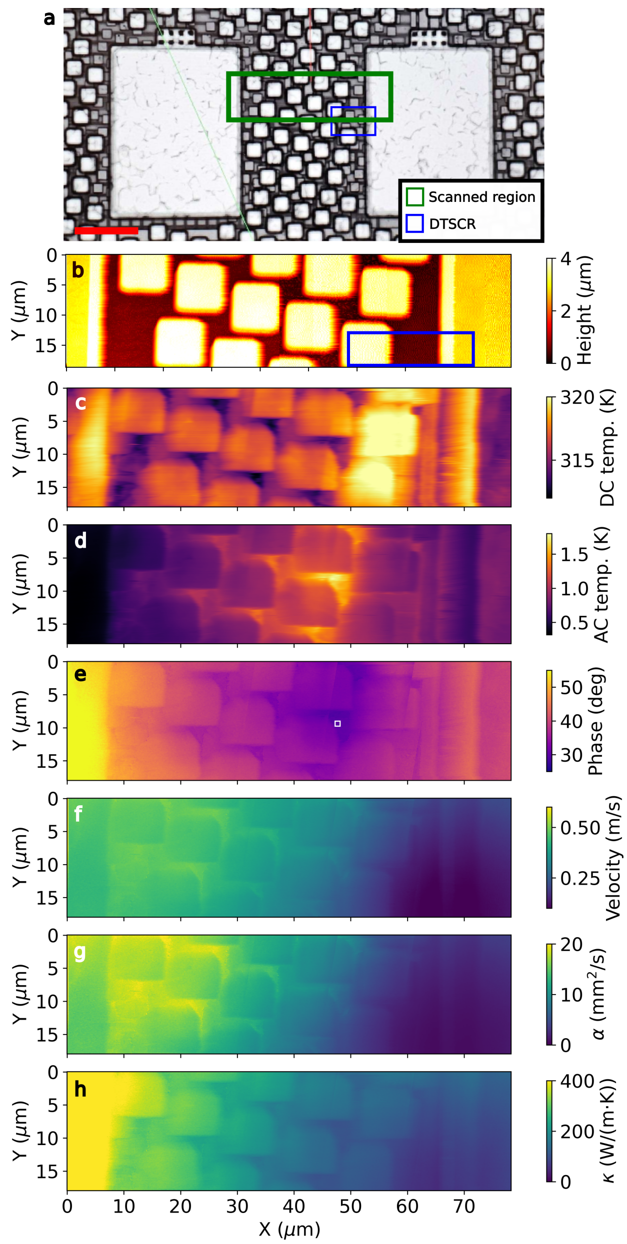

Figure 3: **a** Grayscale optical micrograph of the region of interest with the scan window indicated by the green rectangle. The buried DTSCR heater is indicated by the blue rectangle. Red scale bar: 30 um. **b** Relative topography of the region. **c** Apparent DC temperature map. **d** Calibrated AC temperature obtained via the sideband detection. **e** Relative surface phase lag of the heat wave, obtained through the sideband detection, with the white square indicating the reference region used for the conversion of phase to heat wave velocity. **f** Effective heat wave velocity. **g** Effective thermal diffusivity. **h** Effective thermal conductivity.

observed in and around the region above the DTSCR. The enhanced signal over the floating metal islands relative to the inter-island areas is likely influenced by a combination of thermal contact variations and topographic artifacts that cannot be fully disentangled from the DC response. In contrast, the reduced response on the unpassivated metal pads can be attributed to their large area and high thermal conductance, which facilitate efficient heat dissipation. To obtain the AC temperature map, a calibration procedure is required to extract the tip-sample contact resistance. This is done by leveraging the relation ship between the DC and AC thermal mapping, also known as dual scan SThM. As the diode is intrinsically highly non-linear, we proceed as Harnack *et al.* to obtain the AC temperature map while extracting the contact resistance. From the DTSCR's power density measured at Fig. 2d the $\beta_{1\omega}$ factor can be estimated. As in [40], by assuming that the temperature difference depend linearly on the device self-heating power, the $\beta_{1\omega}$ factor can thus be written as the ratio of the dissipated power in DC and at the first harmonic, obtained from Fig. 2. this holds true as long as the thermal system can be assumed to respond similarly in DC and at the first harmonic.

$$\beta_{1\omega} \;=\; \frac{\Delta T_{\mathrm{AC},1\omega}}{\Delta T_{\mathrm{DC}}} \;\approx\; \frac{P_{\mathrm{dev,AC},1\omega}}{P_{\mathrm{dev,DC}}} \;=\; 0.911 \tag{1}$$

The AC temperature map can thus be obtained using this reformulation, based on [40].

$$\Delta T_{AC,1\omega} \;=\; \Delta T_{\mathrm{sens0}} \frac{\beta_{1\omega}\Delta V_{\mathrm{AC},1\omega}}{\Delta V_{\mathrm{AC},1\omega} - \beta_{1\omega}\Delta V_{\mathrm{DC}}} \tag{2}$$

Using this calibration, the AC temperature map is obtained and amplitude- and offset-dependent studies of the thermal response to DTSCR heating are provided in Figures S1 and S2. From the data in Fig. S1, the sensitivity of the method is estimated to be 254 $\mu\mathrm{K}/\sqrt{\mathrm{Hz}}$.

The AC temperature map shows a reduced response above the DTSCR, with the strongest signal near the center of the scan window. This behavior can be attributed to the signal routing: AC heat transfer is most effective in highly conductive, low–specific-heat materials such as metals. As shown in Fig. 4, the signal-routing metal passes close to the chip surface at the scan center, whereas directly above the DTSCR the thick dielectric layer strongly damps the AC component before it reaches the surface. The ground routing above the DTSCR likely contributes further by connecting to a large chip-spanning metal volume with very high thermal capacitance, thereby masking the local AC response. These findings indicate that insulator and/or ground-metal regions can effectively shield temperature-sensitive components from AC fluctuations. Additional measurements on purpose-designed structures will be required to directly quantify this effect for different geometries and frequencies. To avoid artifacts from heat dissipation in the routing itself, the resistance of the routing should be minimized, as implemented here by using large cross-sections (see Fig. 4).

In the following, we investigate thermal-wave propagation in these devices using our S-STWM approach. Fig. 3e shows the phase lag between the DTSCR driving signal and the SThM response. The central region of the scan window exhibits both the largest AC heat-wave amplitude and the fastest propagation to the chip surface—exceeding even the region directly above the DTSCR. This behavior arises from the higher heat-wave velocity in the metal routing compared to the surrounding dielectric. The small region marked by a white square in Fig. 3e was selected for analysis across DTSCR excitation frequencies to enable phase calibration and extraction of effective material properties such as thermal diffusivity α and conductivity κ.

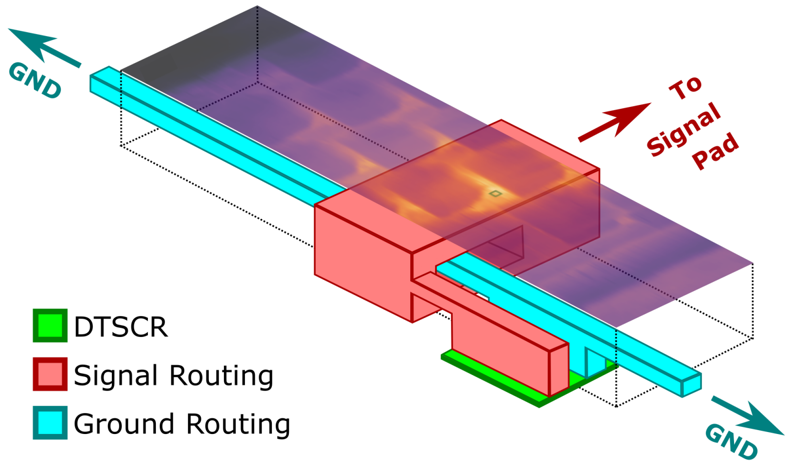

Figure 4: Representative 3D routing scheme for DTSCR signal and ground connections (not to scale). The routing regions indicated include both metal routing layers and vias. Metal-island fill and other routing unrelated to the DTSCR are not shown. A partially-transparent copy of Figure 3d is overlaid to demonstrate the maximum AC heating directly above the near-surface signal routing.

This region's frequency-dependent amplitude and phase responses are shown in Fig. 5a. The theoretical temperature oscillations $T_{\mathrm{ac}}(x, f)$ at a distance x from a heat source with excitation frequency f in a semi-infinite solid are described by [41, 42, 38]:

$$|T_{\mathrm{ac}}(x,f)| = \frac{Q_{\mathrm{o}}}{2\kappa}\sqrt{\frac{\alpha}{2\pi f}}\mathrm{e}^{-x/\mu(f)} = \frac{Q_{\mathrm{o}}}{2\kappa}\sqrt{\frac{\alpha}{2\pi f}}\mathrm{e}^{-x\sqrt{\frac{\pi f}{\alpha}}} \tag{3}$$

$$\phi(x,f) = \frac{2\pi x}{\lambda(f)} = x\sqrt{\frac{\pi f}{\alpha}} \tag{4}$$

where Q_0 is the surface heat flux leaving the heat source; κ is the effective thermal conductivity; $\mu(f) = \sqrt{\alpha/\pi f}$ is the penetration depth of the thermal wave; $\phi(x, f)$ is the phase delay in radians of the thermal wave at distance x from the heat source; and $\lambda(f) = 2\sqrt{\pi\alpha/f}$ is the effective wavelength of the thermal wave. Analysis of the amplitude data is complicated by its dependency on multiple unknown properties, i.e. α and κ. Additionally, as f approaches zero, the theoretical amplitude would approach infinity, making Eqn. 3 invalid for low frequencies. Phase analysis is more straightforward, relying on fewer assumptions and having only α as an unknown dependency. This allows for direct extraction of effective diffusivity from phase data and the known distance x from the DTSCR.

Before processing the phase data, an offset calibration is applied to the raw measured relative phase data such that the phase approaches zero as frequency approaches zero to ensure accurate representation of the physical absolute phase delay. At 1 kHz, the corrected phase delay at this reference region is 28.38°. The 1 kHz phase map in Fig. 3e has the same offset

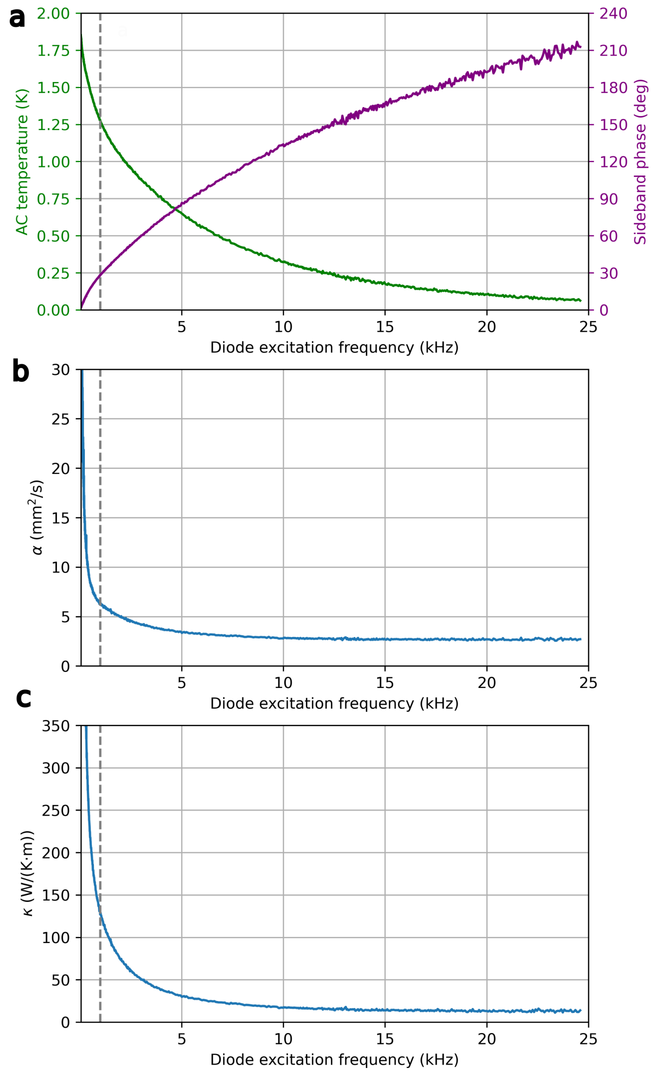

Figure 5: Measured and extracted thermal characteristics at the reference region as a function of the DTSCR's excitation frequency. The excitation is unipolar and its peak-to-peak amplitude is 3 V. The dashed lines highlight the 1 kHz frequency. **a** Measured amplitude and phase of the first sideband signal. **b** Extracted effective thermal diffusivity. **c** Extracted effective thermal conductivity.

applied and is thus an accurate representation of absolute phase delay across the entire region. Since the distance between the contact point and the sensing element is typically below 0.1 µm, any phase delay occurring within the probe can be neglected [43]. To further validate the measured phase, we performed amplitude-dependent SThM traces above the DTSCR heater. The results, presented in Supplementary Information E, show that the lag of the heat waves, represented by the phase signal of the first and second harmonic sidebands, does not depend on the power dissipated at the DTSCR, as expected. This confirms that the observed phase delays are dominated by the propagation of heatwaves.

The distance x is calculated as the approximate straight-line distance in 3D space from the center of the DTSCR heater. The vertical component of distance is determined by applying an offset to the measured topography in Fig. 3b such that the vertical distance is 7.9 µm in the region directly above the center of the DTSCR where there is no Al top metal, based on the 6.9 µm copper metal stackup [39] plus the measured 1 µm passivation thickness. For example, the calculated distance at the small reference region is apx. 22 µm. This value likely represents a slight underestimate, as it does not include the thickness of the dielectric layer directly above the top Cu layer (and directly below the Al top metal layer where present). Additional uncertainties arise from the simplified distance calculation due to the distributed and non-uniform nature of the DTSCR heating and the complex geometry of metals and insulators, which may result in non-straight-line dominant conduction paths. Nonetheless, this approach provides a useful approximation of distance for analysis purposes. For example, the effective heat wave velocity can be mapped as shown in Fig. 3f, where for each point the distance is divided by the propagation time corresponding to the phase delay at that point. The extracted effective diffusivity is plotted across frequency for the reference region in Fig. 5b, showing a decrease in α with increasing frequency. Frequency-dependent diffusivity is commonly reported for heterogeneous structures, as parallel thermal pathways are likely to have different thermal wave cut-off frequencies [44, 45]. The effective diffusivity α at $f = 1$ kHz can also be mapped across the scan window as shown in Fig. 3g. Extracted α values range from $1 \times 5^{-6} - 2 \times 10^{-5}$ $\mathrm{m^2\,s^{-1}}$, with greater effective diffusivity observed on the left side of the window where a greater portion of the heat transfer pathway to the surface is formed of the signal routing metal. For comparison, typical values are $\alpha \approx 7 \times 10^{-7}$ $\mathrm{m^2\,s^{-1}}$ for SiO_2 and $\alpha \approx (2 \times 10^{-5} - 1 \times 10^{-4})$ $\mathrm{m^2\,s^{-1}}$ for thin-film Cu [46, 47]. Other on-chip metals and insulators may exhibit significant variation, but extracted α values between those of SiO_2 and Cu are consistent with thermal paths comprising both materials [48, 47]. Furthermore, thermal boundary resistance at metal–insulator and insulator–insulator interfaces may also contribute to the effective value of α [49]. The range of α values extracted demonstrates strong dependence on routing geometry and frequency, with insulator-dominated heat flow in some conditions and metal-dominated heat flow in others.

With α having been extracted from phase data, the only remaining unknown in Eqn. 3 is κ, assuming Q_{o} can be adequately estimated. The DTSCR power is taken to be 8.75 mW from the model of first-harmonic power in Fig. 2d and is assumed constant over frequency. The DTSCR is approximated as a 2D object, and thus its surface area is given by 2 times the area of the region it occupies (see Supplementary Information 4) for a total of $\sim 500\,\mu\mathrm{m}^2$. This yields $Q_{\mathrm{o}} \approx 1.7 \times 10^7$ $\mathrm{W/m^2}$. Based on this estimate, Eqn. 3 is used to extract κ across frequency for the reference region as shown in Fig. 5c. At the lowest frequencies, the κ values extracted appear too high to be physical, exceeding even the conductivity of Cu, which has $\kappa \approx 109{-}350+$ W/(m·K) at room temperature depending on film thickness [47]. This can likely be attributed to the lack of validity of Eqn. 3 at low frequencies and the added contributions of thermal waves reflected off the chip's bottom surface at low frequencies (when $\mu(f)$ of the substrate material approaches or exceeds two times the thickness of the chip) which violate the assumption of semi-infinite 3D propagation. At the reference region, extracted κ at $f = 1$ kHz is 127 W/(m·K), decreasing to as low as 13 W/(m·K) with increasing frequency. This reflects well the range of conductivities between those of Cu and SiO_2, which has $\kappa \approx 1.1$ W/(m·K) at room temperature [50]. While some overestimation of κ is inherent to the application of this methodology at lower frequencies, decreasing κ with increasing frequency is commonly reported for heterogeneous systems and can be attributed to local nonequilibrium effects and reduced penetration depth at higher frequencies leading to the exclusion of contributions from phonons with larger mean free paths [51, 44].

The extracted conductivity κ at $f = 1$ kHz is mapped across the scan window in Fig. 3h, though extracted values at this frequency may be overestimations. Additionally, Eqn. 3 becomes a worse approximation at greater horizontal distance from the DTSCR, as the solid-air boundary at the chip top surface causes increased deviation in thermal wave propagation compared to the assumed semi-infinite 3D propagation. Higher uncertainty, and therefore error, in extracted κ is also expected in regions of low detected amplitude of temperature oscillations, such as the far left pad region. However, two clear patterns emerge: higher effective κ in regions above the Al top metal islands compared to their surrounding regions, and higher effective κ moving toward the left side of the imaged region. Both of these patterns reflect the higher relative metal content in these regions' paths from the DTSCR, aligning well with expectations.

If the effective mass density ρ of the BEOL material could be reasonably estimated, an estimate of the effective specific heat capacity $c_{\mathrm{p}} = \kappa/\alpha\rho$ could be derived as well. A flowchart of the full procedure of thermal material property extraction is shown in Fig. 6. This highlights that as the extraction moves from α to κ to c_{p}, additional error sources are added at each step, whether from measurement uncertainty, estimations of *a priori* information, or invalid model assumptions. Extraction of c_{p} is not carried out in this work since the complexity of the structure does not allow for a good estimation of effective ρ, but future studies of purpose-designed regions of simpler BEOL composition above a buried heater element may allow for good ρ estimation and useful extraction of effective c_{p}. Measuring several variants of such structures, especially across a range of cryogenic ambient temperatures, could then allow for extraction of individual contributions of different BEOL layers/boundaries and estimates of their independent effective material properties. This would then enable predictive 3D finite element analysis (FEA) simulation capabilities, including transient effects up to the characterized frequency range.

4 Conclusion

Realizing the full potential of quantum computing requires seamless integration of qubit architectures with cryogenic electronics, which in turn demands a detailed understanding of heat propagation within complex 3D circuit structures. Here, we present a novel implementation of AC-Scanning Thermal Microscopy combined with thermal wave analysis and sideband detection, S-STWM, to non-invasively characterize the thermal properties of materials and pathways in the BEOL of a CMOS integrated circuit, spanning from the chip surface to active devices buried within multilayer structures. Our approach provides valuable insight into heat transport in structures where interfacial effects dominate, revealing details that are otherwise

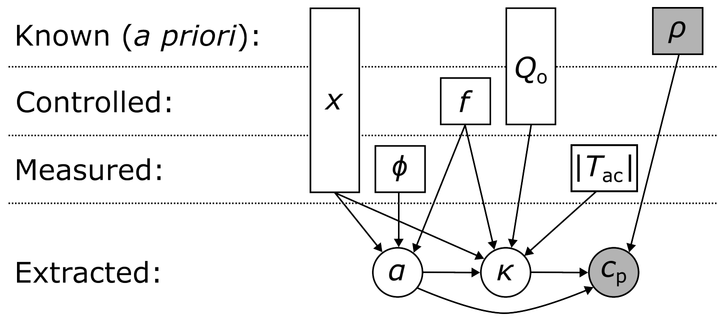

Figure 6: Flowchart of effective thermal material property extraction procedure enabled by S-STWM. Extraction of c_p is not demonstrated in this work.

inaccessible with conventional methods.

While the measurements reported here were performed at room temperature, they establish a foundation for equivalent studies at cryogenic conditions [10], directly relevant to the operating environment of cryo-CMOS devices. Beyond cryo-electronics applications, the rapid development and adoption of ultra-high-power-density CMOS CPUs and GPUs for high-performance compute (HPC) applications presents an additional possible use case for this methodology [52, 53] to augment thermal characterization capabilities of such devices and enable improved thermally-aware design and packaging.

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Author Contributions

V. Fonck and M. Razeghi acquired the data. V. Fonck, M. Razeghi, G. Ridgard, G. M. Noah, and P. Gehring analyzed the data. G. M. Noah and P. Gehring packaged the chip. V. Fonck, G. Ridgard, G. M. Noah, and P. Gehring conceived the experiments. V. Fonck and G. M. Noah conceived the effective thermal material property extraction procedure. P. Dobson and J. Weaver fabricated the SThM probes. G. M. Noah and P. Gehring supervised the work. All authors contributed to the writing of this article.

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