Radiation Degradation and Mitigation of an Ultrathin SOI SPAD Using a Perimeter Gate

Tom Klauner, Nicolas Roisin, Ottilie Bonfanti, Iman Sabri Alirezaei, Nicolas André, *Member, IEEE*, and Denis Flandre, *Senior Member, IEEE*

***Abstract*— This work investigates the robustness of an ultrathin backside-illuminated (BSI) silicon-on-insulator (SOI) single-photon avalanche diode (SPAD) against gamma-ray irradiation for space applications. Experimental results demonstrate a breakdown voltage shift in the studied SPAD from 10.17 to 9.95 V after a total ionizing dose (TID) of 132 krad(Si). An increase in dark count rate (DCR) from 1490 to 2700 cps/μm^2 at 1 V excess bias is shown at this dose. TCAD simulations explain the role of the oxide-trapped charges, induced by irradiation in the insulating layer surrounding the active region, on the SPAD performance. These trapped charges shift the peak electric field, leading to premature breakdown while the extension of the active area affected by impact ionization increases the DCR. Further simulations show that implementing a perimeter-gated structure and reducing oxide thickness can effectively mitigate these effects by leveraging capacitive effects, preventing a breakdown voltage shift. The perimeter gate (PG) lowers the simulated DCR after irradiation from 2700 to 1365 cps/μm^2, thereby enhancing the radiation resilience of ultrathin SOI SPADs beyond a TID of 132 krad(Si).**

***Index Terms*— Breakdown, dark count rate (DCR), mitigation technique, rad-hard, single-photon avalanche diode (SPAD), TCAD.**

I. Introduction

SINGLE-PHOTON avalanche diodes (SPADs) [1] have garnered a significant interest across a variety of fields, including space applications targeting near-ultraviolet (near-UV) and blue detection such as Raman spectroscopy (475 nm) [2], cosmic-ray detector (425 nm) [3], or gamma-ray telescope (400 nm) [4]. These applications expose the device to ionizing particles, such as X-rays, gamma rays, neutrons, and heavy or light ions that progressively degrade the performance of the photodetector [5]. In recent years, numerous studies have investigated these degradation effects on SPADs [5], [6], [7] or on silicon photomultipliers (SiPMs) [8], [9] and have assessed their radiation-hardness capabilities [6], [10], [11], [12].

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Tom Klauner, Nicolas Roisin, Ottilie Bonfanti, Nicolas André, and Denis Flandre are with ICTEAM, Université catholique de Louvain, 1348 Louvain-la-Neuve, Belgium (e-mail: tom.klauner@uclouvain.be).

Iman Sabri Alirezaei is with TE Connectivity, 12459 Berlin, Germany (e-mail: iman.sabri@te.com).

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Irradiation can induce defects either in the silicon bulk due to displacement damage or in the dielectric insulators due to ionizing degradation [13]. These defects can both contribute to an increase in leakage current [5], [6] or dark count rate (DCR) [6], [11], [12]. Focusing on the ionizing effects, device performance is primarily degraded through two mechanisms: the accumulation of positive trapped charges in the oxide layer and the formation of traps at the Si/SiO_2 interface. The impact of total ionizing dose (TID)-induced defects on the electric field density, the breakdown voltage, and premature breakdown have yet to be thoroughly investigated in SPADs with an ultrathin silicon body on silicon-on-insulator (SOI).

The development of backside-illuminated (BSI) SPADs is closely related to advancements in 3-D stacked SPAD technology [14]. The latter allows SPADs to be connected directly to their associated circuitry, enabling independent optimization of each layer and high fill factors. 3-D integration of frontside-illuminated (FSI) bulk SPADs is challenging as it requires complex postprocessing steps, such as the formation of through-silicon vias (TSVs) to connect photodiodes with their corresponding electronics [14]. BSI SPADs address this issue by enabling a direct, face-to-face connection with a maximum fill factor. However, to be optimized for UV and blue light detection, BSI SPADs face the challenge of minimizing the diffusion region, which is the distance from the backside silicon surface to the edge of the depletion region on the front side [15]. This can be achieved using an ultrathin silicon layer, with a thickness of a few microns [14], [15], [16].

In general, the doping profile of a SPAD is designed to create a uniform high electric field at the p-n junction, ensuring efficient photon detection across the entire active area [17]. A major design challenge is to prevent premature breakdown, which arises when impact ionization occurs at the edges of the active region, degrading device performance [16], [18]. As the carrier multiplication does not occur in the desired area, the sensitivity of the device is reduced and the DCR increases. Several techniques are commonly employed to mitigate premature edge breakdown. These include the use of a shallow trench isolation (STI) guard ring [19], a retrograde deep well [20], a buried layer [21], a lightly doped guard ring [22], a virtual guard ring [22], or a perimeter gate (PG) [23]. While these methods are effective for common SPADs, they can be inadequate for ultrathin SOI SPADs under irradiation. For instance, STIs are implemented at the edges of the junction where the electric field is high to avoid premature breakdown as oxide can withstand higher electric fields compared to silicon [19]. However, STIs can become

counterproductive in irradiated environments as they place Si/SiO_2 interfaces and relatively thick oxides, where ionizing defects mostly take place, close to critical regions, potentially degrading SPAD performance [6], [11]. Retrograde wells and buried layers prevent premature breakdown by concentrating the electric field vertically [10]. However, in ultrathin designs, the restricted silicon depth makes retrograde wells and buried layers unsuitable as they create deep junctions [21], [24]. Similarly, doped and virtual guard rings reduce the electric field at the edges of the active region but the silicon depth limits their implantation and reduces their effectiveness [16]. Alternatively, premature breakdown can be mitigated without introducing additional elements into the silicon by using a PG. It locally controls the electric field at the edge of the active region through capacitive coupling with a metal plate or a polysilicon electrode placed over the top oxide layer. The PG can be either grounded [25] or biased with a separate terminal [23], [26].

This work includes both experimental measurements and TCAD simulations to assess the degradation and mitigation of gamma-ray irradiation on an ultrathin SOI SPAD. The methodology used to evaluate the performance is described in Section II. This includes both experimental measurements (I–V curve and DCR curve) and TCAD simulations (carrier densities and electric field) using Atlas [27]. Section III presents the primary effects of irradiation on SPAD characteristics degradation, i.e., premature breakdown and DCR increase. Finally, it assesses the implementation of a PG to mitigate the impact of irradiation on the studied ultrathin SOI SPAD characteristics, demonstrating improvements in radiation hardness.

II. Methodology

A. SPAD Structure

The studied structure is a BSI SPAD targeting high UV efficiency, made from a custom process from our manufacturing facility, as fully detailed in [15]. The previous run had a breakdown voltage of 8.5 V and achieved a peak photon detection probability (PDP) of 69.51 % at a wavelength of 423 nm and 16.56 % at 291 nm, with 3 V excess bias. The device is fabricated on an SOI wafer with a 650-nm-thin top silicon layer, a buried oxide (BOX) of 1 μm, and a silicon substrate below the SPAD removed by etching for BSI. Compared to the previous run, the SPAD has a square shape with rounded corners to limit the electric field concentration at the edges. Its layout is approximated by a circular TCAD structure with its center located at $x = 24$ μm (see Fig. 1). The top oxide is 570 nm thick to insulate the device from the metal pads and withstand the high electric field associated with the cathode bias. The anode (A) and cathode (K) are made of aluminum, with top lengths of 8 and 20 μm, respectively. They are connected to the active silicon layer by vias of 3-μm diameter. The SPAD uses a shallow n++/p-well junction with a highly doped p-well. The p-well is uniformly implanted on the entire silicon surface while a shallow n-well guard ring is implemented at the edges of the n++/p-well junction to avoid premature breakdown. This design has an active area of 676 μm^2 and a low breakdown voltage of about 10 V.

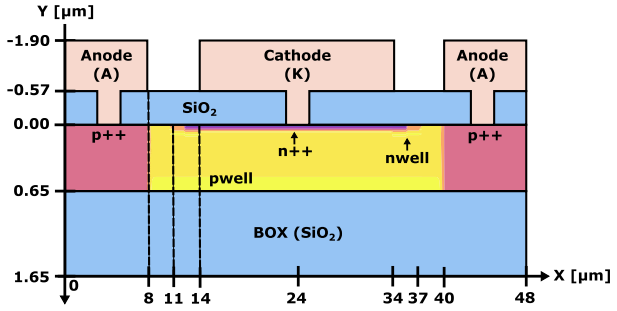

Fig. 1. 2-D cross section of the TCAD structure of the studied 650-nm-thin BSI SOI SPAD based on [15].

B. Measurement Setup and Parameter Extraction

Four samples were exposed to a cobalt-60 source at a dose rate of 520 rad(Si)/h during 254 h. They accumulate a TID of 132 krad(Si), exceeding the threshold of 100 krad(Si) typically used to ensure radiation hardness for space applications [28]. Throughout the irradiation campaign, intermediate evaluations were conducted, including extracting the dark I–V curve and the DCR versus bias voltage for 0, 12, 24, 82, 107, and 132 krad(Si). All measurements were taken within one hour between the extraction and repositioning of the devices at the radiating source to limit room-temperature annealing [29]. The I–V curve was measured on a probe station using an HP 4145B semiconductor parameter analyzer. The breakdown voltage shift is determined from the voltage V_{bd} where the current reaches 100 nA. This value is within the steep I–V region and much higher than the dark current in the 10 pA range. The DCR extraction setup is depicted in Fig. 2(a). The SPAD was passively quenched using an external resistor of 220 kΩ. The DCR measurements were obtained by probing the transient response in dark conditions at the cathode of the photodiode with a Tektronix MSO56 oscilloscope at a sampling rate of 6 GS/s. The quenched SPAD was biased at a given voltage $V_A = V_{bd} + V_{ex}$, with an excess bias (V_{ex}) ranging from 0 to 1.5 V above the breakdown voltage measured at each irradiation step. Our limit of 1.5 V is due to the difficulty of obtaining an accurate DCR measurement at a higher voltage with passive quenching because of the high number of counts. An interarrival time histogram [see Fig. 2(b)] is made from the transient response. The DCR is underestimated for short interarrival times because of the passive recharge (see Fig. 2(b), orange region) [30]. Hence, a first-order log fit is applied to account for the hidden counts (see Fig. 2(b), purple region).

C. TCAD TID Modeling

The TCAD simulations were performed using Atlas [27]. The mechanisms considered include Auger recombination, Shockley–Read–Hall (SRH) recombination and generation, concentration-dependent and field-dependent mobility, bandgap narrowing, trap-assisted tunneling (TAT), Poole–Frenkel (PF) effect, and band-to-band tunneling (BBT). Unless otherwise stated, the parameters used in the simulations are based on the default values given in [27].

Cobalt-60 gamma rays induce ionizing particles and may also create bulk damage in silicon through Compton scattering [6]. However, because of the high doping concentration of the p-well in our ultrathin SPAD, the depletion region

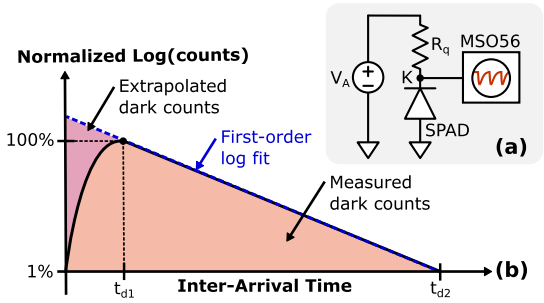

Fig. 2. (a) DCR extraction setup. The SPAD is passively quenched by an external resistor R_q and biased at a given voltage V_A. The dark counts are probed with an oscilloscope at the cathode (K) of the SPAD. (b) Schematic of the normalized interarrival time histogram used to extrapolate the DCR using a first-order log fit (blue line). The orange region corresponds to the measured dark counts, while the purple region accounts for the extrapolated dark counts. t_{d1} and t_{d2} are the interarrival times corresponding to 100% and 1% of the maximum counts, respectively.

remains thin. Hence, the impact of displacement damage on the device characteristics is expected to be limited compared to the ionizing degradation. Therefore, only ionizing effects are considered. It results in the creation of electron-hole pairs in SiO_2 layers. Some of these pairs move in the oxide by drift and diffusion mechanisms [13]. Since the mobility of the electron is much higher than that of the hole, most of the free electrons escape from the oxide, while the holes remain trapped near the Si/SiO_2 interface by hopping transport through localized states in bulk SiO_2 [31]. It forms a positively charged layer that can affect the electric field density near the interface. This layer is considered in the TCAD simulation by specifying a single and uniform positive trapped charge surface density Q_{ox} at the top and bottom Si/SiO_2 interfaces [13]. In addition, interface traps can be created due to the conversion of oxide charges near the Si/SiO_2 interface [32]. However, the build-up of these traps is a much slower process than that of oxide-trapped charges and can take 1×10^5 s before saturating [32]. Since the measurements during the experiment were taken within an hour after exposure at a sufficient dose rate [29], interface traps may not contribute significantly to the observed degradation of the device. Still, these were implemented in the TCAD simulations following the approach described in [13]. They were found to primarily impact the dark current by introducing a surface leakage current, without affecting the breakdown voltage or having a significant impact on the DCR. As their effects do not influence the studied figures of merit, interface traps will not be considered in the remaining part of this work.

D. TCAD DCR Extraction

The simulated DCR extraction is based on the methodology described in [18]. The total DCR is associated with two main contributions: BBT and SRH [33]. Considering a circular-shaped SPAD with a radius R and a silicon device layer depth W, the DCR is computed as follows:

$$\mathrm{DCR} = 2\pi \int_0^R \int_0^W P_p (G_{\mathrm{BBT}} + G_{\mathrm{SRH}}) dy\, r\, dr \tag{1}$$

where P_p is the joint avalanche probability, G_{BBT} is the BBT generation rate, and G_{SRH} is the SRH generation rate, all derived from TCAD simulations. BBT is computed as follows:

$$G_{\mathrm{BBT}} = A_{\mathrm{BBT}} E^{\gamma_{\mathrm{BBT}}} \exp\left(-\frac{B_{\mathrm{BBT}}}{E}\right) \tag{2}$$

where E is the electric field and A_{BBT}, γ_{BBT}, and B_{BBT} are based on the Klassen model [33]. Specifically, B_{BBT} is fixed at the electric field strength of 23.9 MV/cm according to [34] and A_{BBT} serves as a fitting parameter. The SRH generation is enhanced by TAT and can also be influenced by the PF effect [35]. However, the impact of the PF effect on the SRH generation rate is limited compared to TAT under strong electric fields exceeding 0.7 MV/cm, as reported in [33], especially for monocrystalline silicon [35]. This has been confirmed in our TCAD simulations. As a result, the PF effect is excluded from the expression for the SRH generation rate, which is defined as follows [33]:

$$G_{\mathrm{SRH}} = -\frac{np - n_{i,\mathrm{eff}}^2}{\frac{\tau_p}{1+\Gamma_p}(n+n_1) + \frac{\tau_n}{1+\Gamma_n}(p+p_1)} \tag{3}$$

with

$$n_1 = n_{i,\mathrm{eff}} \exp\left(\frac{E_{\mathrm{trap}}}{kT}\right) \text{ and } p_1 = n_{i,\mathrm{eff}} \exp\left(-\frac{E_{\mathrm{trap}}}{kT}\right) \tag{4}$$

where n and p are the electron and hole concentrations, respectively. $n_{i,\mathrm{eff}}$ is the effective intrinsic carrier concentration which depends on the electric field through bandgap narrowing [36]. E_{trap} is the energy trap relative to the midgap energy and is used to fit the SRH generation rate. Γ_n and Γ_p are the field enhancement factors associated with TAT. They are determined by numerical integration in TCAD simulations [27]. τ_n and τ_p are the electron and hole lifetimes, related to the impurity concentration and are expressed as follows:

$$\tau_{n/p} = \frac{\tau_{0,n/p}}{1 + \frac{N}{N_{0,n/p}}} \tag{5}$$

where $\tau_{0,n/p}$ is the low carrier concentration lifetimes, $N_{0,n/p}$ is the roll-off concentrations [37], and N is the local total impurity concentration. The DCR extraction methodology is presented in Fig. 3. Joint avalanche probability, BBT, and SRH generation rates are simulated with Silvaco Atlas. Their values are extracted at each mesh point of half of the 2-D structure, which consists of about 18 000 nodes. The DCR is then numerically computed using (1) and fit to measurements by adjusting E_{trap}, A_{BBT}, and Q_{ox} for SRH, BBT, and TID contributions, respectively. All other parameters are fixed from [18] and [34] and specified in Table I.

TABLE I
SUMMARY OF PARAMETERS USED FOR TCAD DCR EXTRACTION

Model	Parameter	Electron	Hole	Unit
SRH [18]	$\tau_{0,n/p}$	1×10^{-5}	3×10^{-6}	s
	$N_{0,n/p}$	1×10^{16}	3×10^{16}	cm^{-3}
BBT [34]	γ_{BBT}	2.5		-
	B_{BBT}	23.7		MV/cm

III. RESULTS AND DISCUSSION

A. I–V and DCR Measurements

Fig. 4 presents the typical dark I–V curves near breakdown before and after irradiation to 12, 24, 82, 107, and

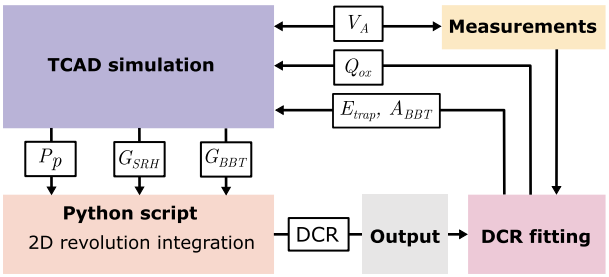

Fig. 3. Overview of the modeling and simulation method to evaluate the SPAD DCR. Joint avalanche probability (P_p), BBT generation rate (G_{BBT}), and SRH generation rate (G_{SRH}) are extracted from the TCAD structure at a given bias voltage V_A. The DCR is then numerically computed and fit to measurements using E_{trap}, A_{BBT}, and Q_{ox}. The methodology is based on [18].

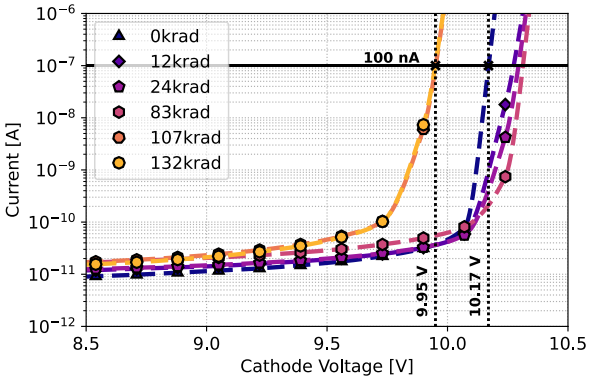

Fig. 4. Measured dark reverse-biased *I–V* curves near breakdown of the typical SPAD for several irradiation doses. Data are interpolated using cubic spline for breakdown extraction. The vertical dotted lines indicate the extracted breakdown voltages at 0 and 132 krad(Si), taken at 100 nA.

132 krad(Si). The leakage current increases progressively with the dose, likely due to the spread of the space charge region associated with Q_{ox} [29]. The current slope near breakdown also slightly decreases, probably due to the change in the current path and its resistance, caused by the modification of the electric field distribution. A notable shift in breakdown voltage occurs at 107 krad(Si), dropping from 10.17 to 9.95 V. Three of the four samples showed similar results. The fourth sample showed no shift up to this dose, possibly due to process variations. The shift is also reflected in the DCR curves shown in Fig. 5. Below 107 krad(Si), the DCR only slightly increases with irradiation. The shift to a lower breakdown voltage causes the DCR curve to move toward lower voltages, resulting in a higher DCR for a given bias voltage. For both dark current and DCR, the degradation appears to reach saturation after 107 krad(Si), probably due to saturation of oxide-trapped charges. Hence, the primary degradation in the studied SPAD performance is attributed to the decrease of breakdown voltage value, which begins above 82 krad(Si) and is likely caused by irradiation-induced premature edge breakdown.

B. TCAD Simulations

Compared to the TCAD structure from Athena simulations in [15], the experimental doping concentration of the p-well has been adjusted from the theoretical target of $5 \times 10^{17}\,\mathrm{cm}^{-3}$ to $2.7 \times 10^{17}\,\mathrm{cm}^{-3}$. It aligns the simulated breakdown voltage with the measured value at 0 krad(Si), enabling calibration of the electric field distribution within the structure [16]. The

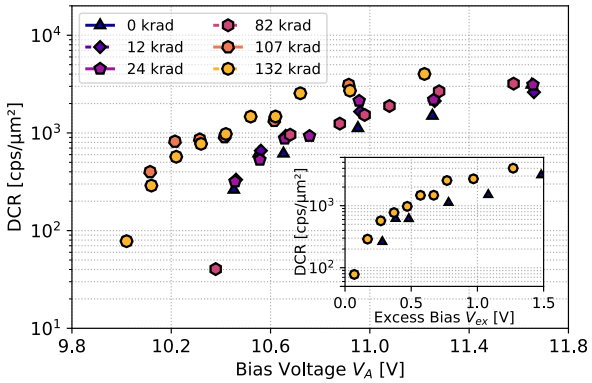

Fig. 5. Measured DCR versus bias voltage at different TID levels. At each irradiation step, the quenched SPAD is biased above the measured breakdown voltage, with an excess bias ranging from 0 to 1.5 V (inset: measured DCR versus excess bias at 0 and 132 krad). Considering the extreme DCR values, their associated interarrival times were measured at 132 krad as $t_{d1} = 17\ \mu$s and $t_{d2} = 23\ \mu$s for $V_{ex} = 0.07$ V and $t_{d1} = 0.7\ \mu$s and $t_{d2} = 2.2\ \mu$s for $V_{ex} = 1.3$ V.

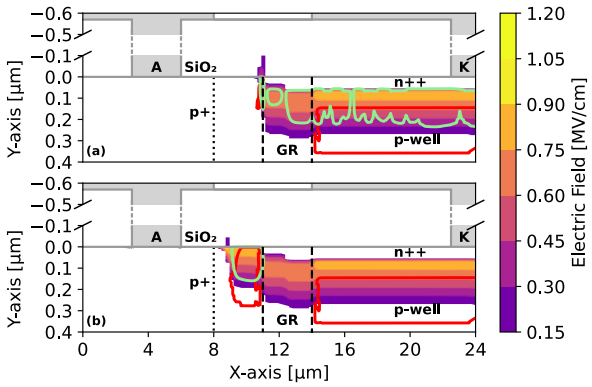

Fig. 6. Electric field in Si at a cathode voltage of 11 V, with (a) $Q_{ox} = 1.0 \times 10^{12}\ \mathrm{cm}^{-2}$ and (b) $Q_{ox} = 6.3 \times 10^{12}\ \mathrm{cm}^{-2}$. Only half of the structure is shown, with A as the anode, K as the cathode, and GR as the guard ring region. The red contour corresponds to a joint avalanche probability of 20%. The green contour encloses the region where the impact generation rate exceeds 1% of its maximum value.

difference in the experimental doping concentration can be attributed to slight changes in the manufacturing steps. The simulated electric field density at a cathode voltage of 11 V is depicted in Fig. 6(a). The peak electric field of 0.81 MV/cm is observed at the n++/p-well junction. However, an electric field of 0.8 MV/cm is also present at the edges of the guard ring. While the breakdown primarily occurs in the active area [enclosed in green in Fig. 6(a)], there is also a contribution of impact ionization at the guard ring edges due to the highly doped structure.

Fig. 7 compares the simulated DCR curves with measurements taken before irradiation and at 132 krad(Si). The initial value for the oxide-trapped charge density, $Q_{ox} = 1.0 \times 10^{12}\,\mathrm{cm}^{-2}$, is based on the typical fabrication process from our manufacturing facility [38]. The preirradiation curve is fit to the measurements by setting E_{trap} to 0.2 eV and A_{BBT} to $2 \times 10^{14}\,\mathrm{cm}^{-1/2}\mathrm{V}^{-1/5}\mathrm{s}^{-1}$ (see Fig. 7, blue curve). These parameter values correspond to typical values reported in [18] and [34]. As exposure to gamma-ray irradiation increases Q_{ox}, both postirradiated breakdown voltage and DCR curve are fit by adjusting the trapped charge density. Setting Q_{ox} to $6.3 \times 10^{12}\,\mathrm{cm}^{-2}$ shifts the simulated breakdown voltage

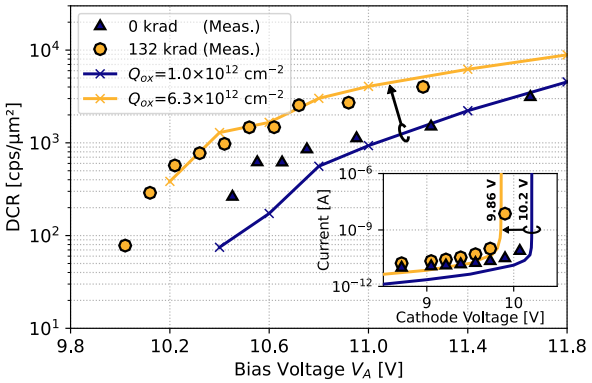

Fig. 7. DCR versus the bias voltage with fit Q_{ox}. The TCAD simulations are shown in plain lines for $Q_{ox} = 1.0 \times 10^{12}$ cm^{-2} (blue line) and $Q_{ox} = 6.3 \times 10^{12}$ cm^{-2} (yellow line). The markers indicate the measurements at 0 krad(Si) (blue) and at 132 krad(Si) (yellow) (inset: a closer view of the dark *I–V* characteristic near breakdown with their corresponding breakdown voltages extracted from the simulations).

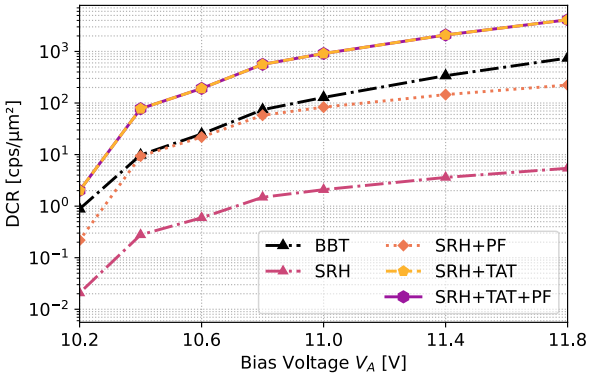

Fig. 8. Simulated DCR versus the bias voltage considering the different generation mechanisms, with $Q_{ox} = 1 \times 10^{12}$ cm^{-2}. The black curve is the BBT contribution. The colored curves show the effects of the SRH generation, successively accounting for pure thermal excitation generation (SHR curve), followed by the additional effects of PF, TAT, and their combined contribution (overlapping with the previous curve).

from 10.2 to 9.86 V (see Fig. 7, inset) and match the DCR curve with the measurements (see Fig. 7, yellow curve). This Q_{ox} value is comparable to radiation-induced oxide-trapped charges in thick oxides [39]. In both cases, the simulated DCR is dominated by SRH associated with TAT, while the contributions of BBT and the PF effect remain at least an order of magnitude lower (see Fig. 8). Increasing Q_{ox} modifies the electric field distribution, particularly enhancing the electric field up to 0.93 MV/cm near the top Si/SiO$_2$ interface in the p-well region [see Fig. 6(b)]. Bottom-trapped charges induce a slight back-depleted region but do not affect the studied characteristics. It remains almost unaffected after accounting for the irradiation-induced Q_{ox}. Therefore, this region is not shown. In contrast, the increase in top oxide-trapped charges is sufficient to modify the location of maximum impact ionization, as shown by the green contour in Fig. 6. This shift is associated with premature edge breakdown and explains the abrupt change in breakdown voltage observed at a dose of 107 krad(Si) (see Fig. 4). The change in the electric field enhances the DCR by two mechanisms. First, the DCR increases due to a lower breakdown, resulting in a higher spontaneous generation rate for a given bias voltage. Second, the area where generation can trigger an avalanche is larger

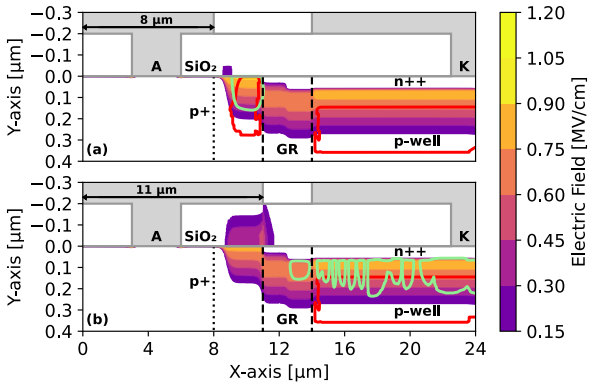

Fig. 9. Electric field distribution at a cathode voltage of 11 V, with $Q_{ox} = 6.3 \times 10^{12}$ cm^{-2} and 200-nm-thick top oxide. In red, the contour where the joint avalanche probability corresponds to 20%. In green, the contour enclosing the impact generation rate exceeding 1% of its maximum value. (a) Before and (b) after implementing the PG by extending the anode top metal length.

(see Fig. 6(b), red contour) and does not benefit the active region, increasing the DCR.

C. PG Implementation

The conventional approach of using a doped guard ring to effectively prevent premature breakdown is limited in this ultrathin structure due to the restricted depth of the top silicon layer. To increase the robustness, a PG associated with a top oxide reduction is added in TCAD simulations to mitigate the increase in Q_{ox} due to irradiation.

First, the oxide thickness is reduced from 570 to 200 nm to enhance capacitive coupling between the metal interconnects and the silicon device layer to better control the electric field at the edge of the GR region. The original thickness was primarily set for safety margins but a 200-nm-thick oxide can withstand breakdown over 100 V [40], ensuring reliable operation at voltages below 20 V. A thinner oxide also reduces the density of radiation-induced trapped charges, allowing the SPAD to withstand higher irradiation doses before experiencing premature breakdown. The length of the anode-metal junction is then increased from 8 to 11 μm, reaching the edge of the guard ring [see Fig. 9(b)]. It results in an electric field that pushes electrons from the Si/SiO$_2$ interface associated with oxide-trapped charges, as the grounded anode is negatively biased relative to the top silicon. This extension in length reduces the maximum electric field in the p-well region from 0.93 MV/cm [see Fig. 9(a)] to 0.86 MV/cm [see Fig. 9(b)]. It reduces the depletion region in the p-well near the top oxide, and suppresses the avalanche region within the p-well region (see Fig. 9, red contour) and shift back the maximum impact ionization region (see Fig. 9, green contour). The effect of the PG on the DCR curve and breakdown voltage is shown in Fig. 10. Extending the metal length from 8 to 11 μm gradually reduces the DCR as it increases the capacitive effect at the top of the p-well region, with no further improvement beyond 11 μm. Limiting the anode length to the edges of the guard ring also ensures that the FSI fill factor is maintained. The DCR curve recovers the prerad results as for $Q_{ox} = 1.0 \times 10^{12}$ cm^{-2} (see Fig. 10, dotted line), with a slightly better performance, and the SPAD restores its original breakdown voltage (see Fig. 10, inset).

TABLE II
OVERVIEW OF DCR PERFORMANCE OF IRRADIATED SPADS

Refs.	PN junction	GR structure	TID [krad(Si)]	Post/Pre-rad V_{bd} [V]	V_{ex} [V]	Post/Pre-rad DCR [cps/μm^2]
[12]	p+/n-well	virtual-GR	100[a]	31.3/31.3	3	0.086 / 0.086
[5]	n+/p+	n-well GR	130	27.5 / 27.3	3	0.0125 / 0.0075
[10]	p-well/p-epi/buried-n	p-well GR	50	25.16 / 25.15	2	0.27 / 0.18
[7]	p+/dnw	p-well GR, STI	1000[a]	21.6 / 21.6	2.8	1.42 / 0.42
[11][b]	p+/dnw	p-well GR, STI	1000[a]	21.9[b] / 21.9[b]	2.5	0.63[b] / 0.42[b]
[6]	n+/p-well	p- GR	160	18 / 18	3	22.75 / 3.75
[6]	p-well/rdnw	virtual-GR, STI	160	14 / 14	2.5	18.4 / 1.4
This work	n++/p-well	n-well GR	132	9.95 / 10.17	1	2700 / 1490
This work[b]	**n++/p-well**	**n-well GR, PG**	**132**	**10.2[b] / 10.2[b]**	**1**	**1365[b] / 1410[b]**

All measurements with gamma-ray irradiation, except [a]X-ray irradiation and [b]simulated.

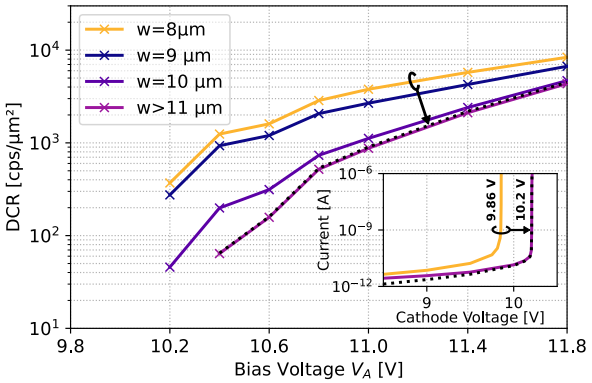

Fig. 10. TCAD simulations of DCR versus bias voltage for different anode pad lengths (w) with a top oxide thickness of 200 nm and $Q_{ox} = 6.3\times10^{12}$ cm^{-2}. The dotted line represents the simulation with an anode pad length of 11μm and $Q_{ox} = 1.0\times10^{12}$ cm^{-2} (inset: shows the shift of the breakdown voltage from 9.86 to 10.2 V in the simulated dark I–V curve with a pad length above 11 μm).

SOI SPADs are more prone to ionizing degradation compared to bulk SPADs due to the Si/SiO$_2$ interface at the bottom of the silicon layer. If the top depletion region extends close to the BOX, electron-hole pairs generated at the interface might drift into the impact region, increasing the DCR [6]. In the studied design, the shallow junction and the highly doped p-well limit this issue by preventing the top depletion region from reaching the BOX. In addition, the DCR here is largely dominated by the high bulk generation associated with SRH-TAT. Therefore, surface generation due to interface traps remains negligible. Bottom oxide-trapped charges can also create a back-depleted area, but the induced field remains negligible compared to the high electric field at the top of the silicon layer. Consequently, the impact of the defects from the BOX is limited for the considered dose.

Table II summarizes the DCR degradation for different SPAD designs under X-rays or gamma rays, as reported in the literature. Low preirradiation DCR is achieved by using low-doping well concentrations, resulting in higher breakdown voltages and reduced tunneling effects [17]. However, compared to the investigated SPAD, these designs are more prone to bulk damage due to their larger depletion regions. While X-ray irradiation only induces ionizing effects, gamma-ray irradiation results in both displacement damage and ionizing degradation [6]. In the latter case, distinguishing their individual contributions to the DCR may be difficult. Still, the DCR increase reported in [6] is partially attributed to interface traps originating from oxide isolation near the depletion region. Similarly, the DCR degradation following X-ray exposure observed in [7] is attributed to STIs close to the active area. Both studies show a DCR increase by at least a factor of 3. Designs employing buried layers [5], [10], [12] or spaced STIs [11] exhibit DCR degradation of less than a factor of 1.6. The reduced impact of TID in these devices is associated with the absence of oxide interfaces near the active area. In contrast, the DCR increase here is primarily attributed to changes in the depletion region due to the accumulation of Q_{ox} after TID. Therefore, the proposed PG structure is implemented to restrain the ionization region, enhancing resistance to premature breakdown and preventing DCR degradation. This approach is compatible with a 650-nm-thick top silicon layer, whereas retrograde wells or buried layers require a thicker silicon depth and deeper junctions. This method ensures high UV and blue light detection efficiency in both FSI and BSI configurations [15].

IV. CONCLUSION

In this study, we investigate the effects of gamma-ray irradiation up to 132 krad(Si) on an ultrathin BSI SOI SPAD. We analyze the measured breakdown voltage and DCR before and after irradiation, using TCAD simulations to identify the key factors influencing the degradation of the SPAD performance. We show that radiation-induced oxide-trapped charges can significantly increase the electric field at the junction edges even in the presence of a doped guard ring, leading to premature breakdown and an increase in DCR. Measurements show a reduction in breakdown from 10.17 to 9.95 V and an increase in DCR from 1490 to 2700 cps/μm^2 at 1 V excess bias. Conventional methods for reducing the electric field at the edges of the active region are not suitable for the studied ultrathin SOI SPAD under irradiation. STIs are prone to irradiation-induced defects, while retrograde junctions or conventional doped guard rings require a thicker silicon layer, making them incompatible with ultrathin designs. TCAD simulations show that, reducing the oxide thickness of the investigated SPAD from 570 to 200 nm and extending the anode metal interconnect from 8 to 11 μm can effectively prevent premature breakdown. We propose this approach as a simple mitigation technique for ultrathin SPADs to improve their robustness against ionizing irradiation without adding complexity to the design. TCAD simulations confirm that this approach can significantly improve the resistance to premature breakdown, even with oxide charge densities up

to $6.3 \times 10^{12}\,\mathrm{cm}^{-2}$. No breakdown shift is observed in the simulation at this trapped charge density. The DCR is also nearly unchanged, with a value of 1365 cps/μm^2 at 1 V excess bias, resulting in radiation robustness above 132 krad(Si).

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References

[1] F. Zappa, S. Tisa, A. Tosi, and S. Cova, "Principles and features of single-photon avalanche diode arrays," *Sens. Actuators A, Phys.*, vol. 140, no. 1, pp. 103–112, 2007.

[2] Y. Maruyama, J. Blacksberg, and E. Charbon, "A 1024×8 700ps time-gated SPAD line sensor for laser Raman spectroscopy and LIBS in space and rover-based planetary exploration," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2013, pp. 110–111.

[3] Y. Yu et al., "The plastic scintillator detector for DAMPE," *Astroparticle Phys.*, vol. 94, pp. 1–10, Sep. 2017.

[4] L. Di Venere et al., "Characterization of a scintillator tile equipped with SiPMs for future cosmic-ray space experiments," *J. Phys., Conf. Ser.*, vol. 1390, no. 1, Nov. 2019, Art. no. 012119.

[5] R. Pagano et al., "Radiation hardness of silicon photomultipliers under 60Co γ-ray irradiation," *Nucl. Instrum. Methods Phys. Res. A, Accel. Spectrom. Detect. Assoc. Equip.*, vol. 767, pp. 347–352, Dec. 2014.

[6] A. Jouni et al., "Effects of X-ray and γ-ray irradiations on 2-D-planar and 3-D-stacked CMOS SPADs," *IEEE Trans. Nucl. Sci.*, vol. 71, no. 8, pp. 1753–1765, Aug. 2024.

[7] L. Ratti et al., "Dark count rate degradation in CMOS SPADs exposed to X-rays and neutrons," *IEEE Trans. Nucl. Sci.*, vol. 66, no. 2, pp. 567–574, Feb. 2019.

[8] A. R. Altamura et al., "Radiation damage on SiPMs for space applications," *Nucl. Instrum. Methods Phys. Res. A, Accel. Spectrom. Detect. Assoc. Equip.*, vol. 1045, Jan. 2023, Art. no. 167488.

[9] F. Acerbi, A. R. Altamura, B. Di Ruzza, S. Merzi, and A. Gola, "Radiation damage effects of protons and X-rays on silicon photomultipliers," *Nucl. Instrum. Methods Phys. Res. A, Accel. Spectrom. Detect. Assoc. Equip.*, vol. 1047, Feb. 2023, Art. no. 167791.

[10] Y. Li, C. Veerappan, M.-J. Lee, L. Wen, Q. Guo, and E. Charbon, "A radiation-tolerant, high performance SPAD for SiPMs implemented in CMOS technology," in *Proc. IEEE Nucl. Sci. Symp., Med. Imag. Conf. Room-Temp. Semiconductor Detect. Workshop (NSS/MIC/RTSD)*, Oct. 2016, pp. 1–4.

[11] F. Shojaee, M. Zarei, L. Ratti, and M. A. Karami, "A new guard ring for ionizing radiation tolerance enhancement in single-photon avalanche diodes," *Microelectron. Rel.*, vol. 135, Aug. 2022, Art. no. 114573.

[12] S. Merzi et al., "Radiation damage on silicon photomultipliers from ionizing and non-ionizing radiation of low-Earth orbit operations," *Sensors*, vol. 24, no. 15, p. 4990, Aug. 2024.

[13] R. Dalal, "Simulation of irradiated detectors," in *Proc. 23rd Int. Workshop Vertex Detectors*, vol. 227, May 2015, pp. 1–13.

[14] M.-J. Lee, P. Sun, G. Pandraud, C. Bruschini, and E. Charbon, "First near-ultraviolet- and blue-enhanced backside-illuminated single-photon avalanche diode based on standard SOI CMOS technology," *IEEE J. Sel. Topics Quantum Electron.*, vol. 25, no. 5, pp. 1–6, Sep. 2019.

[15] I. Sabri Alirezaei, N. Andre, A. Sedki, P. Gerard, and D. Flandre, "An ultra-thin ultraviolet enhanced backside-illuminated single-photon avalanche diode with 650 nm-thin silicon body based on SOI technology," *IEEE J. Sel. Topics Quantum Electron.*, vol. 28, no. 2, pp. 1–10, Mar. 2022.

[16] P. Sun, R. Ishihara, and E. Charbon, "Flexible ultrathin-body single-photon avalanche diode sensors and CMOS integration," *Opt. Exp.*, vol. 24, no. 4, p. 3734, 2016.

[17] R. Henderson and L. A. Grant, "Reduction of band-to-band tunneling in deep-submicron CMOS single photon avalanche photodiodes," in *Proc. Int. Image Sensor Workshop*, Jun. 2009, pp. 1–5.

[18] A. Panglosse, P. Martin-Gonthier, O. Marcelot, C. Virmontois, O. Saint-Pé, and P. Magnan, "Dark count rate modeling in single-photon avalanche diodes," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 67, no. 5, pp. 1507–1515, May 2020.

[19] H. Finkelstein, M. J. Hsu, and S. C. Esener, "STI-bounded single-photon avalanche diode in a deep-submicrometer CMOS technology," *IEEE Electron Device Lett.*, vol. 27, no. 11, pp. 887–889, Nov. 2006.

[20] E. A. G. Webster, L. A. Grant, and R. K. Henderson, "A high-performance single-photon avalanche diode in 130-nm CMOS imaging technology," *IEEE Electron Device Lett.*, vol. 33, no. 11, pp. 1589–1591, Nov. 2012.

[21] D. Han, Y. Xu, F. Sun, and F. Song, "A scalable single-photon avalanche diode with improved photon detection efficiency and dark count noise," *Optik*, vol. 212, Jun. 2020, Art. no. 164692.

[22] B.-L. Bérubé et al., "Implementation study of single photon avalanche diodes (SPAD) in 0.8μm HV CMOS technology," *IEEE Trans. Nucl. Sci.*, vol. 62, no. 3, pp. 710–718, Jun. 2015.

[23] M. Dandin, A. Akturk, B. Nouri, N. Goldsman, and P. Abshire, "Characterization of single-photon avalanche diodes in a 0.5 μm standard CMOS process—Part 1: Perimeter breakdown suppression," *IEEE Sensors J.*, vol. 10, no. 11, pp. 1682–1690, Nov. 2010.

[24] J. M. López-Martínez, R. Carmona-Galán, and A. Rodríguez-Vázquez, "Limitation of SPADs quantum efficiency due to the dopants concentration gradient," in *Proc. 27th IEEE Int. Conf. Electron., Circuits Syst. (ICECS)*, Nov. 2020, pp. 1–4.

[25] M. Sanzaro, P. Gattari, F. Villa, A. Tosi, G. Croce, and F. Zappa, "Single-photon avalanche diodes in a 0.16 μm BCD technology with sharp timing response and red-enhanced sensitivity," *IEEE J. Sel. Topics Quantum Electron.*, vol. 24, no. 2, pp. 1–9, Mar. 2017.

[26] M. S. Ara Shawkat and N. McFarlane, "Fundamentals of perimeter gated single photon avalanche diodes used in silicon photomultipliers for nuclear imaging," in *Proc. IEEE Nucl. Sci. Symp. Med. Imag. Conf. (NSS/MIC)*, Oct. 2019, pp. 1–2.

[27] *Atlas User's Manual Device Simulation Software*, Silvaco, Santa Clara, CA, USA, 2022.

[28] S. Buchner, "Radiation hardness assurance (RHA) for space systems," presented at the Int. School Effects Radiat. Embedded Syst. Space Appl., West Palm Beach, FL, USA, 2008.

[29] Z. Wang et al., "Degradation and annealing studies on gamma rays irradiated COTS PPD CISs at different dose rates," *Nucl. Instrum. Methods Phys. Res. A, Accel. Spectrom. Detect. Assoc. Equip.*, vol. 820, pp. 89–94, Jun. 2016.

[30] M. Fishburn, "Fundamentals of CMOS single-photon avalanche diodes," Ph.D. dissertation, Dept. Microelectron., Delft Univ. Technol., Delft, The Netherlands, 2012.

[31] F. B. McLean and T. R. Oldham, "Basic mechanisms of radiation effects in electronic materials and devices," Tech. Rep., 1987.

[32] J. R. Schwank et al., "Radiation effects in MOS oxides," *IEEE Trans. Nucl. Sci.*, vol. 55, no. 4, pp. 1833–1853, Aug. 2008.

[33] G. A. M. Hurkx, D. B. M. Klaassen, and M. P. G. Knuvers, "A new recombination model for device simulation including tunneling," *IEEE Trans. Electron Devices*, vol. 39, no. 2, pp. 331–338, Feb. 1992.

[34] E. A. G. Webster and R. K. Henderson, "A TCAD and spectroscopy study of dark count mechanisms in single-photon avalanche diodes," *IEEE Trans. Electron Devices*, vol. 60, no. 12, pp. 4014–4019, Dec. 2013.

[35] O. Lui and P. Migliorato, "A new generation-recombination model for device simulation including the poole-frenkel effect and phonon-assisted tunnelling," *Solid-State Electron.*, vol. 41, no. 4, pp. 575–583, Apr. 1997.

[36] J. W. Slotboom and H. C. de Graaff, "Measurements of bandgap narrowing in Si bipolar transistors," *Solid-State Electron.*, vol. 19, no. 10, pp. 857–862, Oct. 1976, doi: 10.1016/0038-1101(76)90043-5.

[37] M. E. Law, E. Solley, M. Liang, and D. E. Burk, "Self-consistent model of minority-carrier lifetime, diffusion length, and mobility," *IEEE Electron Device Lett.*, vol. 12, no. 8, pp. 401–403, Aug. 1991.

[38] Y. Yan et al., "Characterization of thin Al_2O_3/SiO_2 dielectric stack for CMOS transistors," *Microelectron. Eng.*, vol. 254, Feb. 2022, Art. no. 111708.

[39] X. Zhou et al., "Investigation on total-ionizing-dose radiation response for high voltage ultra-thin layer SOI LDMOS," in *Proc. IEEE 30th Int. Symp. Power Semiconductor Devices ICs (ISPSD)*, May 2018, pp. 64–67.

[40] D. J. Dumin, *Oxide Wearout, Breakdown, and Reliability*. Singapore: World Scientific, 2001, pp. 1–102.