Analysis and Specification of an IR-UWB Transceiver for High-Speed Chip-to-Chip Communication in a Server Chassis

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***Abstract*— This paper presents the system architecture, modeling, and design constraints of a wireless chip-to-chip-communication transceiver as a low-power alternative to wireline links, such as PCI-Express. On top of the potential power savings, the wireless link provides lower latency times, better flexibility, lower complexity, and easier heat diffusion. The proposed transceiver uses impulse-radio ultra-wideband communication at 10 GHz. It supports a 2.5-Gb/s data rate with pulse position modulation over short distances (∼10 cm). The hardware complexity is reduced by using a modified non-coherent receiver with a rectifying RF front-end and a relative-compare analog baseband. The system performance is quantified and tradeoffs are explored with the main motivation of reducing power. A discussion of the modulation choice, the performance specifications of the receiver blocks and the clock generation principle is presented. We show that energy efficiency better than 6 pJ/bit could be reached with the proposed architecture.**

***Index Terms*— Chip-to-chip wireless communication, non-coherent transceiver, IR-UWB, PCI-Express.**

I. Introduction

TEN years ago, high-speed serial links massively replaced parallel buses for chip-to-chip communications thanks to key advantages: routing simplicity, noise, power and pin count reduction, etc. Peripheral Component Interconnect Express (PCIe) constitutes one of the major high-speed serial-link standards that connect the components of a modern computer, such as the external graphics card, network interface card, RAID controllers, storage devices and other high-performance peripherals [1]. Data center managers also use PCIe across server backplanes, or to interconnect clustered processors.

Wireless interconnects using antennas may provide advantages over wireline communication such as lower communication latency [2], [3] and higher energy efficiency: [2] estimates that they need less energy per bit for communication distances higher than 1 cm thanks to the absence of wire resistance and capacitance. Moreover, as wireless communications are not limited by wireline routing, the complexity and flexibility in the system can improve [3] allowing broadcast communication and making heat diffusion and cooling easier.

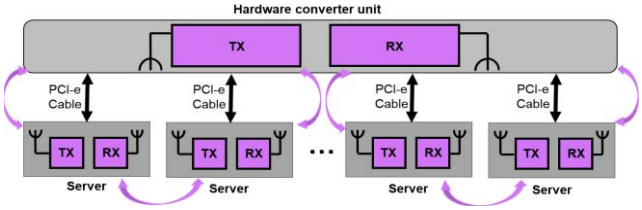

Fig. 1. System concept comparing standard fixed PCIe wired hardware (black) to the proposed flexible wireless connections between main unit and servers, as well as between servers directly.

In this work we investigate the system architecture, modeling and circuit specifications of a wireless chip-to-chip communication transceiver as a low-power alternative to PCIe. The purpose of this paper is to analyze the architectural system-level aspects (spectrum usage, modulation type, performance requirement, propagation of analog non idealities) for designing such a transceiver, rather than circuit-level implementation details. As we propose a fully integrated topology, crystal clock references should be avoided. As the first wireless transceiver proposed for this application, we target a data rate of 2.5 Gb/s, comparable with single-lane PCIe generation 1 [4].

Fig. 1 shows the system concept in the confinement of a server chassis with a TX-RX distance up to 10 cm. In the transmitter design, we have to investigate the most adequate modulation scheme and signal spectrum for the proposed application, taking into account the channel attenuation. Section II develops this discussion. For the receiver, the key performance is the trade-off between its power consumption and the bit error rate (BER) of the demodulated signal. This trade-off is studied in this paper with a top-down approach. An in-depth description of the proposed transceiver architecture is provided in Section III. In Section IV, we develop a behavioral of the RX system and the design tradeoffs are analyzed. The specifications for the different blocks are presented where a 28-nm CMOS technology is used at 1 V for power estimation. Finally, Section VI summarizes the main conclusions of the work.

II. Analysis of Spectrums & Modulation Scheme

To substitute PCIe links, our system is intended to be included inside a server chassis, therefore, substantial amounts metallic objects and a highly reflective metallic case are part of

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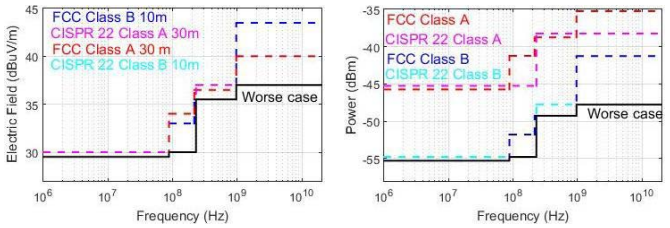


(a) (b)

Fig. 2. EMC regulations for (a) the electric field and (b) equivalent transmitted power considering an antenna gain of 0 dBi. The EMC limitations for Class A devices are given for 30-m distance while 10-m is used for Class B devices. For radiated emissions testing, the BW of the RX used must be at least 100 kHz. The resolution BW for computing the TX output power is 1 MHz for frequencies $>$ 1 GHz.

the transmission medium and the propagation will be a mixture of near- and far-field. According to [5], the propagation path loss in a computer chassis (that is considered a very similar medium to the server chassis in our application) will be in the order of 10 dB over distances of 10 cm.

Wireless communications need to respect the limit on the TX output power and frequency allocations specified by existing regulations. No existing communication standard combines the low power and high data rate targets of the considered application. For example, the unlicensed ultra-wideband frequency band from 3.1 to 10.6 GHz allows low power design but with a limited data rate. However inside a server chassis, short communication distance and limited channel losses may allow the use of a very low TX output power. We propose to limit the TX output power below the EMC regulations [6] so that we are free to use an extremely wide bandwidth (BW) without the restriction of an standard. This goes in the right direction compared to the evolution of nanoscale CMOS technologies showing low intrinsic gain but very high transition frequencies for the MOS transistors [7].

The FCC and other regulatory agencies like the CISPR (adopted by several countries) set EMC limits on the radiated emission of digital devices [8]. In our case, the TX power must stay below the limits for both Class A and Class B devices. Fig. 2 shows the limits of the electric field permitted by main regulations and the corresponding maximum emitted power considering a transmitting antenna with 0-dBi gain.

The received power depends on the channel characteristics. Considering the receiver antenna gain and losses in the matching network, the received signal will be on the order of 10-15 dB below the transmitted signal. On another hand channel multipath is a major constraint as the short distances and metallic case will reflect the electromagnetic waves without losing much of their power. However, the wireless transceiver locations are stationary, and so do the time delay and distances; therefore, they are predictable a priori and time invariant. They could thus be compensated with a digital TX equalizer in a calibration process [9] but this is outside the scope of this paper, where we will focus on the RX design. Table I summarizes key information on the expected values of channel attenuation, noise and electromagnetic interference (EMI) caused by switching circuits in the chassis [5], [9].

TABLE I
CHANNEL CHARACTERISTICS [5], [9]

Antenna and matching network loss	~ 5 dB
Channel attenuation	10 dB@10cm
Noise floor when computer off	~ -70 dBm
EMI when computer on	~ -65 dBm
Blockers	Max. -52.9 dBm @2.5 GHz

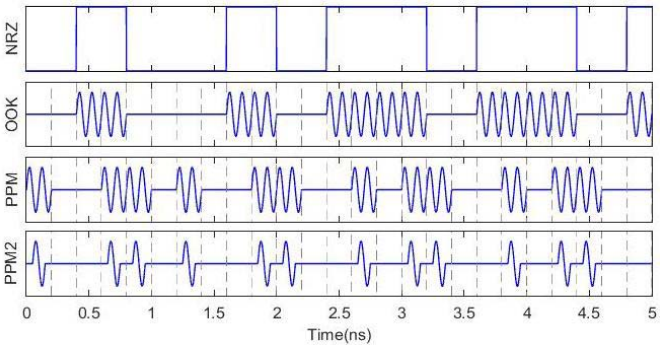


Fig. 3. Candidate non-coherent modulation schemes: OOK, PPM without guard interval and PPM2 with guard intervals.

Now that the communication band and power levels are set, we need to select the modulation scheme. Both coherent and non-coherent communication schemes can be used. Coherent communications require carrier phase information and hence a receiver using matched filters or correlation to recover the transmitted data. Non-coherent receivers can use simpler techniques like energy detection, the so-called impulse-radio ultra-wide-band (IR-UWB) communications [10]. Coherent schemes utilize bandwidth more efficiently and achieve better sensitivity, but require complex phase tracking blocks with significant RX power overhead [11]. Moreover, as our choice to transmit data below the EMC limits enables the use of an ultra-wide 10 GHz, spectrum efficiency is not a critical criterion. We thus select non-coherent communications to target a higher RX energy efficiency at a given data rate.

The simplest non-coherent IR-UWB modulation schemes (Fig. 3) are OOK (On-Off Keying) and PPM (Pulse Position Modulation). With OOK modulation, the symbol-1 (resp. symbol-0) is encoded by the presence (resp. absence) of signal in the symbol period. In PPM modulation, the symbol period is divided in two slots. Symbol-0 (resp. symbol-1) is encoded by the presence of signal in the first (resp. second) slot. In low data rate IR-UWB transceivers, guard intervals are usually added to give more tolerance against multipath interferences. In this case, the PPM slots only occupy a quarter of the symbol period as shown in Fig. 3 (PPM2). Fig. 4 shows the power spectral density of a PPM signal. The PPM signal has maximum TX power at the frequency of the carrier (f_C) and zeros at $f_C \pm f_C \cdot n/P$ where P is the number of f_C periods per symbol and n an integer.

In order to maximize the total TX output power while meeting the EMC regulations, we need to cancel the spectral line at the carrier frequency. For this purpose, the polarity of the transmitted pulses can be scrambled [12]. Fig. 4 shows the

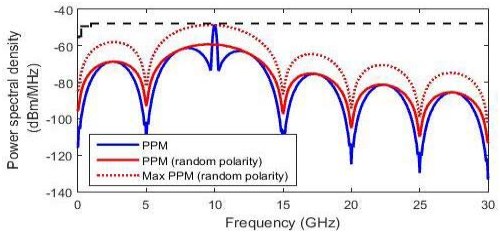


Fig. 4. PSD of PPM signal with and without the pulse polarity scrambling ($f_C = 10$ GHz, 2 periods per bit, no guard interval, FFT performed on ideal signal waveforms in Matlab).

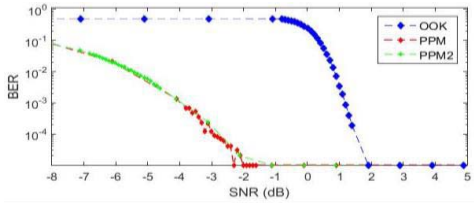


Fig. 5. BER versus SNR for OOK, PPM and PPM2. Matlab simulations have been used to extract and compare the energy in the different time slots of the signals of Fig. 3.

effect of this spectral shaping in the case of PPM modulation: the output power can be increased by 6 dB while meeting the EMC regulation limit.

To select the best modulation scheme, the margin to distinguish between signal and noise at the receiver side should be considered. We have to remember that OOK modulation has twice more pulses in each symbol than PPM but with PPM the receiver is able to relatively compare the signal energy between two time slots. Fig. 5 shows the BER using an ideal receiver model versus the signal-to-noise ratio (SNR). PPM shows better results than OOK because the comparison between two time slots limits the noise effect. PPM2 with guard intervals shows very similar results. PPM2 with guard intervals shows very similar results. Considering the EMC PSD power limit, PPM2 modulation allows to transfer more energy per symbol as it uses a higher bandwidth. This results in a 2 to 3 dB SNR improvement over PPM. However, the peak current consumed by the transmitter has to be doubled to provide higher pulse amplitude, which will lead to a more complex PA. Moreover, as we are working at high data rate, the guard interval duration is short (100 ps) and do not provide robustness against multipath interference. Finally, the recovery of the clock is greatly simplified if we have a 50-% duty cycle for signal presence i.e. equivalent time with the signal than without the signal. For all these reasons, PPM has been chosen in this work.

III. System Architecture

The proposed transceiver block diagram is shown in Fig. 6. To encode the transmitted data, binary PPM achieving a data rate of 2.5 Gb/s is used. The transmitter architecture (Fig. 6 (a)) uses a local oscillator (LO) generating a 10-GHz signal and a power amplifier (PA) that amplifies the signal coming from the mixer and provides output matching for the antenna. A PPM generation block receives the input data and generates the PPM symbol. A phase scrambler provides the randomness of the polarity of the transmitted pulses. The mixer combines the PPM signal with the scrambled LO signal to provide the required PPM modulation with 2 periods of a carrier of 10-GHz sinusoidal signal. Taking into account the power spectrum in Fig. 4, and losses of 5 dB in the antenna due to its gain and matching losses, the expected output amplitude on a 50-Ω antenna is 100 mV, which is compatible with the 1-V supply voltage of the target 28-nm CMOS technology.

Usually, the design of the transmitter is simpler than the receiver. The critical part here would be the design of the power amplifier that has to provide the output power with a sufficient bandwidth. Several papers have reported 60-GHz power amplifiers with power efficiencies between 10% to 20% [13], [14]. This would give power consumptions from 0.2 to 0.8 pJ/bit in our power amplifier due to the low output power needed. Several papers report power consumptions below 2 pJ/bit for UWB-TX [15], [16]. As the transmitted power in the target communication is much lower than for state-of-art transceivers, the power will be also reduced. Therefore, in this paper, the effort is put on the analysis and specifications of the receiver, as it will dominate the total power.

As shown in Fig. 6 (b), the receiver has a simple structure for low power consumption. It features an RF front end, that amplifies the received signal and down converts it by rectifying the signal through a self-mixing squarer. This performs signal power extraction. A low-power mixed-signal baseband block integrates the signal power in each symbol time slots and relatively compares between the two slots to recover the transmitted symbol. The control signal for the baseband are derived from a 2.5-GHz baseband clock recovered from the RF front-end output. With this receiver, PPM signals are easily and reliably demodulated for high data rate. Let us discuss its main blocks into more details.

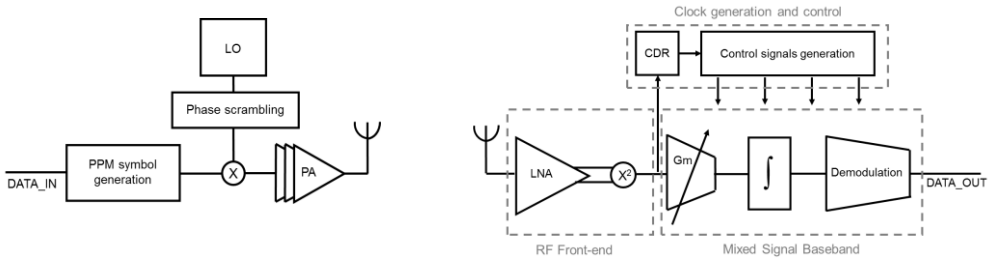
A. RF Front-End

The RF front-end is formed by a low-noise amplifier (LNA) and a squarer. The LNA amplifies the signal from the antenna providing at the same time the required input matching to minimize the return loss to the antenna and a low noise figure (NF) to enhance the sensitivity of the receiver. The LNA should provide enough conversion gain to overcome the $V_{out} = kV_{in}^2$ transfer characteristics of the squarer when small inputs are considered. As the antenna, in most cases, produces single-ended input/output, a single-to-differential conversion is performed using a balun LNA as a differential signal is preferred for robustness against supply and substrate noises.

The LNA and the squarer are AC coupled together as well as to the baseband blocks so that static DC offsets are not propagated to avoid errors in the operation of the circuits.

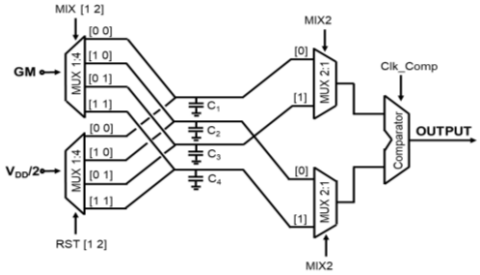
B. Analog Baseband

The analog baseband architecture inspired from [11] is formed by a transconductance block (G_m) that provides the current for the integrator. A demodulation block generates



(a) (b)

Fig. 6. Proposed transceiver block diagram: (a) transmitter and (b) receiver.



	[MIX1 MIX2 /RST1 RST2]	C1	C2	C3	C4
T1 (0 s)	[0 0 / 1 0]	Integrate	Reset	Hold	Hold
T2 (0.2 ns)	[1 0 / 0 1]	Hold	Integrate	Reset	Hold
T3 (0.4 ns)	[0 1 / 1 1]	Hold	Hold	Integrate	Reset
T4 (0.6 ns)	[1 1 / 0 0]	Reset	Hold	Hold	Integrate
T5(0.8 ns)	[0 0 / 0 0]	Integrate	Reset	Hold	Hold
T6(1.0 ns)	[1 0 / 0 1]	Hold	Integrate	Reset	Hold
T7 (1.2 ns)	[0 1 / 1 1]	Hold	Hold	Integrate	Reset

Fig. 7. Proposed baseband block diagram and operation.

the output data by comparing the power in two adjacent periods. Fig. 7 shows the implementation of the integration and demodulation blocks and the operation schedule. Two demultiplexers (DMUX) 1:4, formed by switches, provide the signals to the 4 identical integrating capacitors so that they store analog integration results during the first and second time slots onto separate capacitors C_1 and C_2 (or C_3 and C_4), respectively. A relative energy comparison between the two time slots is performed by a high-speed comparator.

To acquire a symbol sample at each baseband clock cycle given the need to reset the capacitors, we use an interleaved architecture by adding two extra capacitors C_3 and C_4 with analog multiplexers (MUX) 2:1 to the comparator input. Two comparators and a DMUX could be also used but it would require higher power consumption because the comparator power is higher than the DMUX power. The four capacitors rotate between three states, "reset" (the capacitor is charged to $V_{DD}/2$), "integrate" (the G_m block delivers to the capacitor a current proportional to the signal power in that time slot), and "hold" (the output voltage is kept on the capacitor).

C. Clock Generation and Control

For correct operation of the system, we need five digital control signals: MIX1 and MIX2 to control the first DMUX 1:4, RST1 and RST2 to control the second DMUX 1:4 and a CLK_COMP to trigger the comparator sampling; the two MUX 2:1 are also controlled by MIX2. These control signals can be generated from the single reference baseband clock (Clk_{ref}) using simple digital blocks such as frequency dividers, inverters, XOR gates, or delay blocks.

To generate, Clk_{ref}, a clock recovery circuit will be used. We want the frequency of the clock signals and thus the power consumption to be as low as possible. Therefore, the frequency of Clk_{ref} is selected to be the lowest frequency we need for generating the control signals: 2.5 GHz. Fig. 8 shows the clock signals and how they charge the 4 capacitors.

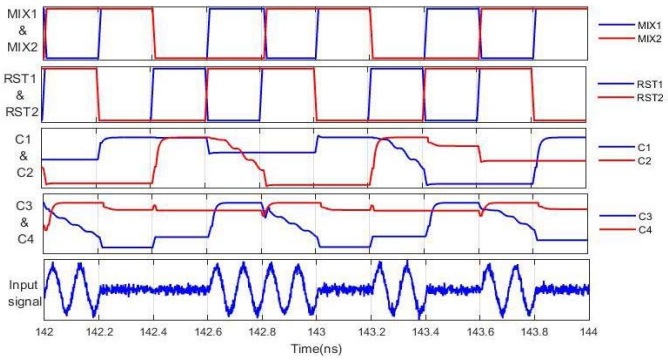


Fig. 8. Clock signals and integrating signals of the capacitors.

IV. Simulation Methodology and Specifications of the Building Blocks

In order to evaluate the feasibility of the proposed RX architecture, we need to specify the performance of its internal blocks from the LNA to the comparator. First, considering antenna and channel losses, the minimum RX input power will be of the order of −65 dBm, which indicates that the total RX gain is an important performance. In particular, enough gain should be provided by the RF front-end as, for correct operation of the baseband, a signal of a few mV is necessary at the output of the squarer. Noise level limits are also important for a correct signal demodulation. Given the ultra-wide band around the 10-GHz carrier, the noise is integrated on a wide frequency range and the RF front-end bandwidth (BW) is thus another important specification. Next, the power consumption

versus uncertainty tradeoffs in the generation of timing signals including jitter, delay, phase error, etc. are critical aspects for a low-power implementation and correct operation of the analog baseband. Finally, in the analog baseband, the systematic DC offset between the inputs of the comparator sets a minimum gain to ensure correct comparison. To budget all these non-idealities while minimizing bit-error rate (BER) and power, we developed a model of the RX system including these non-idealities as described in next section.

A. RX System Model Simulation Methodology

To explore the tradeoffs of the different blocks of the receiver, the system is implemented in Verilog-AMS with behavioral models including their specific non idealities such as limited gain and bandwidth, noise figure, dynamic ranges, and DC offsets. To evaluate the order of magnitude of these non-idealities for each block, we use published data as well as SPICE simulations in a 28-nm technology with 1-V supply voltage. The behavioral simulations will allow us to budget the non-ideality limits of each block. Mixed-signal simulations of the whole system have been performed with Questa-ADMS tool from Mentor, considering an ideal input signal with PPM modulation of a 10-GHz carrier.

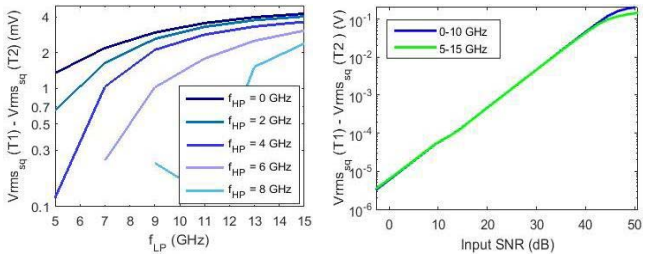
For the channel, a linear model without multi-paths has been assumed with attenuation up to 15 dB corresponding to channel distances up to 10 cm, antenna gains and losses in the matching network. Additive white Gaussian noise is added to the input signal. This allows us to examine the impact of the block non-idealities on the overall system BER performance.

B. RF Front-End

The LNA is a key component and one of the most power consuming blocks of the whole RX. Its BW and noise figure (NF) are critical design requirements as they can significantly affect the SNR of the whole receiver. In conjunction with the squarer, they provide the signal levels for the following power comparison. Using the linear analysis, we explore the front-end specifications and quantify their design tradeoffs.

An important parameter of the front-end is its gain. Worst-case scenario happens when we have a minimum pulse with power equal to or less than the noise floor. As the squarer provides transfer characteristics proportional to V_{in}^2, and SPICE simulations in a 28-nm CMOS technology with 1-V supply voltage show that its input signal should be in the order of tens of mV for proper operation, the LNA should provide enough gain to generate these values for small inputs. In this case, simulations show that gains of 15-dB for the LNA and 10-dB for the squarer and a NF of 3 dB for the LNA are sufficient for achieving a good signal quality. These values are aligned with the state of art LNAs and squarers.

To study the optimum frequency ranges and BW of the RF front-end, we have to consider the output of the squarer as it provides an output signal with amplitude proportional to the power of the input signal. In baseband, the energy of the signal in the two slots of the PPM modulation will be compared. Therefore, the difference (Interval margin) between the RMS output voltages of the squarer in the two time slots can be



(a) (b)

Fig. 9. Difference of the RMS value of the squarer output in two adjacent time slots (a) versus f_{LP} for a fixed SNR and different f_{HP} and (b) versus the input SNR for the same front-end BW ($f_{HP} - f_{LP}$) but different f_{HP} and f_{LP}.

TABLE II
PERFORMANCE COMPARISON OF LNA FIGURES OF MERIT

Ref	Year	Power (mW)	BW (GHz)	FOM
[17]	2014	9.6	3.5-9.25	13.19
[18]	2010	3.9	3-8	23.09
[19]	2012	6.36	3.1-10.6	13.07
[20]	2017	2.1	11.1	37

related to the quality of the signal for power comparison. Calculations use a PPM signal with 2 periods of a 10-GHz sinusoidal carrier signal. NF of 3 dB, gain of 15 dB and 50-Ω input impedance are assumed for the LNA and a gain of 10 dB and a BW of 20 GHz for the squarer so that not to affect the simulation. Fig. 9 (a) shows the interval margin as a function of the high-cut-off frequency (f_{LP}) for different low-cut-off frequencies (f_{HP}) of the pass band. On one hand, the higher the f_{LP} the higher the interval margin because the signal is less filtered. For the other part, for a fixed f_{LP}, the lower the f_{HP} the higher the interval margin, so not only the maximum operating frequency is important but also the lower frequency has a significant effect on the quality of the signal. Therefore, a wideband LNA is highly appreciated in the receiver design. However, an f_{LP} higher than 10 GHz does not yield significant improvement. Fig. 9 (b) shows this interval margin versus the SNR at the input of the RX for a 10-GHz BW LNA but centered in different frequencies. This shows that while a 5 to 15-GHz LNA would suppose a higher power consumption it does not improve the quality of the energy comparison.

State of art wideband LNAs and squarers may give an estimation of power consumption. LNAs are compared in Table II using the following figure of merit (FOM):

$$FOM = 20\log\left(\frac{Gain\,[Lin]\cdot BW\,[GHz]}{Power\,[mW]\cdot(NF\,[Lin]-1)}\right) \quad (1)$$

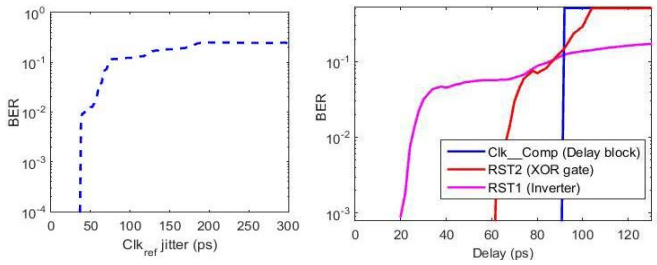
For the design of the LNA, an inductorless balum LNA similar to the one proposed in [20] could be used which gives a power consumption below 3 mW achieving a 10-GHz BW, 15-dB gain, and 3-dB NF.

Although a passive mixer is sometimes used to implement the squarer [21], an active circuit is preferred to introduce a conversion gain. Table III summarizes performance of recent squarers. Along with our SPICE simulation results in 28-nm CMOS technology, we estimate the power consumption of the

TABLE III
PERFORMANCE COMPARISON OF STATE OF ART SQUARERS

Ref	Year	Techno	Power (μW)	BW (GHz)	Gain (dB)
[22]	2013	65 nm CMOS	460	3-8	12
[23]	2009	65 nm CMOS	720	3.1-5	12.6
[24]	2012	0.18 μm CMOS	1650	3-5	21*
SPICE	2017	28-nm FDSOI	<1000	>10	10

*With additional LPF



(a) (b)

Fig. 10. BER (a) versus the peak to peak jitter of the Clk_{ref} and (b) as a function of the delay of the clocks; 3 delays are taken into account: the extra delay of the clock used for the comparator block (Clk_Comp), the delay of RST2 and the delay of RST1.

squarer close to 1 mW. A topology similar to the one proposed in [22] has been used for the simulations.

C. Sampling Clock Generation

Accurate generation of timing signals is another critical aspect. The main issues to study are the jitter performance of the reference clock as well as the delay matching of the different control signals, the phase error between the TX and the RX clocks, and the identification of a sampling clock generation architecture suitable for a low power implementation. Although the absence of guarding interval when using 2 pulses per time slot may introduce tight constraints on the timing of control signals, we will show that the requirements on clock generation remain reasonable.

As all the clocks needed are obtained from the reference baseband clock (Clk_{ref}), its jitter is crucial for demodulation process and data acquisition. Fig. 10 (a) shows the simulated BER as a function of the reference clock jitter. A peak to peak jitter below 36 ps (that relates to ∼12 ps of Gaussian jitter for a BER of 10^{-3}) results in no errors in the simulation of 10^5 transmitted symbols. The corresponding phase noise is directly related with the jitter by [6]:

$$L(\Delta f) \approx 2\pi^2 \sigma_T^2 \left(\frac{f_C}{\Delta f}\right) \frac{1}{T_{symbol}} \quad (2)$$

where σ_T is the total accumulated jitter over period T_{symbol}. This will give a −68 dBc/Hz phase noise at a 1-MHz offset for $f_C = 2.5$ GHz. These values can be easily achieved with a ring oscillator in a clock recovery circuit (CDR). In this way, we avoid the use of external crystal references and the long-term phase misalignments or carrier frequency offset caused by frequency skews are also avoided.

For example [25] provides a back-bias-controlled oscillator that consumes 180 μW when operating at 4.5 GHz and featuring a phase noise of −102 dBc/Hz at 30-MHz offset.

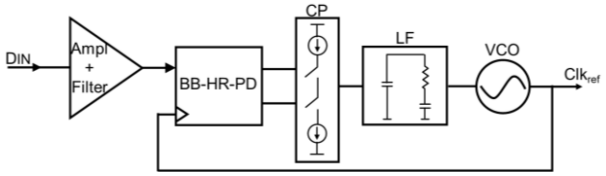


Fig. 11. CDR block diagram with a bang-bang half-rate phase detector (BB-HR-PD).

Regarding the design of the CDR, a simple PLL topology implemented with a bang-bang phase detector, a charge pump and a loop-filter can be used to compensate the misalignments between the clock and the data (Fig11). As the CDR is implemented after the squarer, which doubles the input signal transitions, a half-rate phase detector is a good choice to implement the bang-bang phase detector [26]. This relaxes the speed and power requirements of the CDR blocks.

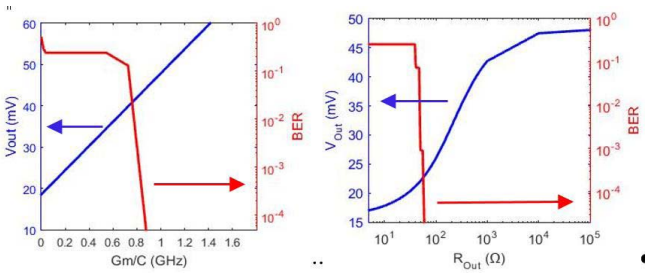
Taking into account the state of art, for example [27] provides a reference-less half-rate CDR circuit working at 2.5 GHz and consuming 2.9 mW with −134-dBc/Hz phase noise at 1-MHz frequency offset, we estimate that a CDR with a power consumption lower than 5 mW can be achieved in a 28-nm technology. The total power consumption will be dominated by the charge pump (that has no DC consumption) and the half-rate phase detector (that is implemented with low-power D flip-flops and logic gates). The power consumption of the oscillator is estimated to be below 1 mW.

The matching or delay between the different clocks must also be accurate enough to allow the digital blocks to perform the correct comparison. Fig. 10 (b) shows the BER as a function of the skews of the different clocks with regards to MIX1 and MIX2 that are considered to have the same delay. We can see that the delay of the RST1 is the first to cause an impact on the BER (≠0 at 20-ps delay). However, this signal can be easily obtained from MIX1 using an inverter as the SPICE-simulated FO1 inverter delay is below 6 ps in a 28-nm technology. For their part, the delay of both the RST2 and CLK_COMP will not significantly affect the BER as they start to have an impact at 60 and 90 ps, respectively. Lower delays are expected with integrated circuits in 28-nm.

Therefore, although we have to take care in the design of the clock generation, the limits are not very critical so low power blocks can be used. References and preliminary simulations in 28-nm allow us to estimate a power consumption of the control block below 1.5 mW.

D. Analog Baseband

One of the first considerations here is the capacitors value. Together with the G_m block performance, they will determine the output voltage available for the comparison. This will be highly affected by the effective transconductance of the G_m block, and its output impedance as this fixes the BW of the G_m-C combination. Fig. 12 shows the voltage at the capacitor output terminal in the presence of signal during the integration period as a function of G_m/C and as a function of the output resistance of the G_m block. Also the BER is shown. The



(a) (b)

Fig. 12. Dependence of the BER, and the output voltage of the capacitor when there is signal during the integration period with (a) G_m/C and (b) the output resistance of the G_m block.

minimum G_m/C value for a correct operation of the system for the previously determined gain of the RF front-end is 1 GHz that, for a capacitor of 0.5 pF, means a G_m of 500 μA/V. It can also be seen that the higher the output resistance, the higher the voltage, that is equivalent to a higher difference in the comparison voltages. This can have a significant effect on the BER of the system if the gain of the G_m block is not sufficiently high. However, the resistance should be higher than 60 Ω, which is not difficult to achieve.

These simulations show that there is a minimum value of the capacitors output voltage below which the comparator is not able to perform the comparison properly and BER increases. A controllable transconductance for the G_m block is thus highly recommendable to save power when higher input signals are received and provide enough gain for small signals. This control is done by means of a 3-bit control word.

The estimation of the power consumption of the G_m block considering the state of art is complicated as G_m blocks are usually described in a filter design with usually lower BW than the one required. In [28] a G_m in the order of 5.6 mA/V is achieved with 1.31 mW for 10-MHz operation. [29] proposes a G_m cell at 837 MHz with 245-μA/V G_m at 2.33 mW. These, together with some simulations in a 28-nm CMOS technology, allow to estimate the power consumption of the required G_m block around 2.5 mW. For the power estimation, a 2 stages cascade current mirror G_m block has been used.

Another critical block at the baseband is the comparator. In practice, there might be a systematic DC offset voltage between the signal paths and therefore between the two inputs of the comparator. This will influence the minimum gain necessary to ensure accurate sampling. Simulations indicate that DC offsets of the order of 10's of mV are usual. If we incorporate in our case capacitive coupling as a method to avoid propagation of the DC offset, this value can be reduced to a few mV avoiding that the systematic offset will swamp the comparator but making still a required gain necessary.

Fig. 13 shows for different G_m/C values the offset ranges for which the comparator is able to perform correct symbol demodulation. The comparator can manage offsets between −15 and 25 mV for an error free simulation.

The estimation of the power consumption of the dynamic comparator block and the rest of the digital circuitry is also difficult looking only at the state of art. For example [30] proposes a 600-μW dynamic comparator in a 0.18-μm CMOS

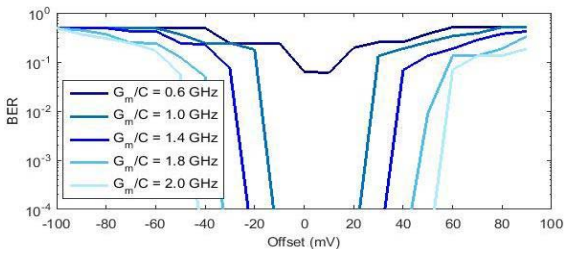


Fig. 13. BER as a function of the offset at the input of the comparator.

TABLE IV
POWER ESTIMATION OF THE PROPOSED RECEIVER

	Block	Power
RF Front-end	LNA	3 mW
	Squarer	~ 1 mW
Analog Baseband	Gm	2.5 mW
	Digital (MUX, DMUX)	< 1 mW
	Comparator	0.6 mW
Clocks	Clocks distribution	1.5 mW
	CDR	5 mW
TOTAL		**< 15 mW**

technology with a clock frequency of 500 MHz and [31] proposes a 3.3-mW comparator in a 0.35-μm CMOS technology with a sampling rate of 1.2 GHz. To estimate this power consumption in a 28-nm FD-SOI technology, we have to take into account that it scales linearly with the power supply (1.8 [30] and 3.3 [31] vs. 1 V), with the load capacitance value that scales linearly with the technology MOSFET length (180 [30] and 350 [31] vs. 30 nm), and it has a linear relationship with the frequency (500 MHz [30] and 1.2 GHz [31] vs. 2.5 GHz); this gives us a lower bound estimation of 280 μW for [30] and 170 μW for [31]. These results, as well as some circuit level simulations we performed in a 28-nm technology, allow us to estimate the power consumption of the comparator around 600 μW and lower than 1 mW for the rest of digital circuitry (MUX, DMUX).

V. VERIFICATION AND TOTAL POWER ESTIMATION

The analysis from previous section lead to the design specifications for each block of the receiver. This section will summarize these and provide an estimation of the total power consumption of the proposed receiver (Table IV).

First, the RF front-end must provide a good signal quality for the subsequent baseband processing. This gives a worst case gain and BW specification. For the proposed LNA a gain of 15 dB, with a NF of 3 dB was assumed. This gives a required bandwidth of 10 GHz. The gain provided by the LNA is enough to overcome the transfer characteristics of the squarer when small inputs are considered. For the squarer, only sufficient BW is required but looking to the state of art 10 dB of gain has been considered.

For the analog baseband, considering capacitors of 0.5 pF, the G_m block should provide 500 μA/V of transconductance with output impedance of at least 60 Ω for a comparator offset below 15 mV. No specific performance is required for the MUX-DMUX blocks apart from sufficient speed operation.

Also some specifications are required for the clocks signals such as jitter of the reference clock and delay limits for the

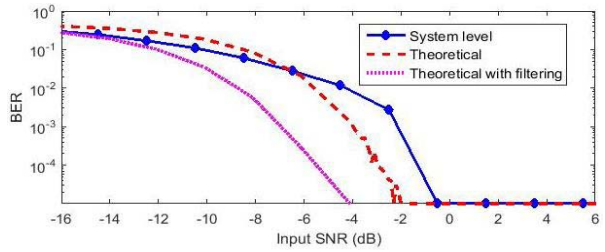


Fig. 14. BER versus input SNR.

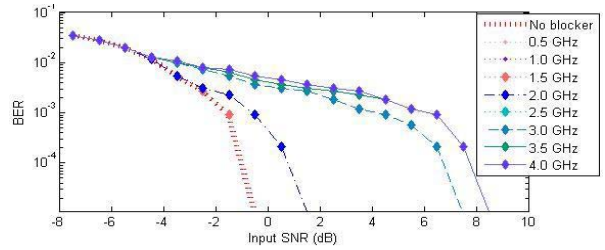


Fig. 15. BER versus input SNR for various −52 dBm blocker frequencies.

control signals. However, it has been shown that using a clock recovery block these values are not critical.

With the proposed receiver simulated at 2.5 Gb/s using a PPM modulation with 2 periods per symbol of a 10-GHz carrier signal, Fig. 14 shows the BER of the data reception as a function of the SNR at the input of the RX. A fixed input power of −43 dBm is used with variable noise power for this simulation. The results are compared with numerical simulations of an ideal RX with and without a band-pass filter (0.1-10 GHz) that filters the noise reducing the BER when the SNR is low. We can see that for SNR higher than −0.8 dB, the system correctly demodulates the data. For lower SNR some symbols are not correctly demodulated. This allows noise levels up to around −42 dBm at 10 GHz which is much higher than expected if we take as a reference the maximum noise of −55 dBm obtained in the measurements campaign of [32].

The previous analysis has been repeated in presence of blockers added to the input signal. A single-tone sinusoidal signal at different frequencies with a power of −52 dBm has been added to the PPM modulated signal with noise and the BER versus the SNR for different frequency blockers have been plotted. Fig. 15 shows that some blockers increase the minimum SNR to reach a 10^{-5} BER (i.e. 2 GHz and 3 to 4 GHz). We have to take into account that in our simulation we made the blocker sinusoidal signal to be in phase with our input signal which would be the worst case for the comparison between the two adjacent time slots. Although filters could be placed at the affected frequencies to reduce the impact of the blockers, there is still plenty of margin if we consider the maximum expected noise of −55 dBm.

Finally, an estimation of the power consumption of the whole receiver is provided in Table IV. The total power consumption is estimated to be less than 15 mW which gives an energy efficiency of 6 pJ/bit at 2.5 Gb/s. Although some wireline transceivers achieve similar energy efficiency (e.g. [33] proposes a transceiver for SERDES at 6pJ/bit), to the authors' knowledge, the best system specifically designed for PCI express links requires 25 pJ/bit [34]. With the proposed transceiver we will obtain lower power consumption than the conventional PCI express link with lower latency times, and higher flexibility allowing broadcast communications.

VI. Conclusions

In this paper, a system architecture for an integrated wireless chip-to-chip communication transceiver is presented and analyzed. The transceiver is proposed as an innovative low-power alternative to wireline PCI-express links, providing other advantages over the wireline solution, such as lower latency times, better flexibility, lower complexity and easier heat diffusion. A simplified non-coherent transceiver based on a rectifying RF front-end and relative-compare baseband in the receiver is proposed for its limited power consumption. Its lower spectrum efficiency is compensated by communicating over an extremely wide band of 10 GHz with TX output power below the EMC regulations. PPM modulation scheme for communication up to 10 cm at 2.5 Gb/s with a 10-GHz carrier is recommended as the best choice for better recovering of data with low amplitude.

The design specifications for the receiver building blocks are quantified while targeting low power. Jitter was found to be critical, so a clock recovery system was proposed for clock generation. In this way, a crystal reference is avoided reducing the system cost. Specifications of the different blocks in the RX system to achieve low BER were derived from system simulation based on realistic behavioral models of the blocks in Verilog-AMS. Finally, an estimation of the total power consumption of the receiver shows an energy per bit less than 6 pJ/bit. To the knowledge of the authors, the detailed transceiver is the first system proposed as an alternative to PCI express wireline links and it can be a future solution.

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