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A method for threshold voltage extraction in junctionless MOSFETs using the derivative of transconductance-to-current ratio

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ABSTRACT

In this paper, using numerical simulations, analytical modeling and experimental data, we validate the applicability of the transconductance-to-current ratio (g_m/I_D) derivative ($d(g_m/I_D)/dV_G$) method for extracting the threshold voltage (V_{TH}) in junctionless (JL) MOSFETs and show its advantages over the commonly-used transconductance derivative (or double derivative of drain current) method ($dg_m/dV_G \equiv d^2I_D/dV_G{}^2$). It is shown that, although both methods are based on the same theoretical V_{TH}-criterion, the $d(g_m/I_D)/dV_G$ method is more accurate than the $d^2I_D/dV_G{}^2$ method due to its lesser sensitivity to the gate-voltage-dependent mobility and series resistance parasitic effects, being particularly important in JL MOSFETs.

1. Introduction

Junctionless (JL) MOSFETs are presently considered to be one of the best candidates for further downscaling of CMOS devices in the nanometer region, due to their simple and flexible fabrication combined with excellent short-channel performance [1–4]. The JL MOSFETs feature a high channel doping, being the same as in source/drain (S/D) regions, and a thin-film or multi-gate, nanowire-like structure needed to provide full depletion of the carriers in the off-state of the device. Although electrical characteristics of JL MOSFETs are similar to those of inversion-mode (IM) MOSFETs, the operation of both types of the devices is not the same. In contrast to IM MOSFETs, in the on-state JL MOSFETs show two operation modes featuring different conduction mechanisms: (a) bulk conduction mode, in which the current flows in undepleted semiconductor volume, and (b) surface accumulation mode. This is similar to accumulation-mode (AM) silicon-on-insulator (SOI) MOSFETs [5], but AM transistors feature a lower doped channel and, as a result, a lower contribution of bulk conduction than JL devices. Because of these different conduction mechanisms, the traditional techniques commonly used for electrical characterization of IM MOSFETs are often inapplicable or leading to erroneous results in the case of JL transistors [6,7]. Therefore, there is a necessity to develop specific methods for the electrical characterization and parameter extraction of JL MOSFETs.

The threshold voltage (V_{TH}) which defines the device turn-on, is a critical parameter for any MOS transistor. Thus, an accurate and unambiguous V_{TH} determination from the experimental characteristics is very important for CMOS device and circuit analysis, design and modeling. In IM MOSFETs, the threshold voltage corresponds to the transition from weak to strong inversion regime, i.e., from exponential to linear variation of the inversion charge with the gate voltage. In JL MOSFETs, the threshold voltage characterizes the transition from full depletion to partial depletion regime. In the partial depletion regime, the mobile charge (Q_m) varies non-linearly with the gate voltage (V_G). As a result, the linear extrapolation methods, such as a linear extrapolation of the drain current (I_D) versus V_G characteristics [8,9] and the *Y*-function method [10], which are widely used for the V_{TH} extraction in IM MOSFETs, cannot be applied for extracting V_{TH} in JL transistors. In JL and AM MOSFETs, it is standard practice to determine the threshold voltage by the transconductance (g_m) derivative (or second derivative of the drain current) method, in which V_{TH} characterizing the onset of bulk conduction is defined from the position of the first maximum of $d^2I_D/dV_G{}^2$, whereas the position of the second is used for extracting the flat-band voltage (V_{FB}) [6,11]. Herewith it is assumed that peak positions of $d^2I_D/dV_G{}^2$ coincide with those of the second derivative of the mobile carrier charge, $d^2Q_m/dV_G{}^2$. However, as shown in our previous publications [12,13], the positions of the maxima of $d^2I_D/dV_G{}^2$ in inversion-mode MOSFETs are influenced by the parasitic effects of the gate-voltage-dependent mobility and the source/drain (S/D) series resistance, which results in uncertainty of the extracted V_{TH}

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values. These parasitic effects are expected to be significant in JL transistors. The above detrimental effects can be eliminated by using the capacitance derivative method [14]; however, it is not appropriate for nano-scale small-area devices.

In [15] it has been proposed to determine V_{TH} in the JL MOSFETs from the gate voltage value, at which transconductance-to-current ratio g_m/I_D is equal to one half of its maximum value, which is shown to correspond to the condition of the equality of drift and diffusion drain current components. However, such V_{TH} extraction is applicable only when the subthreshold behavior of the device is close to ideal, and the g_m/I_D vs. V_G curve shows a well-defined plateau in the range of maximum, whereas it is often distorted due to gate-induced drain leakage, short-channel effects, etc. [16].

Previously, we have proposed the transconductance-to-current ratio (g_m/I_D) derivative method for the experimental determination of the threshold voltage in inversion-mode MOSFETs, in which V_{TH} is defined from the gate voltage corresponding to the minimum of the $d(g_m/I_D)/dV_G$ versus V_G function [12]. It has been shown that, though the $d(g_m/I_D)/dV_G$ method is based on the same theoretical V_{TH}-criterion as the $d^2I_D/dV_G{}^2$ method, it is however much less affected by the parasitic effects of the series resistance and gate-voltage-dependent mobility than the $d^2I_D/dV_G{}^2$ method [13]. Moreover, the $d(g_m/I_D)/dV_G$ method can be used both in linear and saturation regimes [17]. In contrast to the capacitance derivative method, it is applicable to any nano-scale devices.

In this work, using analytical modeling, simulations and experimental data, we prove that the $d(g_m/I_D)/dV_G$ method is valid for the determination of the threshold voltage in JL MOSFETs, though the principle of their operation is essentially different from that of IM MOSFETs. Then, we demonstrate advantages of the proposed method compared to the $d^2I_D/dV_G{}^2$ method.

2. Method validation

2.1. Analytical modeling

The goal of our analytical modeling is to show that, in the long-channel JL MOSFETs in the case of constant mobility and very small drain voltage, the minimum of the derivative of g_m/I_D in respect to V_G is observed at the same gate voltage as the first maximum of the second derivative of the mobile carrier density, or the second derivative of the drain current. In our modeling, we use the derivations of previously developed analytical models for JL MOSFETs [18–21]. Here, we assume a long-channel, n-type symmetric Double-Gate (DG) JL MOSFET with silicon body (Fig. 1).

Then, we assume a very small drain voltage ($V_D \to 0$), so that the channel potential can be considered independent of the position along the gate length. With this assumption, the Poisson equation for the n-type device with channel doping concentration N_D can be written as:

$$\frac{d^2\phi}{dx^2} = \frac{q \cdot N_D}{\varepsilon_{Si}}\left(e^{\frac{\phi}{\varphi_t}} - 1\right) \tag{1}$$

where $\phi_t = kT/q$ is the thermal potential; ε_{Si} is the permittivity of the channel material; other symbols have their usual meaning. Integrating

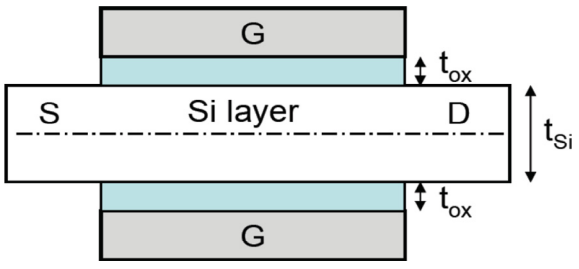

Fig. 1. Schematic representation of a DG JL MOSFET.

from the middle of the channel thickness ($x = 0$) to the surface ($x = t_{Si}/2$) gives:

$$\left[\left.\frac{d\phi}{dx}\right|_{x=\frac{t_{Si}}{2}}\right]^2 = \frac{2 \cdot q \cdot N_D \cdot \varphi_t}{\varepsilon_{Si}}\left(e^{\frac{\phi_s}{\varphi_t}} - e^{\frac{\phi_0}{\varphi_t}} - \frac{\phi_s - \phi_0}{\varphi_t}\right), \tag{2}$$

where φ_s and φ_0 are, respectively, the potentials at the surface and at the middle of the semiconductor film thickness. With the use of parabolic potential approximation, which is justified in JL MOSFETs in the subthreshold region and around threshold, the potential in the channel region can be expressed as [18]:

$$\phi(x) = \frac{4x^2}{t_{Si}^2} \cdot (\phi_s - \phi_0) + \phi_0. \tag{3}$$

From the boundary condition and Gauss' law as well as the potential balance in a MOS structure, for the symmetric DG device, we can write [18–20]:

$$\begin{aligned} -C_{ox}(V_G - V_{FB} - \phi_s) &= -\varepsilon_{Si}\left.\frac{d\phi}{dx}\right|_{x=\frac{t_{Si}}{2}} = \frac{4\varepsilon_{Si}}{t_{Si}}(\phi_0 - \phi_s) = \frac{1}{2}Q_{tot} \\ &= Q_m - \frac{Q_{dop}}{2} \end{aligned} \tag{4}$$

where C_{ox} is the gate dielectric capacitance per unit gate area, V_{FB} is the flat band voltage, t_{Si} is the thickness of the semiconductor film body, Q_{tot} the total charge density, $Q_{dop} = q \cdot N_D \cdot t_{Si}$ is the dopant charge density, and Q_m is half of the charge density of mobile carriers per unit gate area.

Differentiating (4) twice with respect to V_G gives the relationship between the second derivative of the mobile charge density d^2Q_m/dV_G^2 and the second derivative of the surface potential, $d^2\phi_s/dV_G^2$:

$$\frac{d^2Q_m}{dV_G^2} = -C_{ox}\frac{d^2\phi_s}{dV_G^2} \tag{5}$$

Using (4) and (5), we can obtain the relationship between the second derivative of the mobile charge density, d^2Q_m/dV_G^2, and the second derivative of the potential in the middle of the semiconductor body, $d^2\phi_0/dV_G^2$:

$$\frac{d^2Q_m}{dV_G^2} = -2 \cdot \left(\frac{t_{Si}}{4\varepsilon_{Si}} + \frac{1}{C_{ox}}\right)^{-1}\frac{d^2\phi_0}{dV_G^2} = -C_{eff}\frac{d^2\phi_0}{dV_G^2}, \tag{6}$$

where $C_{eff} = \left(\frac{t_{Si}}{4\varepsilon_{Si}} + \frac{1}{C_{ox}}\right)^{-1}$ is the effective gate capacitance for the depletion regime in the symmetric DG JL MOSFET (independent on V_G).

From (5) and (6) it is seen that d^2Q_m/dV_G^2differs from $d^2\phi_s/dV_G^2$ and $d^2\phi_0/dV_G^2$ only by a constant factor (independent on V_G), and thus all these three functions should exhibit an extremum at the same V_G value, at which the condition of equality to zero of their third derivatives is met. Therefore, the threshold voltage extracted by the $d^2I_D/dV_G{}^2$ method in an ideal JL MOSFET corresponds to the inflection point in the rate of the variation of the mobile charge density Q_m, surface potential φ_s, and potential at the middle of the semiconductor channel φ_0.

Now, using modeling results obtained in [18,20], we show that, under our assumptions (i.e., a constant carrier mobility and very low V_D), the $d(g_m/I_D)/dV_G$ versus V_G function should also show an extremum at the same V_G value, as $d^2\phi_0/dV_G^2$ and d^2Q_m/dV_G^2.

According to [18], the mobile charge density Q_m in DG JL MOSFET in the subthreshold and depletion regime at very low drain voltage ($V_D \to 0$) can be expressed as:

$$Q_m = qN_{dop}\int_0^{t_{Si}/2}\exp\left(\frac{\phi(x)}{\varphi_t}\right)dx \approx \frac{1}{2}\sqrt{\pi \cdot Q_{dop} \cdot Q_{cp}}\exp\left(\frac{\phi_0}{\varphi_t}\right) = Q_0\exp\left(\frac{\phi_0}{\varphi_t}\right) \tag{7}$$

where $Q_{cp} = 2\varepsilon_{Si}\varphi_t/t_{Si}$, $Q_0 = \frac{1}{2}\sqrt{\pi \cdot Q_{dop} \cdot Q_{cp}}$. Assuming mobility independence on V_G and considering (7), we can express the transconductance-to-current ratio g_m/I_D as follows:

$$\frac{g_m}{I_D} = \frac{1}{Q_m}\frac{dQ_m}{dV_G} = \frac{d(\ln Q_m)}{dV_G} = \frac{d}{dV_G}\left(\ln Q_0 + \frac{\phi_0}{\varphi_t}\right) = \frac{1}{\varphi_t}\frac{d\phi_0}{dV_G} \tag{8}$$

Differentiating (8) with respect to V_G gives:

$$\frac{d}{dV_G}\left(\frac{g_m}{I_D}\right) = \frac{1}{\varphi_t}\frac{d^2\phi_0}{dV_G{}^2}. \tag{9}$$

Combining (9) with (6) yields:

$$\frac{d}{dV_G}\left(\frac{g_m}{I_D}\right) = -\frac{1}{\varphi_t C_{eff}}\frac{d^2Q_m}{dV_G{}^2}. \tag{10}$$

As follows from (10), the derivative of the transconductance-to-current ratio, $d(g_m/I_D)/dV_G$, differs from d^2Q_m/dV_G^2only by a factor $(-1/\varphi_t C_{eff})$, and therefore the peak positions of these two functions along the V_G axis should coincide.

The same result is obtained using the charge-based models for long-channel DG and cylindrical gate-all-around (GAA) JL MOSFETs developed in [20–22]. Based on findings of [20,21], the charge-control equation for long-channel DG and GAA JL MOSFETs in the depletion region around threshold can be approximated by the following expression:

$$\frac{V_G^* + \frac{Qdop}{2C_{ox}} - V}{\varphi_t} + \frac{Q_{dop}}{4Q_{cp}} = \ln\left(\frac{Q_m}{2Q_{cp}}\right) + \frac{Q_m}{Q_{eq}} \tag{11}$$

where $V_G^* = V_G - V_{FB}$, V is the position-dependent channel potential, for DG devices $Q_{cp} = 2\varepsilon_{Si}\varphi_t/t_{Si}$, $Q_{eq} = [(C_{ox}\varphi_t)^{-1} + (2Q_{cp})^{-1}]^{-1} = C_{eff}\varphi_t$, with C_{eff} the effective gate capacitance in depletion region, for a DG device, $C_{eff} = \left(\frac{t_{Si}}{4\varepsilon_{Si}} + \frac{1}{C_{ox}}\right)^{-1}$ [20]; for cylindrical GAA devices, $C_{eff} = \left(\frac{1}{C_{ox}} + \frac{1}{4\pi\varepsilon_{Si}}\right)^{-1}$ [22,23].

On the assumption of very low V_D, when the channel potential can be considered uniform over the length, differentiating (11) in respect to V_G yields:

$$\frac{dQ_m}{dV_G} = \frac{1}{(dV_G/dQ_m)} = \frac{1}{\varphi_t}\frac{Q_m}{(1 + Q_m/Q_{eq})}. \tag{12}$$

By differentiating (12), we have:

$$\frac{d^2Q_m}{dV_G{}^2} = \left[\frac{d}{dQ_m}\left(\frac{dQ_m}{dV_G}\right)\right]\cdot\frac{dQ_m}{dV_G} = \frac{Q_m}{\varphi_t{}^2(1 + Q_m/Q_{eq})^3}. \tag{13}$$

Next, assuming a constant mobility and using (12), we get the following expression for g_m/I_D in terms of Q_m and Q_{eq}:

$$\frac{g_m}{I_D} = \frac{1}{Q_m}\frac{dQ_m}{dV_G} = \frac{1}{\varphi_t}\frac{1}{(1 + Q_m/Q_{eq})}. \tag{14}$$

Differentiating (14) with considering (12), we obtain:

$$\frac{d(g_m/I_D)}{dV_G} = -\frac{1}{\varphi_t^2 Q_{eq}}\frac{Q_m}{(1 + Q_m/Q_{eq})^3} \tag{15}$$

which, within a factor $(-1/Q_{eq}) = (-1/\varphi_t C_{eff})$, coincides with $d^2Q_m/dV_G{}^2$ [see (13)]; i.e., we have the same result as previously obtained [see (10)].

From the foregoing modeling results, it follows that in JL MOSFETs, the peak position of the derivative of g_m/I_D in respect to V_G can be used for the threshold voltage extraction with the V_{TH} criterion of the maximum of $d^2|Q_m|/dV_G{}^2$, as in the case of IM MOSFETs.

Now, we will find the value of Q_m in JL MOSFETs satisfying our V_{TH} criterion, which can be done by equating $d^3Q_m/dV_G{}^3$ or $d^2(g_m/I_D)/dV_G{}^2$ to zero. Differentiating (13) and using (12), we get:

$$\frac{d^3Q_m}{dV_G{}^3} = \frac{1}{\varphi_t^3}\frac{\left(1 - 2\frac{Q_m}{Q_{eq}}\right)Q_m}{\left(1 + \frac{Q_m}{Q_{eq}}\right)^5}. \tag{16}$$

Setting $d^3Q_m/dV_G{}^3 = 0$ in (16) gives the value of Q_m at threshold:

$$Q_m|_{V_G=V_{TH}} = \frac{1}{2}Q_{eq} = \frac{1}{2}C_{eff}\cdot\varphi_t. \tag{17}$$

Substituting (17) into (14) gives the value of g_m/I_D at threshold:

$$\left.\frac{g_m}{I_D}\right|_{V_G=V_{TH}} = \frac{2}{3}\cdot\frac{1}{\varphi_t} = \frac{2}{3}\left(\frac{g_m}{I_D}\right)_{\max}. \tag{18}$$

Thus, in the ideal long-channel DG JL MOSFET at very low V_D, the condition of the maximum of $d^2|Q_m|/dV_G{}^2$ corresponds to the point on the g_m/I_D vs. V_G curve where $d(g_m/I_D)/dV_G$ shows a minimum and where the value of g_m/I_D is equal to 2/3 of its maximum value, similar to that in IM MOSFETs [16]. However, the value of the mobile carrier density Q_m corresponding to this point is different in these two types of the devices; in JL MOSFETs, it is equal to $\frac{1}{2}C_{eff}\cdot\varphi_t$, whereas in inversion-mode MOSFETs, it is equal to $\frac{1}{2}C_{ox}\cdot\varphi_t$ [16]. Thus the mobile carrier density $N_m = |Q_m|/q$ at threshold condition satisfying the V_{TH} criterion of the maximum of $d^2N_m/dV_G{}^2$ in JL MOSFETs is:

$$N_m|_{V_G=V_{TH}} \approx \frac{1}{2q}\cdot C_{eff}\cdot\varphi_t \tag{19}$$

These findings provide a clearer view on the threshold voltage evaluated by the methods based on the criterion of the maximum of the second derivative of the mobile carrier density in JL MOSFETs.

The above modeling results are obtained on the assumption of a very low drain voltage ($V_D \to 0$), when the channel potential along the gate length can be considered to be constant. For larger drain voltages ($V_D > kT/q$), when the channel potential is position-dependent, the obtained modeling derivations should be valid at the source edge of the channel.

Though our modeling was performed for symmetric DG JL MOSFETs, we can expect that the main findings are valid for various types of multi-gate JL MOSFETs, considering the similarity of their charge-control models [20,21,24]. Below the predictions of analytical modeling will be verified by simulations.

2.2. Simulation results

Validation of modeling results was done using simulations for n-type silicon-based JL MOSFETs, featuring different structure (double-gate, single-gate, and tri-gate), different doping concentration ($N_D = 5 \times 10^{18}$ cm^{-3} and 1×10^{19} cm^{-3}), different thicknesses of the silicon channel, and different thicknesses of the gate oxide. The gate work function in our simulations was assumed to be 4.7 eV. The parameters of double-gate and single-gate long-channel JL MOSFETs were obtained by simulations based on numerical solution of the two-carrier, 1-D Poisson equation for silicon-on-insulator (SOI) MOS structures with proper boundary conditions, using MATHCAD. The parameters of tri-gate nanowire (NW) JL MOSFETs were obtained by 3-D classical simulations using the Synopsis Sentaurus Device Simulator [25].

Fig. 2(a–c) show d^2N_m/dV_G^2 and $[-d^2(\ln N_m)/dV_G^2]$ versus V_G dependencies normalized to their peak values for long-channel single-gate (Fig. 2(a)), double-gate (Fig. 2(b), and tri-gate nanowire (NW) JL silicon-on-insulator (SOI) MOSFETs (Fig. 2(c)) with two different channel doping concentrations, $N_D = 5 \times 10^{18}$ and 1×10^{19}/cm^3. It can be seen from Fig. 2(a–c) that for different device configurations and different channel doping levels, there is a coincidence of the peak position of $[-d^2(\ln N_m)/dV_G^2]$ with that of the lower-V_G maximum of d^2N_m/dV_G^2, as predicted by the analytical modeling.

Fig. 3 presents normalized d^2N_m/dV_G^2, $d^2\phi_s/dV_G^2$, $d^2\phi_0/dV_G^2$ and $[-d^2(\ln N_m)/dV_G^2]$ as a function of the gate voltage obtained by 1-D simulations for a DG JL MOSFET with doping concentration of 5×10^{18}/cm^3, silicon film thickness of 20 nm, and gate oxide thickness of 2 nm. One can see that all the above functions reach their peak values at the

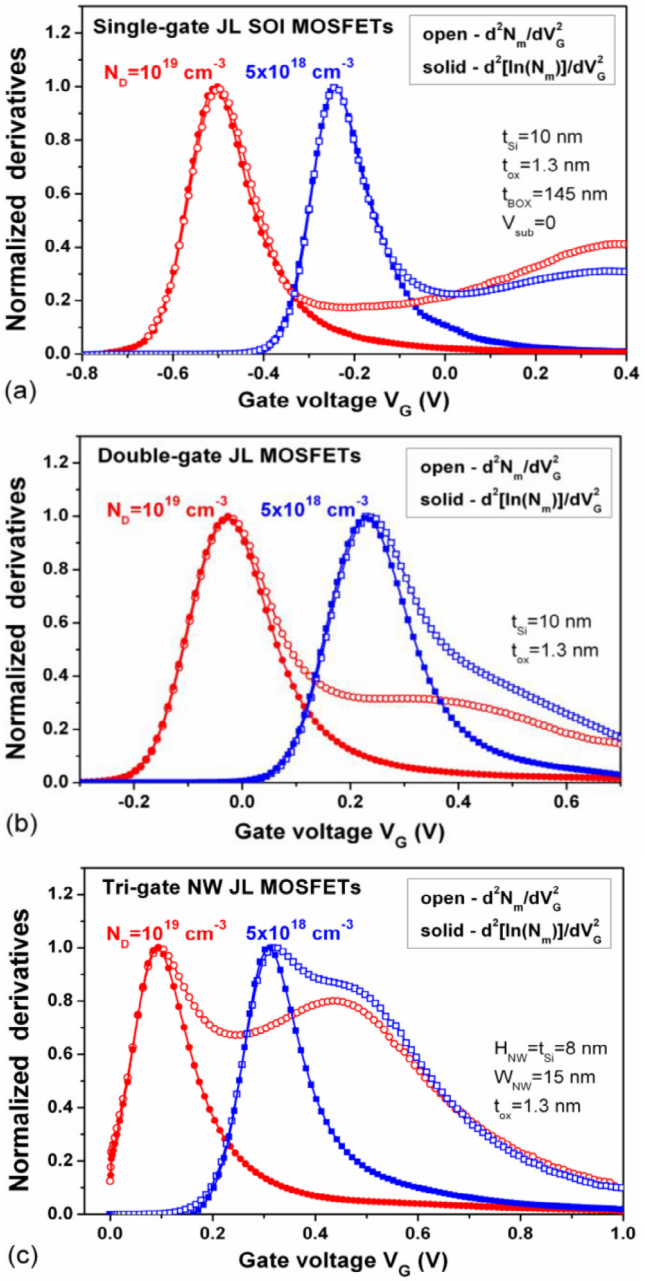

Fig. 2. Normalized d^2N_m/dV_G^2 and $[-d^2(\ln N_m)/dV_G^2]$ versus gate voltage for long-channel JL MOSFETs with different channel doping concentrations, $N_D = 5 \times 10^{18}$ and $1 \times 10^{19}/\text{cm}^3$, and different device configurations: (a) single-gate JL SOI MOSFETs with $t_{Si} = 10$ nm, $t_{ox} = 1.3$ nm and $t_{BOX} = 145$ nm; (b) symmetric double-gate JL MOSFET with $t_{Si} = 10$ nm and $t_{ox} = 1.3$ nm; (c) tri-gate NW JL SOI MOSFETs featuring $H_{NW} = t_{Si} = 8$ nm, $W_{NW} = 15$ nm, $t_{ox} = 1.3$ nm, $t_{BOX} = 145$ nm, and $L = 100$ nm.

same gate voltage, which is in a complete agreement with foregoing modeling predictions (see relationships (5), (9) and (10)).

Results of 1-D simulations for a DG JL MOSFET with the same parameters as in Fig. 3 are also presented in Fig. 4(a–d). Shown in Fig. 4(a, b) are the mobile carrier density N_m (per unit gate area) versus V_G dependence and its second derivative $d^2N_m/dV_G{}^2$, whereas shown in Fig. 4(c), (d) are the g_m/I_D versus V_G function and its derivative, being in the case of the constant mobility and very small drain voltage ($V_D \rightarrow 0$) equal to $d(\ln N_m)/dV_G$ and $d^2(\ln N_m)/dV_G{}^2$, respectively.

Fig. 5(a–d) present similar results for DG JL MOSFETs with gate oxide thickness of 1.3 nm and various silicon film thicknesses,

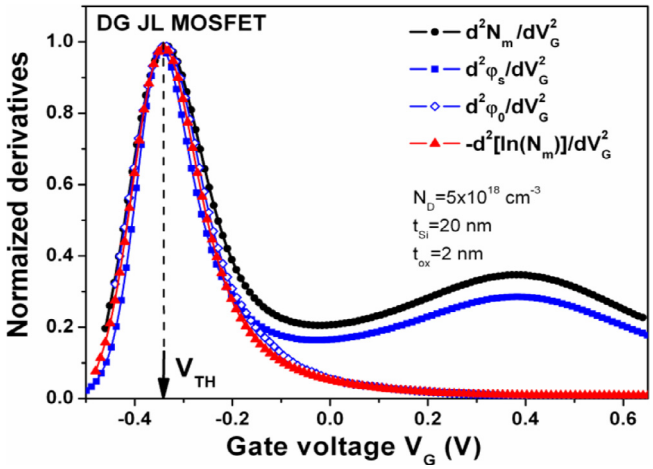

Fig. 3. Simulated d^2N_m/dV_G^2, $d^2\phi_s/dV_G^2$, $d^2\phi_0/dV_G^2$, and $[-d^2(\ln N_m)/dV_G^2]$ normalized to their peak values as a function of the gate voltage in a double-gate JL MOSFET, showing the coincidence of the peak positions of the above functions. The device parameters are $t_{Si} = 20$ nm, $t_{ox} = 2$ nm, and $N_D = 5 \times 10^{18}/\text{cm}^3$.

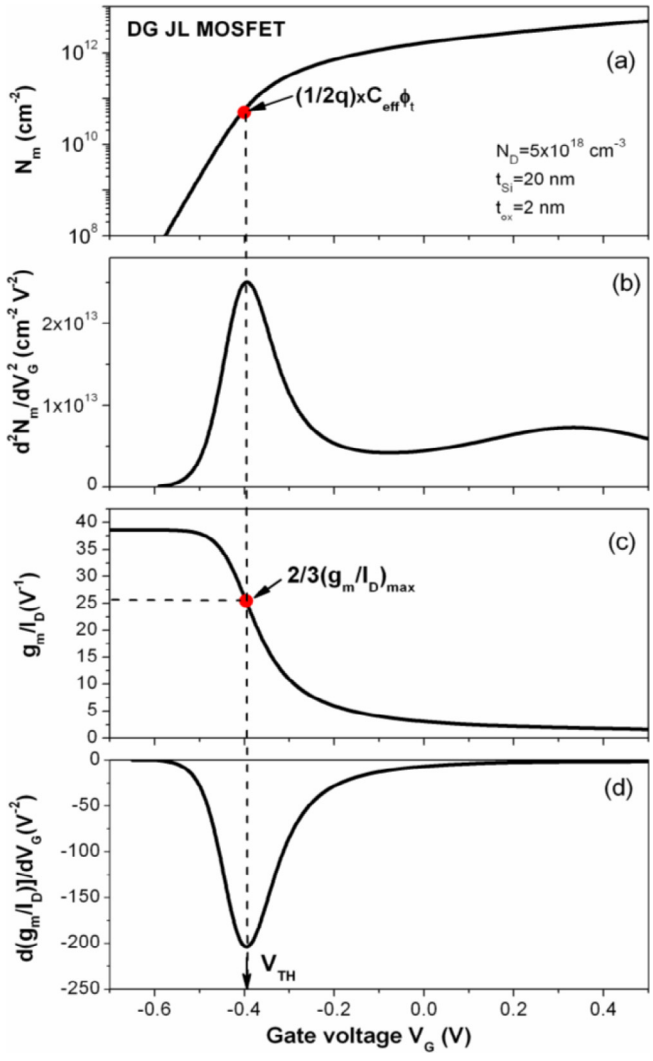

Fig. 4. Results of simulations for the long-channel symmetric DG JL MOSFET: (a) the mobile carrier density N_m per unit gate area versus gate voltage; (b) the second derivative of the mobile carrier density in respect to the gate voltage d^2N_m/dV_G^2; (c) g_m/I_D versus V_G function on the assumption of constant mobility and $V_D \rightarrow 0$; (d) $d(g_m/I_D)/dV_G$ versus V_G. The device parameters are the same as in Fig. 3.

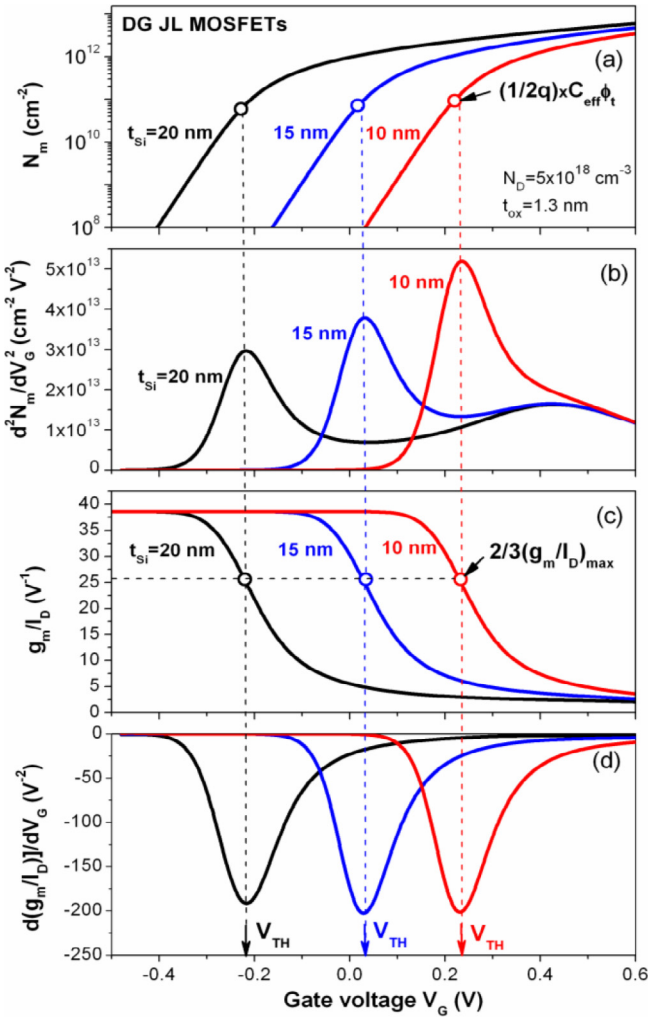

Fig. 5. The same as in Fig. 4 for DG JL MOSFETs with gate oxide thickness t_{ox} = 1.3 nm and different thicknesses of the silicon film, t_{Si} = 10 nm, 15 nm, and 20 nm.

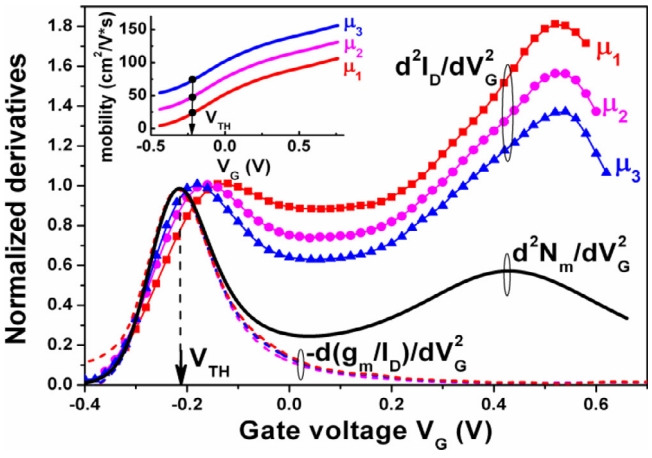

Fig. 6. Normalized simulated "low-V_D" d^2I_D/dV_G^2, $[-d(g_m/I_D)/dV_G]$, and d^2N_m/dV_G^2 as a function of V_G for the long-channel DG JL MOSFET, obtained on the assumption of the electron mobility increasing with V_G as shown in the inset, illustrating the shift of the peak position of d^2I_D/dV_G^2 relative to that of d^2N_m/dV_G^2 and coincidence of the peak positions of $[-d(g_m/I_D)/dV_G]$ and d^2N_m/dV_G^2 (The device parameters are N_D = 5 × 10^{18}/cm^3, t_{ox} = 1.3 nm, t_{Si} = 20 nm).

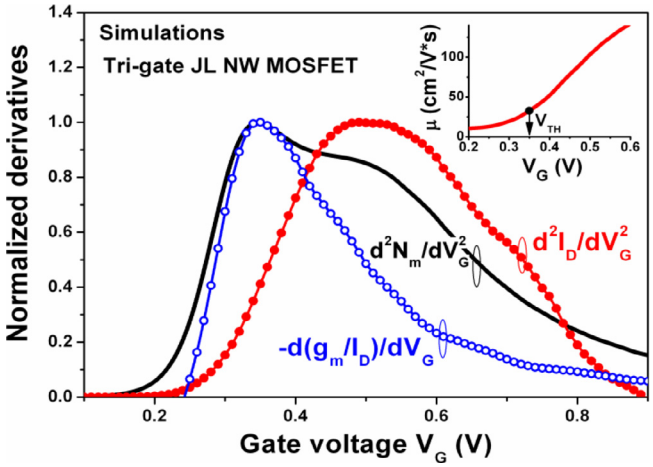

Fig. 7. Normalized "low-V_D" d^2I_D/dV_G^2, $[-d(g_m/I_D)/dV_G]$, and d^2N_m/dV_G^2 as a function of V_G in the long-channel tri-gate NW JL SOI MOSFET, obtained by simulations assuming mobility increasing with V_G as shown in the inset, demonstrating severe distortion of the shape of the d^2I_D/dV_G^2 curve (N_D = 5 × 10^{18}/cm^3, H_{HW} = t_{Si} = 8 nm, W_{NW} = 20 nm, t_{ox} = 1.3 nm).

t_{Si} = 10 nm, 15 nm, and 20 nm. Figs. 4 and 5 clearly demonstrate that in the JL devices with different gate oxide thicknesses and different channel thicknesses, the gate voltage corresponding to the maximum of d^2N_m/dV_G^2 is coincident with that of the minimum of $d(g_m/I_D)/dV_G$. Therewith, at this gate voltage, the value of the carrier density is very close to that given by (19), i.e., $N_m|_{\max(N_m)''} = N_m|_{\min[d(g_m/I_D)/dV_G]} \approx (1/2q)\cdot C_{eff}\cdot\varphi_t$, and the value of g_m/I_D is very close to 2/3 of its maximum value, as predicted by (18).

Thus, simulation results entirely confirm modeling predictions. In particular, they confirm that in long-channel JL MOSFETs with different geometries and device parameters, the position of the minimum of $d^2[\ln(N_m)]/dV_G^2$, being for constant mobility and very small V_D identical to $d(g_m/I_D)/dV_G$, coincides with the position of the lower-V_G peak of d^2N_m/dV_g^2, being identical to d^2I_D/dV_G^2. It is therefore concluded that the peak position of $[-d(g_m/I_D)/dV_G]$ can be used for the V_{TH} extraction in JL MOSFETs, similarly to that of d^2I_D/dV_G^2.

The finding that at the position of min$[d(g_m/I_D)/dV_G]$, coinciding with that of max$[d^2N_m/dV_G^2]$, the value of g_m/I_D is equal to 2/3 of its maximum value, can be used as an alternative method for the experimental V_{TH} extraction in JL MOSFETs with the V_{TH} criterion of the maximum of d^2N_m/dV_G^2. However, such V_{TH} extraction is possible only when the g_m/I_D versus V_G curve has a distinct plateau in the subthreshold region, not distorted by parasitic effects, such as gate-induced drain leakage (GIDL), V_G-dependent mobility, short-channel effects, etc.

The foregoing modeling and simulation results are obtained on the assumption that the carrier mobility (μ) does not depend on the gate voltage. However, as shown in previous experimental and theoretical studies [26–29], the carrier mobility in heavily doped JL devices in a wide range of operation, and in particular around threshold, is governed by Coulomb scattering at ionized impurities, which is characterized by mobility increase with gate voltage.

In Fig. 6, we present normalized d^2N_m/dV_G^2, d^2I_D/dV_G^2 and $[-d(g_m/I_D)/dV_G]$ versus V_G dependencies for a long n-channel DG JL MOSFET at very low drain voltage, obtained on the assumption of the electron mobility increasing with V_G as shown in the inset, and as is typical for JL MOSFETs in bulk conduction regime [26,27]. Here the "low-V_D" drain current was calculated as:

$$I_D(V_G) = q\cdot\frac{W}{L}\cdot\mu(V_G)\cdot N_m(V_G)\cdot V_D, \tag{20}$$

where $\mu(V_G)$ is the V_G-dependent carrier mobility, W/L is width-to-length ratio taken to be equal to 1, and V_D is the drain voltage taken to be equal to 0.001 V. As is seen from Fig. 6, in the case of mobility

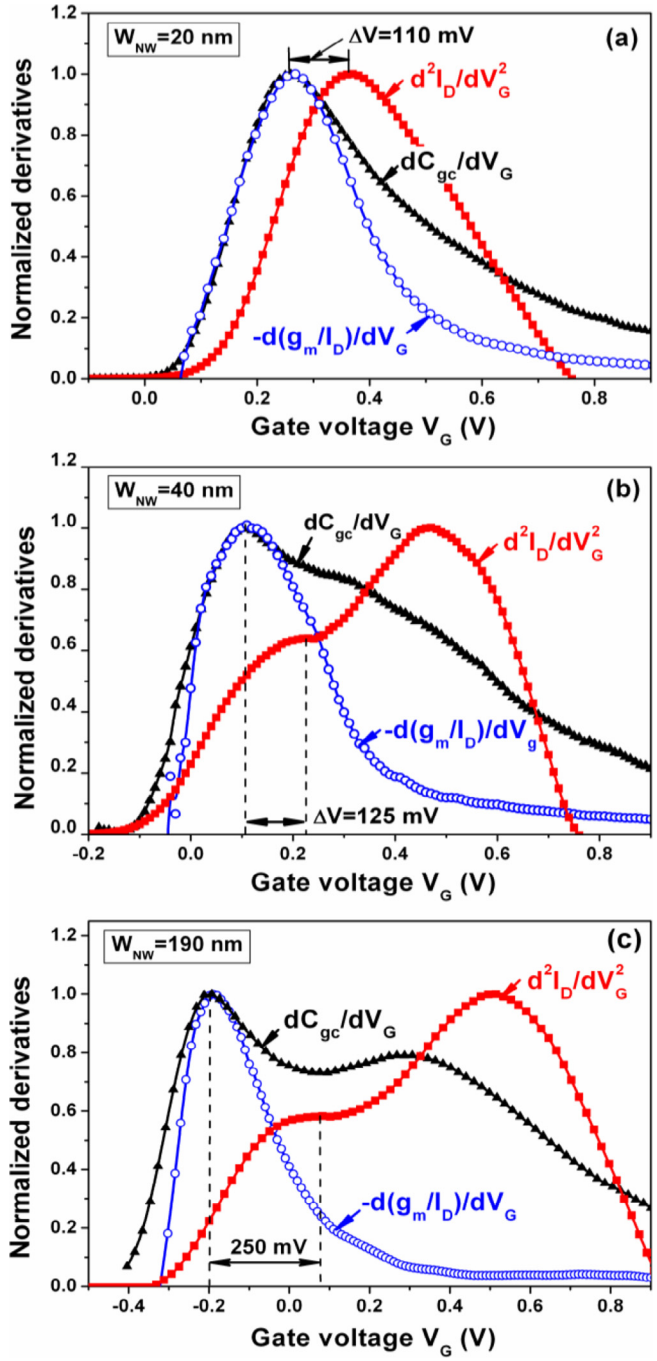

Fig. 8. Comparison of experimental determinations of the threshold voltage by d^2I_D/dV_G^2, $d(g_m/I_D)/dV_G$ and dC_{gc}/dV_G methods for 10 μm-long tri-gate NW JL MOSFETs with different NW widths: (a) W_{NW} = 20 nm; (b) W_{NW} = 40 nm; (c) W_{NW} = 190 nm (V_D = 10 mV, H_{HW} = t_{Si} = 10 nm, t_{EOT} = 1.3 nm).

increase with V_G, the peak positions of d^2I_D/dV_g^2 are shifted relative to that of d^2N_m/dV_G^2 towards higher V_G values; the lower the mobility value at V_{TH}, the larger this shift.

In JL MOSFETs with thin or relatively low-doped channels, featuring two closely located humps of d^2N_m/dV_G^2, mobility increase with V_G can result in severe distortion of the shape of the d^2I_D/dV_G^2 curve, transforming it to a one-hump curve, as shown in Fig. 7. Contrarily, the peak position of $[-d(g_m/I_D)/dV_G]$ in Figs. 6 and 7 remains almost unchanged and coincides with that of the lower-V_G peak of d^2N_m/dV_G^2. These results indicate that in long-channel JL MOSFETs, the $dg_m/dV_G = d^2I_D/dV_G^2$ method should give overestimated V_{TH} values due to

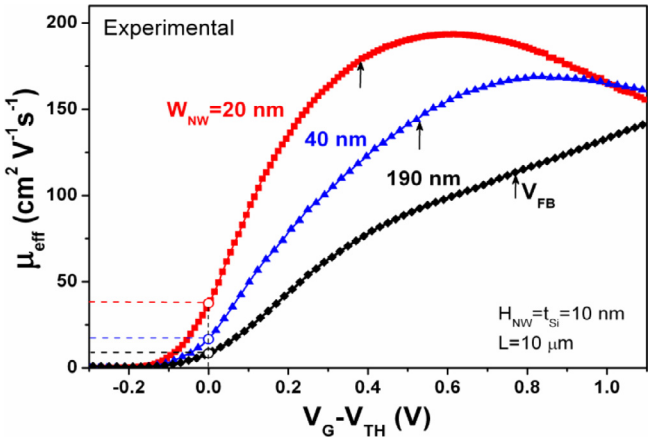

Fig. 9. The effective electron mobility extracted by the split C-V technique in 10-μm-long tri-gate NW JL MOSFETs with different nanowire widths plotted as a function of gate voltage overdrive (H_{HW} = t_{Si} = 10 nm, t_{EOT} = 1.3 nm).

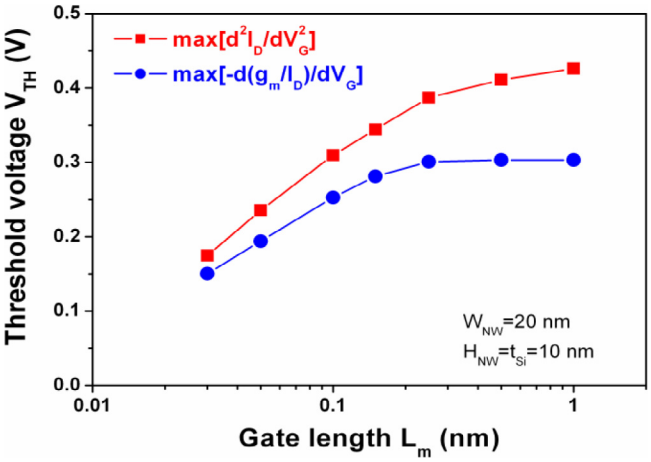

Fig. 10. The gate length dependence of the threshold voltage extracted by d^2I_D/dV_G^2 and $d(g_m/I_D)/dV_G$ methods in one-fin tri-gate NW JL MOSFETs with nanowire width of 20 nm (V_D = 20 mV, H_{NW} = t_{Si} = 10 nm, t_{EOT} = 1.3 nm).

mobility increase with V_G around threshold, while the $d(g_m/I_D)/dV_G$ method should be more accurate due to its much lower sensitivity to the V_G-dependent mobility.

3. Experimental results

The experimental data presented in this study have been obtained on tri-gate nanowire (NW) JL MOSFETs fabricated at CEA-LETI using (1 0 0) SOI wafers with a 145-nm-thick buried oxide and a 10-nm-thick silicon film. Details of the device fabrication process are presented in [30]. The target channel doping concentration in the measured devices was $\approx 10^{19}/cm^3$. The real active doping concentration in the channel region evaluated by the method proposed in [31] was found to be $\approx 5 \times 10^{18}$ cm^{-3}. An additional S/D implantation with doping concentration of $\approx 10^{20}/cm^3$ was performed to reduce S/D resistance. The gate stack consisted of HfSiON with equivalent oxide thickness EOT = 1.3 nm and a TiN/Poly-Si gate electrode.

The measurements were carried out on multi-fin tri-gate NW transistors with the nanowire height H_{HW} = t_{Si} = 10 nm and nanowire widths W_{NW} varied from 20 nm to 190 nm. Gate-to-channel capacitance (C_{gc}) measurements were performed at f = 300 kHz. Drain current measurements used in this study were carried out at V_D = 10 mV (i.e, $V_D < \phi_t/2$). All measurements were performed at room temperature and zero substrate bias (V_{sub} = 0).

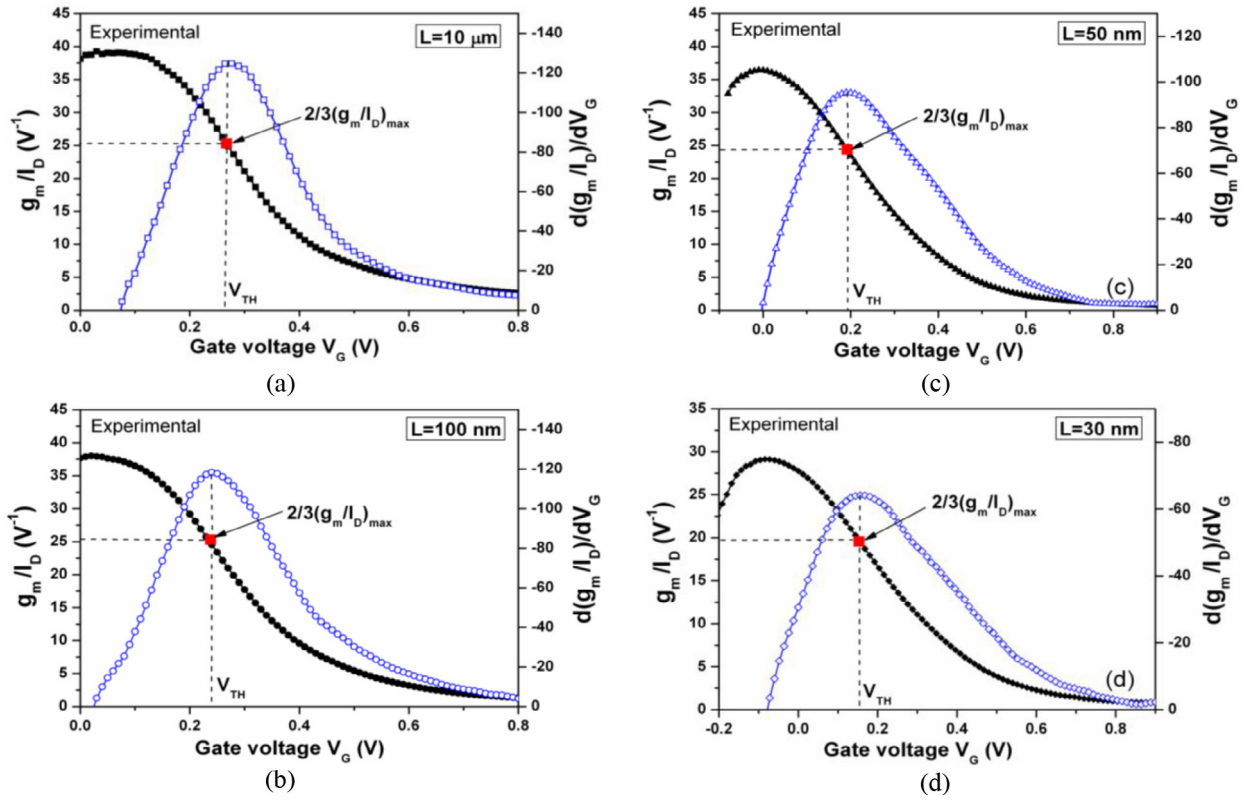

Fig. 11. Experimental g_m/I_D versus V_G dependencies and their derivatives for one-fin NW JL MOSFETs with different gate lengths: (a) L = 10 μm; (b) L = 100 nm; (c) L = 50 nm; (d) L = 30 nm (V_D = 20 mV, H_{NW} = t_{Si} = 10 nm, t_{EOT} = 1.3 nm).

To verify experimentally the findings of modeling and simulations, we performed a comparison of the results of the V_{TH} extraction in tri-gate nanowire (NW) JL MOSFETs by $d^2I_D/dV_G{}^2$ and $d(g_m/I_D)/dV_G$ methods with results of the gate-to-channel capacitance derivative (dC_{gc}/dV_G) method which is insensitive to the V_G-dependent mobility. Fig. 8 shows such a comparison of experimental V_{TH} determinations by dC_{gc}/dV_G, $d^2I_D/dV_G{}^2$ and $d(g_m/I_D)/dV_G$ methods for 10 μm-long multi-fin JL NW devices with different NW widths, W_{NW} = 20 nm, 40 nm, and 190 nm. One can see that, as expected, the $d(g_m/I_D)/dV_G$ method yields V_{TH} values very close to those obtained by the dC_{gc}/dV_G method, being unaffected by the V_G-dependent mobility, whereas the $d^2I_D/dV_G{}^2$ method gives noticeably higher V_{TH} values than dC_{gc}/dV_G. Note that the discrepancy between results of $d^2I_D/dV_G{}^2$ and dC_{gc}/dV_G methods is larger for larger NW widths, namely, it is ≈100 mV for W_{NW} = 20 nm, ≈125 mV for W_{NW} = 40 nm, and ≈250 mV for W_{NW} = 190 nm. It should also be noted that in the long-channel JL MOSFETs the observed difference between V_T extractions by $d^2I_D/dV_G{}^2$ and dC_{gc}/dV_G methods is typically much larger than that in long-channel undoped FinFETs or ultra-thin-body SOI MOSFETs, where this difference is typically 30–40 mV [13].

Based on findings of simulations presented in Figs. 6 and 7 and analytical modeling in [13], the observed difference between V_{TH} extractions by the $d^2I_D/dV_G{}^2$ and dC_{gc}/dV_G methods is attributable to mobility increase with V_G around threshold due to impurity Coulomb scattering, which shifts the peak position of $d^2I_D/dV_G{}^2$ to the higher V_G values. As shown in [13], the shift of the maximum of $d^2I_D/dV_G{}^2$ relative to the maximum of $d^2N_m/dV_G{}^2$ caused by mobility variation with V_G is inversely proportional to the mobility value at threshold $\mu(V_G = V_{TH})$. Thus, the error in the V_{TH} extraction by the $d^2I_D/dV_G{}^2$ method related to the V_G-dependent mobility should be larger in the devices featuring lower μ values around threshold. Therefore, the larger discrepancy between the methods in JL MOSFETs with larger nanowire widths in Fig. 8 can be explained by the lower mobility at V_{TH} in wider devices. The latter is confirmed by the mobility results for different nanowire widths presented in Fig. 9, showing the effective electron mobility μ_{eff} extracted by the split-CV technique as a function of gate voltage overdrive. The vertical arrows in Fig. 9 indicate flat-band conditions evaluated as proposed in [31].

As is seen from Fig. 9, in JL MOSFETs, in most of the operation range, including the bulk conduction region and around threshold, μ_{eff} increases with gate voltage, indicating the predominance of Coulomb scattering. Therewith in this range and at $V_G = V_{TH}$, the value of μ_{eff} is larger for smaller NW widths. Besides, in the devices with smaller NW widths, μ_{eff} increases sharper with gate voltage. This is explained by more effective screening of ionized impurities in narrow devices due to a higher free carrier concentration [26–29,32]. The lower mobility values near threshold also allow to explain the larger difference between V_{TH} extractions by $d^2I_D/dV_G{}^2$ and dC_{gc}/dV_G methods in heavily doped JL MOSFETs compared to undoped-channel SOI MOSFETs.

Thus, experimental results clearly demonstrate that, in long-channel JL MOSFETs, the $d^2I_D/dV_G{}^2$ method gives overestimated V_{TH} values due to mobility increase with V_G around threshold related to Coulomb scattering. It is expected that S/D series resistance, which can be represented as mobility decrease with gate voltage, would have the effect opposite to the mobility variation associated with Coulomb scattering. Indeed, as has been demonstrated in [33], series resistance effects in JL MOSFETS (which are enhanced with reducing the channel length) shift the peak positions of $d^2I_D/dV_G{}^2$ curves to lower V_G values. Therefore, it can be expected that the difference between the methods will decrease with decreasing the channel length. This is confirmed by the results in Fig. 10, which represents V_{TH} extracted by $d^2I_D/dV_G{}^2$ and $d(g_m/I_D)/dV_G$ methods in JL NW MOSFETs with W_{NW} = 20 nm as a function of the gate length. As a consequence of the combined effects of the V_G-dependent mobility and series resistance, the $d^2I_D/dV_G{}^2$ method gives an apparent stronger reduction of V_{TH} when decreasing the gate length, whereas the $d(g_m/I_D)/dV_G$ method, which is less sensitive to the above

parasitic effects, yields a weaker dependence of V_{TH} on the gate length.

To check experimentally whether it is possible to determine V_{TH} in JL MOSFETs from the point where $g_m/I_D = 2/3 \cdot (g_m/I_D)_{max}$, as predicted by modeling and simulations, in Fig. 11 we present the g_m/I_D versus V_G dependencies and their derivatives for different gate lengths, L = 10 μm, 100 nm, 50 nm, and 30 nm. Experimental results in Fig. 11 (a, b) show that in the 10-μm-long and 100-nm-long devices, the determination of V_{TH} from the peak position of $[-d(g_m/I_D)/dV_G]$ and from the point where $g_m/I_D = 2/3 \cdot (g_m/I_D)_{max} \approx 2/3 \cdot (1/\phi_t)$, gives indeed the same V_{TH} values. Surprisingly, in the devices with short channels (L = 50 nm and 30 nm), for which g_m/I_D in the subthreshold region is strongly lowered and distorted, at the point of maximum of $[-d(g_m/I_D)/dV_G]$ the value of g_m/I_D is also very close to $2/3 \cdot (g_m/I_D)_{max}$, though it is noticeably smaller than $2/3 \cdot (1/\phi_t)$. Nevertheless, we believe that, in the general case, the determination of V_{TH} from the position of the maximum of $[-d(g_m/I_D)/dV_G]$ is more reliable and accurate than that using $(g_m/I_D)_{max}$.

4. Conclusions

We have proposed a method for the experimental threshold voltage extraction in JL MOSFETs from the gate voltage corresponding to the minimum of the $d(g_m/I_D)/dV_G$ versus gate voltage function. Using analytical modeling and numerical simulations, we have shown that this method satisfies the criterion of the maximum of the second derivative of the mobile carrier density, i. e., the same physical criterion that underlies the $d^2I_D/dV_G{}^2$ method. Using simulations and experimental data, it has been demonstrated that in long-channel JL MOSFETs, the $d^2I_D/dV_G{}^2$ method gives strongly overestimated V_{TH} values due to mobility increase with gate voltage near threshold related to impurity Coulomb scattering. The errors in the V_{TH} extraction by the $d^2I_D/dV_G{}^2$ method related to the V_G-dependent mobility in JL MOSFETs are typically larger than in undoped-channel SOI MOSFETs, which is explained by lower mobility values at threshold in heavily doped JL devices. At the same time, simulation and experimental results demonstrate that the proposed $d(g_m/I_D)/dV_G$ method for the V_{TH} extraction in JL MOSFETs is significantly less affected by the mobility variation with V_G than the $d^2I_D/dV_G{}^2$ method, and thus it is more accurate and reliable.

Another interesting finding of modeling and simulations is that in the ideal JL MOSFETs at very low drain voltage, the value of g_m/I_D at the position of the minimum of $d(g_m/I_D)/dV_G$ is equal to 2/3 of its maximum value. This could be used as an alternative method for the V_{TH} extraction in JL MOSFETs with the V_{TH} criterion of the maximum of the second derivative of the carrier density. However, this method is not applicable when the subthreshold behavior of the device is distorted by the parasitic effects, such as gate-induced drain leakage, short-channel effects, etc. Thus the $d(g_m/I_D)/dV_G$ method seems to be preferable.

Acknowledgements

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