Design and fabrication of a novel power Si/SiC LDMOSFET for high temperature applications

P.M. Gammon [1a], F. Li [1], C.W. Chan [1], F. Gity [2], T. Trajkovic [3], V. Kilchytska [4],
V. Pathirana [3], N. Udugampola [3], K. Ben Ali [4], D. Flandre [4],
J.W. Gardner [1] and P.A. Mawby [1]

[1] School of Engineering, University of Warwick, Coventry, CV4 7AL, UK
[2] Tyndall National Institute, University College Cork, Lee Maltings, Dyke Parade, Cork, Ireland
[3] Cambridge Microelectronics Limited, Cambridge, United Kingdom
[4] Université catholique de Louvain, Louvain-la-Neuve, Belgium
[a] P.M.Gammon@warwick.ac.uk

***Abstract*—In this paper we present for the first time the design and fabrication of a silicon-on-silicon carbide Si/SiC laterally diffused metal-oxide-semiconductor field-effect transistor (LDMOSFET) targeting 200-600 V blocking voltages for high temperature, harsh environment applications such as space and downhole drilling. The final paper will focus on the electrical characterization of this newly fabricated device.**

Keywords-silicon on silcion carbide; SOI; harsh environment; LDMOSFET; power electronics; characterisation; TEM.

I. INTRODUCTION

Electronic devices that are able to work efficiently and reliably at high temperature (300°C and above) are required for harsh environment applications, such as outer space and downhole drilling. Even though SiC devices are emerging with superior electrical and thermal performance, Si and Silicon-on-Insulator (SOI) devices are still dominating the high temperature market. The main reason is that SiC MOS devices have significant channel issues, making them less attractive for medium and low voltage (<1200 V) applications. An alternative solution has been proposed [1, 2], in which devices are fabricated on substrates made from direct wafer bonding of Si and SiC, in which case the high thermal conductivity of the SiC substrate can be utilized to help dissipate the heat generated in the Si active area, minimizing self-heating effects. Previous simulation results demonstrated that with a junction-to-case temperature 4 x less than SOI [3], power transistors with a breakdown voltage up to 600 V are achievable on Si/SiC substrates [4]. In this paper we present for the first time the design and fabrication of a Si/SiC LDMOSFET targeting 200-600 V blocking voltages.

II. EXPERIMENTAL WORK

The 4-inch Si/SiC wafers shown in Figure 1 were prepared by IceMOS Technology Ltd and the bonding process details are published elsewhere [5]. The rippling pattern on the wafer surface is caused by interface strain; trenches (grid pattern in Figure 1) are etched into the Si top layer to partially release it. 1 µm and 2 µm thick n-type Si layers are lightly doped (5-45 Ω.cm) and bonded to the 300 µm thick on-axis semi-insulating (≥ $1.1x10^7$ Ω.cm) 4H-SiC substrate. TEM was used to characterize the as-bonded Si/SiC interface. It can be seen that in some areas, such as Figure 2 top, a perfectly homogeneous interface was obtained. In some other places (Figure 2 bottom), features of pits or voids are seen, which may cause charge trapping and Fermi-level pinning there. We previously found out that MOS capacitors fabricated on these as-bonded n-type Si layers showed p-type behaviour and it was suggested that a high density of interfacial charge caused band bending, which in such a thin, lightly doped Si layer inverts the doping polarity of the entire layer [5]. As such, phosphorous was implanted and thermally diffused into the as-bonded Si/SiC wafer surface to obtain an initial Si layer n-type doping of around $2x10^{15}$ cm^{-3}.

The device structure is shown in Figure 3. Dopants were then ion implanted into selective areas of the device and thermally annealed to form the desired PN junction profiles. Boron was used for P-well ($5x10^{16}$ cm^{-3}) and P+ region ($5x10^{19}$ cm^{-3}), phosphorous for N-well ($5x10^{16}$ cm^{-3}) and arsenic for N+ regions ($1x10^{20}$ cm^{-3}). After standard RCA 1 and 2 cleaning procedures, 500 nm of SiO_2 was deposited on the sample surface via PECVD to passivate the Si surface dangling bonds. Gate regions were opened via UV photo-lithography and RIE etching of the passivation SiO_2. Gate oxide was grown in 5 L/min O_2 at 900 °C for 6 hours to obtain a thickness around 60 nm, after which a further 1 L/min N2O annealing at the same temperature was applied to densify the gate and surface passivation oxide. 500 nm Al was deposited in the selective areas using an e-beam evaporator to form the gate, source and drain terminals. Finally, the device was annealed in forming gas ($5\%H_2/95\%N_2$) at 450 °C for 2 hours to make Ohmic contacts at source and drain. The forming gas process also helps to reduce MOS interface trap densities.

Characterization of the fabricated device is being carried out and the electrical performance will be presented in the full paper.

III. FIGURES

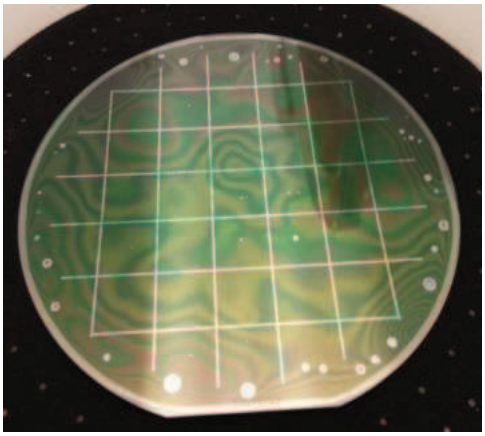

Figure 1. Four inch bonded Si/SiC wafer with 1 µm Si layer

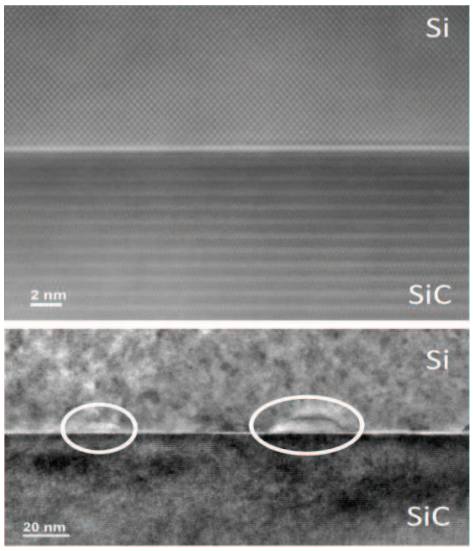

Figure 2. A TEM image of (top) homogeneous, oxide and defect free area and (bottom) another area where voids or pits are present.

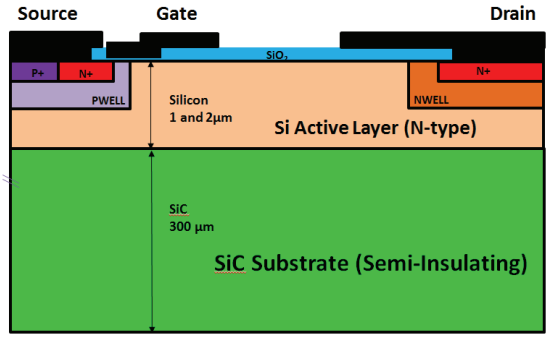

Figure 3. Schematic graph of the fabricated Si/SiC LDMOSFET structure.

ACKNOWLEDGEMENTS

The work presented in this paper has been carried out as part of the EU funded SaSHa Project (Si on SiC for the Harsh Environment of Space): www.sashaproject.eu/. We gratefully acknowledge the support of the European commission for this funding. Dr. Peter Gammon would also like to acknowledge support from the Royal Academy of Engineering, and from the EPSRC (Project EP/N00647X/1).

REFERENCES

[1] S. Lotfi, et al., Solid-State Electronics, vol. 70, pp. 14-19 (2012).

[2] Y. Sasada, et al., Materials Science Forum, vol. 778-780, p. 714 (2014).

[3] C.W. Chan, et al., Materials Science Forum, vol. 821-823, pp. 624-627 (2014)

[4] C.W. Chan, et al., IEEE Transactions on Electron Devices, vol. 63, pp.2442-2448 (2016)

[5] P.M. Gammon, et al., "The effect of interfacial charge on the development of wafer bonded silicon-on-silicon-carbide power devices", submitted to European Conference on Silicon Carbide and Related Materials 2016.