Substrate RF Losses and Non-linearities in GaN-on-Si HEMT Technology

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***Abstract*—** The analysis and mitigation of substrate-related RF losses and non-linearities is crucial to enable GaN HEMTs on silicon for front-end transceivers for 5G and beyond. Here, for the first time, the impact of material growth and HEMT fabrication process on the substrate RF losses and linearity is studied using the effective substrate resistivity, ρ_{eff}, and 2nd harmonic power, *H2*, figures-of-merit. It is shown that CPWs on fully-processed, GaN-on-high resistivity (3-6 kΩ·cm), 200 mm CZ-Si wafers can achieve *H2* levels ~ -85 dBm (at P_{out} ~15 dBm) with ρ_{eff} ~1 kΩ·cm.

I. Introduction

GaN-on-Si HEMTs, when co-integrated with Si-CMOS, have the potential to revolutionize the RF front-end of communication systems for 5G and beyond [1-3]. However, the finite resistivity of the Si substrate can limit the performance of HEMTs [4] as well as passive components [5] and leads to poor RF isolation [6] for switches. Work on RF-SOI technologies has shown that even on high-resistivity Si (HRS) substrates, the linearity and passive performance can be poor due to SOI substrate-fabrication process, which lowers the *effective substrate resistivity,* ρ_{eff} [7- 9]. For RF front-end modules, ρ_{eff} >3 kΩ·cm is required to achieve quasi-lossless substrates [8]. Therefore, for GHz applications, GaN-on-Si HEMTs are generally grown on HRS substrates [1, 2, 10]. However, the reported RF losses after HEMT epitaxy using MOCVD are found to be higher than that expected from the initial high-resistivity substrate [11] and have been attributed to an inversion layer formation at the interface of Si and AlN nucleation layer [12-13], formation of S-O-N complexes near the top of Si substrate [14], and diffusion of Al and Ga into the substrate during III-N epitaxy [11]. However, a detailed study of substrate losses and non-linearities for GaN-on-Si HEMTs which takes both the epitaxial and fabrication process steps into account is lacking. Here, for the first time, we evaluate the impact of material growth and key HEMT processing steps on the RF losses and linearity of the substrates for CMOS-compatible GaN-on-Si technology proposed in [1] (Fig. 1). It is demonstrated that a fully processed GaN HEMT stack grown on high-resistivity (3-6 kΩ·cm) 200 mm Czochralski (CZ) Si wafers can achieve 2nd harmonic levels down to ~-85 dBm for 2 mm long coplanar waveguides (CPWs).

CPWs are used to characterize RF losses and non-linearities due to their high sensitivity to the surface region of the substrate. To fairly compare substrate-related RF losses between various samples, the *effective resistivity* or ρ_{eff} sensed by the CPW lines is used [Fig. 2(a)] [9]. We use ρ_{eff} instead of the line attenuation parameter α, because ρ_{eff} is independent of the metallic losses [9], [Fig. 2(b)] and therefore, represents a true characteristic of the underlying substrate. The modulation of CPW *G* and *C* in response to a large amplitude RF-signal leads to generation of harmonics [7, 8]. Fig. 3 shows our harmonic measurement setup with a fundamental tone f_0 of 0.9 GHz. At output, the powers of fundamental (*H1*), 2nd (*H2*), and 3rd (*H3*) harmonics are measured at 0.9 GHz, 1.8 GHz, and 2.7 GHz, respectively.

II. Impact of HEMT Epitaxy and Processing on Substrate RF Performance

A. Impact of III-N Epitaxy

One of the major contributions to RF losses in GaN-on-Si HEMTs is due to the formation of a parasitic conductive channel (PSC) at the Si substrate top surface. For the layer stacks discussed here, the main source of the PSC is proven to be back-diffusion of Al and Ga atoms during the III-N growth, which form a p-type layer in Si [11, 15-16]. The concentration and diffusion depth of Al and Ga are strongly dependent on the epitaxial growth conditions, the quality of the AlN nucleation layer, and the total thermal budget of the complete stack. To investigate these effects, different material stacks [shown in Fig. 4 (a-c)] were grown using a *Veeco Maxbright* MOCVD reactor on 1.15 mm thick and 200 mm diameter, B-doped (ρ ~3-6 kΩ·cm) CZ-Si (111) substrates [1, 11, 15]. Both ρ_{eff} and harmonics were extracted from small- and large-signal characterization on 1.8 mm long lines. Material stack-B gives the highest ρ_{eff} and the lowest harmonic components [Fig. 4 (d)]. These results can be understood from the post-epitaxy resistivity profiles inside the Si substrate, obtained from the spreading resistance profiling (SRP) technique (Fig. 5). Stack-A has the lowest ρ_{eff} and largest harmonic components because it shows the strongest Al and Ga in-diffusion. It is noted that for all three of the stacks, a conductivity type inversion (from P to N type) is observed. This is related to the activation of the interstitial oxygen impurities as *thermal double donors* (TDDs) [17], which is discussed in section II-C. Stack-C shows lower Al/Ga diffusion due to shorter growth time for the thinner stack (i.e. reduced thermal budget), however, it is concomitant with a higher TDD concentration, which ultimately leads to inferior RF performance. Owing to its better performance, stack-B was used to study the impact of HEMT fabrication steps in the next sections.

B. Impact of Isolation Implant

DC isolation for CMOS compatible GaN HEMTs can be achieved through ion (e.g. N) implantation [1, 18]. High energy nitrogen ion implantation creates a large density of traps in the GaN HEMT active layers and suppresses the 2-DEG at Al(Ga)N barrier and GaN channel interface. These trapped charges in the top III-N layers can impact the PSC at AlN/Si interface in an analogous manner to the HR-SOI substrates where bulk oxide charges induce a PSC at oxide/Si interface [9]. This in turn can further degrade the ρ_{eff} and linearity, resulting in poor performance for passives and low RF isolation. To assess the impact of isolation implant on the RF performance of the substrate, samples with N-implants in 3 steps of increasing energy: 75 keV (implant I), 150 keV (implant II), and 375 keV (implant III), were fabricated. The depth profiles of N atoms, simulated using the TRIM program, are shown in Fig. 6. The ρ_{eff} extracted from CPW lines for various implant combinations is shown in Fig. 7. It is found that the

combination of all the three implants (also used in [1]), leads to a ρ_{eff} degradation by up to ~50%, which is attributed to enhancement of the PSC at the Si surface. This also manifests as a larger conductance *G* as shown in Fig. 8, where small-signal *G* as a function of DC bias applied to the CPW center conductor is plotted for various implant combinations. Ion implantation clearly leads to an increased *G* and a shift in the flat-band voltage towards more positive bias. In addition, for implanted samples, the relative modulation of *G* (and ρ_{eff}) is smaller below the flat-band voltage as compared to the sample without implant. For SOI substrates, a larger overall *G* has been linked to larger distortion, but on the other hand, its reduced bias-modulation can help lower the distortion [8]. *H2* and *H3* measured on 4 mm long lines for the samples with different implants are shown for different DC biases in Fig. 9. *H2* and *H3* are plotted against *H1* of P_{out} instead of P_{in} to remove the contribution of the losses along the line. *H3* is lower than *H2* by >20 dB in the power range shown. Hence, only *H2* is used for sample to sample comparison and benchmarking. Comparing *H2* (at *H1* = 15 dBm) for different implants, combined implants I (75 keV) and II (150 keV) achieve the best linearity performance (Fig. 10). Furthermore, the implanted samples show much smaller variation of *H2* with DC bias, consistent with the fact that relative modulation of *G* is very small in these samples in the -15V to 15V bias range. However, the sample which received all the three implants, displays degraded linearity (i.e. larger *H2*) due to its lower ρ_{eff} / higher *G* [8]. In summary, even though the implant damage is mainly confined to the top layers (< 1 µm) [Fig. 6], ion implantation significantly impacts the RF losses and distortion.

C. Impact of Thermal Annealing

CZ-Si contains interstitial oxygen (O_i) impurities from dissolution of the silicon oxide crucible during growth. During a thermal treatment in the 350-500 °C range, these O_i showed the strongest tendency to form clusters which act as electrically active thermal double donors (TDDs), leading to a change in the substrate resistivity [17]. The TDD generation rate depends on the starting O_i concentration ([O_i]) and thermal history of the sample. For GaN HEMT integration on Si, the substrate is subjected to thermal cycling in this temperature range during III-V epitaxy, dielectric deposition, and ohmic anneals [1]. As shown in Fig 5, the substrate exhibits an inversion of conductivity type from P to N, implying that a sufficiently large thermal budget in the 300-500 °C range has been applied inside the MOCVD reactor. Further, RTA in 500 - 600 °C range is needed to achieve CMOS-compatible low resistance ohmic contacts [1]. We find that RTAs (90s in N_2) in the 400-600 °C range can further degrade ρ_{eff} for substrates with various combinations of starting resistivities and [O_i], as shown in Fig. 11. ρ_{eff} averaged from 0.91 GHz to 5.11 GHz for the samples in Fig. 11 is plotted in Fig. 12. For the substrate HRS-1 (ρ ~3-6 kΩ·cm with unspecified [O_i]) ρ_{eff} shows a monotonic reduction with RTA temperature. On the other hand, substrates HRS-2 (ρ ~7.53 kΩ·cm, [O_i] ~3.8 ppma), HRS-3 (ρ ~4.3 kΩ·cm, [O_i] ~3 ppma) exhibit a relatively temperature independent ρ_{eff} in this range, but an overall degradation in ρ_{eff} due to RTA is still present. *H2* (@ *H1* = 15 dBm) for as grown and 500 °C RTA samples are compared in Fig. 13. At 0V, HRS-1 and HRS-3 show an increment in *H2* after RTA at 500 °C, which is in line with their ρ_{eff} reduction, however, HRS-2 shows minimal difference in *H2* levels. Different bias dependences of *H2* are probably due to variation in the effective doping (i.e. O_i related TDDs) in these substrates due to different starting [O_i] [17].

Finally, ρ_{eff} and distortion were evaluated for samples subjected to key HEMT processing steps (Fig. 14). The isolation implant (combination of I, II & III as in [1]) leads to degradation of ρ_{eff} for both the samples with and without Al(Ga)N top barrier. In addition, ion implanted samples with Al(Ga)N top barrier show only a small impact of RTA on ρ_{eff}. This can be explained by a strong PSC in the implanted samples, which can prevent the ξ-field from penetrating deeper into the substrate, even though the RTA reduces the bulk Si resistivity. *H2* is relatively independent of DC bias in the implanted samples as expected (Fig. 15). For GaN-on-HR-Si (n_i ~10^{12} cm^{-3}), one concern can be the degradation of Si resistivity if the substrate temperature rises above ~130 °C [19] due to device self-heating. 2-D thermal simulations indicate that the temperature at the AlN/Si interface remains below this limit for DC power dissipation up to 8 W/mm in the GaN channel (Fig. 16). It is verified that a significant degradation in *H2* happens at temperatures only above 150 °C for HRS-1 samples (Fig. 17).

III. HARMONICS BENCHMARKING

ρ_{eff} and distortion sensed by the CPW lines are strongly dependent on the line dimensions (see Fig. 18), because, in general the ξ-field penetration into the substrate increases as the spacing is increased at a given frequency. Therefore, *H2* (at *H1* = 15 dBm) for our representative samples is shown in Fig. 19 for commonly reported 2 mm long lines (*W* = 23.4 µm, *S* = 12.5 µm) instead of *S* = 50 µm lines in last section. The best '0V bias *H2'* in Fig. 19 is ~-85 dBm. This level of harmonic distortion compares well with the available trap-rich (TR), SOI substrates (Fig. 20). However, advanced SOI technologies can achieve ~10 dB lower *H2* than GaN/Si technology presented in this work [8,17-19]. Further improvements can be achieved by optimization of III-N growth on Si substrates with resistivity >7.5 kΩ·cm and O_i <3 ppma.

IV. CONCLUSION

The impact of GaN HEMT epitaxy and key processing steps on the RF losses in the substrate is studied using *effective substrate resistivity* and *harmonic power* figures-of-merit. Both the HEMT epitaxy and processing significantly impact the RF losses and linearity in CZ-Si substrates. 2nd harmonic (*H2*) down to ~ -85 dBm (at P_{out} ~15 dBm) is measured on 2 mm long CPW lines, which compares well with the commercial HR-SOI technologies.

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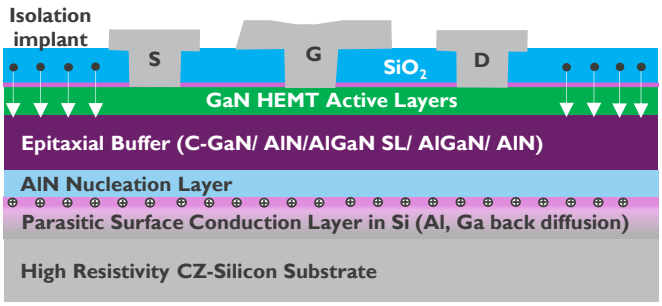

Fig. 1. Substrate RF losses in the GaN-on-Si HEMTs can be impacted by: (i) Starting Si substrate resistivity and interstitial impurity (e.g., O) concentration, (ii) III-N epitaxy leading to Al and Ga diffusion into the substrate, traps, and unintentional conductive channels in the epitaxial layers and at interfaces, (iii) HEMT device processing steps such as isolation implant, dielectric deposition, and thermal annealing during front- and back-end processing.

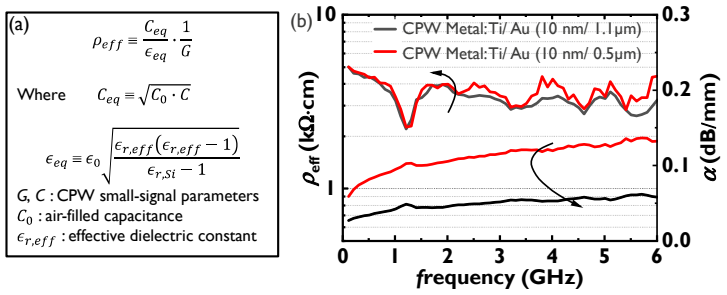

Fig. 2. (a) Effective substrate resistivity (ρ_{eff}) can be extracted using small-signal C and G of CPWs [14]. (b) ρ_{eff} and total RF loss parameter (α), extracted for identical substrates but with different CPW metal thicknesses. α significantly increases for the sample with 0.5 μm thick metal stack as compared to the 1.1 μm one, due to increased conductor losses but ρ_{eff} is essentially independent of metal thickness. ρ_{eff}, therefore, represents the true substrate losses.

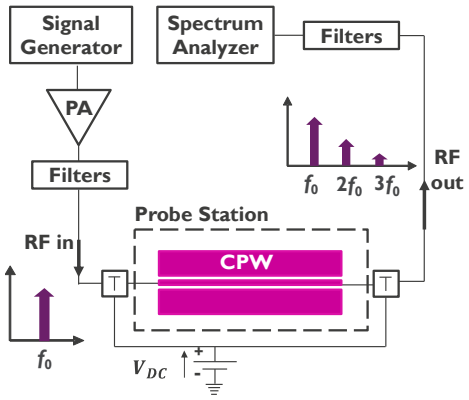

Fig. 3. Set-up for the harmonic distortion measurements at 0.9 GHz. Powers for the first 2 harmonics are measured. DC bias can be applied to the CPW center conductor using the bias-T. PA: power amplifier, T: bias-T.

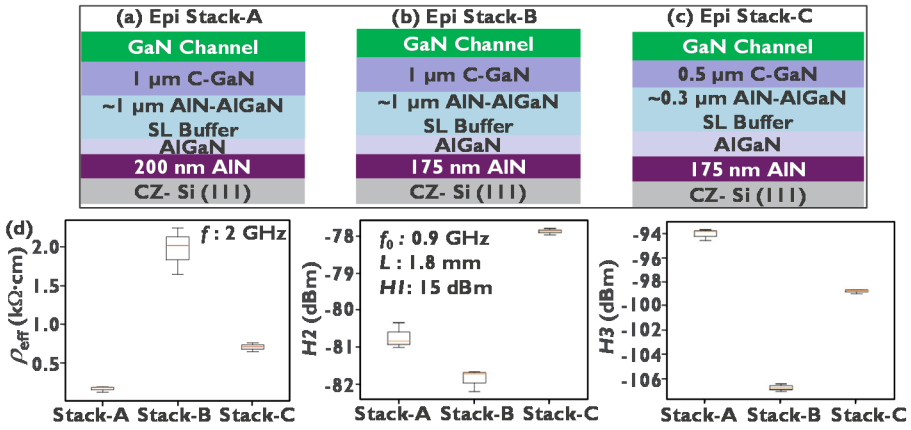

Fig. 4. (a), (b), (c). Epitaxial stacks considered during growth optimization. (d) Left: ρ_{eff} extracted from CPW lines [center conductor width (W) = 75 μm and slot width (S) = 50 μm] fabricated on the samples in Fig. 4 (a), (b), (c). Middle and right: *H2* and *H3* for the samples measured at the fundamental (f_0) frequency of 0.9 GHz and *H1* of 15 dBm for l.8 mm long lines. Both from the ρ_{eff} and linearity points of view, Stack-B (total thickness ~2.5 μm) gives the best performance.

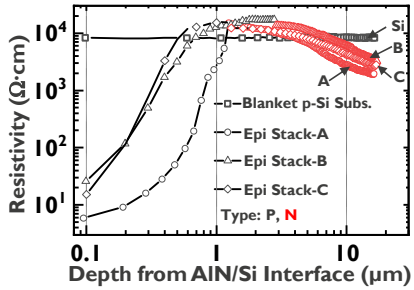

Fig. 5. Spreading resistance profiles (SRP) in Si for the epitaxial stacks in Fig. 4 and the starting blanket p-Si substrate. Conductivity in the Si substrate and its type (P/ N), strongly depend on the epitaxial growth conditions, the quality of the AlN nucleation layer, and overall thermal budget.

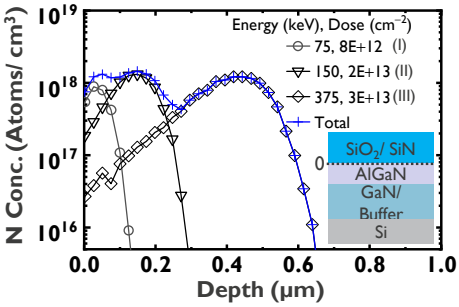

Fig. 6. Concentration of implanted N-atoms as a function of depth in the GaN HEMT layers, simulated using the TRIM program (http://www.srim.org/) for various ion energies and doses used in this work. The N-atom profiles are shown starting from the AlGaN surface. Implant damage is likely confined to the top ~1 μm of the stack.

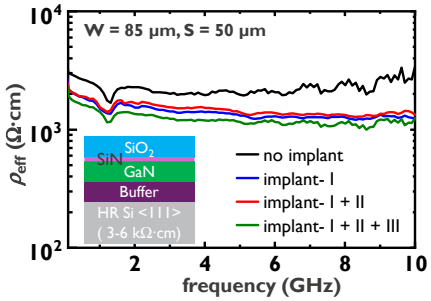

Fig. 7. The impact of nitrogen isolation implant on ρ_{eff}. Implant-I: 75 keV. Implant-II: 150 keV, Implant-III: 375 keV. Ion implant leads to degradation of ρ_{eff}, due to creation of trapped charges in the top III-N layers, which enhance the parasitic channel (PSC) at the AlN/Si interface.

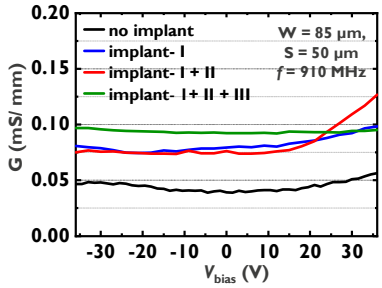

Fig. 8. CPW small-signal G at 0.91 GHz, as a function of center conductor DC bias for samples with various implant combinations as in Fig. 7. DC hold time : 100 ms.

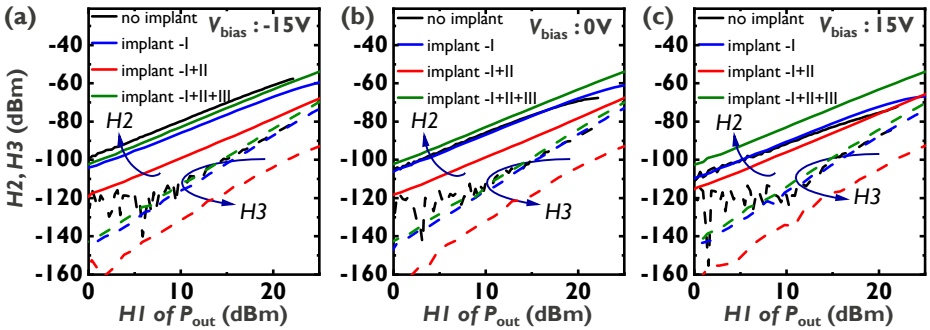

Fig. 9. (a), (b), and (c) Impact of ion-implantation on 2nd and 3rd harmonics (*H2* and *H3*) measured for f_0 = 0.9 GHz on 4 mm long lines (W = 85 μm, S = 50 μm) at different DC biases.

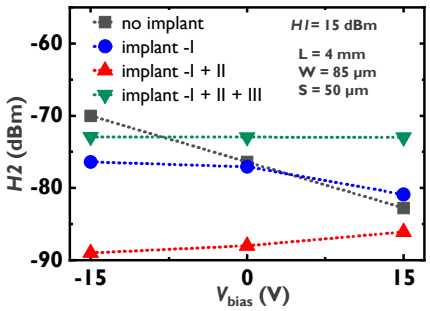

Fig. 10. *H2* as a function of DC bias applied to the center conductor, extracted from Fig. 9 (a), (b), (c) at *HI* of 15 dBm. Combination of implants I (75 keV) and II (150 keV) led to lowest distortion. *H2* for implanted samples showed weaker bias dependence than the non-implanted ones.

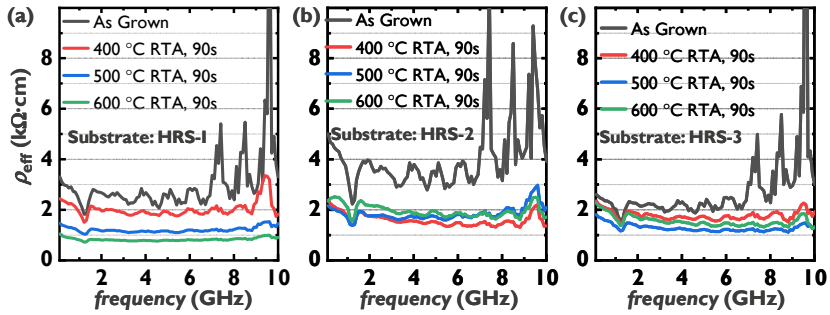

Fig. 11. ρ_{eff} for 3 different substrates: (a) HRS-1, (b) HRS-2, (c) HRS-3, with different starting resistivity and interstitial oxygen content [O_i] and subjected to various rapid thermal anneal (RTA) conditions. Substrate information- HRS-1: 3-6 kΩ·cm with unspecified [O_i]; HRS-2: 7.53 kΩ·cm with [O_i] of 3.8 ppma; HRS-3: 4.3 kΩ·cm with [O_i] of 3 ppma. CPW dimensions: W = 85 µm, S = 50 µm. In these samples, Al(Ga)N top barrier was not grown to avoid 2-DEG formation at Al(Ga)N/ GaN interface.

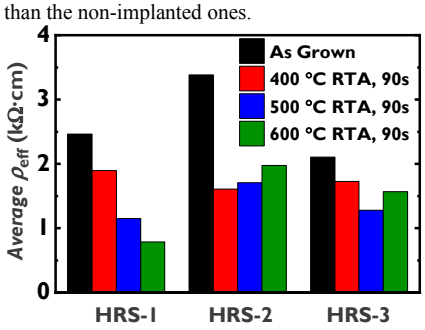

Fig. 12. ρ_{eff} from Fig. 11, averaged over frequency range of 0.91 GHz to 5.11 GHz. For HRS-1, ρ_{eff} monotonically reduces as RTA temperature is increased. For HRS-2 and HRS-3, ρ_{eff} tends to recover at 600 °C, potentially due to lower starting [O_i] and annihilation of O-clusters. RTA splits were applied to independent samples.

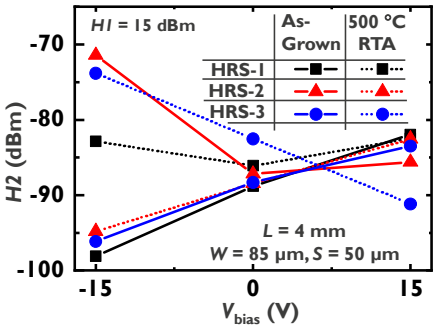

Fig. 13. Impact of RTA conditions on 2nd harmonic power, *H2* as a function of bias for the same samples as in Fig. 11. For HRS-1 and HRS-3, distortion at 0V DC bias increases after annealing at 500 °C, in line with the reduction in ρ_{eff}. HRS-2 exhibits negative correlation with ρ_{eff} following RTA.

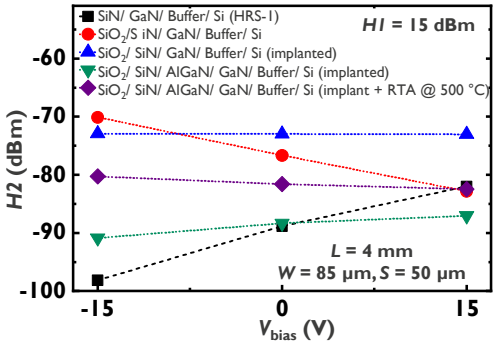

Fig. 15. *H2* for samples with various processing steps applied to them as shown in Fig. 14. *H2* for the implanted samples (both with and without Al(Ga)N top barrier) show only a weak dependence on DC bias as expected from the line *G-V* characteristics.

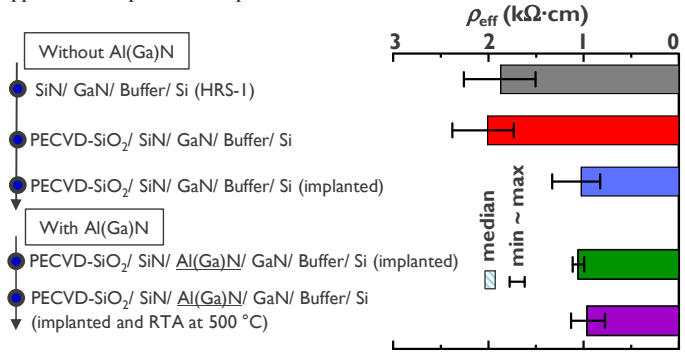

Fig. 14. ρ_{eff} (averaged over 0.91-5.11 GHz for each measured CPW on a sample) for GaN-on-Si samples (HRS-1 with buffer stack-B), subjected to key HEMT processing steps. Isolation implant (I+II+III) has a large impact on ρ_{eff} and therefore on substrate losses.

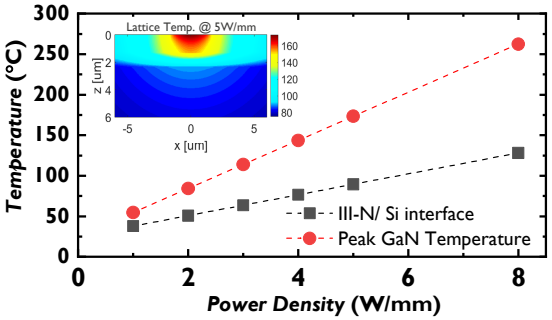

Fig. 16. Temperature at the AlN/Si interface and the peak device temperature as a function of DC power density. Temperatures are obtained from 2D thermal simulations on a similar layer stack as used in this work at chuck temperature of 25°C. The inset shows a detail of the 2D temperature distribution at power density of 5 W/mm.

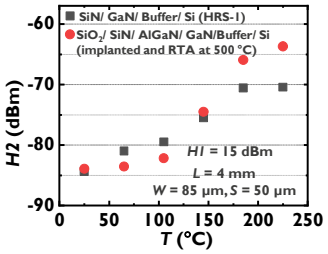

Fig. 17. *H2* at different chuck temperatures for as-grown HRS-1 sample (no 2-DEG) and the full HEMT sample subjected to SiO_2 deposition, implantation, and RTA at 500 °C. Non-linearities in both samples do not increase below ~130 °C.

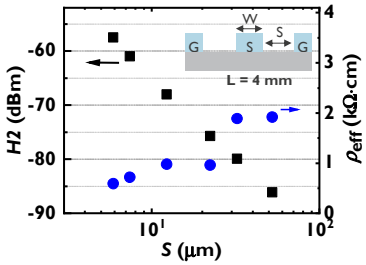

Fig. 18. *H2* and ρ_{eff} as function of CPW slot-width (*S*) for HRS-1 sample. ρ_{eff} decreases as S is reduced due to ξ-field confinement in the PSC at the AlN/Si interface and a corresponding increment is observed on *H2* (@ *HI* = 15 dBm). The CPW characteristic impedance is maintained at 50 Ω in all the designs.

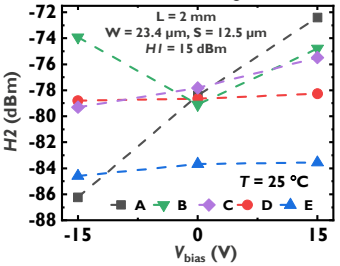

Fig. 19. *H2 versus* DC bias, measured on lines with *L* = 2 mm, *W* = 23.4 µm, and *S* =12.5 µm, for key samples at *HI* = 15 dBm. Samples: A: HRS-1, B: HRS-2, C: HRS-3, D: SiO_2/SiN/GaN/ Buffer/ Si (implant I&II), E: SiO_2/SiN/AlGaN/GaN/Buffer/Si (implanted and annealed at 500 °C).

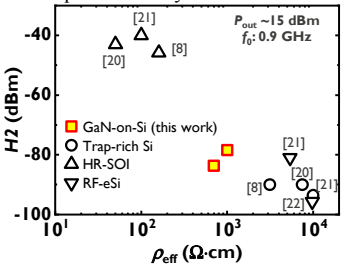

Fig. 20. *H2* benchmarking of GaN/Si technology in this work (2 mm CPWs, with *W* = 23.4 µm, *S* =12.5 µm) against various RF technologies at *HI* (~ P_{out}) of 15 dBm. Optimized GaN-on-HRSi technology can achieve linearity at par with HR-SOI technologies.