

Exploring the Back-End-of-Line Impact on Self Heating in Advanced Silicon-on-Insulator RF MOSFETs

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Abstract

To accurately evaluate transistor performance, it is imperative to consider not only its electrical characteristics but also its thermal behaviour. With the advent of next-generation mobile networks and the Internet of Things, there is a growing demand for robust devices capable of maintaining consistent performance across diverse operating conditions. Temperature variations significantly impact various performance metrics of MOSFETs, underscoring the importance of understanding transistor temperatures and the factors influencing their fluctuations.

The consideration of the thermal aspect of MOSFETs specifically becomes important in state-of-the-art devices due to two main reasons. Firstly, applications in harsh environments that face extreme temperature conditions affect the device performance strongly compared to their operation at standard room temperatures. While such applications were historically reserved for niche deployments in drilling and geothermal energy areas, modern applications in booming electronic sectors such as automotive face temperatures considerably higher than room temperature. Secondly, the self-heating effect that causes heating in the MOSFETs due to the flow of current in the channel as a consequence of Joule's law of heating is a growing concern. While the downscaling of transistors has greatly reduced area footprint and costs while enhancing device performance, the higher current and power densities in these devices have given rise to more self-heating and thus higher device temperatures. The lower thermal conductivity of some of the oxides and thin films used in these devices further adds to the problem.

This thesis investigates these thermal aspects in MOSFETs using the industrial 22 nm FDSOI technology from GlobalFoundries to provide a precise understanding of the thermal landscape in advanced technology nodes.

An experimental assessment is conducted to evaluate the impact of elevated ambient temperatures on device performance, revealing significant variations in key performance metrics at 175 °C compared to room temperature. These findings emphasize the necessity of considering temperature-related performance issues during device design and highlight the need for accurate foundry models to accommodate ambient temperatures exceeding the current 125 °C limit of standard product design kits.

Self-heating assessment has been made using two of the most prominent and suitable characterization techniques for advanced devices, namely the RF

technique and the gate-resistance technique. A thorough evaluation of the pros and cons of both techniques is made; this reveals notable differences in thermal resistance, with the RF technique showing higher thermal resistance than the gate-resistance technique on the same device test structures. This raises questions about the underlying theory of the gate-resistance technique which considers that the channel temperature and gate temperature are equal while opening up the discussion on heat evacuation through the upward gate path that could result in such a difference. Cooling through additional gate accesses in the gate-resistance technique is demonstrated experimentally, showing that layout-related aspects can also affect self-heating characterization and showcasing that heat evacuation through the gate path is possible.

A solution to the self-heating problem is proposed in the form of heat sinks in the back-end of line (BEOL) connected to the device. Designed metal sinks connected to the gate of the device presents up to 20% lower thermal resistance in our work. From further studies comparing sinks of different sizes, it is noted that the sink efficiency is greater for a larger sink area. On the other hand, with larger sink sizes, more parasitics are encountered which degrade the RF performance. A tradeoff is thus established between the thermal efficacy of the sink and the degradation in the RF performance.

With the thermal problem in state-of-the-art MOSFETs presented, this thesis additionally provides perspectives on the heat evacuation paths in these devices for improving thermal modelling and characterization.

Author's Publication List

Journal Papers

1. **A. Halder**, M. Vanbrabant, D. Lederer, J.-P. Raskin, and V. Kilchytska, "Impact of Device Layout on Self-heating Extraction in MOSFETs," Solid-State Electronics, Publisher: Elsevier. *Submitted*.
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4. **A. Halder**, L. Nyssens, M. Rack, D. Lederer, J.-P. Raskin, and V. Kilchytska, "Heat sink implementation in back-end of line for self-heating reduction in 22nm FDSOI MOSFETs," Solid-State Electronics, vol. 184, p. 108 088, Oct. 2021, ISSN: 0038-1101. DOI: 10.1016/j.sse.2021.108088.
5. L. Nyssens, M. Rack, **A. Halder**, J.-P. Raskin, and V. Kilchytska, "On the Separate Extraction of Self-Heating and Substrate Effects in FD-SOI MOSFET," IEEE Electron Device Letters, vol. 42, no. 5, pp. 665–668, May 2021, ISSN: 1558-0563. DOI: 10.1109/LED.2021.3071272.
6. V. Kilchytska, S. Makovejev, B. K. Esfeh, L. Nyssens, **A. Halder**, J.-P. Raskin, and D. Flandre, "Extensive electrical characterization methodology of advanced MOSFETs towards analog and RF applications," IEEE Journal of the Electron Devices Society, vol. 9, pp. 500–510, 2021. DOI: 10.1109/JEDS.2021.3057798.
7. L. Nyssens, **A. Halder**, B. K. Esfeh, N. Planes, M. Haond, D. Flandre, J.-P. Raskin, and V. Kilchytska, "Self-heating in FDSOI UTBB MOSFETs at cryogenic temperatures and its effect on analog figures of merit," IEEE Journal of the Electron Devices Society, vol. 8, pp. 789–796, 2020. DOI: 10.1109/JEDS.2020.2999632.
8. L. Nyssens, **A. Halder**, B. K. Esfeh, N. Planes, D. Flandre, V. Kilchytska, and J.-P. Raskin, "28-nm FD-SOI CMOS RF Figures of Merit Down to 4.2 K," IEEE Journal of the Electron Devices Society, vol. 8, pp.

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Conference Papers

1. **A. Halder**, L. Nyssens, M. Rack, D. Lederer, V. Kilchytska, and J.- P. Raskin, “22 nm FD-SOI MOSFET Figures of Merit at high temperatures upto 175 °C,” in 2022 IEEE 22nd Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF), ISSN: 2474-9761, Jan. 2022, pp. 27–30. DOI: 10.1109/SiRF53094.2022.9720052.
2. L. Nyssens, M. Rack, **A. Halder**, M. Vanbrabant, V. Kilchytska, and J.- P. Raskin, “Back-Gate Network Extraction Free from Dynamic Self-Heating in FD SOI,” in 2021 International Symposium on VLSI Technology, Systems and Applications (VLSI-TSA), IEEE, 2021, pp. 1–2. DOI: 10.1109/VLSI-TSA51926.2021.9440125.
3. V. Kilchytska, S. Makovejev, B. K. Esfeh, L. Nyssens, **A. Halder**, J.- P. Raskin, and D. Flandre, “Electrical characterization of advanced MOS-FETs towards analog and RF applications,” in 2020 IEEE Latin America Electron Devices Conference (LAEDC), IEEE, 2020, pp. 1–4. DOI: 10.1109/LAEDC49063.2020.9073536.
4. **A. Halder**, L. Nyssens, M. Rack, J. - P. Raskin, and V. Kilchytska, “Effect of Heat Sink in Back-End of Line on Self-Heating in 22 nm FDSOI MOSFETs,” in 2020 Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon (EUROSOI-ULIS), ISSN: 2472-9132, Sep. 2020, pp. 1–4. DOI: 10.1109/EUROSOI-ULIS49407.2020.9365293.
5. L. Nyssens, **A. Halder**, B. K. Esfeh, N. Planes, M. Haond, D. Flandre, J.- P. Raskin, and V. Kilchytska, “Self-Heating in 28 FDSOI UTBB MOS-FETs at Cryogenic Temperatures,” in ESSDERC 2019 - 49th European Solid-State Device Research Conference (ESSDERC), ISSN: 2378-6558, Sep. 2019, pp. 162–165. DOI: 10.1109/ESSDERC.2019.8901704.
6. L. Nyssens, **A. Halder**, B. K. Esfeh, N. Planes, D. Flandre, V. Kilchytska, and J.- P. Raskin, “28 FDSOI RF Figures of Merit down to 4.2 K,” in 2019 IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S), 2019, pp. 1–3. DOI: 10.1109/S3S46989.2019.9320656.



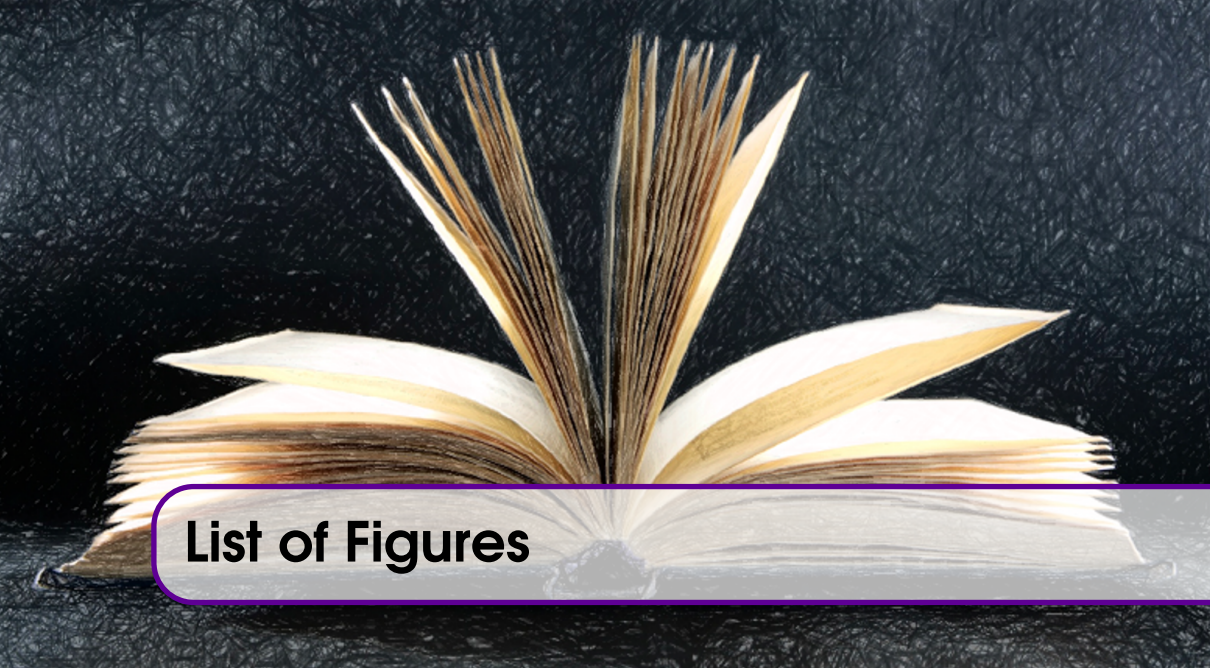
Contents

Acknowledgements	i
Abstract	iii
Author's Publication List	v
Table of contents	x
List of figures	xviii
1 Introduction	1
1.1 Operation Temperature of MOSFET	1
1.1.1 Harsh Environments	2
1.1.2 Self-Heating Effect	7
1.2 Limitations of Devices at High Temperatures	9
1.3 22FDX® Technology	11
1.3.1 Applications	11
1.3.2 Features	11
1.3.3 Back-gate Biasing	12
1.4 Objectives and Thesis Structure	13

2	Impact of High Temperature on MOSFET Performance	15
2.1	Introduction	15
2.1.1	Impact of Temperature on Device Performance Metrics	17
2.1.2	SOI versus Other Technologies	22
2.1.3	High-Temperature Studies on SOI Devices in Literature	24
2.2	High-Temperature Characterization	27
2.2.1	RF Characterization	27
2.2.2	High-Temperature Characterization Setup and Equipments	28
2.2.3	High-Temperature Characterization Safety Tips	30
2.3	22FDX® MOSFET Performance at High Temperatures	32
2.3.1	Objectives	32
2.3.2	Experimental Details	33
2.3.3	Results and Discussion	34
2.3.4	Performance Tuning with Back-Gate	60
2.4	Conclusions	63
3	Self-Heating Characterization Techniques	65
3.1	Introduction to Thermal Characteristics: Thermal Resistance, Thermal Capacitance and Thermal Time Constant	65
3.1.1	Thermal and Electrical Analogy	66
3.2	Self-Heating Effect	67
3.3	Thermal Conductivities of Materials in MOSFETs	69
3.3.1	Mechanisms Affecting Thermal Properties of Thin Films	70
3.3.2	Thermal Conductivity Variation with Temperature	72
3.4	Self-Heating Studies in Literature	73
3.4.1	Self-Heating with Dimension Scaling	73
3.5	Self-Heating Characterization Techniques	74
3.5.1	Pulsed IV Technique	75
3.5.2	Gate Resistance Technique	79
3.5.3	AC Conductance Technique	80
3.5.4	RF Technique	81
3.5.5	Other Mechanisms Affecting RF Transition	87
3.5.6	Drain Current vs Temperature	90

3.6	Impact of Variability on Self-heating Extraction: Corner Simulations in PDK	97
3.6.1	EXT and PLUS PDK Results	97
3.7	Thermal Resistance Variation with Temperature	101
3.7.1	Device Details	101
3.7.2	Measurement Results	101
3.7.3	PDK Results	103
3.7.4	Summary	105
3.8	Gate resistance vs RF technique: A comparative study	106
3.8.1	Device under Test	106
3.8.2	Gate Resistance Technique	107
3.8.3	RF Technique	113
3.8.4	Comparison of EXT and PLUS PDK	118
3.9	Discussion	119
3.9.1	4T Gate Resistance vs RF Technique	119
3.9.2	Reasons of Difference in the Techniques	122
3.9.3	Shortcomings of the Techniques	125
3.9.4	Summary	128
3.10	Impact of Device Layout on Self-heating Extraction	129
3.10.1	Device under Test	129
3.10.2	Experimental results and Discussion	130
3.10.3	Summary	134
3.11	Conclusion	135
4	Self-Heating Mitigation Techniques	137
4.1	Introduction: Heat Evacuation in MOSFETs	137
4.1.1	Heat Evacuation Paths	138
4.1.2	Impact of Technology type on Heat Evacuation	139
4.1.3	Impact of Channel Dimensions on Heat Evacuation	140
4.2	Benefits of Self-Heating Reduction	141
4.3	Different Methods of Self-Heating Reduction	142
4.3.1	Substrate Engineering	142
4.3.2	Layout Optimization	145
4.3.3	Heat Sinks	146

4.4	Heat Sink in BEOL	148
4.4.1	Idea and Background	148
4.4.2	Device under Test	148
4.4.3	Measurement Setup	151
4.4.4	Results and Discussion	153
4.4.5	Summary	161
4.5	Comparison of Sink Efficiency with Area	162
4.5.1	Device under Test	162
4.5.2	Measurement Setup	163
4.5.3	Results and Discussion	164
4.5.4	Summary	175
4.5.5	Impact of Device Length Variation on SH and RF FoMs	176
4.6	Conclusions	177
5	Conclusion and Perspectives	179
5.1	Conclusion	180
5.1.1	Summary	180
5.1.2	Connection Between the Chapters	183
5.2	Perspectives	184
5.2.1	FDSOI technology for temperature applications	184
5.2.2	Thermal Modelling and Challenges	184
	Appendices	187
A	Analytical Thermal Model	188
A.1	Complexity of the Real Thermal Problem	188
A.2	Computation of Thermal Resistances	189
	Bibliography	193



List of Figures

1.1	Harsh environments and self-Heating: Two situations leading to increased device temperatures.	2
1.2	Temperature range of operation of various high-temperature environments.	5
1.3	Temperature distribution in different parts of the car (7). . .	6
1.4	Typical cross-section of an NFET in 22FDX® (19).	12
1.5	Structure of the Thesis.	14
2.1	Overview of Chapter 2.	16
2.2	Comparison of different technologies for high-temperature applications.	24
2.3	Variation of Output Power P_{out} versus Temperature for FMCW Radar in (45). The impact of temperature on circuit performance is demonstrated.	26
2.4	Calibration Kit 101-190C used for calibration in this thesis. . .	28
2.5	PM8 Probe Station with Thermochuck.	29
2.6	Measurement setup on the MPI Probe Station.	30
2.7	IZI Probe used for high-temperature measurements. . .	31

2.8	Normalized drain current I_d in linear scale versus gate voltage V_g at drain voltage $V_d = 0.8$ V at different temperatures for measurements and PDK.	35
2.9	Normalized drain current I_d in logarithmic scale versus gate voltage V_g compared in measurements and PDK for $V_d = 0.8$ V. The deviation between measurements and PDK is stronger at higher temperatures.	35
2.10	Variation of g_m from DC measurements and PDK at $V_d = 0.8$ V with temperature.	36
2.11	Variation of maximum normalized transconductance $g_{m,max}$ from DC measurements and PDK simulations at $V_d = 0.8$ V with temperature.	37
2.12	Variation of threshold voltage V_{th} with temperature in measurements and PDK.	38
2.13	Small-signal equivalent circuit for MOSFET.	39
2.14	SSEC for modelling MOSFET in cold bias ($V_d = 0$ V) and high inversion ($V_g > V_{th}$).	41
2.15	Frequency variation of $\text{Re}(Z_{11} - Z_{12})$ for R_g extraction.	42
2.16	Linear regression of $\text{Re}(Z_{11} - Z_{12})$ with reciprocal of overdrive voltage for R_g extraction.	43
2.17	Frequency variation of $\text{Re}(Z_{12})$ for R_s extraction.	44
2.18	Linear regression of $\text{Re}(Z_{12})$ with reciprocal of overdrive voltage for R_s extraction.	44
2.19	Frequency variation of $\text{Re}(Z_{22} - Z_{12})$ for R_d extraction.	45
2.20	Linear regression of $\text{Re}(Z_{22} - Z_{12})$ with reciprocal of overdrive voltage for R_d extraction.	45
2.21	SSEC for modelling MOSFET in cold bias ($V_d = 0$ V) and deep depletion ($V_g < 0$ V) (58).	46
2.22	Extraction of extrinsic capacitances $C_{gd,e}$, $C_{gs,e}$ and $C_{ds,e}$ from the imaginary part of Y parameters.	47
2.23	SSEC for modelling MOSFET in saturation ($V_d = 0.8$ V) and strong inversion ($V_g > V_{th}$) (58).	48
2.24	Variation of maximum normalized intrinsic and extrinsic transconductance $g_{m,i}$ and $g_{m,e}$ and output intrinsic and extrinsic conductance $g_{d,i}$ and $g_{d,e}$ with temperature at $V_d = 0.8$ V (solid lines) and 0.6 V (dashed lines) and V_g corresponding to $g_{m,max}$	50

2.25	Variation of normalized total intrinsic gate capacitance $C_{gg,Tl}$ ($C_{gs,l} + C_{gd,l}$) with temperature at $V_d = 0.8$ V and 0.6 V with V_g corresponding to $g_{m,max}$	51
2.26	Variation of intrinsic voltage gain A_V with temperature for $V_d = 0.8$ V and V_g corresponding to $g_{m,max}$	52
2.27	Variation of gate resistance R_g and source-drain resistance R_{sd} ($R_s + R_d$) with temperature.	52
2.28	Comparison of S-parameters measured and reconstructed from SSEC at room temperature for $V_d = 0.8$ V and $V_g = 0.6$ V.	53
2.29	Short-circuit current gain H_{21} and unilateral power gain U plots versus frequency for $V_d = 0.8$ V and $V_g = 0.6$ V.	54
2.30	Variation of normalized current-gain cut-off frequency f_T with temperature at $V_d = 0.8$ V and V_g corresponding to $g_{m,max}$, g_m -ZTC and 0.3 V (below g_m -ZTC). Normalization with respect to f_T at V_g corresponding to $g_{m,max}$ at 25°C, $V_d = 0.8$ V.	56
2.31	Variation of normalized maximum oscillation frequency f_{max} with temperature at $V_d = 0.8$ V and V_g corresponding to $g_{m,max}$, g_m -ZTC and 0.3 V (below g_m -ZTC). Normalization with respect to f_{max} at V_g corresponding to $g_{m,max}$ at 25°C, $V_d = 0.8$ V.	57
2.32	P_{dc} variation with V_d showing percentage P_{dc} reduction at various biases.	58
2.33	Variation of normalized current-gain cut-off frequency f_T with temperature at $V_d = 0.6$ V and V_g corresponding to $g_{m,max}$, g_m -ZTC, and 0.3 V (below g_m -ZTC). Normalization with respect to f_T at V_g corresponding to $g_{m,max}$ at 25°C, $V_d = 0.6$ V.	58
2.34	Variation of normalized maximum oscillation frequency f_{max} with temperature at $V_d = 0.6$ V and V_g corresponding to $g_{m,max}$, g_m -ZTC, and 0.3 V (below g_m -ZTC). Normalization with respect to f_{max} at V_g corresponding to $g_{m,max}$ at 25°C, $V_d = 0.6$ V.	59
2.35	Using back-gate voltage V_{bg} to offset the change in threshold voltage V_{th}	61
3.1	Overview of Chapter 3.	66
3.2	Analogy of the thermal and electrical problem.	67
3.3	Relation between thermal and electrical parameters.	67
3.4	Thermal equivalent circuit.	68

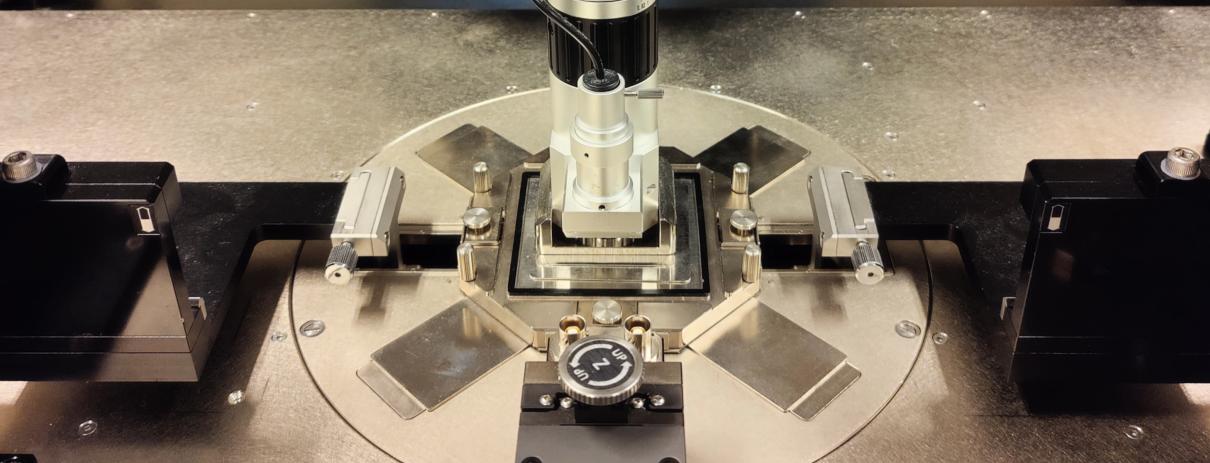
3.5	Variation of thermal conductivity of Si and Ge thin films with film thickness (74). The reduction in thermal conductivity with reduced film thickness is a direct consequence of phonon scattering.	71
3.6	Variation of thermal conductivity of Si and SiO ₂ with temperature (78).	72
3.7	Increase of R_{th} with decreasing device length in 28 nm FDSOI MOSFETs reported by Nyssens (83) and Makovejev (82) using RF technique for SH characterization.	74
3.8	I_d - V_d obtained from DC and pulsed measurements with the pulse width from 10 ns to 1 μ s at room temperature and $V_g = 1.8$ V. Inset: high V_d region. (89).	76
3.9	Output characteristics at $V_g = 1.8$ V obtained from the 50-ns pulsed I-V measurements at various chuck temperatures and from the DC measurement at room temperature. Inset: a schematic of the device (not to scale). (89).	77
3.10	4-Terminal sensing electrical circuit diagram.	79
3.11	4T Method circuit schematic applied on a MOSFET.	80
3.12	Variation in g_d with frequency reported in (89).	84
3.13	Variation in C_{dd} with frequency reported in (89).	84
3.14	Fourth order thermal network for the fitting model used in (48).	86
3.15	Thermal network fitting for g_d based on order of network in this work. A fourth-order network is seen as necessary to fit measurements.	86
3.16	Variation of g_d and C_{dd} with frequency below and above ZTC (98).	88
3.17	Impact of floating body effect on g_d vs frequency (95).	89
3.18	Impact of gate resistance on g_d vs frequency (99).	89
3.19	Drain current vs temperature for PDSOI and FDSOI MOSFETs using hot chuck measurements at $V_g = V_d = 2.5$ V in (95).	90
3.20	Drain current vs temperature using hot chuck measurements for multifinger MOSFETs with $N_f = 30$ and $W_f = 2 \mu$ m at $V_g = 2$ V and $V_d = 1.8$ V in (100).	91
3.21	Drain Current I_d vs temperature on three dies and their averaged value at $V_g = V_d = 0.8$ V.	92

3.22	Drain current I_d vs temperature in EXT and PLUS PDK at $V_g = V_d = 0.8\text{ V}$. A nonlinear I_d vs temperature trend is seen in both cases which results in a variation in dI_d/dT over temperature.	94
3.23	Drain current I_d vs temperature in EXT and PLUS PDK and corresponding power law fitting coefficient f values at $V_g = V_d = 0.8\text{ V}$. A good fit on both PDKs is seen with a fitting coefficient of 0.2.	95
3.24	Variation of drain current I_d and its slope dI_d/dT with temperature in measurements and corresponding fitting with power law fitting coefficient $f = 0.15$ at $V_g = V_d = 0.8\text{ V}$	96
3.25	Drain current I_d and transconductance g_m vs gate voltage V_g for the different corners in EXT and PLUS PDK in saturation at $V_d = 0.8\text{ V}$	98
3.26	Variation of dg_m/dV_g vs gate voltage V_g for the different corners in EXT and PLUS PDK in linear at $V_d = 50\text{ mV}$	99
3.27	Output conductance g_d vs frequency for different corners in EXT and PLUS PDK at $V_{ov} = 0.53\text{ V}$ and $V_d = 0.8\text{ V}$	99
3.28	Drain current I_d vs temperature in EXT PDK at $V_{ov} = 0.53\text{ V}$ and $V_d = 0.8\text{ V}$	100
3.29	Slope of drain current with temperature dI_d/dT in EXT and PLUS PDK at $V_{ov} = 0.53\text{ V}$ and $V_d = 0.8\text{ V}$	100
3.30	Output conductance g_d vs frequency for different temperatures at $V_g = V_d = 0.8\text{ V}$	102
3.31	Output conductance g_d vs frequency for different temperatures in EXT and PLUS PDK at $V_g = V_d = 0.8\text{ V}$	104
3.32	Thermal resistance R_{th} variation with temperature in EXT and PLUS PDK at $V_g = V_d = 0.8\text{ V}$	104
3.33	Overview of the device layout with the two measurement RF and four DC pads.	106
3.34	Layout the gate fingers of the core FET and the 4T gate accesses.	107
3.35	Schematic of 4-terminal gate resistance technique. . .	108
3.36	Schematic of 2-terminal gate resistance technique. . .	108
3.37	DC Gate Resistance vs temperature when device is off made for TCR calibration.	110
3.38	Temperature rise versus power for different V_g at $V_d = 0.8\text{ V}$	111

3.39	Output conductance g_d vs frequency for different V_g biases at $V_d = 0.8$ V.	114
3.40	Drain current I_d vs temperature for different V_g biases at $V_d = 0.8$ V. The variations above and below ZTC of $V_g = 0.6$ V are seen.	115
3.41	Drain current I_d vs temperature for $V_g = 0.8$ V at $V_d = 0.8$ V.	117
3.42	Averaged drain current I_d vs temperature over the measured dies for $V_g = 0.8, 0.9$ V at $V_d = 0.8$ V.	117
3.43	R_{th} as a function of L_g for SOI MOSFETs with a t_{BOX} of 6, 21, and 147 nm in (105). Channel thickness t_{SOI} was approximately 50 nm.	120
3.44	R_{th} extracted from gate-resistance and RF technique in (47).	121
3.45	Temperature of gate and channel and the electrical representation of the thermal equivalent.	123
3.46	Gate Resistance vs chip temperature T_{chip} dependence of change in R_{gate} for typical devices used in (105) and conventional polysilicon gate electrode.	126
3.47	Drain current I_d and transconductance g_m vs gate voltage V_g for 4T and no 4T device in saturation at $V_d = 50$ mV.	130
3.48	Drain current I_d and transconductance g_m vs gate voltage V_g for 4T and no 4T device in saturation at $V_d = 0.8$ V.	131
3.49	Output conductance g_d vs. frequency for 4T and non-4T devices in saturation at $V_d = 0.8$ V and $V_g = 0.8$ V and 0.9 V. ..	131
3.50	Drain current I_d vs temperature for 4T and non-4T devices in saturation at $V_d = 0.8$ V and $V_g = 0.8$ V and 0.9 V.	132
3.51	Output conductance g_d vs frequency for the device in PDK for varying R_d computed in saturation at $V_d = 0.8$ V and $V_g = 0.8$ V.	133
4.1	Overview of Chapter 4.	138
4.2	MOSFET heat evacuation paths.	139
4.3	Comparison of heat evacuation in PDSOI and FDSOI ..	140
4.4	Variation of heat evacuation areas with different channel dimensions.	141

4.5	Variation of device lifetime with temperature reported by Honeywell in (43).	142
4.6	Decrease of R_{th} with BOX thinning from experimental results using RF technique by Babak in (47). Three different BOX thicknesses were studied.	143
4.7	2-D simulations of the lattice temperature versus BOX thickness in 70 nm long SOI MOSFETs with (a) SiO_2 or (b) alumina BOX ($t_{\text{Si}} = 10$ nm) (114)	144
4.8	Thermal coupling in multi-finger device. Top view of transistor and schematic of the typical temperature rise in the channel, along the heat source in the x-direction, taken from (100). . .	146
4.9	BEOL versus FEOL for sink realization.	149
4.10	Schematic of the gate-connected sink.	150
4.11	Schematic of the floating sink.	150
4.12	Drain current I_d and transconductance g_m vs gate voltage V_g for the "gate connected" and "floating" sinks recorded in saturation at $V_d = 0.9$ V.	153
4.13	Drain current I_d and transconductance g_m vs gate voltage V_g for the "gate connected" and "floating" sinks recorded in linear at $V_d = 50$ mV.	154
4.14	Drain current I_d vs drain voltage V_d for the "gate connected" and "floating" sinks measured at $V_g = 0.9$ V, I_d vs temperature measured shown in inset.	154
4.15	Output conductance g_d vs frequency for the "gate connected" and "floating" sinks at $V_g = V_d = 0.9$ V.	156
4.16	Drain capacitance C_{dd} vs frequency for the "gate connected" and "floating" sinks at $V_g = V_d = 0.9$ V.	156
4.17	Drain current I_d vs Temperature and slope $\frac{dI_d}{dT}$ based on a power law $I_d/I_{d0} \sim \mu/\mu_0 \sim (T/T_0)^{-k}$	158
4.18	Percentage reduction in R_{th} from floating sink to gate connected sink for different bias conditions and over multiple dies.	159
4.19	Averaged drain current I_d vs temperature over the measured dies for the gate-connected and floating sink cases at $V_g = V_d = 0.8$ V.	160
4.20	Cross-sectional schematic of the sink device in BEOL. . .	162
4.21	Schematic for 3D sink configuration.	163

4.22	Drain current I_d and transconductance g_m vs gate voltage V_g for the different sink cases recorded in saturation at $V_d = 0.8$ V.	164
4.23	Drain current I_d and transconductance g_m vs gate voltage V_g for the different sink cases recorded in linear at $V_d = 50$ mV.	165
4.24	Drain current I_d and output conductance g_d vs drain voltage V_d for the different sink cases at $V_g = 0.8$ V.	165
4.25	Output conductance g_d vs frequency for no sink and bigger sink cases at $V_d = 0.8$ V and $V_g = 0.8$ and 0.9 V.	166
4.26	Gain A_V vs frequency for the no sink and bigger sink cases at $V_d = 0.8$ V and at V_g of 0.8 and 0.9 V.	167
4.27	Drain current I_d vs temperature for the different sink cases at $V_d = 0.8$ V and at V_g of 0.8 and 0.9 V.	168
4.28	Drain capacitance C_{dd} vs frequency for the different sink cases at $V_d = V_g = 0.8$ V.	169
4.29	Averaged drain current I_d vs temperature over the measured dies for the three sink cases at $V_g = V_d = 0.8$ V.	170
4.30	Reduction in peak cutoff frequency f_T at $V_g = 0.6$ V (corresponding to $g_{m,\max}$) and $V_d = 0.8$ V. $f_T - f_{\max}$ are normalized with respect to the no-sink case.	174
4.31	Variation in total gate capacitance $C_{gg,T}$ and gate resistance R_g , normalized with respect to the no-sink case.	174
5.1	Connections between the ideas explored in the thesis.	183



1. Introduction

This chapter introduces the background of the thesis. Harsh environments and self-heating, two primary causes of high device operation temperatures are presented. The physical impact of high temperatures on device performance from a theoretical perspective is discussed. Following this, three main scientific questions aimed to be addressed through this research are raised, providing a platform for the context of this research.

1.1 Operation Temperature of MOSFET

Electronics has become an integral part of human life with applications all around us from communications, wearables, healthcare, environmental sensing, smart homes and so on. The scaling of semiconductor technology has helped shrink device size while providing enhanced performance at reduced costs. Recently, the development of advanced generations of mobile networks (5G and now 6G upcoming) along with the Internet-of-Things makes sure that electronic devices pervade further into different domains of applications. To cater to the diverse needs of the upcoming applications to be met, electronics need to be robust and operate reliably over a wide range of application scenarios and conditions. In this thesis, the operation temperature of the device, a parameter that can affect the device's performance and behaviour to a considerable extent, is investigated thoroughly.

For a device operating in a certain environment, we analyze the difference

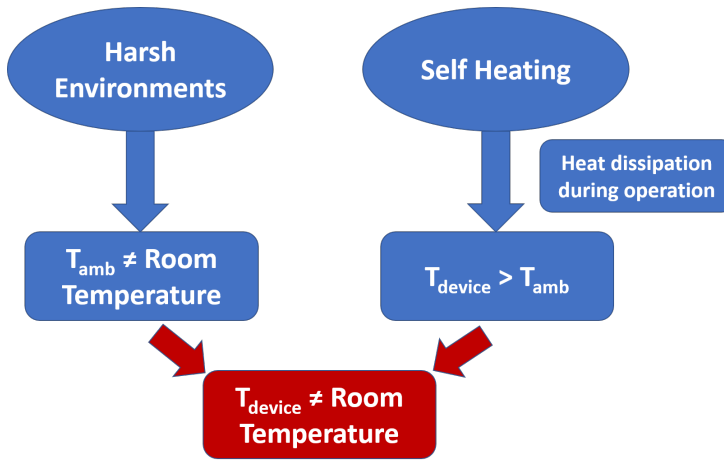


Figure 1.1: Harsh environments and self-Heating: Two situations leading to increased device temperatures.

between two entities: the ambient temperature T_{amb} and the device temperature T_{device} . The ambient temperature T_{amb} and device temperature T_{device} are defined as that of the environment and the device, respectively. While T_{amb} is generally equal to room temperature, thereby giving one the perception that the device operation temperature T_{device} should be equal to that of room temperature, that is not always the case. Two main reasons for different device operation temperatures are:

- Harsh environments
- Self-Heating (SH)

While harsh environments pose a temperature of operation different from room temperature due to an ambient temperature, self-heating raises the device temperature from the ambient temperature due to the device operation. These two cases thus lead to the same end result of having T_{device} different from room temperature as illustrated in **Figure 1.1**. We now delve into a deeper discussion on both of these situations.

1.1.1 Harsh Environments

Harsh environments (also referred to as extreme environments or hostile environments in literature) are those in which applications are subject to one or more of the following extreme conditions: high operating temperature, high

pressure, significant vibration, high humidity, high radiation levels, aggressive media (corrosive, toxic, explosive) and electromagnetic spikes [1].

In this thesis, the focus shall be on high-temperature environments but an overview of radiation environments and low-temperature environments is provided to supplement the discussion. Avenues of applications of radiation-hardened electronics (also referred to as rad-hard electronics) which are less susceptible to radiation damage and low-temperature electronics are also looked into. This shall provide a base for future comparison of different technologies with respect to harsh environment applications in **Chapter 2**.

The study of electronic devices for working in harsh environments is not new; back in 1994, an overview of high-temperature electronics and their potential applications was provided in [2]. A comparison of the above work with a more recent review in 2018 [3] shows that the operation of electronic devices under these conditions is of growing importance day by day due to tremendous growth in the sectors that require their usage. Some of the main types of harsh environments are classified below [3].

Radiation-Rich Environments

Radiation-rich environments are mainly found in space applications, biomedical instruments, nuclear power plants and high-energy physics experiments like the Large Hadron Collider at CERN. An in-depth study of radiation environments, damage mechanisms in such environments and their impacts on semiconductor devices across different technologies can be found in [4].

The interaction of a semiconductor device with an energetic particle results in two main types of damage mechanisms, ionization damage and displacement damage.

- **Ionization damage:** This process disrupts electronic bonds, creating free electron-hole pairs. It is the primary mechanism when energetic photons such as gamma rays and X-rays interact with semiconductor devices.
- **Displacement damage:** High-energy particles displace atoms or nuclei from their usual lattice sites. Generally, displacement damage requires much higher energies than those needed for ionization damage.

Low-Temperature Environments

Cryogenic temperatures below the standard operating range of CMOS ICs, generally specified as $-40\text{ }^{\circ}\text{C}$ constitute low-temperature environments. [3] lists

some of the diverse electronic applications that need cryogenic environments:

- Cooled detectors are used in applications like medical imaging instruments, high-performance computers, satellite receivers, and astronomical instruments. Low-temperature operations help improve system sensitivity given that noise in electronic devices reduces with temperature.
- Electronics for deep space applications like detectors of the James Webb Space Telescope require operation at temperatures as low as -246°C .
- Quantum computing is a very popular domain currently that requires cryogenic operation [5]. With the potential of the quantum computer in solving Quantum chips containing qubits operating at a few tens of mK require CMOS circuits operating down to 4 K for closer system integration [6].

High-Temperature Environments

On the other end of the spectrum of low-temperature environments are high-temperature environments that surpass operation temperatures of 125°C , the conventional maximum limit of operation temperature for commercial and military electronics. With a specific stress on such environments in this thesis, we shall look deeper into the cases where high-temperature electronics become of great interest. A diagrammatic overview of different high-temperature environments is provided in **Figure 1.2**.

1. Automotive Electronics

The automotive industry is a rapidly emerging application domain for the usage of high-temperature electronics. Moving from old-fashioned mechanical and hydraulic systems to newer electromechanical or mechatronic systems causes putting sensors and control electronics closer to heat sources in automobiles. As more electronic components find their way into cars, the automotive electronics market is becoming increasingly popular as an extreme environment.

Under-the-hood automotive environment is a great example of such a high-temperature environment where the necessity to put electronics close to the engine or transmission raises the ambient temperature above 125°C . The temperature faced itself could specifically vary based on the part of the automotive where it is used as shown in **Figure 1.3**; temperatures could vary from 150 to 250°C for on-wheel sensing, 150 to 200°C around on-engine and in transmission, 200 to 300°C for cylinder pressure and

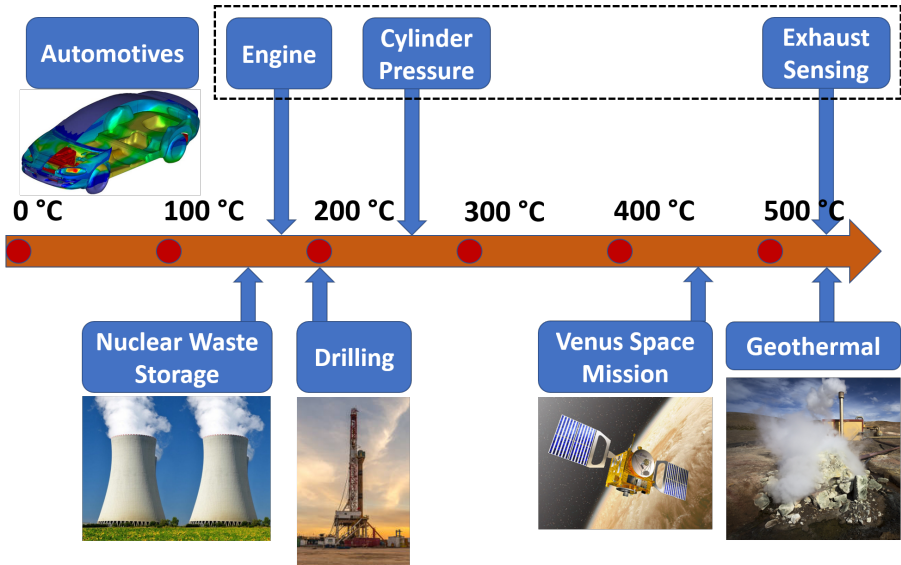


Figure 1.2: Temperature range of operation of various high-temperature environments.

can go up to as high as 850 °C for exhaust sensing, respectively [7]. The sensors to be used in each of these applications must be able to operate at the respective temperature ranges. With the addition of power transistors and smart power devices into the electromechanical actuator, power devices would have to operate at 175 to 200 °C [7]. SOI-based ICs for electronic modules in engines of automobiles could face temperatures up to 175 °C as reported in [8].

Furthermore, hybrid electric vehicles and fuel cell vehicles face high temperatures due to power dissipation. Having devices that can reliably operate at such high temperatures is a big bonus because using thermal management or cooling systems would add weight and cost.

In addition to standard commercial cars, brakes in heavy vehicles like city buses and trucks could face temperatures higher than 500 °C quite regularly for short periods [2]. The brake wear associated with this can cause accidents involving these heavy vehicles and therefore tracking brake temperature using high-temperature resistant antilock brake systems is a way of improving and monitoring the safety of these vehicles.

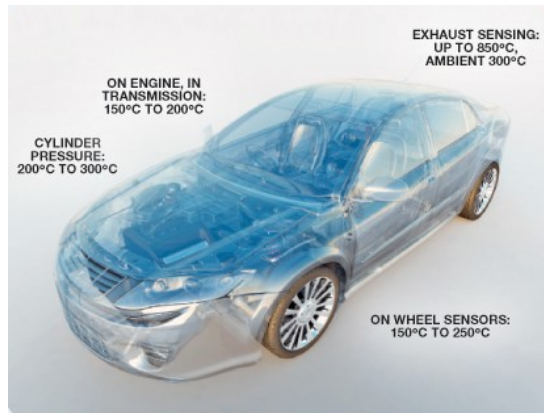


Figure 1.3: Temperature distribution in different parts of the car [7].

2. Aviation Electronics

Another substantial market in the 21st century is that of electronics for aircraft and aerospace applications. Similar to automotive, electronic sensors used in jet engines face high temperatures and therefore many are either placed remotely from the actual measurement point, for example, hydraulic fluid pressure sensors at the ends of isolation tubes or cooled down to below 125 °C. The presence of electronics that would withstand high temperatures would increase the aircraft's reliability while removing the weight of cooling systems [2].

Aerospace electronics is another growing sector for high-temperature applications. Space exploration missions like the Venus mission report temperatures as high as 460 °C [9].

3. Drilling and Geothermal

The down-hole oil and gas industry is one of the oldest users of high-temperature electronics. Both drilling and geothermal wells require sophisticated sensors and electronic components. The operating temperature is directly related to the depth of the well. In general, a geothermal gradient of 25 °C per kilometre of depth is observed but in some cases, it can even be higher. Previously, the maximum temperature limit from drilling stagnated at 150 – 175 °C but with more advanced technologies it is possible to drill deeper. As a consequence of the same, temperatures in such wells can reach over 200 °C with high pressure too. [10].

Geothermal temperatures can go up further to 500 °C [11].

4. High-Temperature Radiation Environments

Nuclear reactors and nuclear waste storage plants are examples of environments where high temperatures can be encountered in addition to radiation. Temperatures in waste storage tanks at the Hanford reservation containing millions of gallons of radioactive chemical wastes can rise up to 150 °C [2].

With a background on how the device operation temperature is affected by the environment it operates in, we shall look at the other possibility where self-heating effect in devices causes an increase in device temperature.

1.1.2 Self-Heating Effect

Self-heating (SH), also known as self-heating effect (SHE) or local thermal effect (LTE) in literature [12], is the phenomenon of a transistor heating up during its operation. As this occurs without the application of any external heating, the name self-heating effect is justified. This phenomenon causes an increase in the device operating temperature with respect to that of the surrounding ambient temperature. More details on SH shall be studied in [Chapter 3](#).

Causes

The primary cause of SH in MOSFETs is Joule's heating arising from the power dissipation due to flow of current in the channel. With this general cause that is responsible for affecting SH in all MOSFETs, there can be specific reasons for enhanced SH as well. In advanced nodes, greater current and power densities are encountered, thereby raising SH concerns. SH is related to heat accumulation in the channel; this means that the evacuation of heat from the channel becomes an important condition in the SH problem. The lesser the ease of heat evacuation from the channel, the higher the SH and vice versa. This implies that the thermal conductivity of the materials used in the MOSFET is crucial: the presence of materials with low thermal conductivities worsen the SH problem. Further details of this in terms of practical situations in advanced MOSFETs where low thermal conductivity of films affects the heat evacuation from the device shall be discussed later in [Chapter 3](#).

Having established that high-temperature environments and SH both result in having higher device operating temperatures, we move to the background of

the physical impacts of high temperatures on device performance and behaviour.

1.2 Limitations of Devices at High Temperatures

The theoretical background on the physics behind why high temperatures affect device performance and in what ways has been studied in [2], [10]. Apart from device performance, reliability is an important aspect to consider at high temperatures; in addition to performance degradation, elevated temperatures greatly reduce device lifetime too [13]. In [14] the thermal dependence of transistor parameters and reliability mechanisms was summarized.

Some of the major factors affecting device performance and reliability at high temperatures are:

1. Increasing intrinsic carrier density: On increasing temperature, the intrinsic carrier density increases owing to the generation of carriers from thermal excitation, rendering doping less effective [2].
2. Increasing junction leakage currents: The increase of junction leakage currents is a strong limiting factor at high temperatures as described in [15].
3. Reduced mobility: In MOSFETs, higher temperatures result in reduced mobility because of higher phonon scattering.
4. Greater electromigration issues: Electromigration in conductors leads to open circuits due to mass transport of the material when stressed at high current densities [16]. The impact of SH on the long-term reliability of CMOS circuits was studied in [17]. Higher device temperatures from SH cause metallization lifetime degradation with the interconnect time-to-failure (TTF) expressed in **Equation 1.1**.

$$\text{TTF} = \frac{A \exp\left(\frac{E_a}{kT}\right)}{J_{\text{ave}}^2} \quad (1.1)$$

where TTF represents the Time to Failure of interconnect, where A is the process-dependent constant, k is Boltzmann's constant, E_a is the activation energy (typically around 0.7–0.9 eV for Cu interconnections), T signifies the absolute temperature of the interconnect, and J_{ave} is the average current density. The time to failure is inversely proportional to temperature, resulting in shorter lifetimes at increased temperatures.

5. Lesser Time to breakdown in ultrathin gate oxides: The TBD in ultrathin gate oxides was also found to be inversely proportional exponentially to the junction temperature as related in **Equation 1.2** below [17]:

$$TBD = T_0 \cdot \exp \left[\gamma \left(\alpha \cdot T_{OX} + \frac{E_a}{kT_j} - V_g \right) \right] \quad (1.2)$$

Where γ represents the acceleration factor, E_a is the activation energy, α denotes the acceleration factor for oxide thickness, T_{OX} is the gate oxide thickness, V_g is the gate voltage, T_0 stands as a constant specific to a particular technology, and T_j corresponds to the average junction temperature. Results there show that the TBD degradation of gate oxides due to SH becomes significant for sub-0.09- μm CMOS nodes.

6. Variation in circuit performance: The physical changes in mobility, intrinsic carrier density etc. can in turn affect circuit performance by inducing temperature dependence in output currents, conductances, transconductances, leakage currents, and threshold voltages.
7. Mechanical stress: Due to a mismatch in coefficients of thermal expansion of materials, mechanical stress can be encountered too [10].

The above limitations showcase the impact high-temperature environments or self-heating can have on devices and stresses on the importance of an in-depth study in this direction.

1.3 22FDX® Technology

The 22 nm FDSOI (Fully Depleted Silicon-on-insulator) technology node (22FDX®) has been used for the studies in this work. Being one of the most advanced nodes in the current market, investigation results on this technology would serve as a great benchmark for comparison of thermal performance and self-heating effect with respect to previous and future technology nodes. 22FDX® is a technology of choice for a wide variety of applications (including some like automotive electronics which are subject to high-temperature environments), making it a suitable candidate for this study. It is reported in [18] that in the first half of 2019, around half of all technical papers on FDSOI technologies were on 22FDX®.

1.3.1 Applications

An extensive review by Chen and Schaeffer [18] highlights numerous research articles published on the 22FDX® technology and establishes the wide applicability of this technology. Research works in diverse domains below for upcoming IoT, 5G/6G applications have been referred to in the review above and are summarized below.

1. Ultra-low voltage, ultra-low power
2. Ultra-low Leakage
3. Power efficient RF for wireless protocols
4. Ultra-low power sensors, eNVMs (embedded non-volatile memories)
5. Energy harvesting
6. 5G: Receivers, LNAs, PAs, VCOs
7. Automotives: FMCW (Frequency-Modulated Continuous-Wave) radars

1.3.2 Features

Carter et al. in [19] published features of 22FDX®; typical cross-section of an nFET device in this technology is shown in **Figure 1.4**. Incorporating the basic ideas of UTBB (ultra-thin body and Buried Oxide) FDSOI technology, the top channel is made so thin that the depletion region beneath the inversion channel extends to the buried oxide (BOX) layer. Due to this, the whole top Silicon film is depleted of carriers and therefore the name fully depleted (FD). The channel is undoped as it helps reduce device variability [20]. The SiO₂ BOX below the channel helps in electrically isolating it from the substrate. The FDSOI transistor architecture in 22FDX® offers a planar alternative to 3D FinFETs

while using a process flow with 30% fewer masks making it more cost-efficient. From an RF performance point of view, excellent RF figures of merit (FoMs) are seen; f_T and $f_{\max}$ values as high as 347 GHz and 371 GHz are demonstrated in [21].

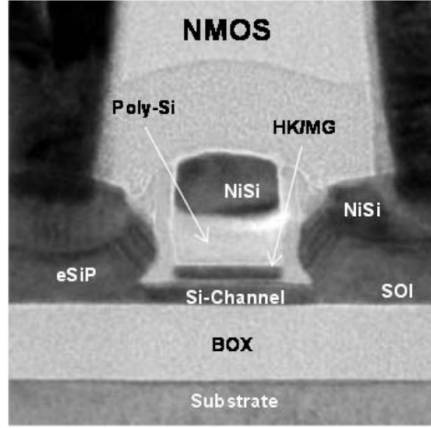


Figure 1.4: Typical cross-section of an NFET in 22FDX[®] [19].

1.3.3 Back-gate Biasing

A unique feature of UTBB FDSOI technology is that of the back-gate biasing. In this technology, by applying a voltage on the back-gate (a doped region below the BOX), electrostatic control of the channel is possible. This can be imagined as a double gate scenario with the regular gate and the gate oxide on top and the back-gate and buried oxide below.

Using back-gate biasing in 22FDX[®], designers can tune the threshold voltage V_{th} of the MOSFET even after it has been processed. While body biasing in bulk is only limited to a small extent and is less efficient in advanced nodes, using back-gate biasing in FDSOI can help tune the V_{th} to a much larger range, allowing performance optimization. A comparison of the above was made in [22] on the 28 nm node for bulk and FDSOI: 1 V variation in V_{bg} is seen to change V_{th} by 25 mV in bulk compared to 85 mV in FDSOI. Biases of either polarity can be applied on the back gate to decrease or increase V_{th} and thereby make the device more suitable for ultra-low power (ULP) or ultra-low leakage (ULL) applications respectively.

1.4 Objectives and Thesis Structure

With the high-temperature device operation scenario in mind, three main scientific questions are framed. The target of this thesis is to answer these questions with the theoretical background in mind backed by experimental results and model data. Each question is addressed in a different chapter with the structure described below and represented pictorially in **Figure 1.5**.

Question 1: What impact do high-temperature environments have on the RF and DC performance of state-of-the-art FDSOI MOSFETs?

Chapter 2 tries to answer this question by mimicking high-temperature conditions in the laboratory. 22 nm FDSOI MOSFETs are heated up to temperatures as high as 175 °C and an experimental assessment of the impact of higher operating temperatures on the MOSFET performance is carried out. The variation of different RF and DC performance metrics is studied under different bias conditions.

Question 2: What are the best techniques of self-heating characterization and what are the related shortcomings?

In **Chapter 3**, the various methods of self-heating assessment are discussed and the two most prominent techniques suited for state-of-the-art devices are investigated in detail. The pros and cons of the traditional gate-resistance technique and the RF technique are assessed. Additionally, factors like test structure layout impact on the extraction of SH parameters are investigated.

Question 3: What could be done to mitigate self-heating? What are the pros and cons of different methods of doing so?

Chapter 4 aims to look into methods of addressing the self-heating problem. Heat sinks in the back-end of line are proposed to reduce thermal resistance in MOSFETs and through designed sinks of different sizes, the efficiency of the sink with respect to its area is demonstrated. The impact of the sink on RF performance due to additional parasitics coming from the sink is studied and a tradeoff between SH reduction and RF performance degradation is established. The pros and cons of heat sinks and other SH reduction methods are studied.

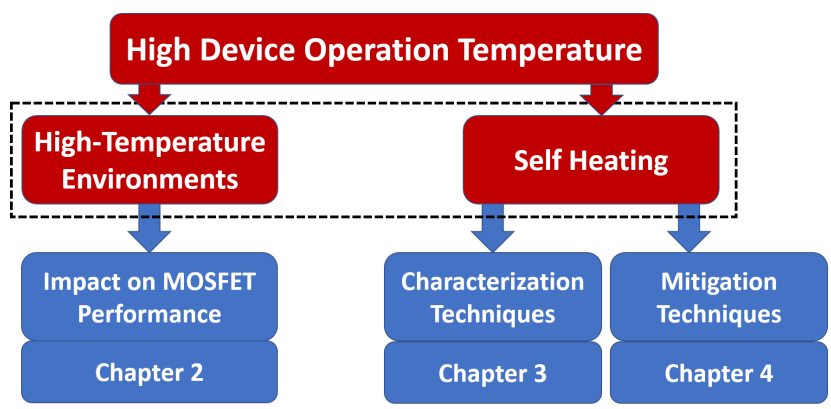
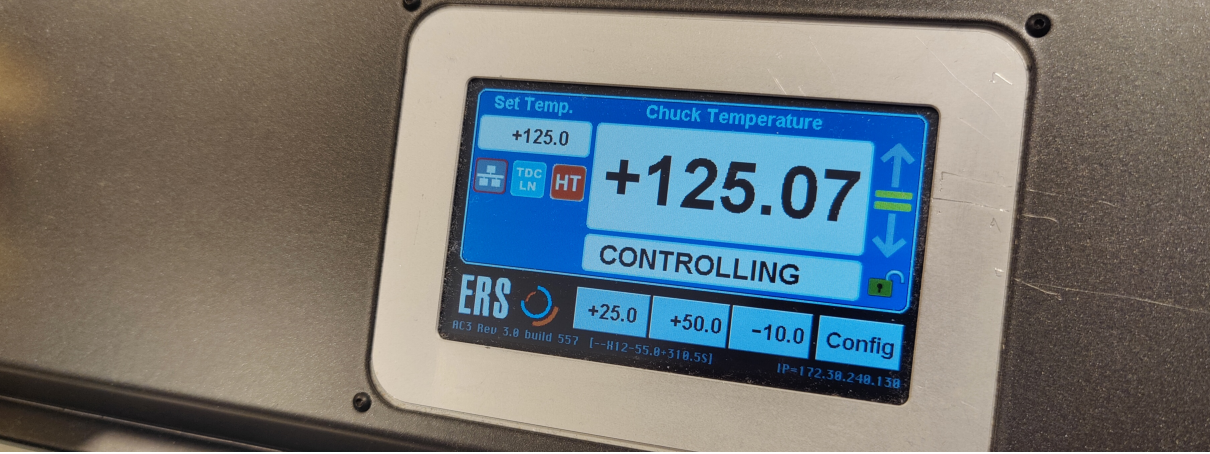


Figure 1.5: Structure of the Thesis.



2. Impact of High Temperature on MOSFET Performance

This chapter delves into the study of the performance of transistors at high temperatures. State-of-the-art MOSFETs on 22FDX[®] from GlobalFoundries, a technology node of choice for current and upcoming market applications, are subjected to high temperatures in the laboratory for this study. The variations in RF and DC figures of merit under different bias conditions are investigated and perspectives on the usage of FDSOI technology for high-temperature environments are provided.

2.1 Introduction

With a background of different harsh environments in [Subsection 1.1.1](#) of [Chapter 1](#), the focus shall be on high-temperature environments. A comparison between different technologies based on their high-temperature performance is first made with a specific focus on silicon-based technologies. Demonstrating the strengths of SOI technology in this regard, a literature review of high-temperature studies on SOI MOSFETs made previously is carried out. Following this, our original research on the impact of temperatures up to 175 °C on the RF and DC FoMs of state-of-the-art 22FDX[®] MOSFETs is shown. The experimental results are also compared with that of PDK models and general perspectives including that of back-gate biasing to help counter temperature variations are provided. The chapter flow is shown in [Figure 2.1](#).

The major physical effects limiting device performance at high temperatures

have been listed in **Section 1.2** of **Chapter 1**. To recap, the main concerns for high-temperature operation are degraded device performance and reliability issues. While our main focus in this thesis shall be on the MOSFET performance perspective, it is necessary to highlight some other crucial aspects.

Reliability is a major factor to take into account for such operation scenarios: it is important to emphasize that for modern robust IoT applications having a long device lifetime is crucial. Moreover, it is important to understand that passive components and packaging technologies can profoundly influence device functionality and system reliability. It is therefore essential to address packaging limitations and explore alternative solutions to meet the demands of harsh environmental applications as stressed by Hassan in [3]. Additionally, from an ecological perspective in general, having higher device lifetimes is always desired; therefore understanding the causes of failure and limitations of device technologies from a thermal aspect is worth looking into.

With these general viewpoints, we now delve into a comparison of different technologies and their behaviour in high-temperature environments.

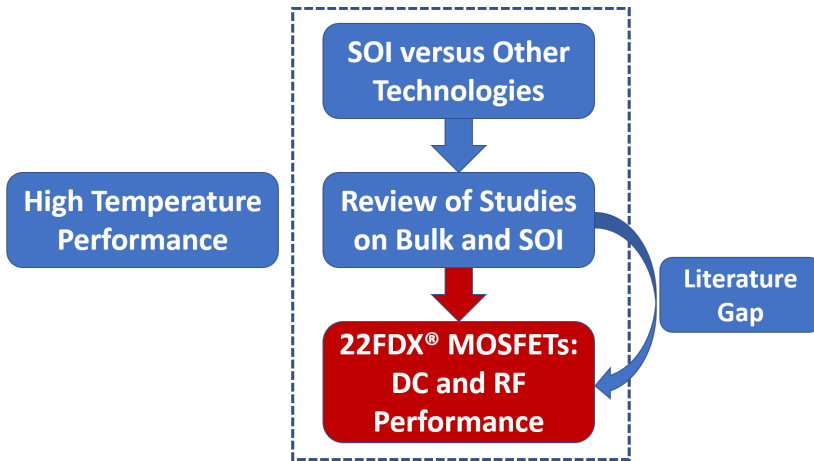


Figure 2.1: Overview of Chapter 2.

2.1.1 Impact of Temperature on Device Performance Metrics

Having summarized the main limitations of device performance at high temperatures in [Section 1.2](#), a more detailed discussion on the theoretical background is done here.

Mobility

The mobility of carriers in a semiconductor is affected by mainly two types of scattering mechanisms: lattice scattering and impurity scattering. In lattice scattering, phonons are either absorbed or emitted. As the density of phonons in a solid increases with temperature, the scattering time associated with this process decreases with temperature, reducing mobility. Impurity scattering occurs when charge carriers interact with impurity atoms or defects within the crystal lattice. These impurities create localized electric fields that scatter the carriers [23].

At high temperatures, the amplitude of lattice vibrations increases, leading to more frequent scattering events and significantly reducing mobility. At low temperatures, impurity scattering becomes the primary mechanism limiting carrier mobility due to the reduced influence of lattice vibrations. Therefore, in the case of high-temperature environments (which are the main targets to study in this thesis), lattice scattering is the dominant mechanism.

As per [Equation 2.1](#) below as described in [24]. μ_{eff} represents the effective mobility, μ_{eff0} denotes the effective mobility at room temperature, T is the mean channel temperature, T_0 is the ambient temperature, and k stands for the temperature-dependent factor affecting mobility degradation, with k ranging from 0.8 to 2.1 in MOSFETs.

$$\mu_{\text{eff}} = \mu_{\text{eff0}} \left(\frac{T}{T_0} \right)^{-k} \quad (2.1)$$

Threshold Voltage

The threshold voltage V_{th} is a key parameter in MOSFET modelling, referring to the gate voltage at which significant drain current begins to flow. The variation of the threshold voltage of an n-channel MOSFET (bulk or SOI) has been documented in detail in [15] and [25].

$$V_{\text{th}} = \Phi_{\text{MS}} + 2\Phi_F - \frac{Q_{\text{ox}}}{C_{\text{ox}}} - \frac{Q_{\text{depl}}}{C_{\text{ox}}} \quad (2.2)$$

where Φ_{MS} , Φ_F , Q_{ox} , Q_{depl} , and C_{ox} are the metal-semiconductor work function difference, the Fermi potential, the charge density in the gate oxide, the depletion charge controlled by the gate, and the gate oxide capacitance, respectively.

For PDSOI devices, the depletion charge Q_{depl} is replaced by $qN_a x_{dmax}$, where x_{dmax} is the maximum depletion width allowed for the doping concentration N_a under consideration, and is equal to

$$x_{dmax} = \sqrt{\frac{4\epsilon_{Si}\Phi_F}{qN_a}} \quad (2.3)$$

where ϵ_{Si} is the relative permittivity of Silicon and q is the charge of the electron.

For n^+ polysilicon gates, the value of the work function difference is given by [26]:

$$\Phi_{MS} = -\frac{E_g}{2} - \Phi_F, \quad \text{with} \quad \Phi_F = \frac{kT}{q} \ln\left(\frac{N_a}{n_i}\right) \quad (2.4)$$

where E_g , T , k and n_i are the silicon energy band gap, temperature, Boltzmann's constant and the silicon intrinsic carrier concentration, respectively.

The intrinsic carrier concentration n_i varies with temperature as per the relation:

$$n_i = 3.9 \times 10^{16} T^{3/2} e^{\left(\frac{-E_g}{2kT}\right)} \quad (2.5)$$

The temperature dependence of the threshold voltage can be obtained from **Equation 2.2** and **Equation 2.4**. For simplification, we will assume that Q_{ox} and E_g show no temperature dependence and $\frac{d\Phi_F}{dT}$ is given by:

$$\frac{d\Phi_F}{dT} = 8.63 \times 10^{-5} \left[\ln(N_a) - 38.2 - \frac{3}{2} \{1 + \ln(T)\} \right] \quad (2.6)$$

In the case of bulk or thick-film SOI devices, the threshold voltage shift with temperature is:

$$\frac{dV_{th}}{dT} = \frac{d\Phi_F}{dT} \left[1 + \frac{q}{C_{ox} V_t} \frac{\epsilon_{Si} N_a}{\ln\left(\frac{N_a}{n_i}\right)} \right] \quad (2.7)$$

For thin-film FDSOI devices, Q_{depl} ranges between $qN_A t_{si}$ and $\frac{qN_A t_{si}}{n}$, where t_{si} the silicon film thickness and n ranges between 1 and 2. Assuming that these

two parameters are temperature independent, the threshold voltage shift with temperature further simplifies to **Equation 2.8**.

$$\frac{dV_{th}}{dT} = \frac{d\Phi_F}{dT} \quad (2.8)$$

As reported in [27], the values for $\frac{dV_{th}}{dT}$ range between -0.7 and -0.8 mV/°C in thin-film SOI MOSFETs and between -2.4 and -3 mV/°C for bulk and thick film SOI MOSFETs. A significantly high $\frac{dV_{th}}{dT}$ is thus seen for bulk devices with respect to thin film FDSOI devices.

Transconductance

For an applied drain-source voltage V_d , a MOSFET's ability to amplify the input signal is quantified by its transconductance g_m , which is defined as **Equation 2.9**.

$$g_m = \frac{\partial I_d}{\partial V_g} \quad (2.9)$$

If the applied drain voltage V_d causes the MOSFET to operate in the saturation region, the transconductance is called saturated transconductance.

The drain current I_d in the saturation region is given by **Equation 2.10**:

$$I_d = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L} \right) (V_g - V_{th})^2 (1 + \lambda V_d) \quad (2.10)$$

To find the transconductance g_m in saturation, we take the derivative of I_d with respect to V_g .

$$g_m = \frac{\partial I_d}{\partial V_g} = \frac{\partial}{\partial V_g} \left(\frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L} \right) (V_g - V_{th})^2 (1 + \lambda V_d) \right) \quad (2.11)$$

Assuming $\lambda V_d \approx 0$ (for simplicity):

$$g_m = \mu_n C_{ox} \left(\frac{W}{L} \right) (V_g - V_{th}) \quad (2.12)$$

Considering the temperature dependence of the carrier mobility μ_n :

$$\mu_n(T) = \mu_{n0} \left(\frac{T}{T_0} \right)^{-k} \quad (2.13)$$

Therefore, the temperature-dependent transconductance $g_m(T)$ in the saturation region is:

$$g_m(T) = \mu_{n0} \left(\frac{T}{T_0} \right)^{-k} C_{ox} \left(\frac{W}{L} \right) (V_g - V_{th}(T)) \quad (2.14)$$

where:

- μ_n is the carrier mobility
- C_{ox} is the oxide capacitance per unit area
- W is the width of the MOSFET channel
- L is the length of the MOSFET channel
- V_g is the gate-source voltage
- V_d is the drain-source voltage
- V_{th} is the threshold voltage
- λ is the channel-length modulation parameter
- μ_{n0} is the mobility at a reference temperature T_0
- T is the operating temperature
- k is a positive constant (typically around 0.8 to 2.1 for MOSFETs).
- $V_{th}(T)$ is the threshold voltage at temperature T

Zero Temperature Coefficient

Considering the relation between for the drain current I_d in the saturation region in **Equation 2.10**, it is observed that there are two temperature-dependent parameters: mobility μ_n and threshold voltage V_{th} . I_d is directly proportional to μ_n and inversely proportional to V_{th} as $(V_g - V_{th})$ reduces with increasing V_{th} .

With an increase in temperature, both the threshold voltage and the mobility decreases. It is seen that these two mechanisms affect the drain current differently with an increase in temperature as listed below (and vice versa with a decrease in temperature).

- I_d should decrease due to mobility reduction with temperature.
- I_d should increase due to V_{th} reduction with temperature as it causes $(V_g - V_{th})$ to increase.

At lower V_g , the V_{th} reduction effect causes the I_d to increase with temperature and at higher V_g , the mobility reduction comes into play and causes I_d to reduce with temperature. These two mechanisms balance each other at a Zero Temperature Coefficient (ZTC) point where I_d is invariant with temperature. At the I_d -ZTC, these two mechanisms balance each other resulting in a temperature-invariant I_d . The existence of the ZTC point has been reported in studies in literature [28] [29]. In [30] it was observed that designing circuits (particularly for analog applications) to operate at the ZTC point results in significantly less variation of device parameters with temperature.

It is to be noted that a similar ZTC point (referred to as g_m -ZTC in this work) is also obtained for g_m , but at a different V_g . Equation shows that μ_n and V_{th} affects g_m in a similar manner as I_d , which results in having a similar ZTC point for g_m too.

2.1.2 SOI versus Other Technologies

A comparison between some of the most prominent modern technologies and their advantages and disadvantages for harsh environment applications is now made.

Bulk Silicon

While bulk technologies work reliably for most standard commercial applications, they face limitations for operation in temperature ranges outside the standard commercial range of -55 to 125 °C. At higher temperatures, rising leakage currents turn out to be a hindrance and can result in I_{on}/I_{off} ratios which are unacceptable for many circuits [31]; moreover threshold voltage is also seen to have temperature sensitivity. Bulk Silicon technologies are also sensitive in radiation environments; radiation exposure considerably impacts device operation and could result in device failure.

SOI

SOI turns out to be an enhanced alternative to bulk Silicon technology. The presence of the Silicon dioxide buried oxide (BOX) reduces the junction leakage currents and enables operation up to higher temperatures. Compared to bulk Silicon, SOI circuits are therefore capable of operating at temperatures higher than 300 °C due to reduced leakage currents are much smaller (often by one to two orders of magnitude) and the threshold voltage is also less sensitive to temperature [32].

With FinFETs being one of the other prominent choices for commercial applications, a brief look at their harsh environment application perspective is made. Limited studies on the high-temperature performance of FinFETs are observed: in [33], TCAD simulations of FinFETs are made to compare bulk and SOI FinFETs. It is observed that the performance metrics like I_{on}/I_{off} ratio, subthreshold swing and transconductance vary with the fin dimensions which play a crucial role. It is observed that the aforementioned performance metrics are better on SOI substrate compared to bulk. However, multi-fin transistors on bulk silicon show higher on-current but with increased leakage current.

SiGe

SiGe has shown capabilities of functioning in harsh conditions over a wide temperature range from cryogenic to high temperatures and under exposure to radiation. It was argued in [34] that the distinctive bandgap-engineered characteristics of SiGe HBTs hold immense potential to fulfil the requirements

of all three extreme environmental applications concurrently. From a high-temperature perspective, using SiGe circuits up to 300 °C has been shown in [35].

SiC

In applications where extreme environmental conditions have a moderate intensity (up to 300 °C), bulk Silicon, SOI and SiGe technologies are appropriate choices to fulfil electrical and electronic requirements. However, as the environmental conditions become extremely harsh, the aforementioned semiconductors become less effective [3]. In such cases, an advanced semiconductor generation, like silicon carbide (SiC), needs to be developed to meet the demanding requirements, with demonstrated operation as high as 500 °C [36].

GaN

Due to its high-voltage operational capacity and minimal resistive losses, the GaN platform is identified as a suitable option for power amplification and switching applications across a broad operational temperature range as high as 600 °C [37]. Nonetheless, challenges such as thermal management, manufacturing costs, wafer-level uniformity, and enhancing reliability serve as obstacles to the successful commercialization of this technology [3].

The temperature range of applicability of different technologies are illustrated in **Figure 2.2**. A summary of the different technologies in [3] shows that in general SOI is of the technologies that ticks mostly all the boxes concerning high-temperature, low-temperature and radiation environments while being easily available and cost-efficient. While SiC and GaN technologies are even more robust for applications in harsh environments, it is to be kept in mind that their costs and manufacturing ability are not as great as SOI. Apart from being an established mature technology, with SOI not using as many rare materials or complicated material extraction processes (like GaN technology for example), it provides a viable, simple and ecological solution for high-temperature applications in moderately harsh environments [38].

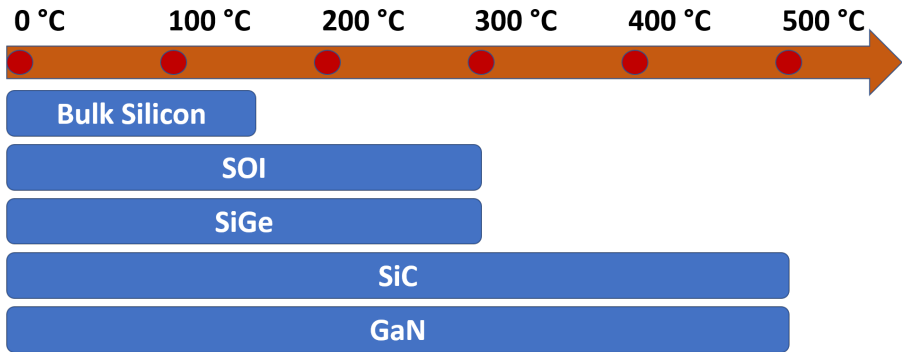


Figure 2.2: Comparison of different technologies for high-temperature applications.

2.1.3 High-Temperature Studies on SOI Devices in Literature

With the prospect of SOI technology for high-temperature applications established, a review of previous studies is made.

Over a couple of decades back, the advantages of SOI over bulk Silicon CMOS processes especially as a candidate for high-temperature electronics were highlighted in [2] and [15]. While bulk CMOS circuits could not operate above 180°C, their SOI counterparts could still operate at 300°C due to lesser leakage currents in the latter. Colinge in [15] reported junction leakage currents in SOI device three orders of magnitude lesser than its bulk counterpart.

A summary of comparison on bulk, PDSOI and FDSOI MOSFETs for use elevated temperatures was proposed in [38] based on maintaining acceptable standards of threshold voltage and leakage currents:

- Bulk MOSFETs are suitable for use up to 200 °C, requiring intricate optimization of process and circuit designs beyond this temperature threshold.
- PDSOI transistors expand the temperature range to 250 °C and may confer radiation hardness, which can be advantageous for nuclear applications.
- FDSOI devices could operate 50 °C higher than PD devices.

Floating-body (FB) and body-tied (BT) PDSOI transistors were studied at high temperatures over a range of 25 to 250 °C back in 2008 [39]. The impact

of temperature on certain RF FoMs like intrinsic transconductance and cutoff frequency was seen to be relatively higher compared to that on some other small-signal equivalent circuit (SSEC) parameters. While the FB devices exhibited poorer DC performance (higher leakage and a worse $I_{\text{on}}/I_{\text{off}}$ ratio), they outperformed BT devices from a temperature stability standpoint, particularly in terms of intrinsic transconductance. Optimizing the features of FB and BT devices in order to attain good performance was therefore recommended. A decade back [40] compared PDSOI and bulk Silicon MOSFETs which were mainly the two possible frontrunners in the technology of choice going forward with respect to low-voltage and low-power applications.

From a more practical perspective, some solutions available commercially from industry solutions or research organizations are looked into. Fraunhofer Institute for Microelectronic Circuits and Systems reports a specialized 0.35 μm high-temperature SOI-CMOS technology that has been developed to accommodate operations at temperatures as high as 300 °C [41]. To enhance the reliability of high-temperature electronics and mitigate electromigration-induced degradation, this technology incorporates tungsten instead of conventional aluminium metallization. On this technology, high-temperature electronics up to 300 °C for signal conditioning tasks for sensors in harsh environments were demonstrated in [42].

Honeywell, a leading provider of high-temperature electronic components, uses SOI CMOS technology [43]. Back in 1999, a high-sensitivity piezoresistive SOI sensor operating up to 300 °C was demonstrated in [44]. Honeywell's products offer notable reliability and performance benefits over conventional silicon integrated circuits, particularly in operating conditions exceeding 150 °C. Reliable operation for five years at 225 °C is advertised with brief excursions to higher temperatures being possible.

From a circuit perspective, an example of an FMCW automotive radar on 22FDX[®] has been shown by Lee in [45]. It is observed that there is a temperature impact on the output power; the output power (shown in **Figure 2.3**) is seen to drop from 10.6 dBm at 25°C to 8.8 dBm at 125°C, emphasizing on the impact of temperature at a circuit level.

There is a dearth of work at high temperatures on state-of-the-art technology nodes. To the authors' best knowledge, just [46] studied the performance of MOSFETs in 22FDX[®] technology, although the main goal of the work was the high-frequency performance of these devices rather than high temperature with

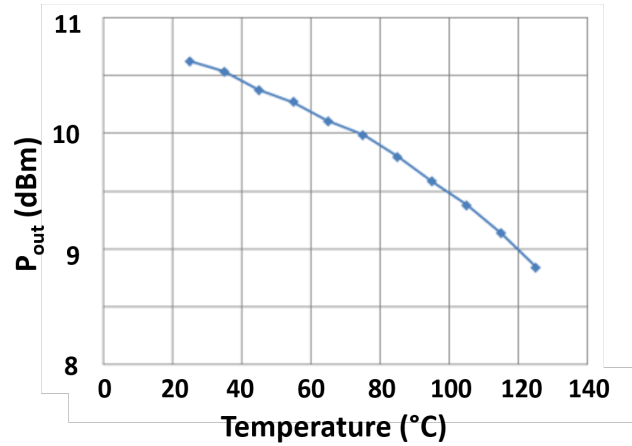


Figure 2.3: Variation of Output Power P_{out} versus Temperature for FMCW Radar in [45]. The impact of temperature on circuit performance is demonstrated.

limited discussion on data versus temperature. The variation in RF FoMs was presented as a secondary message from measurements on three temperature data points of 25, 75 and 125 °C. A thorough study in this direction would help in advancing the state-of-the-art especially also concerning low-power applications by considering trends under different bias conditions.

2.2 High-Temperature Characterization

To supplement the background on-wafer device characterization used in this thesis, we discuss various aspects related to it, specifically concerning high-temperature characterization.

2.2.1 RF Characterization

The general flow of the RF characterization used in this work is as follows:

1. Connect and interface equipment: Gather all necessary equipment including the probe station, VNAs, DC and RF probes, DC and RF cables, IV instruments for biasing, and a computer for equipment control. Connect them using GPIB cables to interface and communicate with the equipment via the Integrated Circuits Characterization and Analysis Program (IC-CAP).
2. Probe Planarization: Ensure that the tips of the RF probes are on the same horizontal plane [25]. By making contact with a substrate, compare the scratches made by the probe tips and adjust the probe's planarity to match.
3. Calibration: Perform RF measurements to ensure that S-parameter measurements are corrected to eliminate parasitic effects caused by cables, connectors, and probes.
4. Measurements: After calibration, conduct measurements on the Device Under Test (DUT) through IC-CAP. Define the necessary DC and RF fields to be measured, along with biasing conditions and settings for the VNAs and Source-Measure Units (SMUs). Measured results can be viewed instantly on IC-CAP.
5. Extractions and Post-Processing: Export the measured data as .mdm files and utilize extraction routines in MATLAB to analyze the results in detail.

Calibration

The S-Parameters measured by the VNA need to be corrected ("calibrated") to remove the effect of the cables and connectors. The calibration step brings the reference plane from the VNA to that of the RF probe tips. During calibration, error terms are determined on each port of the VNA which are removed from the measured data in an error-correction step [47]. The error correction terms are computed by measuring different standards. Details of the calibration process can be found in [48].

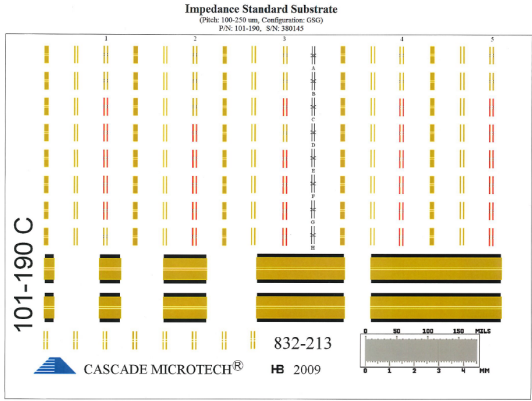


Figure 2.4: Calibration Kit 101-190C used for calibration in this thesis.

Various types of calibration methods exist, each relying on the measurement of certain standards. For example, the very popular SOLT calibration method makes use of Short, Open, Load and Thru standards. An Impedance Standard Substrate (ISS), also known as a calibration kit or calkit, provides the standards necessary for calibration.

Interfacing with the Wincal software helped communicate with the VNA and set up the calibration process by listing the types of probes and calkit information easily. The type of calibration (SOLT, LRRM etc) could also be chosen directly on the software. In our case the ISS 101-190C from Cascade Microtech (**Figure 2.4**) which is compatible with the calibration of GSG probes of pitch 100 – 250 μm is used in this work.

2.2.2 High-Temperature Characterization Setup and Equipments

In all of the studies in this work, high-temperature characterization has been used. Details about the specific equipment and probes that need to be kept in mind for these measurements are listed below.

The measurements were carried out at the WELCOME characterization facility at Université catholique de Louvain. For high-temperature characterization, two probe stations with hot-chuck capabilities, namely the PM8 and MPI TS3000-SE, were used.

PM8 Probe Station with Thermochuck

From a measurement setup point of view, a chuck that can be thermally controlled to have an elevation in temperature is needed. A thermochuck from Temptronic associated with a PM8 probe station allows us to increase chuck temperature up to 300 °C allowing excellent control of the temperature too (Figure 2.5).

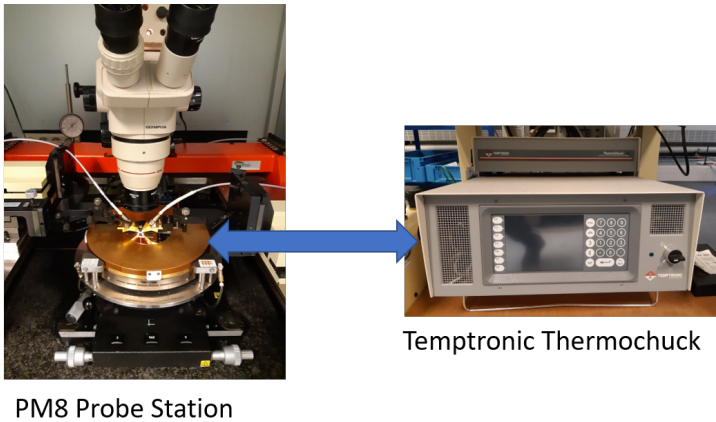


Figure 2.5: PM8 Probe Station with Thermochuck.

MPI TS3000-SE Probe Station with Thermal Chuck

The MPI TS3000-SE probe station provides a more advanced semi-automatic measurement setup for various types of characterization as seen in Figure 2.6. This probe station comes with thermal chuck integration: chuck temperatures up to 300 °C can also be reached similarly on the MPI TS3000-SE semi-automatic probe station. Accurate temperature control is guaranteed and the setup provides a more closed environment. The thermal systems are operable through a fully integrated touchscreen display positioned conveniently in front of the operator, enabling quick operation and providing immediate feedback.

Probes

|Z| probes from FormFactor (Figure 2.7), which are compatible with high-temperature measurements are predominantly used in this work. These probes are specifically engineered for testing in harsh environments, making them ideal for our characterization needs. The patented technology behind the |Z| Probe

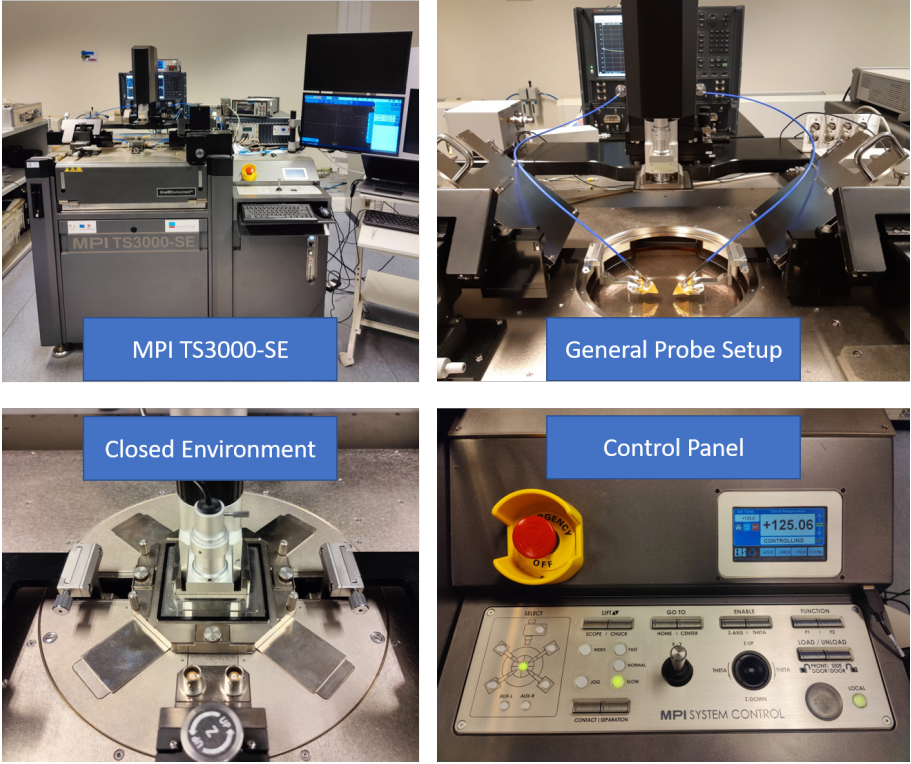


Figure 2.6: Measurement setup on the MPI Probe Station.

ensures precise measurements with minimal contact resistance and superior impedance control. By confining the RF/Microwave signal to a single transition within the shielded, air-isolated probe body’s coplanar contact structure, signal integrity remains intact even in extreme temperature conditions [49].

The three-tip GSG (ground-signal-ground) with a pitch of 100 μm is taken in our case, with equivalent RF pads used in our design. We limit operation to 175 $^{\circ}\text{C}$ to ensure probe safety and long-term operability. From a frequency point of view, the Z40 probes used in this work are limited to 40 GHz.

2.2.3 High-Temperature Characterization Safety Tips

Some of the recommended tips to keep in mind during high-temperature characterization are:

- 1. Separation between the probe and die during temperature change: While



Figure 2.7: |Z| Probe used for high-temperature measurements.

changing temperature from one value to another, the probe should not be kept in contact with the die from a probe safety point of view. Changes due to thermal expansion cause an increase in the height, and in fact, the contact needs to be readjusted at each temperature point too.

2. Duration of contact: At temperatures over 150°C, limiting probing contact duration is recommended. Ensuring that the probes are separated from the die as soon as the measurements are completed is suggested.
3. Steadying temperature: While the chuck sensor reaches the targeted temperature value, it should still be left to stabilize for 30 minutes to ensure the device is also at the same temperature. Ideally, the longer this duration, the better, but a timeframe of around 20-30 minutes is recommended.

2.3 22FDX[®] MOSFET Performance at High Temperatures

Having discussed the background of high-temperature electronics, the physical effects happening in devices at high temperatures, literature review on the same and characterization setup, we come to our contribution in this domain. The lack of a thorough study at high temperatures on the most advanced nodes provides the perfect opportunity to add to the existing literature. With the 22 nm FD-SOI technology from GlobalFoundries being an established choice for a broad range of applications including harsh environment applications like automotive electronics, it has been used as the base for devices studied in this work.

In addition to high-temperature applications, 22FDX[®] serves low-power applications, which is of growing importance owing to the widespread expansion of the IoT. Specific applications where low-power RF applications like ultra-low-power (ULP) radios and RF front-ends are of interest are those of Bluetooth Low Energy Receiver front-ends [50] [51]. A proposed Ultra-low-voltage (ULV) RF front-end is shown in [50]. In [52], the use of forward body biasing on 22 nm FD-SOI MOSFETs has been introduced to design LNAs under low supply voltage and DC power. In particular, automotive IoT deploys low-power technology that requires operation under harsh environments [53]. These aforementioned works underline the growing importance of low-power RF applications in the current electronics market. As applications like automotive electronics potentially face high temperatures along with in-demand state-of-the-art low-power electronics applications, an attempt to study the temperature aspects at different bias conditions has also been made.

2.3.1 Objectives

In this work, the results of which have been published in [54] and [55], the target is to focus entirely on the high-temperature performance of 22FDX[®] MOSFETs for a temperature range from room temperature of 25 °C to 175 °C, going beyond the standard maximum rated PDK temperature value of 125 °C and that done in the work from Dadash [46]. Having established the fact that modern high-temperature electronic applications would have to reliably work at temperatures higher than 125 °C, this prepares a case study of high-temperature MOSFET performance on an advanced node.

The effect of increased temperature on the RF and mm-wave performance metrics of advanced FDSOI MOSFETs using on-wafer measurements under

different drain (V_d) and gate (V_g) bias conditions is studied. With an eye on low-power applications, studies are additionally made in this work at a lower drain voltage V_d of 0.6 V compared to the nominal value of 0.8 V. To go beyond our initial conclusions in [55], we study in detail the small-signal equivalent circuit (SSEC) parameters and compare the f_T and $f_{\max}$ coming from the computation from SSEC parameters in [54]. The trends are verified with repeatable measurements over multiple dies. The variation of the RF FoMs and SSEC parameters of MOSFETs on 22 nm FD-SOI technology going up to 175°C is demonstrated for the first time to our best knowledge, while the Process Design Kit (PDK) models are limited to a maximum temperature value of 125°C. Apart from studying the impact of temperature on peak f_T and $f_{\max}$, the significance of the g_m zero temperature coefficient (ZTC) point is stressed on. RF FoMs are extracted at three different gate bias conditions (V_g) corresponding to the maximum g_m , to the g_m -ZTC, and below the g_m -ZTC.

2.3.2 Experimental Details

Device under Test

The device details of the 22FDX[®] MOSFETs in this study are as follows: nMOSFETs in common source configuration are used with gate length 20 nm, total width 60 μm composed of 120 fingers (20 fingers with a multiplicity of 6) of 0.5 μm finger width.

Measurement Setup

A detailed description of a background on the characterization procedure, equipment, probes and VNAs used for measurements has been discussed in [Section 2.2](#).

For the RF characterization, S-parameters are measured in a frequency range from 200 MHz up to 40 GHz. The measurements are made on an MPI TS3000-SE probe station. A PNA-X vector network analyzer and two Ground-Signal-Ground RF $|Z|$ probes of 100 μm -pitch are used for these measurements. The probes are compatible with high-temperature measurements up to the necessary temperature value of 175°C. LRRM (Load-reflect-reflect-match) method is used for calibration at each temperature point separately. While the devices are placed on the primary chuck of the probe station that is heated up, the calibration kit is placed on an auxiliary chuck beside the primary chuck. The calibration procedure needs to take into account the variation of temperature on the standard values themselves. It is therefore verified that the resistance of the

load standard is very steady with temperature and a variation of just 0.3% is seen which is comparable with the variation of one load standard to another. For each device, dedicated Open and Short structures are measured and used for de-embedding. The measurements are carried out at 4 temperature points: 25, 75, 125 and 175°C. The de-embedding structures are measured at each temperature and used correspondingly for the extractions at those temperature values. While the primary chuck on the MPI probe station can be heated up to 300°C with accurate and stable temperature control, the limit of safe temperature range of operation was the reason for limiting the highest temperature value to 175°C. To have a steady temperature value while measuring, the whole system was let to steady for at least half an hour at each set temperature. The back-gate of FD-SOI was grounded for all the experiments ($V_{bg} = 0$ V).

2.3.3 Results and Discussion

IV Characterization

The I_d - V_g characteristic of the device is shown in **Figure 2.8** in saturation at $V_d = 0.8$ V for temperatures varying from 25 to 175°C. One of the primary observations is that of the Zero Temperature Coefficient (ZTC) point for drain current I_d -ZTC. This is the V_g bias corresponding to which I_d is constant with temperature, observed at around 0.62 V (at $V_d = 0.8$ V) in measurements. The I_d -ZTC observed in the PDK model with the MOSFET is at V_g 0.57 V. The difference compared with values extracted from measurements is expected to be due to external series resistances on the source and drain which can affect these DC curves.

Another observation that is observed from the logarithmic I_d - V_g plot in **Figure 2.9** is the increase in the leakage current I_{off} with increasing temperature. Quantitatively, the measured leakage current is seen to rise by over two orders of magnitude as the temperature is increased from 25 to 175 °C. This is in accordance with the theory that thermal generation on carriers at higher temperatures gives rise to greater leakage and quantitatively from [15] which reported an increase in the leakage current in SOI from pA range at 25°C to around nA range at around 200 °C. One difference that needs to be pointed out is that of the subthreshold current modelling in the PDK. As shown in **Figure 2.9**, it is seen that the agreement between the measured and PDK for I_d is quite good at room temperature but the difference gets stronger at higher temperatures. The I_{off} in the measurements is seen to be lower than predicted by the PDK.

In **Figure 2.10**, the ZTC point for the transconductance g_m is found to be

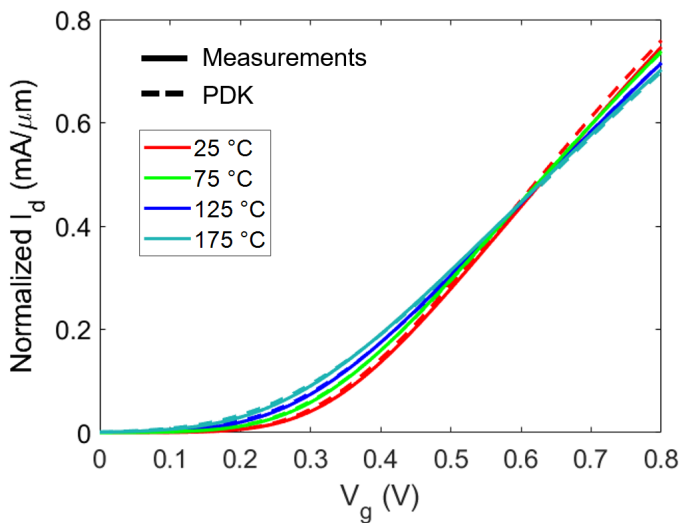


Figure 2.8: Normalized drain current I_d in linear scale versus gate voltage V_g at drain voltage $V_d = 0.8$ V at different temperatures for measurements and PDK.

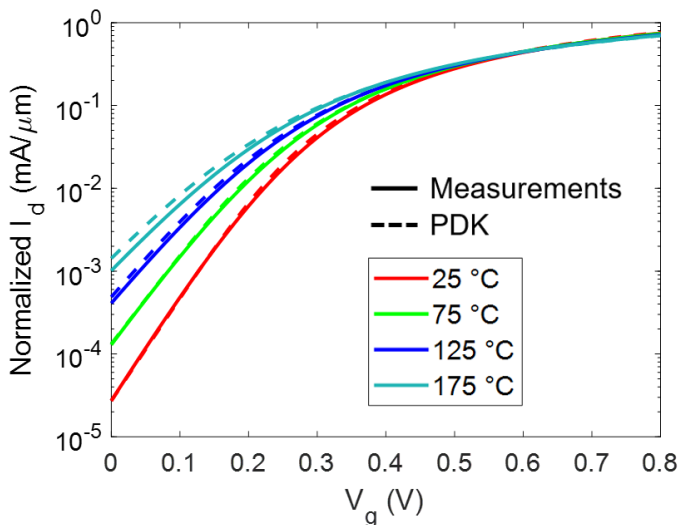


Figure 2.9: Normalized drain current I_d in logarithmic scale versus gate voltage V_g compared in measurements and PDK for $V_d = 0.8$ V. The deviation between measurements and PDK is stronger at higher temperatures.

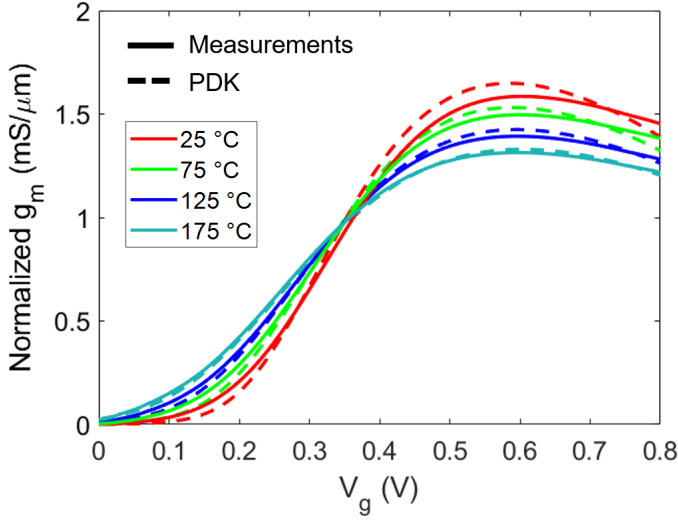


Figure 2.10: Variation of g_m from DC measurements and PDK at $V_d = 0.8$ V with temperature.

for V_g around 0.36 V in measurements and at 0.35 V in PDK, for which g_m is constant with temperature. The reduction in maximum transconductance $g_{m,\max}$ with temperature obtained from DC measurements and PDK simulations is shown in **Figure 2.11** and documented in **Table 2.1**. While the trends are quite similar, the percentage variation is seen to be slightly less in the measurements when compared to the PDK.

Table 2.1: $g_{m,\max}$ and its Percentage Reduction with Temperature in PDK and Measurements at $V_d = 0.8$ V.

Temperature (°C)	PDK $g_{m,\max}$ (mS/μm)	PDK % Redn	Meas $g_{m,\max}$ (mS/μm)	Measurements % Redn
25	1.65	0	1.59	0
75	1.53	7.07	1.50	5.60
125	1.42	13.52	1.39	12.15
175	1.33	19.31	1.31	17.14

Similar to the I_d behavior compared to the I_d -ZTC, g_m increases and decreases, respectively, below and above the g_m -ZTC point. The g_m -ZTC could

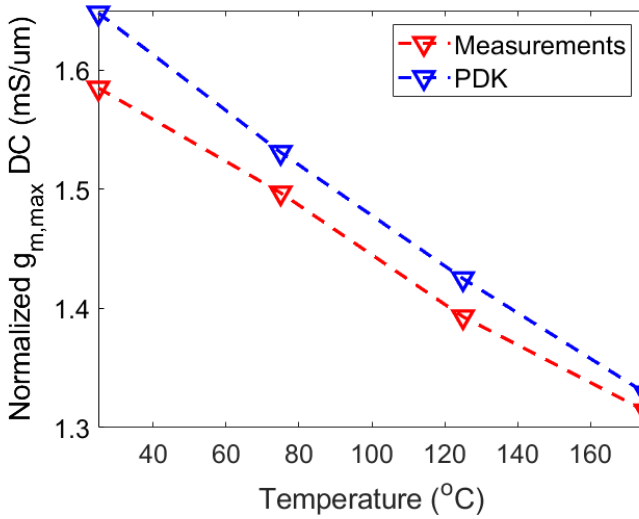


Figure 2.11: Variation of maximum normalized transconductance $g_{m,\max}$ from DC measurements and PDK simulations at $V_d = 0.8$ V with temperature.

be of great importance for applications that require temperature-invariant g_m . As f_T is proportional to g_m , this relates to a ZTC in f_T (where f_T does not change with temperature) at that corresponding ZTC point for g_m provided that the total gate capacitance $C_{gg,T}$ is relatively independent of temperature (this shall be shown later).

Threshold Voltage

The threshold voltage has been computed based on the second-derivative method from [56] in the linear regime. In this method, the V_g at which a maximum in the second derivative of I_d with V_g (that is the first derivative of g_m with respect to V_g) is observed is estimated as the threshold voltage.

Over a range of 25 °C to 175 °C, the measured V_{th} is seen to decrease considerably from 0.28 V to 0.19 V, thereby showing a reduction of 0.6 mV/°C as seen in **Figure 2.12**. These trends are verified from the PDK where the V_{th} values obtained from the second-derivative method obtained at 25, 75, 125, and 175 °C are 0.29, 0.26, 0.23, and 0.2 V respectively, giving a 0.6 mV/°C reduction in V_{th} with temperature. To compare with literature, a 0.6 mV/°C V_{th} shift with temperature was reported on UTBB SOI MOSFETs in [57] while

in [27], the values for $\frac{dV_{th}}{dT}$ ranged between -0.7 and -0.8 mV/°C in thin-film SOI MOSFETs and between -2.4 and -3 mV/°C for bulk and thick film SOI MOSFETs. A significantly lower $\frac{dV_{th}}{dT}$ is thus seen for UTBB FDSOI devices with respect to bulk devices.

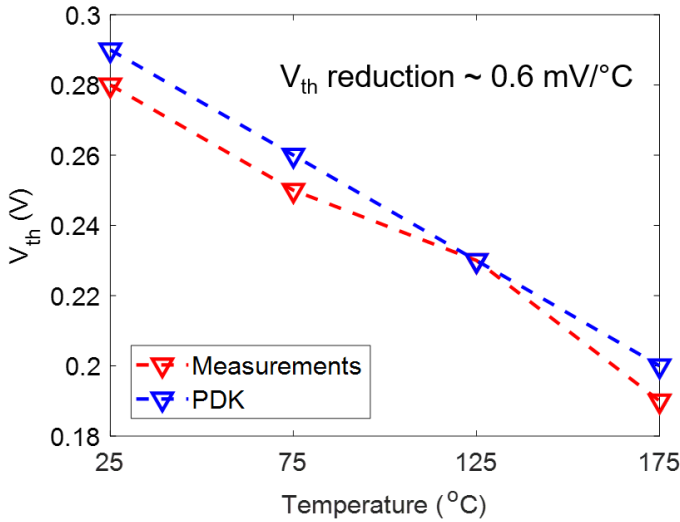


Figure 2.12: Variation of threshold voltage V_{th} with temperature in measurements and PDK.

Small Signal Equivalent Circuit

Figure 2.13 represents the MOSFET small-signal equivalent circuit (SSEC) used in this study. The circuit consists of an intrinsic part and an extrinsic part, where the extrinsic part includes the parasitic series resistances and parasitic shunt capacitances. To extract the various SSEC elements, the measured S-parameters are converted into Y and Z-parameters. The conductances and capacitances are obtained from the real and imaginary parts of the Y-parameters, respectively, whereas the resistances are from the real parts of the Z-parameters. The extraction procedure of SSEC elements is described in [58]. Extrinsic transconductance $g_{m,e}$ and extrinsic output conductance $g_{d,e}$ are obtained from the real part of Y_{dg} and Y_{dd} respectively and include the contributions of the parasitic resistances. The other extrinsic parameters refer to the parasitic elements while intrinsic parameters refer to the case where the parasitics are removed.

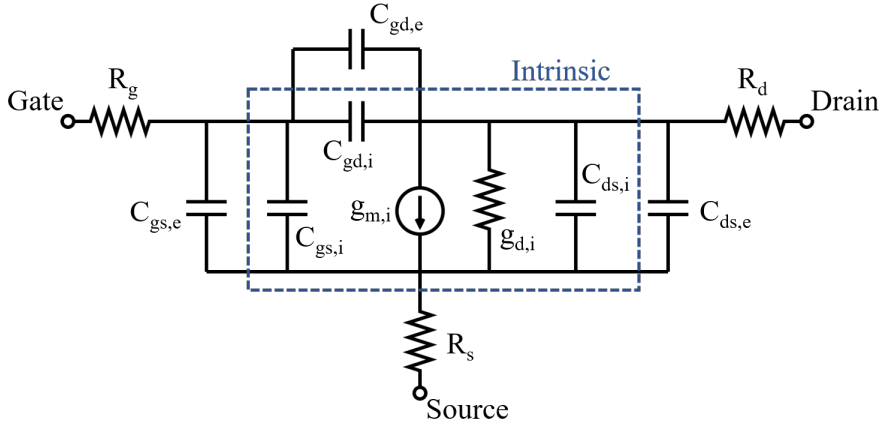


Figure 2.13: Small-signal equivalent circuit for MOSFET.

Thus, extrinsic parameters $C_{gd,e}$, $C_{gs,e}$, and $C_{ds,e}$ refer to the parasitic gate-to-drain capacitance, gate-to-source capacitance, and drain-to-source capacitance, respectively, while $g_{m,i}$, $C_{gd,i}$, $C_{gs,i}$, and $C_{ds,i}$ represent their intrinsic counterparts. The gate, drain, and source resistances are represented as R_g , R_d , and R_s respectively. The total gate capacitance $C_{gg,T}$ is the sum of the total gate-to-drain capacitance $C_{gd,T}$ and total gate-to-source capacitance $C_{gs,T}$, while the source-to-drain resistance R_{sd} is defined as the sum of source resistance R_s and drain resistance R_d .

The process of extraction of the SSEC elements has been described in detail by Babak in [58] and can be referred to for detail. There it was shown that the procedure of equivalent circuit is valid for UTBB MOSFETs up to 110 GHz.

The initial measurements without de-embedding will still have the parasitics from the connection pads. Using open de-embedding, the pad parasitics are removed as shown in **Equation 2.15**.

$$Y_{\text{Open}} = \begin{bmatrix} Y_{gp} & 0 \\ 0 & Y_{gp} \end{bmatrix} \quad (2.15)$$

The de-embedded impedance with open de-embedding is given by **Equation 2.16**:

$$Z'_{\text{DUT}} = [Y_{\text{Measured}} - Y_{\text{Open}}]^{-1} \quad (2.16)$$

In the case of Open-Short de-embedding, a couple of additional steps are needed. First, the capacitance of the short is removed by subtracting Y_{Open} as below in **Equation 2.17**:

$$Y'_{Short} = Y_{Short} - Y_{Open} \quad (2.17)$$

The impedance after Open-Short de-embedding is obtained by subtracting Z'_{Short} as **Equation 2.18**.

$$Z''_{DUT} = Z'_{DUT} - Z'_{Short} \quad (2.18)$$

Extraction of Series Resistances

The de-embedded total impedance Z_{Total} is therefore Z'_{DUT} for the Open de-embedding case and Z''_{DUT} for the Open-Short de-embedding case.

The total impedance is a sum of the parasitic series impedance Z_{Series} and the device impedance Z_{Device} from **Equation 2.19**.

$$Z_{Total} = Z_{Series} + Z_{Device} \quad (2.19)$$

From this Z_{Total} , the impact of the series resistances is removed first to extract the device impedance Z_{Device} in **Equation 2.20**.

$$Z_{Device} = Z_{Total} - Z_{Series} \quad (2.20)$$

The general procedure with which this computation has been made is discussed below with sample extraction plots depicting the process. Amongst different methods in literature [59] [60] to extract SSEC, Bracale's method [61] is demonstrated to be the most robust and precise. This approach relies on the correlation between the MOSFET's channel conductance g_d and the overdrive voltage ($V_g - V_{th}$) in cold FET condition ($V_d = 0$ V) and in high inversion ($V_g > V_{th}$). For this biasing condition, the small-signal equivalent circuit of the MOSFET simplifies to the configuration in **Figure 2.14** [58].

With port 1 being connected to the gate and port 2 to the drain, the equations for the extrinsic series resistances formulated by Bracale [61] are given in **Equations 2.21, 2.22, and 2.23**:

$$\text{Re}(Z_{22} - Z_{12}) = R_d + \frac{1}{2g_d} \quad (2.21)$$

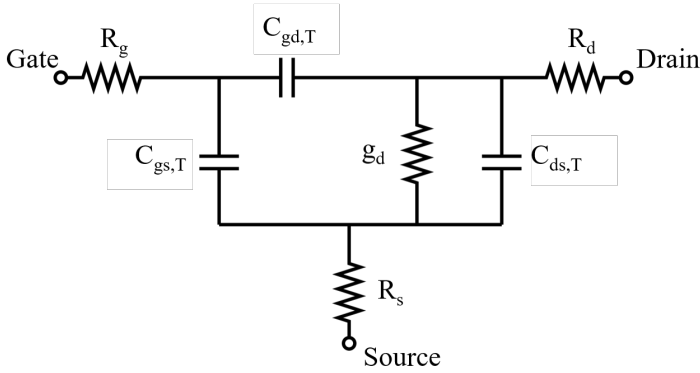


Figure 2.14: SSEC for modelling MOSFET in cold bias ($V_d = 0$ V) and high inversion ($V_g > V_{th}$).

$$\text{Re}(Z_{12}) = R_s + \frac{1}{2g_d} \quad (2.22)$$

$$\text{Re}(Z_{11} - Z_{12}) = R_g - \frac{1}{4g_d} \quad (2.23)$$

From the corresponding Z-parameter plots, a suitable averaging frequency range is selected over a region where the curves are mostly flat. In that range, based on the different considered V_g bias points in strong inversion in cold FET condition ($V_d = 0$ V), a simple linear regression of the averaged values with respect to the reciprocal of the overdrive voltage helps in extracting the series resistances [61]. A sample extraction process with corresponding plots is shown below.

1. Series Gate Resistance

For R_g extraction, the $\text{Re}(Z_{11} - Z_{12})$ is first taken at 4 different strong inversion biases of 0.6, 0.7, 0.8, and 0.9 V. Averaging is made over the frequency range from 15 to 20 GHz in this case, as seen below from the dashed lines in the **Figure 2.15**. The extraction of R_g is relatively trickier compared to the other resistances and it is therefore important to have a good contact during measurements backed by careful extraction based on the frequency range of averaging.

A linear regression of the $\text{Re}(Z_{11} - Z_{12})$ values is made with respect to the overdrive voltage ($V_g - V_{th}$) for the four V_g biases considered. R_g is extracted as the Y-intercept of the linear regression plot in **Figure 2.16**.

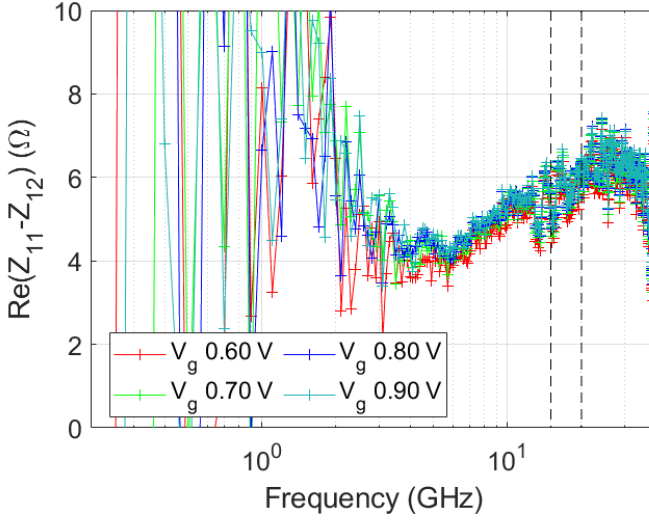


Figure 2.15: Frequency variation of $\text{Re}(Z_{11} - Z_{12})$ for R_g extraction.

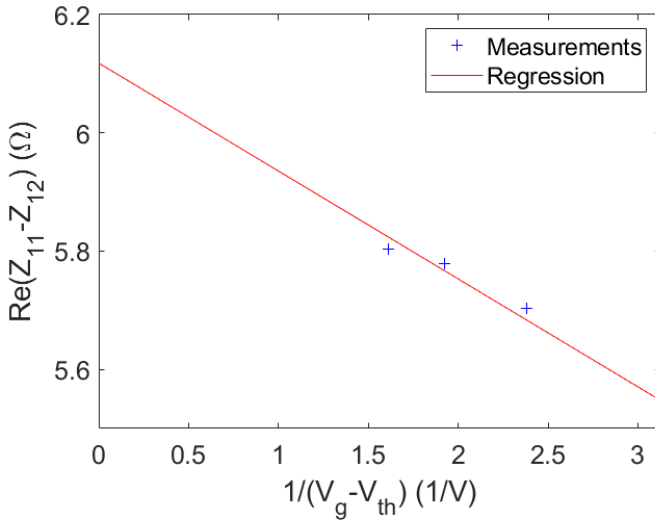


Figure 2.16: Linear regression of $\text{Re}(Z_{11} - Z_{12})$ with reciprocal of overdrive voltage for R_g extraction.

2. Series Source Resistance

The procedure for R_s extraction from $\text{Re}(Z_{12})$ is similar to that of R_g , except for the fact that the averaging frequency range in this case is from 3 - 6 GHz (**Figure 2.17** and **Figure 2.18**). It is to be noted that selecting the averaging frequency is crucial for each extraction; it needs to be selected properly based on the inspection of the plot. A similar linear regression helps in obtaining R_s from its Y-intercept.

3. Series Drain Resistance

R_d is extracted from $\text{Re}(Z_{22} - Z_{12})$ over an averaging frequency range, in this case, from 3 to 6 GHz as well. **Figure 2.19** and **Figure 2.20** show the corresponding extractions.

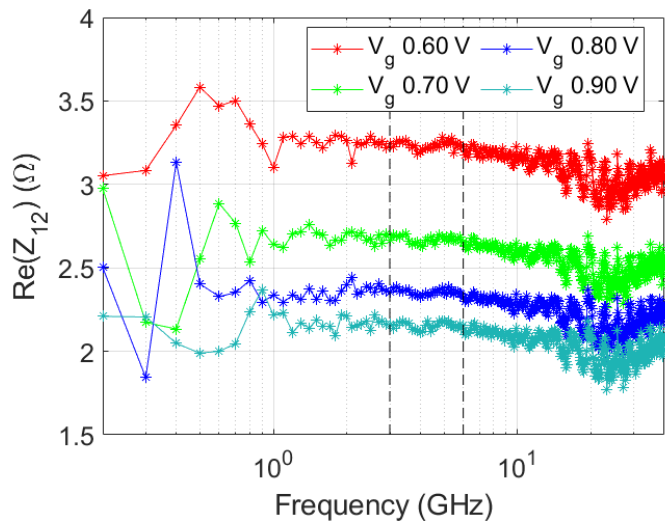


Figure 2.17: Frequency variation of $\text{Re}(Z_{12})$ for R_s extraction.

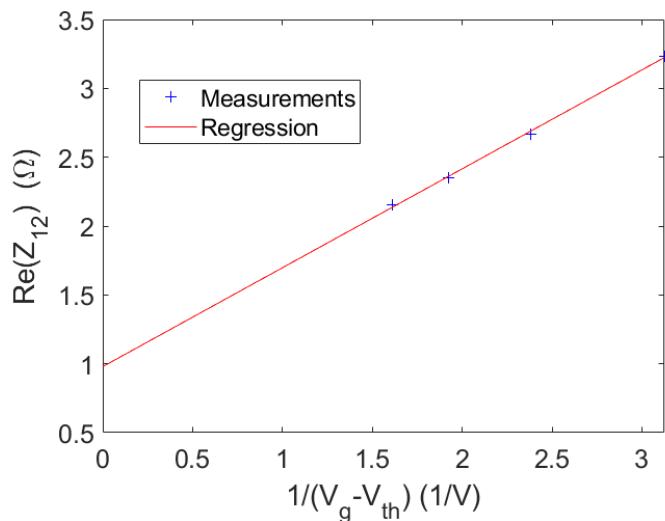


Figure 2.18: Linear regression of $\text{Re}(Z_{12})$ with reciprocal of overdrive voltage for R_s extraction.

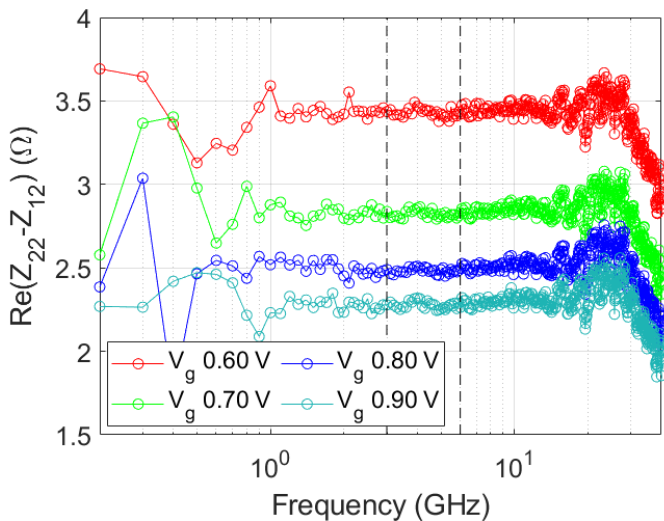


Figure 2.19: Frequency variation of $\text{Re}(Z_{22} - Z_{12})$ for R_d extraction.

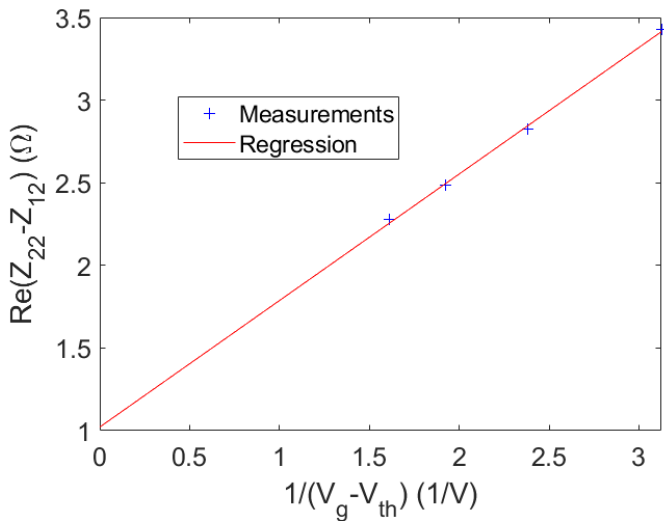


Figure 2.20: Linear regression of $\text{Re}(Z_{22} - Z_{12})$ with reciprocal of overdrive voltage for R_d extraction.

Extraction of Extrinsic Capacitances

The device admittance Y_{Device} , reciprocal of Z_{Device} , then allows for the extraction of the intrinsic and extrinsic elements from Equation 2.24.

$$Y_{\text{Device}} = Z_{\text{Device}}^{-1} = Y_{\text{intrinsic}} + Y_{\text{extrinsic}} \quad (2.24)$$

Following the extraction of the series resistances, the parallel extrinsic capacitances can be then extracted in deep depletion ($V_g < 0\text{ V}$) in cold bias condition ($V_d = 0\text{ V}$) in which the SSEC is reduced to the one shown in Figure 2.21.

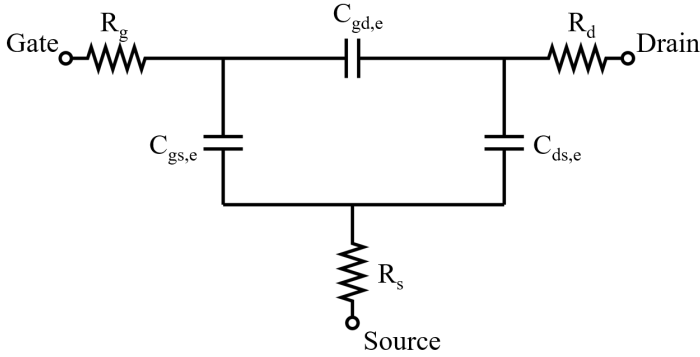


Figure 2.21: SSEC for modelling MOSFET in cold bias ($V_d = 0\text{ V}$) and deep depletion ($V_g < 0\text{ V}$) [58].

As there is no intrinsic part in this condition, g_d and g_m are neglected. $Y_{\text{extrinsic}}$ can be related to the extrinsic capacitances by Equation 2.25.

$$Y_{\text{extrinsic}} = \begin{bmatrix} j\omega(C_{gs,e} + C_{gd,e}) & -j\omega C_{gd,e} \\ -j\omega C_{gd,e} & j\omega(C_{ds,e} + C_{gd,e}) \end{bmatrix} \quad (2.25)$$

$C_{gs,e}$, $C_{ds,e}$ and $C_{gd,e}$ can be obtained using Equations 2.26, 2.27 and 2.28.

$$C_{gs,e} = \frac{\text{Im}(Y_{11} + Y_{12})}{\omega} \quad (2.26)$$

$$C_{ds,e} = \frac{\text{Im}(Y_{22} + Y_{12})}{\omega} \quad (2.27)$$

$$C_{gd,e} = -\frac{\text{Im}(Y_{12})}{\omega} \quad (2.28)$$

An example of extraction of extrinsic capacitances is shown in **Figure 2.22**, the averaging of Y/ω is made over a selected frequency range of 1.5 - 3 GHz.

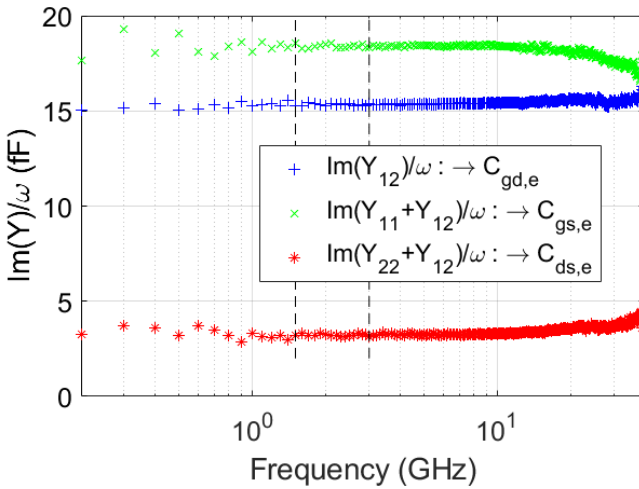


Figure 2.22: Extraction of extrinsic capacitances $C_{gd,e}$, $C_{gs,e}$ and $C_{ds,e}$ from the imaginary part of Y parameters.

Extraction of Intrinsic Elements

The intrinsic parameters, namely the transconductance g_{mi} , output conductance g_{di} and the total capacitances $C_{gs,T}$, $C_{gd,T}$ and $C_{ds,T}$ are then extracted in saturation and strong inversion ($V_d = 0.8$ V, $V_g > V_{th}$). The equivalent circuit after removal of the series resistances is shown in **Figure 2.23**.

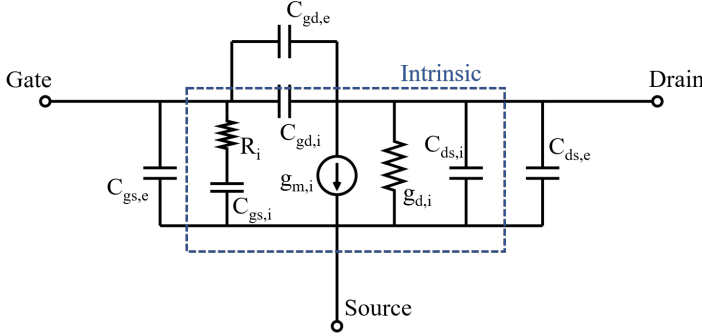


Figure 2.23: SSEC for modelling MOSFET in saturation ($V_d = 0.8$ V) and strong inversion ($V_g > V_{th}$) [58].

From the equivalent circuit above, Y_{device} can be obtained from the **Equation 2.29** below:

$$Y_{device} = \begin{bmatrix} j\omega(C_{gs,T} + C_{gd,T}) & -j\omega C_{gd,T} \\ g_{m,i} - j\omega C_{gd,T} & g_{d,i} + j\omega(C_{ds,T} + C_{gd,T}) \end{bmatrix} \quad (2.29)$$

The intrinsic transconductance and output conductance are obtained from **Equations 2.30** and **2.31**:

$$g_{m,i} = |\text{Im}(Y_{21} - Y_{12})| \quad (2.30)$$

$$g_{d,i} = \text{Re}(Y_{22}) \quad (2.31)$$

The total capacitances are obtained from the following **Equations 2.32 - 2.34**:

$$C_{gs,T} = \frac{\text{Im}(Y_{11} + Y_{12})}{\omega} \quad (2.32)$$

$$C_{ds,T} = \frac{\text{Im}(Y_{22} + Y_{12})}{\omega} \quad (2.33)$$

$$C_{gd,T} = -\frac{\text{Im}(Y_{12})}{\omega} \quad (2.34)$$

Finally, the intrinsic capacitances can be extracted as the difference between the total and the extrinsic capacitances as shown in **Equations 2.35 - 2.37**.

$$C_{gs,i} = C_{gs,T} - C_{gs,e} \quad (2.35)$$

$$C_{gd,i} = C_{gd,T} - C_{gd,e} \quad (2.36)$$

$$C_{ds,i} = C_{ds,T} - C_{ds,e} \quad (2.37)$$

With the SSEC parameter extraction process described, the obtained results are illustrated. Both the maximum intrinsic and extrinsic transconductances $g_{m,i}$ and $g_{m,e}$ show a degradation of around 18% going from 25 to 175°C, respectively, as demonstrated in **Figure 2.24**. The trends are verified for two different V_d cases, 0.8 V and 0.6 V with V_g corresponding to $g_{m,max}$. A similar range of degradation in $g_{m,i}$ was observed in case of bulk and PDSOI technologies studied in [40] was found to be 16.5% and 20.2% respectively. An increase of around 10% is observed in intrinsic and extrinsic g_d . The absolute value of $g_{m,e}$ extracted from RF measurements is noted to be higher than that from DC measurements because of the removal of dynamic self-heating in the former case.

Figure 2.25 demonstrates the variation of total intrinsic gate capacitance $C_{gg,Ti}$ ($C_{gs,i} + C_{gd,i}$) versus temperature, extracted for $V_d = 0.8$ V and 0.6 V each.

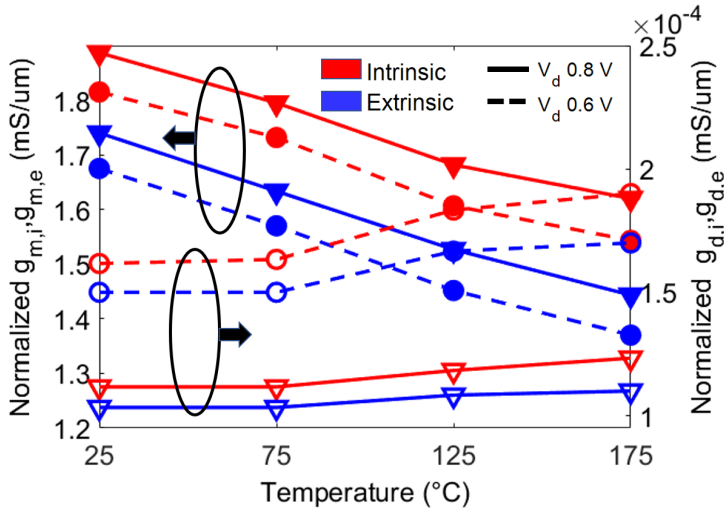


Figure 2.24: Variation of maximum normalized intrinsic and extrinsic transconductance $g_{m,i}$ and $g_{m,e}$ and output intrinsic and extrinsic conductance $g_{d,i}$ and $g_{d,e}$ with temperature at $V_d = 0.8$ V (solid lines) and 0.6 V (dashed lines) and V_g corresponding to $g_{m,max}$.

$C_{gg,Ti}$ extracted is mainly steady over the temperature range of 25 to 175°C , varying by only a few fF which is within the range of the extraction precision. Capacitances $C_{gs,i}$, $C_{gd,i}$, $C_{ds,i}$ are also individually found to be steady with temperature.

The degradation of gain A_V , calculated as the ratio of $g_{m,i}/g_{d,i}$, with increasing temperature at the bias condition $V_d = 0.8$ V and $V_g = 0.6$ V is shown in **Figure 2.26**. A 23% reduction in A_V is followed up from decreasing intrinsic $g_{m,i}$ and slightly increasing $g_{d,i}$ on increasing the temperature from 25 to 175°C .

Figure 2.27 shows the variation of resistances with temperature. It is observed that both the gate resistance R_g and the source-to-drain resistance R_{sd} ($R_s + R_d$) increase with temperature. In [46], R_g was observed to rise around 22% on increasing the temperature from 25 to 125°C , in line with the 15% rise in R_g observed in the trends in this work. In the PDK, the increase in R_g is modelled to be higher than the values reported in our work and in [46] too, with a 34% rise over the 25 to 125°C mentioned above. The rise in R_g from 25 to 175°C in the PDK is found to be as high as 50%. This is one specific aspect that

needs to be studied better, given that it also dictates strongly the f_{max} extraction.

Using the SSEC, the S-Parameters are reconstructed; a comparison between the measured S-parameters and the ones reconstructed using the SSEC in **Figure 2.28** shows a good fit for the room temperature measurements.

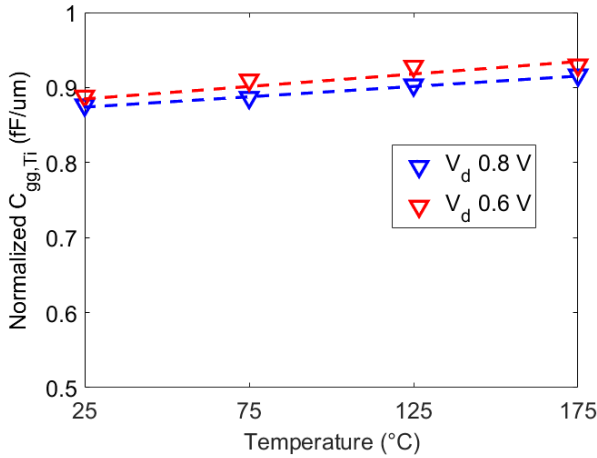


Figure 2.25: Variation of normalized total intrinsic gate capacitance $C_{gg,Ti}$ ($C_{gs,i} + C_{gd,i}$) with temperature at $V_d = 0.8$ V and 0.6 V with V_g corresponding to $g_{m,max}$.

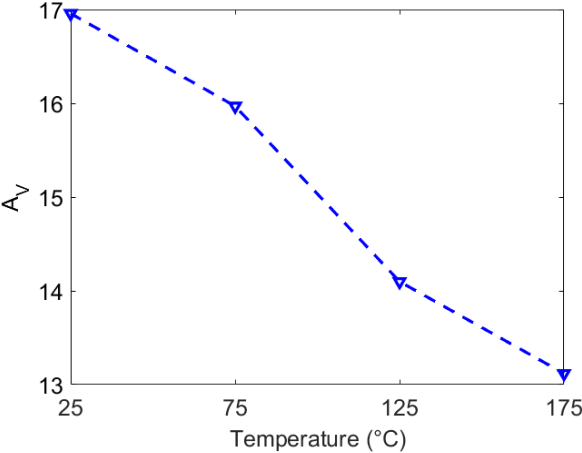


Figure 2.26: Variation of intrinsic voltage gain A_V with temperature for $V_d = 0.8$ V and V_g corresponding to $g_{m,max}$.

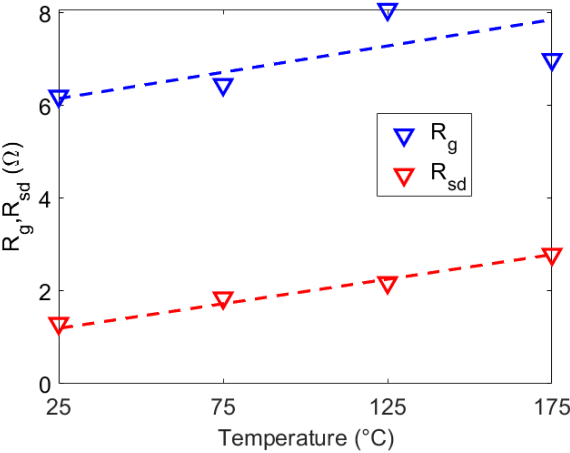


Figure 2.27: Variation of gate resistance R_g and source-drain resistance R_{sd} ($R_s + R_d$) with temperature.

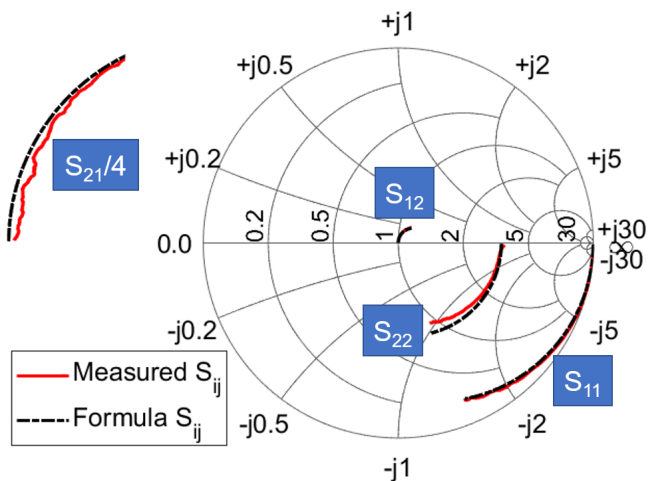


Figure 2.28: Comparison of S-parameters measured and reconstructed from SSEC at room temperature for $V_d = 0.8$ V and $V_g = 0.6$ V.

Extraction of RF Figures-of-Merit

Two salient RF Figures of Merit (FoMs) are the current-gain cut-off frequency f_T and maximum oscillation frequency $f_{\max}$. f_T is recognized as the unity current gain frequency, where the short circuit current gain (H_{21}) reaches unity (0 dB), and the maximum oscillation frequency, $f_{\max}$, denotes the frequency at which the unilateral power gain (U) equals unity (0 dB). f_T and $f_{\max}$ can also be related to SSEC parameters. Commonly used expressions for computing f_T and $f_{\max}$ in this way are shown in **Equations 2.38** and **2.39**.

$$f_T \approx \frac{g_{m,e}}{2\pi C_{gg,T}} \quad (2.38)$$

$$f_{\max} \approx \frac{f_T}{2\sqrt{(2\pi f_T R_g C_{gd,T}) + (R_s + R_g)g_{d,e}}} \quad (2.39)$$

An example of f_T and $f_{\max}$ computation from H_{21} and U plots can be seen in **Figure 2.29**. Computation of f_T and $f_{\max}$ are done by averaging over a desired frequency range; reaching at least 15 GHz is necessary to have reliable f_T and $f_{\max}$ results.

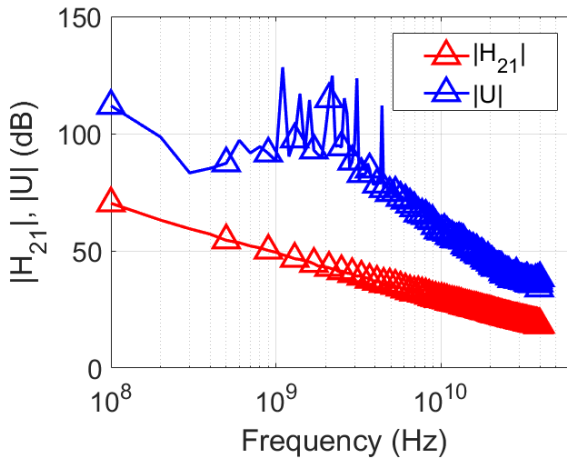


Figure 2.29: Short-circuit current gain H_{21} and unilateral power gain U plots versus frequency for $V_d = 0.8$ V and $V_g = 0.6$ V.

The effect of an increase in temperature on f_T and $f_{\max}$ is now investigated. f_T and $f_{\max}$ are computed by two methods: first from the extrapolation of the current gain H_{21} and unilateral gain to 0 dB, respectively (which are in turn found from the S-parameter measurements). The values obtained from this method are referred to as those measured. Second, f_T and $f_{\max}$ are also computed from formulae **Equations 2.38** and **2.39**, respectively, involving the extracted SSEC parameters. The values obtained thus are referred to as the formula. While a good correlation is demonstrated between the f_T and $f_{\max}$ values obtained from the measurements and the formula using SSEC parameters, it is to be noted that the frequency range of averaging impacts the extracted values. All the f_T and $f_{\max}$ values have been normalized with respect to the peak f_T and $f_{\max}$ value (for V_g corresponding to maximum g_m) at room temperature of 25°C. Computation of f_T and $f_{\max}$ has been carried out under three different bias conditions as well in order to better demonstrate the significance of the g_m -ZTC point. Each of these cases has V_d of 0.8 V or V_d of 0.6 V (for low power applications) whereas the V_g is varied (i) corresponding to $g_{m,\max}$ in which case the peak f_T and $f_{\max}$ are observed, (ii) corresponding to g_m -ZTC, and (iii) below g_m -ZTC, at a value of V_g of 0.3 V.

Extractions at $V_d = 0.8$ V

Firstly, considering the V_g corresponding to $g_{m,\max}$ bias condition and $V_d = 0.8$ V, it is observed from **Figure 2.30** that f_T degrades in a similar manner to g_m as expected. Qualitatively, referring back to **Equation 2.38**, f_T is proportional to $g_{m,e}$ and this is the basis of this deduction. Following up from this, $f_{\max}$ is seen to be degrading with temperature as well in **Figure 2.31**. Going from room temperature of 25 °C to 175 °C, a reduction of around 20% can be observed for both peak f_T and $f_{\max}$, respectively, for V_g corresponding to $g_{m,\max}$.

Secondly, the bias condition considered was V_g corresponding to g_m -ZTC (0.36 V in this case) and $V_d = 0.8$ V. At this g_m -ZTC bias point, g_m is independent of temperature and therefore we expect a much steadier f_T and $f_{\max}$ value with temperature since g_m is one of the main factors affecting both. This is verified from the **Figures 2.30** and **2.31** below where f_T is extremely stable with temperature (varying by 3% only over the temperature range) and $f_{\max}$ also shows a relatively reduced variation of 10%. The fact that the variation of the resistances also come into play for the $f_{\max}$ reduction makes its behaviour somewhat more variable than that of f_T . Given the fact that the absolute value of g_m at this bias point is lesser than that at the $g_{m,\max}$ point, the absolute values

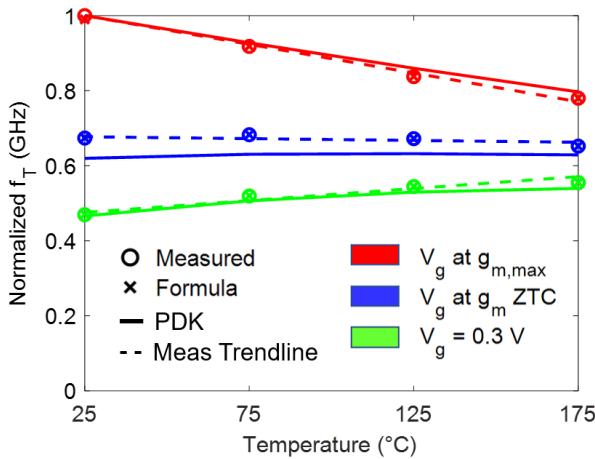


Figure 2.30: Variation of normalized current-gain cut-off frequency f_T with temperature at $V_d = 0.8\text{ V}$ and V_g corresponding to $g_{m,\max}$, g_m -ZTC and 0.3 V (below g_m -ZTC). Normalization with respect to f_T at V_g corresponding to $g_{m,\max}$ at 25°C , $V_d = 0.8\text{ V}$.

of f_T and $f_{\max}$ are lower compared with the $g_{m,\max}$ case that is evident from the magnitude of the normalized values at this bias condition.

Thirdly, for a bias condition situation where V_g is 0.3 V and $V_d = 0.8\text{ V}$, that is V_g is below the g_m -ZTC of 0.36 V , an improvement in f_T of around 20% is observed with temperature in Figure 2.30. This is due to an expected improvement in g_m with temperature under this bias condition. The $f_{\max}$ degradation at this bias is also much lesser than in the two aforementioned cases. $f_{\max}$ is found to be relatively steady with temperature. This can be explained by the improvement of f_T with temperature that is directly proportional to $f_{\max}$ in Equation 2.39. Note that the magnitudes of f_T and $f_{\max}$ are reduced further in this case because of further reduction in the magnitude of g_m itself at lower V_g bias. At $V_d = 0.8\text{ V}$, the absolute values of peak f_T and $f_{\max}$ were 325 GHz , and 352 GHz respectively.

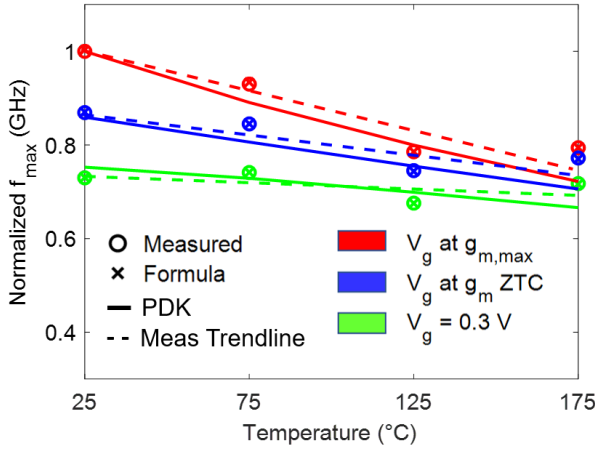


Figure 2.31: Variation of normalized maximum oscillation frequency $f_{\max}$ with temperature at $V_d = 0.8 \text{ V}$ and V_g corresponding to $g_{m,\max}$, $g_{m,\text{ZTC}}$ and 0.3 V (below $g_{m,\text{ZTC}}$). Normalization with respect to $f_{\max}$ at V_g corresponding to $g_{m,\max}$ at 25°C , $V_d = 0.8 \text{ V}$.

Extractions at $V_d = 0.6 \text{ V}$

From a DC power point of view, $P_{\text{dc}} = I_d V_d$, lowering V_d results in lower I_d as well, thereby further lowering the $I_d V_d$ product P_{dc} . When V_g is kept constant at 0.8 V at 25°C , P_{dc} is reduced around 29% from 35 mW to 25 mW by stepping down V_d from 0.8 V to 0.6 V in line with low power application trends. Alternatively, at $V_d = 0.8 \text{ V}$, stepping down V_g to 0.6 V and 0.36 V corresponding to $g_{m,\max}$ and $g_{m,\text{ZTC}}$ respectively reduces P_{dc} by 41% and 87%, seen in **Figure 2.32**.

The variation in f_T and $f_{\max}$ is studied next with V_d being stepped down to 0.6 V (from the earlier case of 0.8 V) for the three different V_g bias conditions again: V_g for $g_{m,\max}$, V_g at $g_{m,\text{ZTC}}$, and $V_g = 0.3 \text{ V}$ (below $g_{m,\text{ZTC}}$). The trends observed in **Figure 2.33** and **Figure 2.34** are similar and the f_T and $f_{\max}$ ZTC are observed around $g_{m,\text{ZTC}}$ and $V_g = 0.3 \text{ V}$, respectively. At $V_d = 0.6 \text{ V}$, the absolute values of peak f_T and $f_{\max}$ were 302 GHz and 322 GHz respectively.

From a magnitude point of view, moving to $V_d = 0.6 \text{ V}$ reduces peak f_T and $f_{\max}$ by 7% and 10.8%, respectively. Thanks to the high f_T and $f_{\max}$ offered by this technology, moving from $V_d = 0.8 \text{ V}$ to 0.6 V provides around 29%

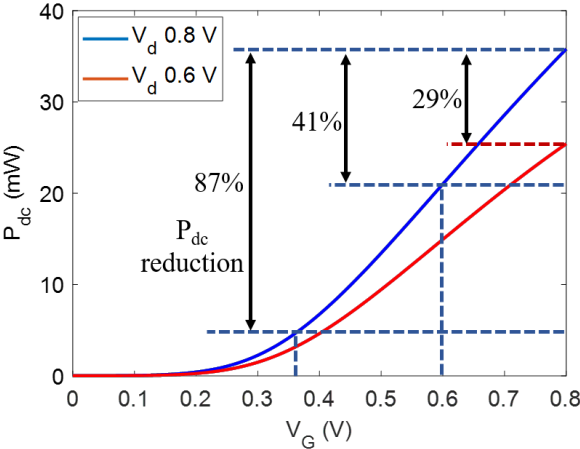


Figure 2.32: P_{dc} variation with V_d showing percentage P_{dc} reduction at various biases.

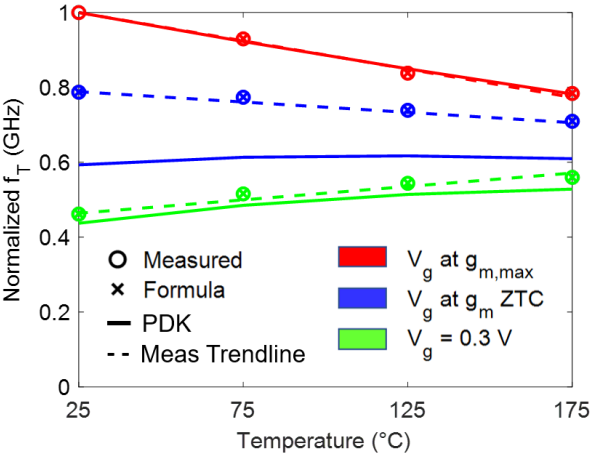


Figure 2.33: Variation of normalized current-gain cut-off frequency f_T with temperature at $V_d = 0.6$ V and V_g corresponding to $g_{m,max}$, g_m -ZTC, and 0.3 V (below g_m -ZTC). Normalization with respect to f_T at V_g corresponding to $g_{m,max}$ at 25 $^{\circ}$ C, $V_d = 0.6$ V.

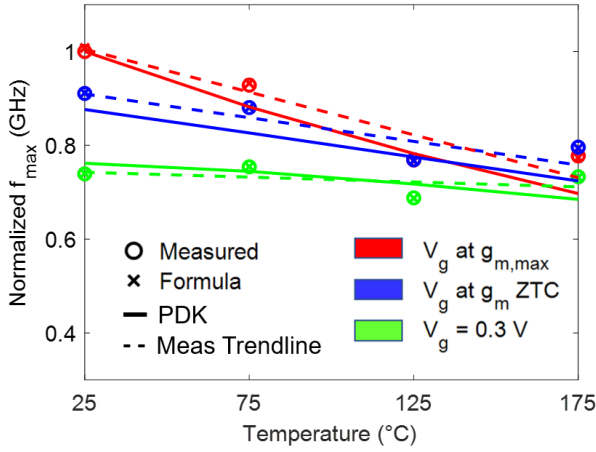


Figure 2.34: Variation of normalized maximum oscillation frequency $f_{\max}$ with temperature at $V_d = 0.6$ V and V_g corresponding to $g_{m,\max}$, g_m , ZTC, and 0.3 V (below g_m -ZTC). Normalization with respect to $f_{\max}$ at V_g corresponding to $g_{m,\max}$ at 25°C, $V_d = 0.6$ V.

reduction in P_{dc} while affecting f_T , $f_{\max}$ to a very limited extent. The resulting f_T , $f_{\max}$ values are high enough for standard RF applications.

The variation in f_T and $f_{\max}$ from 25 to 175 °C is compared between PDK simulations and measurements in the tables below. **Table 2.2** displays the percentage variations of f_T , while **Table 2.3** presents the percentage variations of $f_{\max}$.

The analysis of both the PDK and measured data shows that while the overall trends in f_T and $f_{\max}$ variations are consistent across PDK simulations and measurements, the exact magnitudes mainly of $f_{\max}$ differ. A closer agreement is seen with the trends in f_T , specifically the reduction in that of peak f_T corresponding to V_g at $g_{m,\max}$. Especially, at $V_g = 0.3$ V, the PDK still shows a perceivable reduction in $f_{\max}$ whereas in measurements $f_{\max}$ is found to vary little with temperature at that bias.

Table 2.2: Percentage Variations of f_T over 25 to 175 °C at Different V_d and V_g Biases.

V_d (V)	V_g Bias Condition	Measurements	PDK
0.8	At $g_{m,max}$	-22%	-20%
0.8	At g_m ZTC	-3%	+2%
0.8	$V_g = 0.3$ V, Below g_m ZTC	+18%	+16%
0.6	At $g_{m,max}$	-22%	-22%
0.6	At g_m ZTC	-10%	+3%
0.6	$V_g = 0.3$ V, Below g_m ZTC	+21%	+21%

Table 2.3: Percentage Variations of f_{max} over 25 to 175 °C at Different V_d and V_g Biases.

V_d (V)	V_g Bias Condition	Measurements	PDK
0.8	At $g_{m,max}$	-21%	-28%
0.8	At g_m ZTC	-11%	-18%
0.8	$V_g = 0.3$ V, Below g_m ZTC	-2%	-11%
0.6	At $g_{m,max}$	-22%	-30%
0.6	At g_m ZTC	-13%	-17%
0.6	$V_g = 0.3$ V, Below g_m ZTC	-1%	-10%

2.3.4 Performance Tuning with Back-Gate

Using the back-gate bias to improve the performance or leakage applications by shifting the threshold voltage has been a prominent technology offering in 22FDX[®] [19]. By biasing on the back-gate, the impact of temperature variation on the device threshold voltage can be countered, making this an efficient tuning switch.

While an increase in temperature from 25 to 125 °C decreases the threshold voltage from 0.29 V to 0.23 V at 0.6 mV/°C, a similar trend can be seen by increasing the V_{bg} . From PDK simulations, it is seen that the variation in V_{th} with V_{bg} is around 80 mV/V, in line with the 85 mV/V value reported in [22] on 28 nm FDSOI technology. This means that at high temperatures, by using a suitable voltage on the back-gate, the V_{th} can be increased to offset the V_{th} shift due to temperature and thus keep the voltage overdrive ($V_g - V_{th}$) for a certain V_g bias of operation. As an example, let us consider the cases at 25 °C

and 125 °C from the PDK model. This 100 °C rise in temperature reduces the V_{th} from 0.29 to 0.23 V, a reduction of 60 mV. Knowing the 80 mV/V variation rate of V_{th} with V_{bg} , applying -0.75 V on the back-gate should compensate for the temperature effect on V_{th} . From the PDK simulations at V_{bg} -0.8 V, the V_{th} offset is seen in **Figure 2.35**.

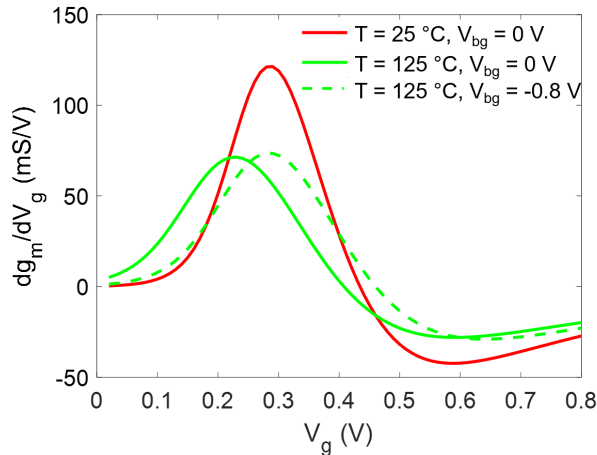


Figure 2.35: Using back-gate voltage V_{bg} to offset the change in threshold voltage V_{th} .

Further studies to ascertain the impact of V_{bg} on other FoMs are investigated in the PDK. The expectation from DC results is that the V_{bg} can help in tuning the device performance. However, it is seen that the impact of varying V_{bg} on the FoMs is much more limited compared to that of temperature. Without V_{bg} , the variation of peak f_T and f_{max} taken at $V_d = 0.8\text{ V}$ and $V_g = 0.59\text{ V}$ is shown in Table as follows:

Table 2.4: Variation of Peak f_T and f_{max} without V_{bg} variation

Without V_{bg}	25 °C	75 °C	125 °C	175 °C
f_T (GHz)	323	299	278	257
f_{max} (GHz)	342	305	274	247

Following this, by adjusting V_{bg} in a way that V_{ov} remains the same for the different temperatures, the f_T and f_{max} obtained by using V_{bg} is given below.

Table 2.5: Variation of Peak f_T and $f_{\max}$ with V_{bg} variation to keep same overdrive voltage

With V_{bg}	25 °C $V_{bg} = 0\text{ V}$	75 °C $V_{bg} = -0.4\text{ V}$	125 °C $V_{bg} = -0.8\text{ V}$	175 °C $V_{bg} = -1.2\text{ V}$
f_T (GHz)	323	300	277	256
$f_{\max}$ (GHz)	342	312	287	259

It is noted that while there is a slight improvement in $f_{\max}$ (10-15 GHz) on using the V_{bg} bias in comparison to the case where V_{bg} is not used, the variation in f_T is very small.

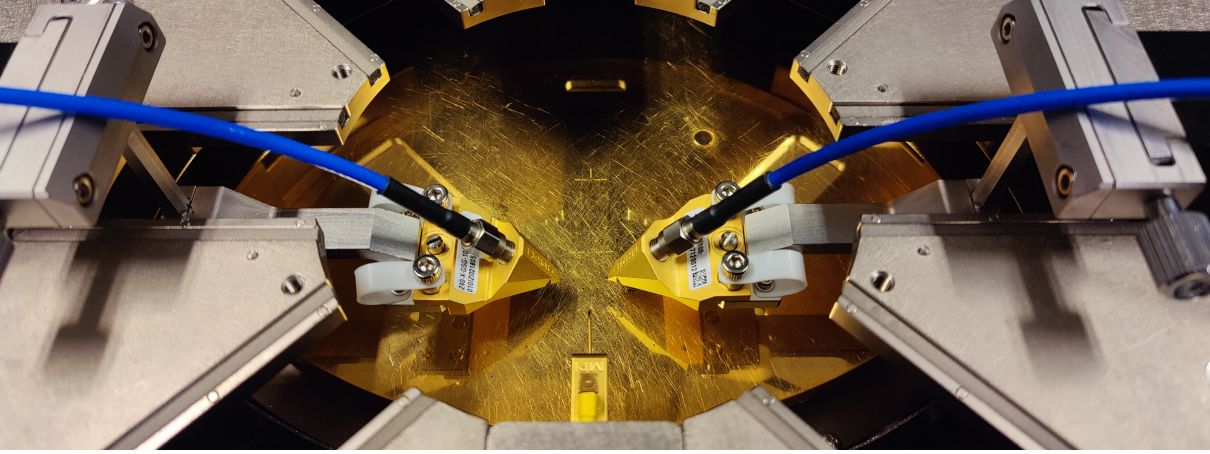
2.4 Conclusions

The impact of increased ambient temperature on the performance of 22 nm FD-SOI MOSFETs is investigated in this chapter. This becomes crucial for understanding and predicting the behaviours of electronic devices and circuits working in high-temperature environments, many of which see a stark increase in applications.

From the I_d - V_g characteristics, ZTC points for I_d and g_m were found to be at gate voltages V_g of 0.62 V and 0.36 V, respectively. For the RF FoMs, around 20% reduction in both peak f_T and peak $f_{\max}$ was observed when the temperature is increased from 25 to 175°C. Thanks to the extraction of the SSEC, the degradation in g_m with temperature was found to be one of the major factors for the reduction in the aforementioned FoMs with the capacitances being mostly steady with temperature while the resistances are seen to increase. At the g_m -ZTC point, f_T and $f_{\max}$ are found to be more stable with temperature, with f_T varying within 3% and $f_{\max}$ varying around 11%. Below the g_m -ZTC point for V_g of 0.3 V, an improvement in f_T with temperature of around 20% is seen whereas $f_{\max}$ is found to be rather steady with temperature. From a low-power application point of view, stepping down V_d from 0.8 V to 0.6 V helps in reducing P_{dc} while affecting f_T and $f_{\max}$ limitedly, motivating the possibility to go to this bias condition when necessary.

Comparisons with the PDK are also made for high-temperature studies and similar trends on threshold voltage variation, $g_{m,\max}$ reduction and also f_T variation are obtained. However, measurements consistently report lower I_{off} than PDK predictions and $f_{\max}$ variation seems to be somewhat greater in the PDK.

Utilizing the back-gate in FDSOI technology to tune RF performance over temperature is a prospect for future research. The threshold voltage impact coming from temperature can be improved by using a suitable back-gate bias. However, it is seen that the temperature impact on g_m degradation reduces peak f_T and $f_{\max}$ strongly rendering back-gate bias ineffective in improving the RF FoMs.



3. Self-Heating Characterization Techniques

This chapter studies the different aspects of self-heating characterization, especially the most relevant ones for state-of-the-art MOSFETs. From literature, two of the most widely used techniques for advanced MOSFETs, namely the gate-resistance technique and the RF technique are investigated in detail. Through experimental analysis of the techniques on the same devices, the advantages and limitations of each of the techniques are highlighted. Furthermore, the impact of device layout on SH characterization is looked into; it is seen that for the same core MOSFET, layout-related factors (like specific test structures for characterization) could affect SH extraction. In the process, an attempt is made to understand the SH problem better and the heat evacuation paths in devices. The chapter flow can be seen in **Figure 3.1**.

3.1 Introduction to Thermal Characteristics: Thermal Resistance, Thermal Capacitance and Thermal Time Constant

Thermal resistance and thermal capacitance are two main figures of merit that help in quantifying the thermal characteristics of devices.

Thermal resistance R_{th} is a measure of the resistance that a material offers to the flow of heat. It is defined as the ratio between the temperature difference between the two faces of the material and the rate of heat flow. The higher the thermal resistance, the more difficult it is for the heat to flow through the

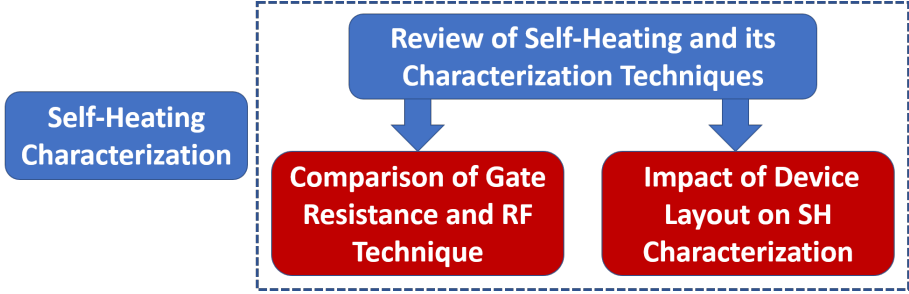


Figure 3.1: Overview of Chapter 3.

material.

Thermal capacitance C_{th} , on the other hand, represents the heat stored in a material. While thermal resistance R_{th} is related to heat transfer through the material, thermal capacitance pertains to heat storage in the material [62]. The thermal resistance is mainly related to the surface area for heat evacuation while the thermal capacitance is related to the device volume.

The thermal time constant of the device is the product of the thermal resistance and thermal capacitance (**Equation 3.1**).

$$\tau_{th} = R_{th}C_{th} \quad (3.1)$$

The characteristic thermal frequency is related to the thermal time constant as per **Equation 3.2**:

$$f_{th} = \frac{1}{2\pi\tau_{th}} \quad (3.2)$$

The thermal time constant is inversely proportional to the surface-to-volume ratio which increases highly in advanced devices. Therefore a reduction of thermal time constants is observed as technology advances from PSDOI to advanced FDSOI nodes like UTB, UTBB, FinFETs and nanowires as reported in [63].

3.1.1 Thermal and Electrical Analogy

The thermal problem can be represented as an analogous equivalent electrical problem: an analogy between the electrical and thermal Ohm's law can be seen in **Figure 3.2**.

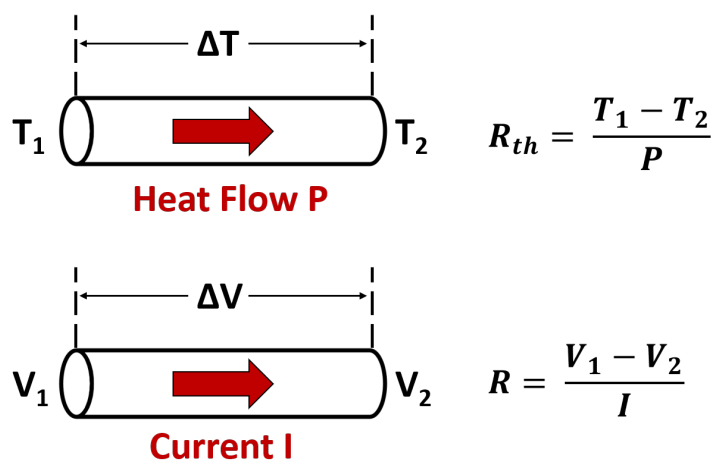


Figure 3.2: Analogy of the thermal and electrical problem.

The corresponding electrical and thermal parameters and how they are interrelated are demonstrated in **Figure 3.3**.

Electrical	Electrical Resistance $R \text{ (}\Omega\text{)}$	Voltage difference $\Delta V \text{ (V)}$	Current $I \text{ (A)}$
Thermal	Thermal Resistance $R_{th} \text{ (}^\circ\text{C/W)}$	Temperature $\Delta T \text{ (}^\circ\text{C)}$	Heat Flow $P \text{ (W)}$

Figure 3.3: Relation between thermal and electrical parameters.

With a background on the thermal parameters that will be necessary in assessing the thermal performance of our devices, we move to an in-depth discussion of SH.

3.2 Self-Heating Effect

With the basics of SH its causes the impacts elevated device temperatures on performance and reliability introduced in **Chapter 1** and **Subsection 2.1.1**, the thermal equivalent circuit of SH (**Figure 3.4**), with the temperature rise with respect to the ambient being seen as a result of power dissipation in the device.

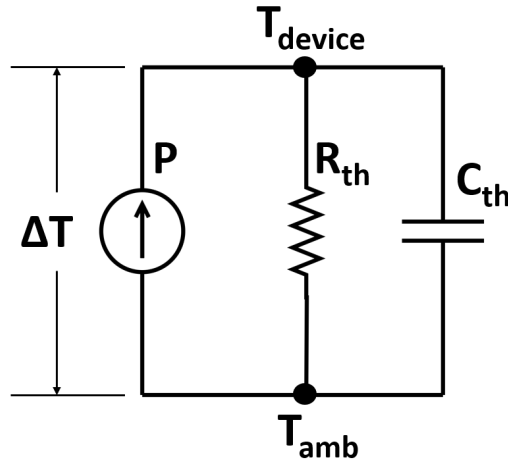


Figure 3.4: Thermal equivalent circuit.

SH is not a recently discovered phenomenon, it has been reported in literature for over a few decades. At high power dissipation levels, local hotspots were seen in MOSFETs almost 50 years back in [64]. Back in 1989, Mautry and Trager found MOSFET temperature rises of up to 60 °C on a 0.6 μm MOSFET [65].

SH was studied on SOI devices too. In 1992, the fact that SH is the reason behind negative differential resistance in SOI MOSFETs was proposed by McDaid et al. [66]. In the same year, the influence of SH on SOI MOSFET parameters was studied through a comparison of electrical and electrothermal modelling in [67]. Also in 1992, a method of computing dynamic self heating was proposed by Caviglia in [68]. In 1999, Jin [69] explained a way of estimating R_{th} and C_{th} using the variation in output conductance g_d in AC conductance studies.

All of the above clearly shows that the scientific community has been aware of the self-heating phenomenon for a while. Building upon the same, we investigate the current scenario of SH on the most advanced devices with a comparison of the SH problem on older devices (on other technologies too) with respect to the latest ones. To investigate SH in state-of-the-art devices, we look into these devices' material properties and heat transfer mechanisms.

3.3 Thermal Conductivities of Materials in MOSFETs

As stated previously in the causes of SH, the thermal conductivity of the materials used for the fabrication of the MOSFET comes into play in determining the heat evacuation. We take a look at the values for some of the commonly used materials and thin films in advanced MOSFETs:

Table 3.1: Thermal Conductivity of Various Materials used in MOSFETs.

Material	Thermal Conductivity ($\text{Wm}^{-1}\text{K}^{-1}$)
Si (bulk) [70]	148
Ge (bulk) [70]	60
Silicides [70]	40
Si (10 nm) [70]	13
SiO ₂ (bulk) [70]	1.4
HfO ₂ (bulk) [71]	1.3

From **Table 3.1** above, the following inferences can be made for the different materials:

1. Bulk Silicon Substrate: The bulk Si substrate is relatively one of the most thermally conductive layers with a thermal conductivity of $148 \text{ Wm}^{-1}\text{K}^{-1}$ [70].
2. Silicon Thin-film: The thermal conductivity of thin Silicon films are observed to be degraded drastically from the bulk silicon value. This happens due to phonon boundary scattering in thin films, as described later. This implies that the thermal conductivity of thin channel, source and drain regions in advanced MOSFETs would be lower than the bulk silicon value.
3. SiO₂: In SOI MOSFETs, an SiO₂ BOX is employed to better electrical isolation of the channel from the substrate. However, with the thermal conductivity of bulk SiO₂ being $1.4 \text{ Wm}^{-1}\text{K}^{-1}$, which is two orders of magnitude lower than that of bulk Silicon. Additionally, the thermal conductivity of a 20 nm thin SiO₂ film (used in the 22FDX[®] technology in this study) can be further degraded to around $1 \text{ Wm}^{-1}\text{K}^{-1}$, owing to dominant boundary resistances described later.
4. HfO₂: In [72], the thermal conductivity of HfO₂ film was reported to be around $0.4 - 0.7 \text{ Wm}^{-1}\text{K}^{-1}$ for thicknesses varying from 5.6 nm to 20 nm compared to bulk values of around $1.3 \text{ Wm}^{-1}\text{K}^{-1}$ [71]. With thin film

HfO₂ being a widely used gate-dielectric material, this is representative of the thermal resistance of the gate region.

3.3.1 Mechanisms Affecting Thermal Properties of Thin Films

For thin films, some specific mechanisms and effects come into play to dictate heat transport. Two such dominant mechanisms are listed here.

Phonon Scattering

Heat transmission in metals is dominated by electrons whereas in semiconductors and dielectrics, phonons conduct the thermal energy [73]. Therefore, the mobility of the phonons determines the thermal properties of semiconductor and dielectric materials. The significance of boundary scattering becomes more pronounced as the ratio between the mean free path of the primary heat carriers (phonons) and the thickness of the layer increases [73]; as the layer thickness reduces and approaches the phonon mean free path, a decrease in thermal conductivity is encountered.

1. Silicon: The phonon mean free path for bulk Silicon is around 200-300 nm, therefore Silicon channels in MOSFETs thinner than these values shall show lesser thermal conductivity compared to the bulk value. Using Matthiessen's rule estimate for the phonon mean free path, the thermal conductivity of undoped ultrathin silicon and germanium films plotted in [74] has been shown in **Figure 3.5**. A drastic degradation of the thermal conductivity Silicon films in ranges upto 30 nm is seen below compared to a bulk Silicon conductivity value of $148 \text{ Wm}^{-1}\text{K}^{-1}$ [70].
2. SiO₂: Phonon boundary scattering for SiO₂ is only expected to be of importance in films thinner than 3.5 nm and most authors converge on the opinion that it is not of much practical significance unlike that of Silicon [75]. However, the thermal conductivity of thin SiO₂ films below 100 nm decreases due to thermal boundary resistance with surrounding layers which is explained next.

Thermal Boundary Resistances (TBR)

Thermal Boundary Resistances (TBR), also known as interfacial thermal resistance (ITR) or Kapitza resistance is the resistance coming up at the boundaries (or interfaces) between materials. TBRs are present between different types of interfaces like metal-semiconductor, semiconductor-dielectric etc where various effects result in the lowering of thermal conductivity.

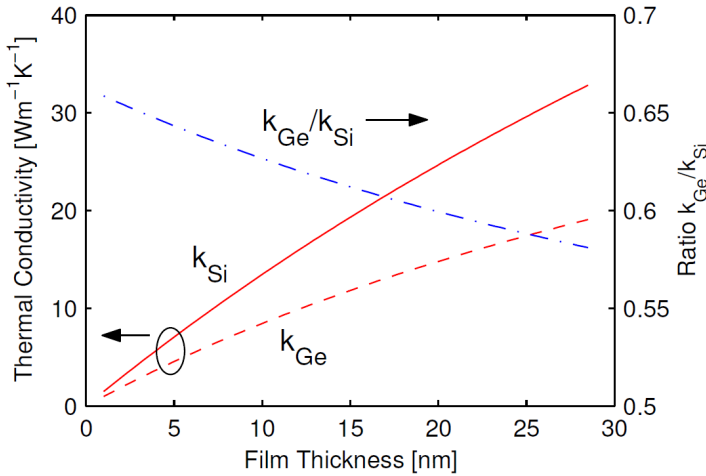


Figure 3.5: Variation of thermal conductivity of Si and Ge thin films with film thickness [74]. The reduction in thermal conductivity with reduced film thickness is a direct consequence of phonon scattering.

In Pop et al. [70], the main origins of TBR are reported to be not well understood but are most likely attributed to factors such as phonon dispersion mismatch, energy conversion between heat carriers (electron–phonon), atomic-scale surface irregularities or porosity at the interface of the two materials [76]. Back in 1997, Lee et al. demonstrated that for thin SiO_2 films, a TBR equivalent to a 20 nm thick layer of SiO_2 is present between the SiO_2 –Si interface that comes into play as the physical thickness of the film decreases [75]. More recently in 2022, Wu et al. [77] comparative study of interfacial thermal conductance between metal and semiconductor reported that the phonon-phonon interaction at metal-semiconductor interface plays the main role in in heat transport.

An in-depth understanding of TBRs is crucial going ahead to estimate thermal properties of the most advanced MOSFETs. With thin films and different types of materials (high-k dielectrics, multi-layer gate stacks) and therefore multiple interfaces (metal-dielectric, semiconductor-dielectric) being used, more research in this area is needed.

3.3.2 Thermal Conductivity Variation with Temperature

It is pertinent to note that the material thermal conductivity is dependent on temperature, especially given the different studies in this thesis related to various high-temperature impacts on devices. The variation of thermal conductivities of Si and SiO₂ with temperature is shown in **Figure 3.6** below, taken from [78] which could result in a variation in R_{th} . It was revealed that the R_{th} in FDSOI MOSFETs was mainly dictated by the thermal conductivity of the BOX with the channel thickness playing a secondary role. The degradation of thermal conductivities of both Si and SiO₂ at cryogenic temperatures was the reason for the increased thermal resistance of SOI MOSFETs at these temperatures. There is approximately an order of magnitude degradation in the thermal conductivity of SiO₂ at 10 K compared to room temperature; this is shown to increase the R_{th} almost four times as reported in [78].

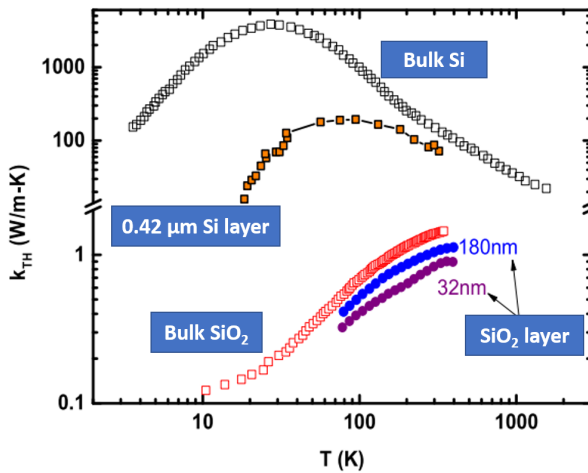


Figure 3.6: Variation of thermal conductivity of Si and SiO₂ with temperature [78].

As the thermal conductivity of SiO₂ increases with temperature, we intuitively expect a reduction of R_{th} on going to temperatures higher than room temperature. However, as the increase in thermal conductivity going from 300 K to 400 K is not as drastic as the increase from 10 K to 300 K, R_{th} reduction is expected to be limited. The variation of R_{th} at higher temperatures, the range of our interest in this thesis, is studied later in **Section 3.7**.

3.4 Self-Heating Studies in Literature

The fact that the lower thermal conductivity of the BOX is worsening the SH problem in SOI devices compared to bulk has been widely reported in literature over the years.

Back in 1994, Su [79] demonstrated that device temperature rise as high as 100 °C can occur due to SH in SOI devices. In 1995, Dallmann showcased SH aggravation in SOI MOSFETs compared to bulk through simulated temperature profiles [80].

More recently in 2016, [81], for 28 nm gate length devices, the thermal resistance in FDSOI was observed to be 143 K μ m/mW compared to 42 K μ m/mW for its bulk counterpart, a factor of around 3.4 times higher. The temperature rise from SH at a V_d and V_g bias of 1 V was found to be 32 °C and 87 °C in bulk and FDSOI for the 28 nm length devices. The dependence of R_{th} on the gate length was less pronounced in bulk devices compared to FDSOI: the dominance of the thermal path through the substrate in bulk devices across all gate lengths was attributed to be the main reason for the same.

3.4.1 Self-Heating with Dimension Scaling

The primary reason for growing SH in smaller devices is that of higher power densities with ever-shrinking device sizes. In 2006, Pop [70] showed the trends in exponentially increasing on-chip power density trends with miniaturization and reported that power density trends in nanoscale devices could be as much as a nuclear reactor and expected to increase further.

Rising thermal resistance with reducing gate length has been reported in 28 nm FDSOI technology using the RF characterization technique for SH as shown below in **Figure 3.7** [82] [83]. The fact that technology scaling increases the thermal resistance in bulk MOSFETs was demonstrated in recent studies in 2016 by Uchida [84] using the gate-resistance technique. Rising R_{th} trends were also observed from device simulations by Fiegna in [85].

It is therefore established that increasing R_{th} with reduced device lengths is a factor affecting advanced nodes regardless of the type of technology (bulk, SOI etc); this makes it necessary to study it thoroughly in such devices.

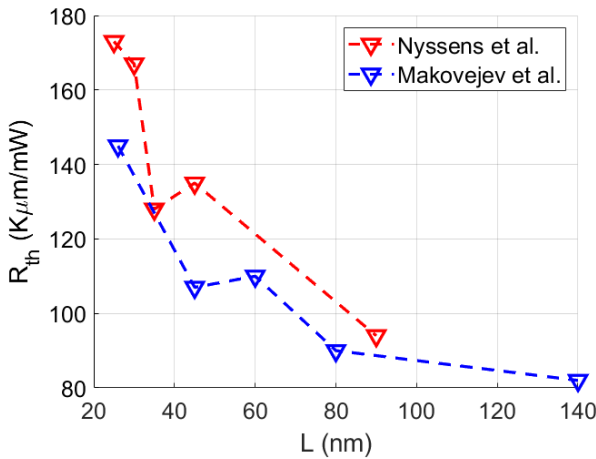


Figure 3.7: Increase of R_{th} with decreasing device length in 28 nm FDSOI MOSFETs reported by Nyssens [83] and Makovejev [82] using RF technique for SH characterization.

3.5 Self-Heating Characterization Techniques

Different techniques of experimentally estimating SH exist in literature: the basic idea behind these techniques is to have a thermally sensitive metric that can help in this assessment. Prasad extensively reviews various such techniques in [12] ranging from analytical techniques like scanning thermal microscopy, thermal IR imaging, time-integrated near-infrared (NIR) emission to electrical DC and RF techniques like thermometry based on a neighbour transistor or diode, noise thermometry amongst others.

An interesting quote from [12] is that “there is no right or wrong measurement technique—the choice depends on the requirements and constraints of the end-user”. Cross-validation of different techniques could be important to get a clearer picture of the thermal problem given the imperfections of each technique. this makes it important to assess the applicability of these techniques and possible differences (along with reasons for the same) arising in extractions from them.

In this work, we limit ourselves to the analysis of the few most prominent DC and RF electrical techniques for SH characterization of advanced MOSFETs and evaluate their strengths and weaknesses.

3.5.1 Pulsed IV Technique

The pulsed IV technique was proposed by Jenkins back in 1995 [86]. It has been used for self-heating estimation in numerous following works, detailed by Jenkins further in [87] and used in Anghel in [88].

In the pulsed IV technique, adequately short gate voltage pulses compared to the thermal time constant of the device are used to not heat the channel. This enables obtaining drain current I_d that is free of SH. Once a voltage pulse is applied to the gate and a DC voltage is supplied to the drain, the resulting drain current travels through a shunt, typically with a resistance of $50\ \Omega$, connected in series with the drain. The voltage drop across this shunt is then recorded using an oscilloscope. By knowing the predetermined drain voltage, the amplitude of the drain voltage pulse, and the shunt resistance, it becomes possible to reconstruct the pulsed drain current. For this setup to function optimally, the drain current should be nearly zero when the gate pulse is not applied. The resolution of the current in this configuration is constrained by both the voltage resolution of the oscilloscope and the shunt resistance. Additionally, the maximum detectable drain current is limited, as a high drain current would generate a significant drain voltage pulse [87]. Consequently, the effective gate width of the device under test (DUT) needs to be carefully chosen—sufficiently large to avoid limitations due to drain current resolution but small enough to meet the constraints on the amplitude of the drain voltage pulse. This consideration is particularly pertinent for advanced devices structured with parallel fingers, resulting in a substantial effective gate width.

Makovejev in [63] and [89], described the process in detail and SH measurements on Body-tied PDSOI MOSFETs are made. By changing the pulse width from $1\ \mu\text{s}$ (reported to be the highest available pulse width) to $10\ \text{ns}$ (reported to be the lowest available pulse width), the I_d - V_d characteristics seen in **Figure 3.8** clearly show the removal of SH. In fact it is observed that with pulse width of $50\ \text{ns}$, SH is removed totally as reducing the pulse width to $20\ \text{ns}$ and $10\ \text{ns}$ do not increase I_d further. From the SH-free I_d obtained above, there are two ways by which R_{th} and device temperature can be obtained, these are shown below.

Pulsed I-V Hot Chuck

In this method used in [86], the chuck temperature is varied and I_d - V_d measurements are made with sufficiently short gate pulses. Using short gate pulses makes sure that the device is not heated up due to the pulses and the device tem-

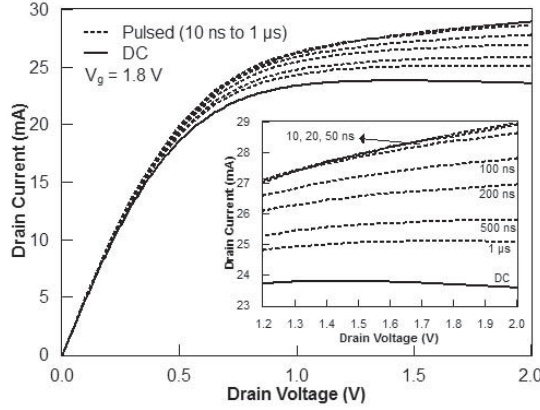


Figure 3.8: I_d - V_d obtained from DC and pulsed measurements with the pulse width from 10 ns to 1 μ s at room temperature and $V_g = 1.8$ V. Inset: high V_d region. [89].

perature is defined by the temperature of the chuck. The points of intersections of the DC I_d - V_d curve that is affected by SH with the SH-free I_d - V_d curves at different temperatures give information on the device temperature at different bias conditions (**Figure 3.9**). From the device temperature at different biases, R_{th} can be extracted.

Pulsed I-V k-coefficient

Another way to find device temperature based on SH-free pulsed IV data was proposed in [88] and used in [90] and [89]. It assumes that self-heating primarily influences mobility, and the decline in current as temperature rises is a direct result of reduced mobility. The increase in temperature can be approximated by **Equation 3.3**:

$$\Delta T = T_0 \left[\left(\frac{I_{d0}}{I_d} \right)^{\frac{1}{k}} - 1 \right] \quad (3.3)$$

Here, ΔT represents the temperature increase, T_0 is the reference temperature (typically room temperature), I_d signifies the drain current at temperature T_0 under self-heating conditions (at DC conditions), I_{d0} is the drain current when self-heating is absent (determined through pulsed I-V measurements in this study), and k is the coefficient associated with the degradation of low-field

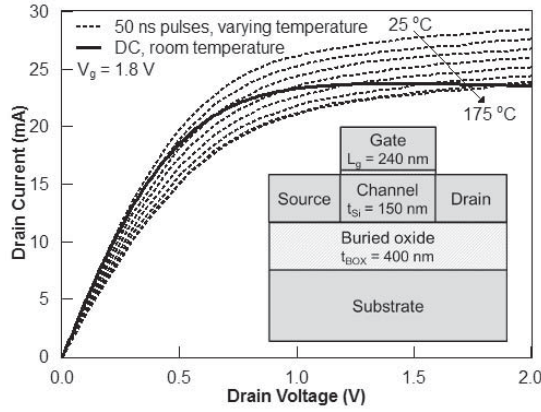


Figure 3.9: Output characteristics at $V_g = 1.8$ V obtained from the 50-ns pulsed I–V measurements at various chuck temperatures and from the DC measurement at room temperature. Inset: a schematic of the device (not to scale). [89].

mobility with temperature. The mobility temperature degradation coefficient k can be estimated from the variation of low field mobility with temperature in **Equation 3.4**.

$$\mu_{\text{eff}} = \mu_{\text{eff}0} \left(\frac{T}{T_0} \right)^{-k} \quad (3.4)$$

Here, T denotes the temperature, μ_{eff} represents the mobility at temperature T , and $\mu_{\text{eff}0}$ corresponds to the mobility at temperature T_0 . In [89], the k -coefficient is derived by analyzing the mobility across different temperatures. The mobility is determined by examining the slope of the $I_d/\sqrt{g_m}$ variation with V_g at various temperatures. From the determined k -coefficient, the device temperature and thus the R_{th} can be extracted.

It was shown in [89] that the hot-chuck method is more accurate than the k -coefficient method as it does not require any assumptions about current degradation mechanisms.

Shortcomings of the Pulsed IV Technique

With technical constraints restricting the minimum pulse width to a few tens of nanoseconds (or a few megahertz when translated into the frequency domain),

the pulsed IV methods were deemed to be unlikely to be adequate for cutting-edge devices, where the thermal time constant (τ_{th}) diminishes with scaling [89]. This is the principal limitation of using the pulsed IV technique for SH estimation in advanced nodes which would require even thinner pulses compared to those commercially available. Moreover, the pulsed I–V method is constrained to devices with a certain extent of gate widths due to limitations in current resolution and the V_d pulse limit. This restriction is particularly crucial for devices with multiple fingers, where the total gate width can be substantial. Additionally, the pulsed I–V technique imposes constraints on the device off-current, influenced by short-channel effects in advanced MOSFETs. With these shortcomings, the RF technique was recommended over pulsed IV for state-of-the-art devices in [89].

3.5.2 Gate Resistance Technique

The gate resistance technique or gate thermometry is the method that uses the temperature-dependent gate resistance to estimate the device temperature. While a simple 2-terminal method could help in estimating gate resistance, a 4-terminal sensing technique is generally used to enhance the extraction accuracy. The electrical principle of this technique dates back to the Kelvin bridge in 1861 invented by Lord Kelvin for the precise measurement of low resistances.

The 4-terminal technique utilizes separate pairs of current-carrying and voltage-sensing nodes to make accurate resistance measurements compared with the simpler 2-terminal (2T) sensing technique. By sourcing a current through the resistance to be estimated using the current-carrying electrodes (2 and 4 in **Figure 3.10**), the voltage drop across the voltage sensing electrodes (1 and 3 in **Figure 3.10**) is measured and the resistance is calculated as the ratio of this voltage drop and the sourcing current. Separating the current and voltage electrodes helps in eliminating additional access and contact resistance from measurements that can arise from 2-terminal measurements. Additionally, the voltage-sensing electrodes are kept inner in order to further reduce the impact of resistance in the measurement.

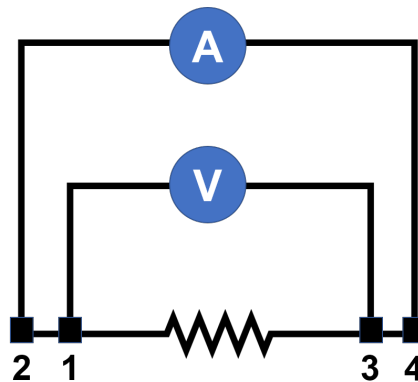


Figure 3.10: 4-Terminal sensing electrical circuit diagram.

The schematic for the 4T method for estimating MOSFET SH is shown below. Apart from the standard gate and drain biasing, additional contacts are made on the gate to have the current forcing and voltage sensing electrodes.

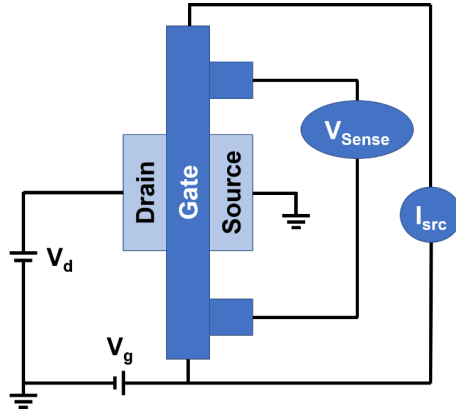


Figure 3.11: 4T Method circuit schematic applied on a MOSFET.

A detailed discussion on this technique shall be made in [Subsection 3.8.2](#).

3.5.3 AC Conductance Technique

Proposed by Tu in 1995 [91], the AC conductance technique is based on the idea that due to finite thermal capacitance of the device, the device temperature cannot follow the voltage oscillations at high frequencies [24]. As a result, at a specific frequency, the dynamic self-heating effect is effectively eliminated. To derive parameters related to self-heating, such as temperature rise or thermal resistance, the output conductance g_d is measured at both high and low frequencies. The difference in conductance serves as the basis for extracting self-heating parameters. An impedance analyzer is employed to measure the output conductance at different frequencies.

The AC conductance technique offers simplicity in both setup and measurements, as the variation of output conductance with frequency can be directly assessed using an impedance analyzer. However, limitations of the measurement setup make this method operate up to 5 MHz [91]. This could be a serious problem for characterizing SH in advanced devices with smaller time constants that require reaching higher frequencies for SH-free characteristics. It is mainly because of this reason that the RF technique, which can go up to much higher frequencies, has been deployed for SH characterization over the AC conductance technique for state-of-the-art MOSFETs.

3.5.4 RF Technique

The RF technique extends the AC conductance technique by allowing operation at higher frequencies and allowing more precise extraction of R_{th} and C_{th} for state-of-the-art devices. With the thermal time constants of advanced devices reducing, reaching higher frequencies are essential in order to have SH-free characteristics and while measurement setup limitation of the AC conductance technique is limited to MHz range, the RF technique can go up to tens of GHz based on the S-parameter measurement possibilities used.

In this technique, S-parameter measurements are made on the devices up to high frequencies. From two-port measurements (with Gate as Port 1 and Drain as Port 2), the S-parameters are converted to Y-parameters. The Y parameters can be obtained from the S parameters with the formulae provided below:

$$Y_{11} = \frac{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}}{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}} Y_0 \quad (3.5)$$

$$Y_{12} = \frac{-2S_{12}}{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}} Y_0 \quad (3.6)$$

$$Y_{21} = \frac{-2S_{21}}{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}} Y_0 \quad (3.7)$$

$$Y_{22} = \frac{(1 + S_{11})(1 - S_{22}) + S_{12}S_{21}}{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}} Y_0 \quad (3.8)$$

Where Y_0 is the characteristic admittance (reciprocal of the characteristic impedance).

Dedicated open de-embedding structures were then used for de-embedding. The Y parameters of the open structures are subtracted from the measured Y parameters of the device to take away the parasitics coming from the pads and access lines. The de-embedding process in general has been described earlier in Chapter 2 and can be found in detail in [47].

Specifically of interest, for a MOSFET, the Y_{21} and Y_{22} parameters are:

$$Y_{21} = g_m - j\omega C_{dg} \quad (3.9)$$

$$Y_{22} = g_d + j\omega C_{dd} \quad (3.10)$$

where g_m is the transconductance, g_d is the output conductance, C_{dg} is the drain-to-gate capacitance, C_{dd} is the total drain capacitance, and ω is the angular frequency.

Rinaldi in [92] found through rigorous mathematical computations a relation between the thermal impedance Z_{Th} and Y parameters for a two-port network.

$$Y_{ij} = Y_{ijT} + Z_{th} \frac{\partial I_i}{\partial T_{amb}} (V_g Y_{1jT} + V_d Y_{2jT} + I_j) \quad (3.11)$$

where Y_{ij} is the admittance parameter, Y_{ijT} is the Y_{ij} parameter at a high enough frequency where the dynamic self-heating effect is removed, T_{amb} is the ambient temperature and Z_{th} is the thermal impedance.

Regarding the dI_d/dT_{amb} term, Rinaldi's work proposes the estimation of the temperature variation of drain current with respect to the ambient temperature as a more elegant approach. The same method is also employed by Scholten in [93] where the derivative of drain current with the ambient temperature and not the lattice temperature is considered. As the device temperature cannot be directly measured, it is reported there that some studies [24] use analytical models for this purpose which would depend on the precision of the thermal resistance extraction model. Alternatively, an iteration method to compute dI_d/dT at a predicted channel temperature could be made as in [94]. In our work, it is noted that the I_d dependence with temperature is approximately linear at high temperatures and thus the variation of slope at ambient temperature and higher temperatures is negligible.

In general, there is a transition in the Y parameters due to SH. While both Y_{21} and Y_{22} show this transition, the transition in Y_{22} with frequency is more pronounced, hence that is the one mainly used to extract the thermal parameters. Considering the real part of the Y -parameter equation above, the thermal resistance R_{th} can be obtained by:

$$\text{Re}(Y_{ij}) = g_{ij} = g_{ijT} + R_{th} \frac{\partial I_i}{\partial T_{amb}} (V_g g_{1jT} + V_d g_{2jT} + I_j) \quad (3.12)$$

Of the **Equation 3.12**, considering the transition in Y_{22} due to the reasons given above provide a relation between R_{th} and the output conductance g_d as

given below. This is quite in line with the equation obtained from the AC conductance technique.

$$g_{22} = g_{22T} + R_{th} \frac{\partial I_d}{\partial T_{amb}} (V_d g_{22T} + I_d) \quad (3.13)$$

The computation can be made from the imaginary part of the Y parameter as well:

$$\text{Im}(Y_{ij}) = \text{Im}(Y_{ijT}) + \text{Im}(Z_{th}) \frac{\partial I_i}{\partial T_{amb}} (V_g g_{1jT} + V_d g_{2jT} + I_j) \quad (3.14)$$

$$C_{ij} = C_{ijT} + \frac{\text{Im}(Z_{th})}{\omega} \frac{\partial I_d}{\partial T_{amb}} (V_g g_{1jT} + V_d g_{2jT} + I_j) \quad (3.15)$$

The variation in the Y_{22} parameter corresponds to a variation in C_{dd} from the above equation. C_{dd} is seen to vary by a few orders of magnitude with frequency, and from this information, C_{th} can be computed.

$$C_{th} = \frac{1}{\omega \cdot \text{Im}(Z_{th})} \quad (3.16)$$

The aforementioned transition in Y parameters is manifested as a transition in conductances and capacitances. The output conductance g_d is computed as the real part of output admittance Y_{dd} , transconductance g_m is the real part of transadmittance Y_{dg} . The g_d versus frequency curve and the drain capacitance C_{dd} versus frequency curve show a transition due to SH (coming from the transition in Y_{dd}), which allows to assess SH-related features (e.g. R_{th} and C_{th}). R_{th} and capacitance C_{th} are then extracted using **Equations 3.17 and 3.18** given below.

$$R_{th} = \frac{\Delta g_d}{(I_d + V_d g_{d,LF}) \frac{\partial I_d}{\partial T}} \quad (3.17)$$

$$C_{th} = \frac{\Delta C_{dd}}{R_{th}^2 (I_d + V_d g_{d,LF}) \frac{\partial I_d}{\partial T}} \quad (3.18)$$

Where Δg_d (ΔC_{dd}) is the difference between $g_{d,LF}$ ($C_{dd,LF}$) and $g_{d,HF}$ ($C_{dd,HF}$), the output conductance g_d (capacitance C_{dd}) at low and high frequencies, respectively. I_d is the DC drain current, $g_{d,LF}$ is the output conductance g_d at low frequency, and $\partial I_d / \partial T$ is the slope of the I_d versus temperature plot extracted from $I_d - V_g$ curves measured over a temperature range, taken at ambient temperature T_{amb} .

In [89], the transition of g_d and C_{dd} in frequency was demonstrated in PDSOI MOSFETs as seen in **Figure 3.12** and **Figure 3.13** respectively.

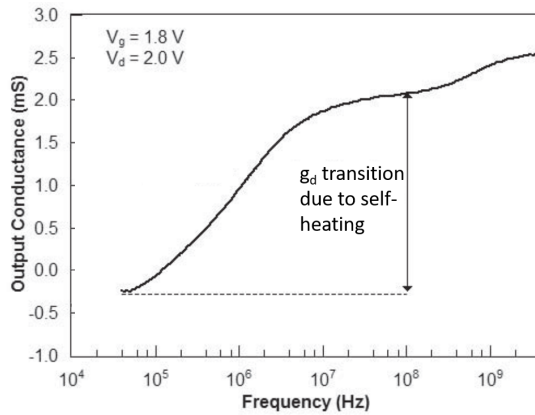


Figure 3.12: Variation in g_d with frequency reported in [89].

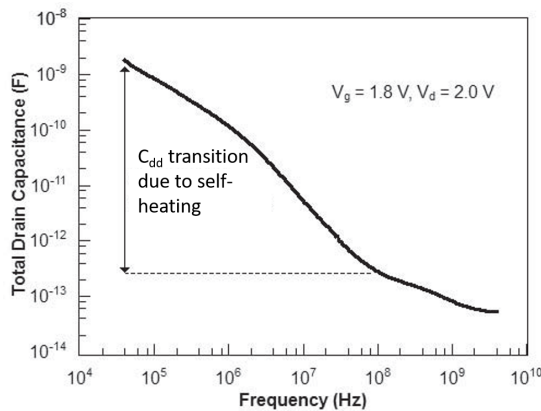


Figure 3.13: Variation in C_{dd} with frequency reported in [89].

Isothermal Frequency

The isothermal frequency is the frequency above which the impact of dynamic self-heating is removed completely; this can be visualized from a plateau in the output conductance g_d or drain capacitance C_{dd} seen in **Figure 3.12** and **Figure 3.13** respectively. The transition of g_d or C_{dd} from low to high frequencies helps in estimating the thermal resistance and thermal capacitance. The same has also been seen from measured data in [47]. Note that the transition can also be affected by other factors apart from SH like substrate effect or gate resistance effect due to which a clear plateau might not be seen, more is discussed on this aspect later.

Characteristic Thermal Frequency

The characteristic thermal frequency is not to be confused with the isothermal frequency. It is related to the thermal time constant and is lesser than the isothermal frequency at which SH-free conditions are attained.

An empirical way of estimating the characteristic thermal frequency proposed by Jin in [95] is the frequency at which the following **Equation 3.19** is respected:

$$g_d = g_{d,LF} + \frac{\Delta g_d}{3} \quad (3.19)$$

where g_d is the frequency-dependent output conductance, $g_{d,LF}$ is the output conductance at low frequency, and Δg_d is the transition in g_d from low to high frequency due to removal of dynamic SH.

While the background of this empirical method was not discussed, it is argued that this is done in line with the thermal time constant of an RC circuit where the time taken to discharge to 37% of the total charge is defined as the time constant. In this case, the assumption of one-third of the transition would correspond to a 33% discharging of the RC circuit equivalent which is not far from the defined value.

Extraction of the characteristic thermal frequency enables estimating the thermal time constant from which thermal capacitance can be obtained.

Fitting model

To have an accurate estimation of SH parameters, measurements of the Y parameters are tried to fit with an RC network of different orders. An example of a fourth-order RC network for fitting is seen in **Figure 3.14**.

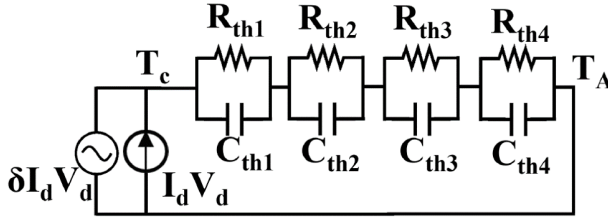


Figure 3.14: Fourth order thermal network for the fitting model used in [48].

It is noted by Nyssens [48] that while PDK models use a first-order RC network for fitting, it is not adequate as the transition is not well fit. At least a third or fourth-order network is needed for accurate fitting and thereby SH parameter extraction. The above is also verified in this work where a first or second-order network is inadequate for fitting properly, a fourth-order network is seen to be best in **Figure 3.15**. A major takeaway from this point is that the transition is not modelled well enough in the PDK, given that the measurements require a fourth-order network for the fitting.

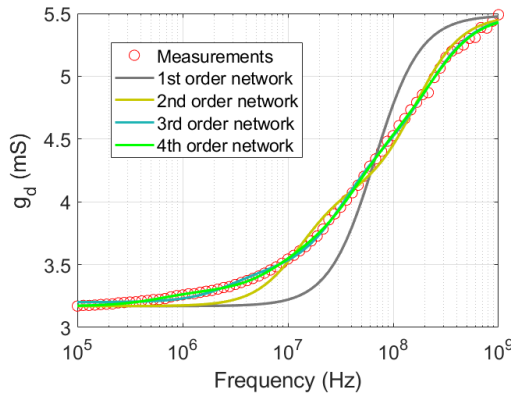


Figure 3.15: Thermal network fitting for g_d based on order of network in this work. A fourth-order network is seen as necessary to fit measurements.

3.5.5 Other Mechanisms Affecting RF Transition

In order to study the SH parameters from a transition in g_d versus frequency, it is of prime importance to make sure that the transition itself is solely caused due to SH and not other effects. In practice, there can be various reasons due to which the g_d versus frequency transition is not caused solely by SH, some other mechanisms causing the same are studied below.

Substrate Effect

Substrate-related coupling below the BOX could considerably affect the g_d curve versus frequency resulting in another transition. While both the SH and substrate effects affect the g_d curve, the issue is trickier because of the frequency range over which they come into play. Theoretically, the time constants of these effects are dependent heavily on various factors like device design, geometries, and technological parameters, in advanced FDSOI MOSFETs, SH transition shows up from the kHz to GHz range whereas the substrate effect comes into play around the MHz to GHz range thereby causing an overlapping frequency range where they both affect the output characteristics. It is therefore necessary to decouple other effects in order to have accurate SH extraction.

It was shown previously in [96] that for thin BOX FDSOI devices, while thinning the BOX gave reduced thermal resistance, it however gave rise to greater source to drain coupling below the BOX that was confirmed through experimental studies in [96]. Studies by Makovejev in [97] showed that the extent of substrate effect on the g_d transition at high frequencies can be even more dominant than SH. Subsequently, it was found that using a heavily doped ground plane (GP), a Silicon layer underneath the BOX, helps in suppressing the substrate-related transition.

In more recent studies by Nyssens [98], it was deemed that ignoring the substrate-related transition just because it is supposedly suppressed enough with the ground plane is not accurate and could lead to misinterpretation of SH. A process of decoupling the substrate effect from the SH was demonstrated in this work by using the ZTC bias point where dynamic SH vanishes and using that bias condition to extract SH-free device characteristics. **Figure 3.16** below from the work shows the variation of g_d versus frequency for different biases including the ZTC bias point of $V_g = 0.62$ V in that work. Although no SH-related transition was expected at that point, the fact that a transition is seen shows that that is the one due to the substrate effect. This can also be visualized by the plots at values of V_g lower than ZTC where the g_d versus frequency curve

was supposed to be pushed down due to SH but starts rising at around 100 MHz range with the onset of SE.

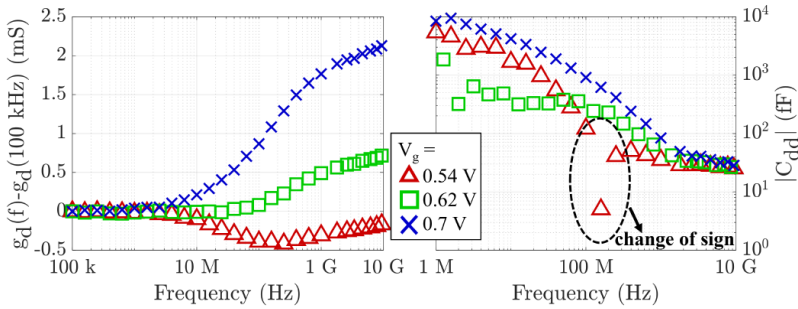


Figure 3.16: Variation of g_d and C_{dd} with frequency below and above ZTC [98].

Floating Body Effect

Although the floating body effect (FBE) is specifically a phenomenon present in floating body PDSOI MOSFETs and does not pertain directly to our work on FDSOI devices here, it is important to note the transitions in g_d versus frequency due to such effects in floating body PDSOI MOSFETs.

Jin showed in [95] the difference in the g_d versus frequency response for FDSOI and floating body PDSOI devices, and the sample curve in **Figure 3.17** below clearly shows that FBE also comes into play in a similar frequency range as SH and needs to be decoupled, just like substrate effect. Additionally, it needs to be taken into account that FBE has a bias-dependent nature with V_d too, unlike SH, as reported in [95].

Gate Resistance Effect

Another factor that causes a transition in the g_d curve is gate resistance. However, as this transition appears at relatively higher frequencies compared to that of SH, it does not directly affect the SH extraction problem to a great extent. An example of all the 3 effects and their impact on the g_d versus frequency curve is shown in **Figure 3.18** from [99]. The transition due to gate resistance reduction in that work was observed to come into play at around 10 GHz.

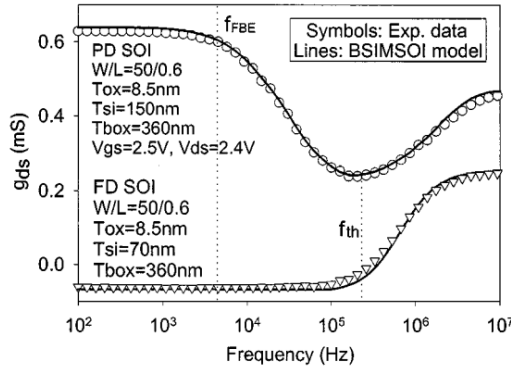


Figure 3.17: Impact of floating body effect on g_d vs frequency [95].

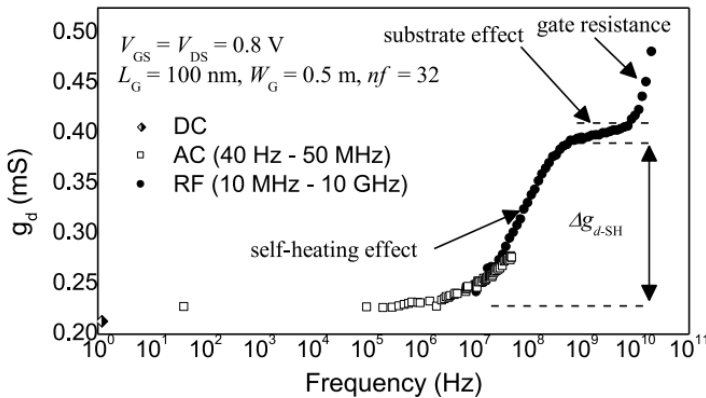


Figure 3.18: Impact of gate resistance on g_d vs frequency [99].

In addition to these factors, specific parameters that can affect the R_{th} extraction using the RF technique are discussed next. The extraction of the derivative of the drain current with temperature, dI_d/dT , is crucial in determining R_{th} ; finer aspects of its extraction process are discussed in [Subsection 3.5.6](#). In [Section 3.6](#) it is seen from corner simulations in the PDK that die-to-die variability can also give rise to variations in the thermal resistance extracted. The ambient temperature is another factor that affects thermal resistance, this has been studied in [Section 3.7](#). A detailed study of these parameters gives us deeper insights into the extraction of thermal parameters using the RF technique.

3.5.6 Drain Current vs Temperature

For the extraction of thermal parameters using the RF technique, another important parameter is the slope of drain current I_d with temperature, dI_d/dT . The extraction of this slope can be tricky at times, and this might in turn impact the extracted thermal resistance. This subsection dedicates itself specifically to studying this parameter; results obtained in literature are compared with our measurements and PDK model.

Literature

Previous studies utilising the RF technique for SH characterization used the slope of a linear I_d versus temperature fit as dI_d/dT . This is verified from hot chuck measurement results by Jin in [95] for both PDSOI and FDSOI MOSFETs as seen in **Figure 3.19**. The trends are backed by recent studies by Gonzalez [100] on 180 nm multifinger SOI MOSFETs on XT018 technology from XFAB where a linear fit is seen over a temperature range of 30 to 160 °C in **Figure 3.20**. A linear I_d versus temperature fit was also seen from characterization results for SOI FinFETs from Makovejev [101] where the slope was estimated over a temperature range of 25 to 65 °C.

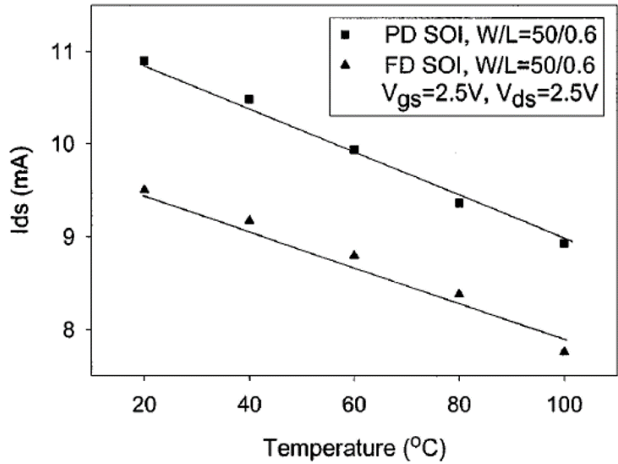


Figure 3.19: Drain current vs temperature for PDSOI and FDSOI MOSFETs using hot chuck measurements at $V_g = V_d = 2.5$ V in [95].

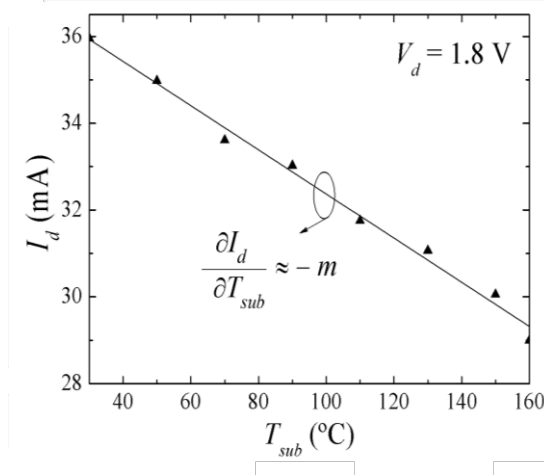


Figure 3.20: Drain current vs temperature using hot chuck measurements for multifinger MOSFETs with $N_f = 30$ and $W_f = 2 \mu\text{m}$ at $V_g = 2 \text{ V}$ and $V_d = 1.8 \text{ V}$ in [100].

Measurements

A linear fit is observed in all the instances of I_d versus temperature in this work for SH estimation using the RF technique. To study this trend with better accuracy, a specific measurement set with multiple temperature points over a temperature range of 25 to 125 °C with steps of 12.5 °C was carried out. The characterized data shown below is for 20 nm FDSOI nMOSFETs (on the 22FDX[®] technology from GlobalFoundries). The device dimensions are as follows: gate length is 20 nm, total width is 30 μm for each of these devices composed of 60 fingers of 0.5 μm finger width. The back-gate MOSFET was grounded for all the experiments ($V_{bg} = 0 \text{ V}$).

For the drain current I_d versus temperature plot, an overall linear trend is observed on all three dies measured and the averaged I_d results over the three dies as seen in **Figure 3.21** below.

Variability of dI_d/dT in Measurements

It can be seen from **Figure 3.21** that the dI_d/dT can vary based on point-to-point slopes. While the best linear fit over the measured points results in a particular dI_d/dT value, the variation in dI_d/dT with respect to this value if other point-to-point slopes are considered can help in understanding the impact

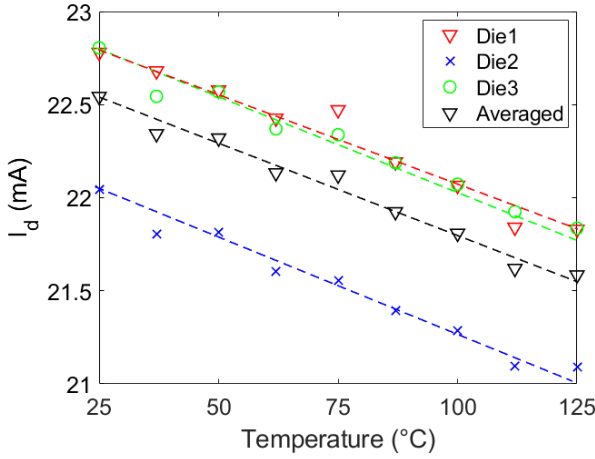


Figure 3.21: Drain Current I_d vs temperature on three dies and their averaged value at $V_g = V_d = 0.8$ V.

of the accuracy of the resulting thermal resistance extraction.

To do so, we compare the variation of extracted R_{th} based on the computed dI_d/dT for the Die3 case shown here. In **Figure 3.21**, the measured points and the linear regression for the fitting over all the temperature points are shown. In **Table 3.2**, the slope of I_d versus temperature as a two-point slope with respect to the 25 °C point is first estimated based on the measurements at the temperature points, to get an idea of the extent of variation in dI_d/dT . The corresponding R_{th} for these different dI_d/dT values extracted by the RF technique (in **Subsection 3.5.4**) using **Equation 3.17** are shown. It is seen that excluding a couple of outliers at 37.5 and 62.5 °C, the variation of R_{th} remains between a range of 190 to 206 K μ m/mW compared to the computed value of 194 K μ m/mW from the regression with all points. A variation of around 6% with respect to the computed value from linear fit is thus seen thereby highlighting the variation coming from dI_d/dT extraction point of view. Additionally, the importance of having a good linear fit over temperature points is demonstrated; in all our studies (and the references [95], [100] and [101]) at least 5 temperature points were taken.

Table 3.2: dI_d/dT computed by taking a two-point slope between 25 °C and other temperature points and its impact on extracted R_{th} .

Temperature (°C)	dI_d/dT ($\mu\text{A}/^\circ\text{C}$)	R_{th} ($\text{K}\mu\text{m}/\text{mW}$)
25	NA	NA
37.5	-21.7	88
50	-9.48	202
62.5	-11.77	163
75	-9.33	206
87.5	-9.96	193
100	-9.77	196
112.5	-10.11	190
125	-9.69	198
Regression	-9.09	194

PDK

To compare the measurement results obtained, the corresponding device is studied in the PDK. In the PDK model, the I_d vs temperature trend is not linear. There are two PDK models for 22FDX[®] technology, EXT and PLUS and this nonlinear trend is seen in both PDKs, which is reflected in a stark variation of dI_d/dT with temperature, unlike a relatively steady value obtained from the linear trend in measurements. The difference between the two PDKs is in the way the self-heating effect is modelled; a detailed study on that has been made in [Subsection 3.8.4](#).

EXT PDK and PLUS PDK Comparisons

For both EXT and PLUS PDKs, I_d and dI_d/dT versus temperature plots at $V_g = V_d = 0.8$ V are shown in [Figure 3.22](#). For the EXT PDK, the slope dI_d/dT varies from $-13.9 \mu\text{A}/^\circ\text{C}$ to $-11.4 \mu\text{A}/^\circ\text{C}$ between 25 °C and 125 °C. In contrast, for the PLUS PDK, dI_d/dT ranges from $-13.2 \mu\text{A}/^\circ\text{C}$ to $-10.3 \mu\text{A}/^\circ\text{C}$ over the same temperature range. Unlike the linear dI_d/dT trend over temperature in measurements, the variation in dI_d/dT over temperature in the PDK makes it important to select the suitable value at ambient temperature for R_{th} computation as per [Equation 3.17](#).

The impact on R_{th} , extracted by the RF technique (refer to [Subsection 3.5.4](#)) using [Equation 3.17](#), is investigated for both PDKs. For the EXT PDK, the variation in R_{th} ranges from 138 to 168 $\text{K}\mu\text{m}/\text{mW}$ based on selection of

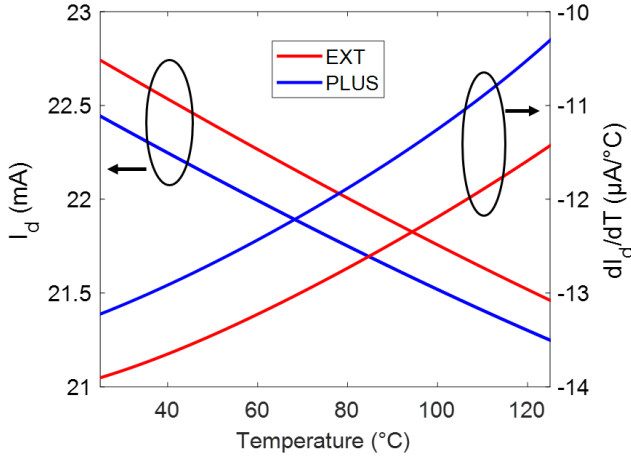


Figure 3.22: Drain current I_d vs temperature in EXT and PLUS PDK at $V_g = V_d = 0.8V$. A nonlinear I_d vs temperature trend is seen in both cases which results in a variation in dI_d/dT over temperature.

dI_d/dT at 25 °C or 125 °C while for the PLUS PDK the corresponding R_{th} variation is from 186 to 239 K $\mu m/mW$. This comparative analysis highlights the variation and impact of temperature on R_{th} across the two PDKs.

It is therefore observed from the PDK that:

1. The dI_d/dT reduces in magnitude with temperature increase, based on the nonlinear I_d versus temperature trend.
2. The extracted R_{th} varies based on the temperature variation of dI_d/dT , which is an important consideration if the I_d versus temperature plot is not linear, unlike most trends assumed in measurements.

Fitting with Nonlinear Power Law Equation

It is seen from the PDK that the I_d versus temperature plot in the PDK is nonlinear. The I_d trend obtained in the PDK is tried to be fit by a nonlinear power law function. In **Equation 3.20** (similar to mobility degradation in **Equation 2.13**), the relation for I_d at different temperatures is shown with T_0 being room temperature and I_{d0} being the I_d at room temperature and f is the power law fitting coefficient.

$$I_d(T) = I_{d0} \left(\frac{T}{T_0} \right)^{-f} \quad (3.20)$$

In **Figures 3.23**, it is seen that a good fit with the both the EXT and PLUS PDK models is obtained with $f = 0.2$.

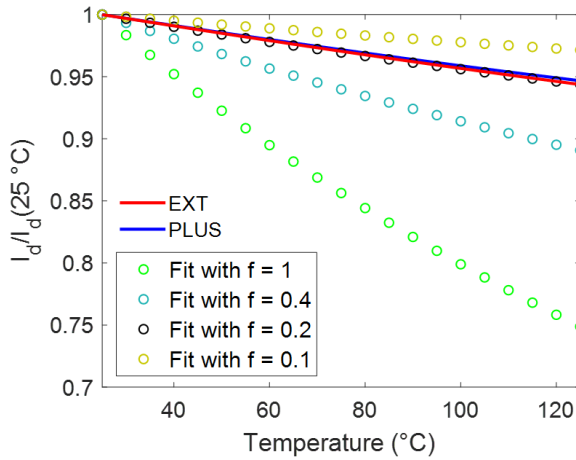


Figure 3.23: Drain current I_d vs temperature in EXT and PLUS PDK and corresponding power law fitting coefficient f values at $V_g = V_d = 0.8$ V. A good fit on both PDKs is seen with a fitting coefficient of 0.2.

For the nonlinear fit with $f = 0.2$ obtained above, we implement the same in our measurements to compare the two trends. In **Figure 3.24**, it is seen that $f = 0.15$ gives a slightly better fit with the averaged I_d vs temperature measurements shown previously in **Figure 3.21**. It is to be noted that with such a fit with $f = 0.15$, the dI_d/dT varies from -11.34 to $-8.13 \mu\text{A}/^\circ\text{C}$ over a temperature range of 25 to 125 °C as also seen in **Figure 3.24**. Using these slopes in the extractions would result in an R_{th} ranging from 169.1 to 235.9 $\mu\text{A}/^\circ\text{C}$. This highlights that taking dI_d/dT at a higher temperature with such a nonlinear fit results in an overestimated R_{th} , similar to the trends observed in the PDK.

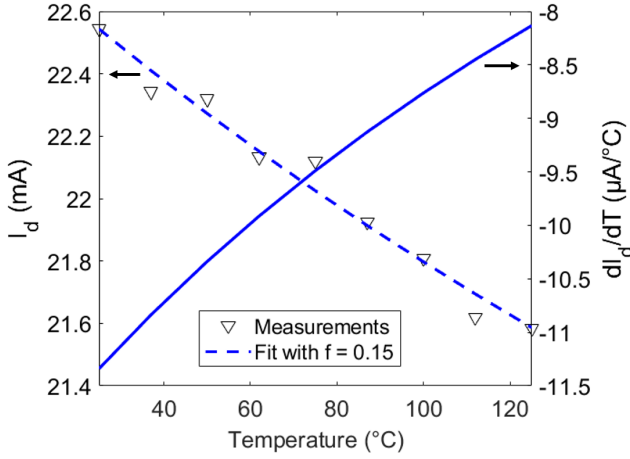


Figure 3.24: Variation of drain current I_d and its slope dI_d/dT with temperature in measurements and corresponding fitting with power law fitting coefficient $f = 0.15$ at $V_g = V_d = 0.8$ V.

Takeaways: I_d versus Temperature

It is thus observed that the drain current versus temperature characteristic is an important aspect of R_{th} extraction. While characterization results in literature consider a linear trend, a nonlinear relation is seen in the PDK models. On a closer look by performing measurements with multiple temperature points, we observe that obtaining such a nonlinear trend is very difficult to establish precisely, but on positioning our measured data with a power law fitting it seems to be possible; this demonstrates that fine margins exist in the I_d versus temperature fitting. It is seen that there is a variation in dI_d/dT over temperature with the nonlinear fit, the impact of this variation is reflected in the extracted R_{th} . Estimating the dI_d/dT at higher temperatures results in a higher R_{th} , therefore showing the importance of estimating it at the desired ambient temperature. The error bars on R_{th} extraction due to dI_d/dT are studied; for linear regression used to calculate this slope, an adequate number of temperature points are recommended for measurement accuracy.

3.6 Impact of Variability on Self-heating Extraction: Corner Simulations in PDK

In order to see the impact of die-to-die variability on the extraction of thermal parameters in the PDK, simulations on slow-slow (SS), typical-typical (TT) and fast-fast (FF) corners are performed. These corners refer to variations in the manufacturing process that affect the electrical characteristics of the devices. While TT represents the standard case, SS and FF are the two extreme corners, thereby giving us an idea of the impact of variability on the device performance. The study is made on both the EXT and PLUS PDKs on the same device in this chapter (the gate length is 20 nm, and the total width is 30 μm for each device composed of 60 fingers, each finger having a width of 0.5 μm) and the results are shown below.

3.6.1 EXT and PLUS PDK Results

From DC measurements, the variation in IV curves for the different corner cases is observed. I_d - V_g and g_m - V_g curves in saturation for TT, SS, and FF corner cases for $V_g = V_d = 0.8\text{ V}$ are shown in **Figure 3.25**. A shift in threshold voltage is apparent for the different corners. From **Figure 3.26**, using the second derivative method in the linear regime ($V_d = 50\text{ mV}$), the shift in the peak of dg_m/dV_g demonstrates this V_{th} shift. It is observed that the V_{th} for the FF, TT, and SS dies vary as 0.25, 0.27, and 0.29 V respectively.

The thermal resistance estimation is made next at the same overdrive voltage V_{ov} for the three corner cases. For $V_d = 0.8\text{ V}$, extractions are made at V_g of 0.78, 0.8, and 0.82 V for FF, TT, and SS corners respectively, resulting in V_{ov} of 0.53 V for all cases. The g_d versus frequency and I_d versus temperature plots are shown in **Figure 3.27** and **Figure 3.28** respectively. The variation of dI_d/dT with temperature is also seen in **Figure 3.29**.

In **Table 3.3**, the variation of R_{th} as a result of process variability is shown by comparing the results on the three corners. It is seen that the FF and SS corners show an R_{th} increase of 8.55% and a decrease of 6.83% with respect to the TT corner, respectively for the EXT PDK. For the PLUS PDK, the FF and SS corners show an R_{th} increase of 9.57% and a decrease of 7.38% with respect to the TT corner, respectively.

It is seen that the R_{th} extraction can be impacted by process variability. Around 7-9% R_{th} variation with respect to the typical corner case is observed in both EXT and PLUS PDKs.

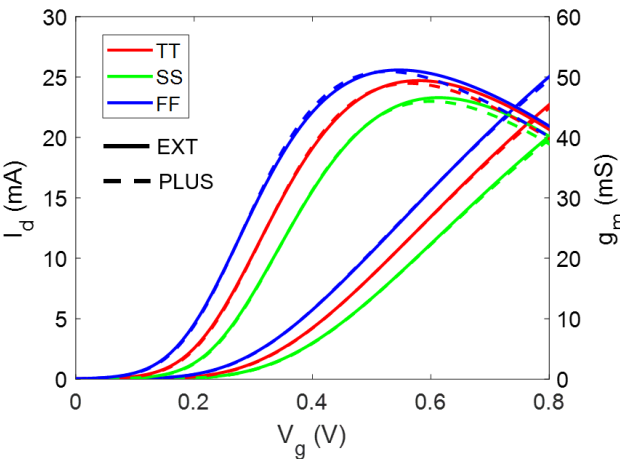


Figure 3.25: Drain current I_d and transconductance g_m vs gate voltage V_g for the different corners in EXT and PLUS PDK in saturation at $V_d = 0.8$ V.

Table 3.3: Comparison of Thermal Resistance Values Across Different Corners for EXT and PLUS PDKs at the Same Overdrive Voltage

	EXT PDK			PLUS PDK		
Corner	TT	FF	SS	TT	FF	SS
R_{th} (K μ m/mW)	137	149	128	186	204	172

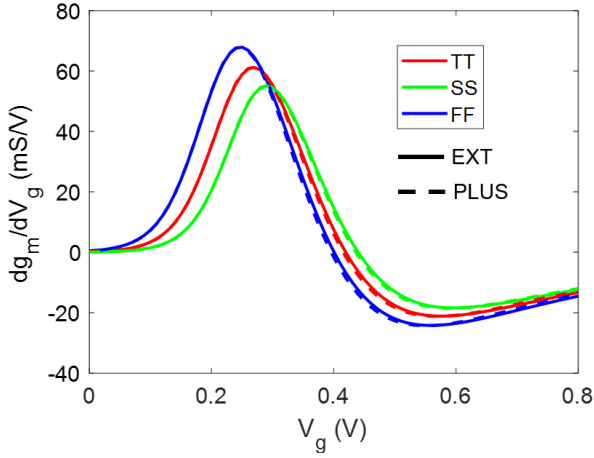


Figure 3.26: Variation of dg_m/dV_g vs gate voltage V_g for the different corners in EXT and PLUS PDK in linear at $V_d = 50$ mV.

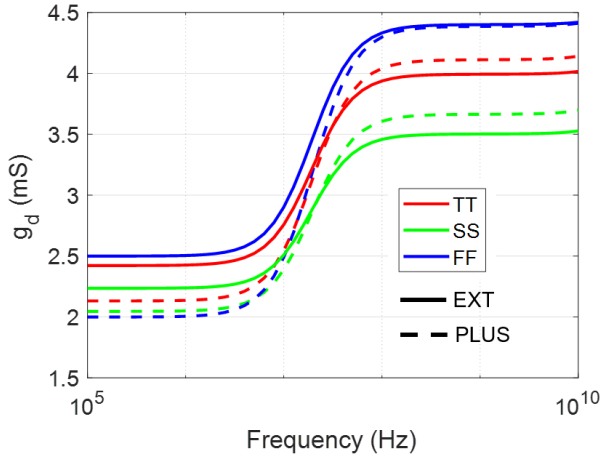


Figure 3.27: Output conductance g_d vs frequency for different corners in EXT and PLUS PDK at $V_{ov} = 0.53$ V and $V_d = 0.8$ V.

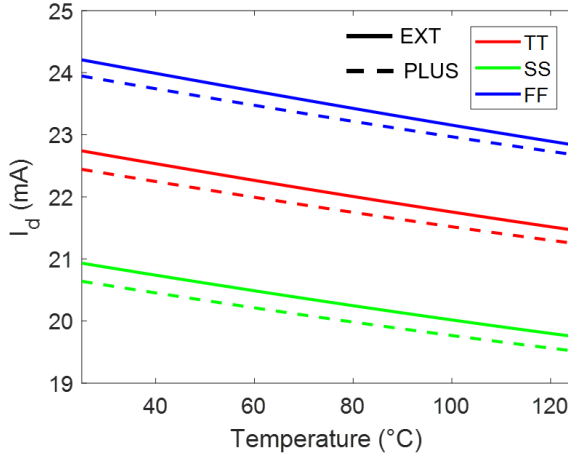


Figure 3.28: Drain current I_d vs temperature in EXT PDK at $V_{ov} = 0.53$ V and $V_d = 0.8$ V.

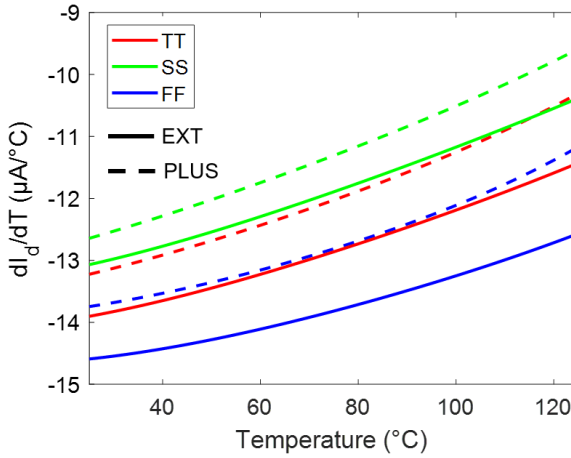


Figure 3.29: Slope of drain current with temperature dI_d/dT in EXT and PLUS PDK at $V_{ov} = 0.53$ V and $V_d = 0.8$ V.

3.7 Thermal Resistance Variation with Temperature

The variation of thermal resistance with ambient temperature is studied in this section. This is particularly important in applications where the device is not working at room temperature, which happens in harsh environments as discussed in **Chapter 2** earlier. Jomaah investigated the impact of temperature on SH from room temperature down to cryogenic liquid Helium temperatures in [102]. A reduction in thermal resistance with temperature was seen; the variation was especially stronger at low temperatures. These trends are backed by a more recent study in 2022 by Ghibaudo [103]. The underlying idea of the variation of material thermal conductivities causing this R_{th} variation is discussed in **Subsection 3.3.2**. It was shown by Triantopoulos in [78] that the thermal conductivity of the BOX mainly dictates the thermal resistance in FDSOI transistors.

In this section, an analysis of the high-temperature impact on device thermal resistance is made through measured data and compared with the PDK model results.

3.7.1 Device Details

The device measured in this study is an NFET in the common source configuration (with source grounded) which originates from the 22 nm FD-SOI technology from GlobalFoundries [21]. The gate length is 20 nm, total width is 30 μm for each of these devices composed of 60 fingers of 0.5 μm finger width. The back-gate MOSFET was grounded for all the experiments ($V_{bg} = 0\text{ V}$).

3.7.2 Measurement Results

The devices were measured using the RF technique for SH characterization at different temperatures. The output conductance g_d versus frequency plot at different temperatures under bias condition $V_g = V_d = 0.8\text{ V}$ is shown below in **Figure 3.30**. An increase in g_d with temperature is observed for this bias condition on all the three dies that were measured.

For the drain current I_d versus temperature plot, an overall linear trend is observed on all three dies and the averaged results measured as seen in **Figure 3.21**. Note that these results are the same which have been discussed in **Subsection 3.5.6** previously. The measurements were made for a temperature range of 25 to 125 $^{\circ}\text{C}$ with 12.5 $^{\circ}\text{C}$ steps to have a finer resolution on the I_d versus temperature response.

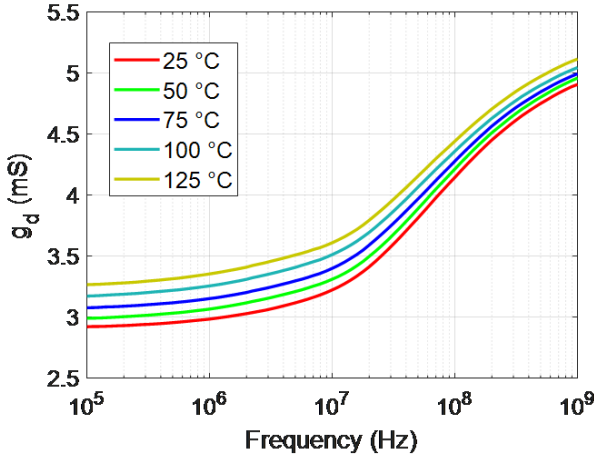


Figure 3.30: Output conductance g_d vs frequency for different temperatures at $V_g = V_d = 0.8$ V.

For the computation of R_{th} from the g_d vs frequency and I_d vs temperature information, **Table 3.4** below summarizes the results taken at $V_g = V_d = 0.8$ V:

Table 3.4: Thermal Resistance Extraction at Different Temperatures.

Temperature (°C)	$g_{d,LF}$ (mS)	$g_{d,HF}$ (mS)	Δg_d (mS)	$\frac{\partial I_d}{\partial T}$ ($\mu A K^{-1}$)	I_d (mA)	R_{th} ($K\mu m/mW$)
25	2.92	4.91	1.53	9.84	22.05	190.9
50	2.99	4.96	1.50	9.84	21.81	189.1
75	3.08	4.99	1.46	9.84	21.55	185.5
100	3.17	5.05	1.42	9.84	21.29	182.0
125	3.27	5.12	1.40	9.84	21.09	180.3

The variation of computed R_{th} over temperature for the three dies is shown in **Table 3.5**. The reduction in R_{th} with temperature trend is established on all the three dies but limited to 6% on temperature increase from 25 to 125 °C.

The percentage R_{th} reduction is 6.8%, 5.55%, and 6.04% over Dies 1, 2, and 3 respectively, and 6.11% on average. We shall now look at the results from the PDK model.

Table 3.5: Thermal Resistance across 3 dies at Different Temperatures.

Temperature (°C)	R_{th} Die1 (K μ m/mW)	R_{th} Die2 (K μ m/mW)	R_{th} Die3 (K μ m/mW)	R_{th} Average (K μ m/mW)
25	194.1	190.9	193.7	192.9
50	191.0	189.1	190.9	190.3
75	188.8	185.5	189.0	187.8
100	183.7	182.0	184.9	183.5
125	180.9	180.3	182.0	181.1

3.7.3 PDK Results

Having established the measured results, we take a look at the results obtained for the same device from the PDK model simulations on both the EXT and PLUS PDK models for 22FDX[®].

EXT and PLUS PDK

In **Figure 3.31** the output conductance versus frequency plot at $V_g = V_d = 0.8$ V in the EXT and PLUS PDK also shows a rising $g_{d,LF}$ with temperature, although the $g_{d,HF}$ is seen to be mostly steady. The corresponding I_d and dI_d/dT vs temperature plot has been shown in **Figure 3.22**, the same as the drain current versus temperature study.

Based on dI_d/dT at the corresponding temperature points, R_{th} at different temperatures is calculated from 25 to 125 °C using the RF technique (refer to **Equation 3.17**) as shown in **Figure 3.32**. A reduction of 5.9% and 7.6% in R_{th} is observed on moving from 25 to 125 °C for the EXT and PLUS PDK respectively.

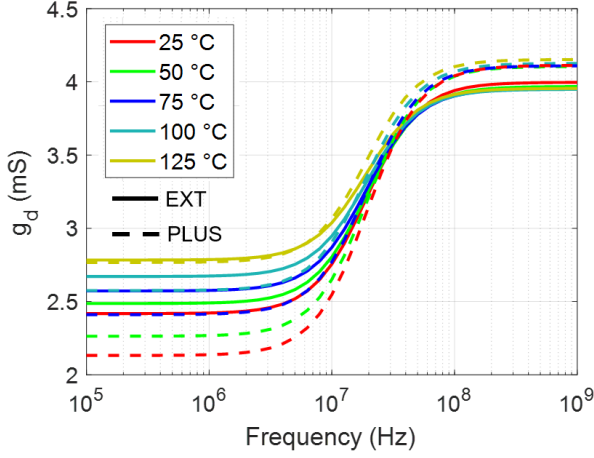


Figure 3.31: Output conductance g_d vs frequency for different temperatures in EXT and PLUS PDK at $V_g = V_d = 0.8$ V.

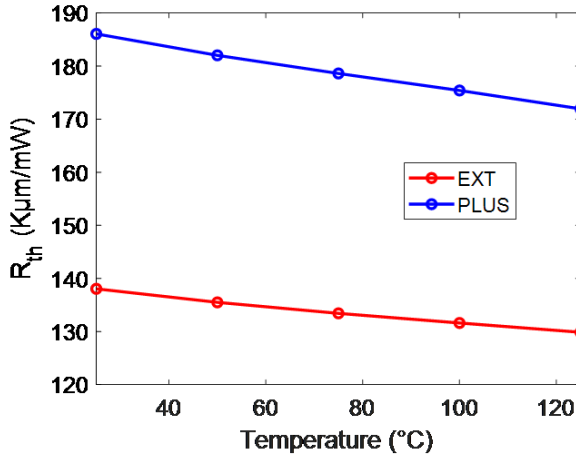


Figure 3.32: Thermal resistance R_{th} variation with temperature in EXT and PLUS PDK at $V_g = V_d = 0.8$ V.

3.7.4 Summary

A reduction of thermal resistance with increasing temperature is observed in measurements; around 6% R_{th} reduction is seen on increasing temperature from 25 to 125 °C. The trends are verified with the results from PDK simulations. In the EXT and PLUS PDK, the corresponding R_{th} reduction is 5.9% and 7.6% respectively. While the extent of R_{th} reduction depends on the dI_d/dT used for extraction, the reducing trends are established in all cases. This is in agreement with studies in literature which demonstrate that the variation of the thermal conductivity of the SiO₂ BOX with temperature causes this trend.

3.8 Gate resistance vs RF technique: A comparative study

Having discussed an overview of the various SH characterization techniques, we shall put our focus on two main ones used by the industry and academics to model the self-heating characteristics of the most advanced MOSFETs, namely the Gate Resistance and the RF technique. In this work, these two characterization methods are applied and compared on the same devices. The strengths and weaknesses of each are discussed and possible reasons for differences of extracted thermal resistance and channel temperature are analyzed.

3.8.1 Device under Test

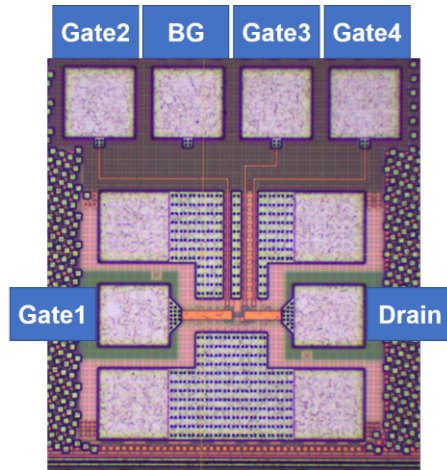


Figure 3.33: Overview of the device layout with the two measurement RF and four DC pads.

The device measured in this study is an NFET in the common source configuration (with source grounded) which originates from the 22 nm FD-SOI technology from GlobalFoundries [21]. The gate length is 20 nm, total width is 30 μm for each of these devices composed of 60 fingers of 0.5 μm finger width. The back-gate MOSFET was grounded for all the experiments ($V_{bg} = 0\text{ V}$). In order to measure the device using the gate resistance technique, special test structures were designed and a 4-terminal (4T) gate access design was made as seen in the design layout in **Figure 3.33**. In addition to the ground-signal-ground (GSG) pads for the RF measurements on gate (left) and drain (right), 4 DC pads on top are used for the additional accesses on the gate for the 4T

method and the back-gate (BG).

3.8.2 Gate Resistance Technique

Methodology

The DC gate resistance technique is one of the primary ways of estimating thermal resistance R_{th} and temperature rise ΔT based on the temperature dependence of the transistor gate resistance. Being first proposed in the 1990s [65] [104], it has stayed in practice due to its simple measurement process [105] [79], which requires neither very complex test devices nor specific test equipment. The layout of our device is made as follows: there are four contacts to the gate, two on each side of the gate finger network as shown in **Figure 3.34**. The resistance of the metallic interconnects from the 4 gate contacts to the corresponding pads is represented as R_{Metal} . The contacts closest to the core gate resistance R_{Gate} , (namely Gate1 and Gate3 here) are used for voltage sensing whereas the outer two (Gate2 and Gate4 here) are used for forcing the current as illustrated in the schematic representation in **Figure 3.35**. In the 4-terminal method, the current and voltage electrodes are separated; this implies that the sourcing current flows only through the sourcing path and no current flows through the voltage sensing path. Therefore, there is no voltage drop across the resistances in the voltage sensing paths (namely R_{Metal1} and R_{Metal3}) and thus the voltage drop measured across the voltage sensing pads (Gate1 and Gate3) is equal to that actually across the R_{Gate} . This allows accurate extraction of the gate resistance.

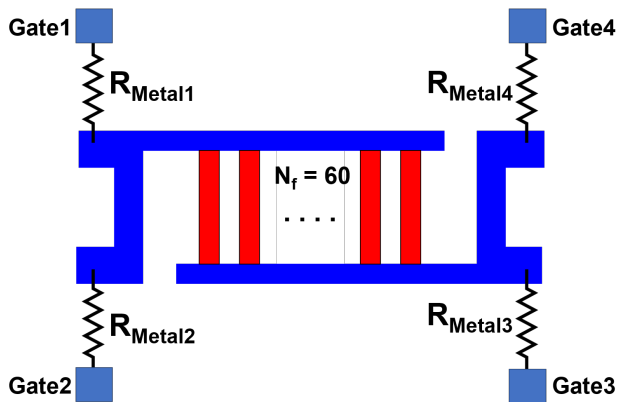


Figure 3.34: Layout the gate fingers of the core FET and the 4T gate accesses.

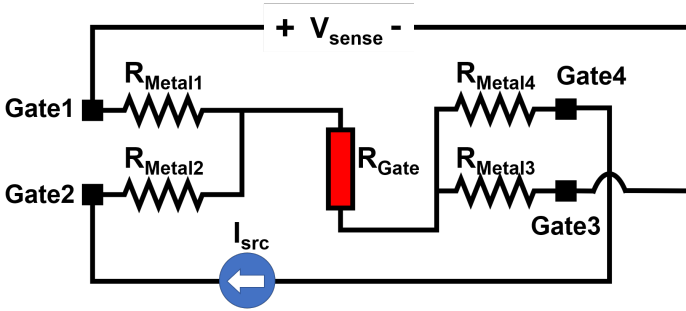


Figure 3.35: Schematic of 4-terminal gate resistance technique.

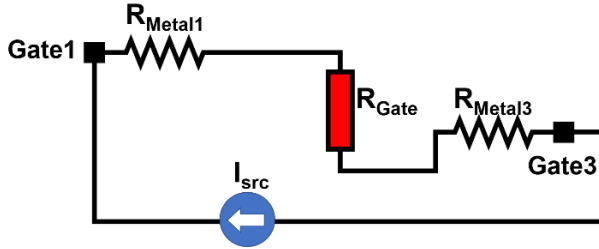


Figure 3.36: Schematic of 2-terminal gate resistance technique.

On the other hand, if a 2-terminal technique were used for this computation as shown in **Figure 3.36**, the metallic resistances would need to be extracted accurately and removed to precisely obtain the actual gate resistance R_{Gate} . It is essential to try to extract R_{Gate} as accurately as possible as the TCR of the gate material is different from that of the metals used for the accesses. The forced current I_{src} would flow through access resistances (R_{Metal1} and R_{Metal3} in this example), and the voltage sensed (across Gate1 and Gate3) would not be equal to that across R_{Gate} . To do so, de-embedding structures would be required. Furthermore, it is observed that measuring the resistance using this technique is also dependent on the probe contact to a certain extent and thus accuracy of this extraction method is also not as good as the 4T method. All these reasons mentioned above highlight the importance of using the 4-terminal technique for gate resistance measurement compared to the simpler 2-terminal method from a measurement accuracy point of view. In cases where the usage of the 2T resistance method is unavoidable, for example, to prevent cooling from gate contacts [106], one needs to be aware of these necessary challenges and

address them well for the sake of measurement accuracy. Alternatively, one disadvantage of the 4T technique would be the cooling which could happen through the gate contacts, this has been studied later in [Section 3.10](#).

Experimental Results

In addition to the standard biases on the gate and the drain using a B2902A, additional Keithley 2400 SMUs were used to compute the DC gate resistance. As the first step, the device was kept off ($V_d = V_g = 0$ V) and the gate resistance was measured at different chuck temperatures varied from 25 to 125 °C. This allowed for obtaining the temperature dependence of the gate resistance (or one can say perform a calibration). The system was kept to steady for around 30 minutes at each new temperature point to ensure temperature stability. Then, in the second step, the device is measured at room temperature at various bias conditions and the gate resistance featured by the device at these conditions is extracted. The value obtained in the second step is correlated to the temperature in the first step giving the device temperature. R_{th} refers to the resistance to heat flow and is linked to the temperature rise ΔT and power P as:

$$\Delta T = R_{th} \cdot P \quad (3.21)$$

$$P = I_d \cdot V_d \quad (3.22)$$

Choosing a suitable forcing current I_{src} is an important aspect of the measurement procedure. The drop in voltage V_{sense} across R_{Gate} is directly proportional to I_{src} following Ohm's law; therefore the higher the I_{src} , the more perceivable the drop and more accurate estimation of R_{Gate} as at very low values of I_{src} this drop might not be estimated accurately. However, if I_{src} is too high, (i) it itself generates heat in the R_{Gate} , (ii) a high voltage drop across the gate would mean an uneven biasing of the gate fingers. Both of the above are undesirable as the objective of the forcing current I_{src} is just to have a way of measuring R_{Gate} while affecting the working of the MOSFET or the thermal environment to the least possible extent. A tradeoff is therefore seen and the choice of an optimal value of I_{src} . From [Table 3.6](#), we observe that having a sourcing current of 100 - 200 μ A gives a good range for voltage sensing with a voltage drop of around 5 - 10 mV. For values of I_{src} lesser than or equal to 1 μ A, the voltage difference sensed is too small to be accurately perceived by the measuring instrument.

Table 3.6: Variation of Sensing Voltage with Forcing Current for $V_g = V_d = 0\text{ V}$.

$I_{\text{src}}(\mu\text{A})$	$V_{\text{sense}}(\text{mV})$
1	Too small to be sensed by instrument
10	0.5
50	2.5
100	4.99
200	10.2
500	25.5

Figure 3.37 shows the gate resistance versus temperature when the device is off. Using the information obtained from the above, we obtain the gate resistance versus temperature characteristic, allowing us to estimate the temperature coefficient of resistance (TCR) using a linear regression over all the temperature points. Measured results for three different dies are shown here. The TCR is observed to be roughly $0.07\text{ }\Omega/^{\circ}\text{C}$ for all the dies. The information of the TCR and the resistance at room temperature then enables us to estimate the device temperature (under operation) from a given gate resistance by extrapolation.

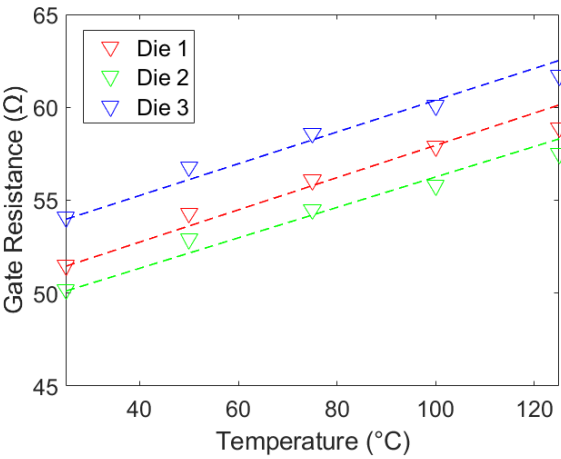


Figure 3.37: DC Gate Resistance vs temperature when device is off made for TCR calibration.

The device is then turned on by biasing it with the desired V_d and V_g respectively with the chuck brought back to room temperature. The gate resistance

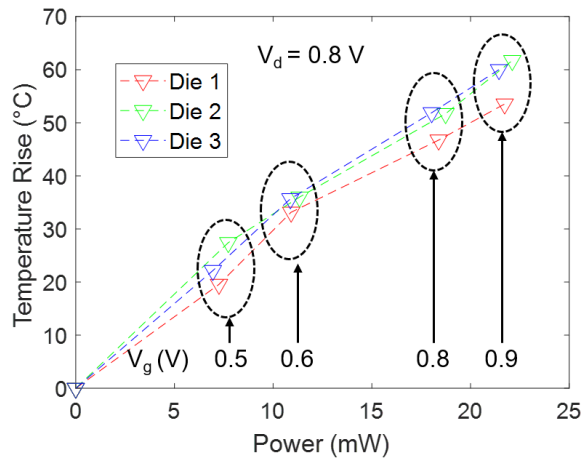


Figure 3.38: Temperature rise versus power for different V_g at $V_d = 0.8$ V.

Table 3.7: Thermal Resistance Using 4T Gate Resistance Technique at Different V_G Biases for $V_d = 0.8$ V.

Gate bias condition (V)	Gate temperature ($^{\circ}\text{C}$)	R_{th} ($\text{K}\mu\text{m}/\text{mW}$)
0.5	47.2	95.7
0.6	60.7	98.4
0.8	76.9	86.3
0.9	85	84

is then measured at each bias point and the gate temperature is estimated from the TCR found out before. **Figure 3.38** shows the device temperature rise (with respect to room temperature) under different bias conditions of gate voltage V_g varying from 0.5 to 0.9 V at a given drain voltage V_d of 0.8 V (and thereby different power levels as due to different drain current I_d for each bias condition).

Table 3.7 shows the estimated gate temperature and the corresponding R_{th} for the aforementioned bias conditions. The mean R_{th} is $91 \text{ K}\mu\text{m}/\text{mW}$ obtained over the bias range considered.

As the extracted thermal resistance is directly related to the accuracy of extraction of the gate temperature and the power dissipated, estimation at lower biases can be more error-prone. This is because the actual gate temperature is

lower because of less heating at lower biases: small errors in gate temperature estimation affect the extraction to a greater extent in such cases.

Variability and Error Bars of Extraction

The estimated results of R_{gate} versus temperature over the three dies have been shown in **Figure 3.37**. Additionally, the impact of the extraction of the TCR is investigated further. It is seen that the R_{gate} versus temperature plot is not perfectly linear: on all the dies measured, the slope at lower temperatures is systematically steeper than that at higher temperatures. This is demonstrated by comparing the slope of R_{gate} between the first temperature point (25 °C in our case) with the second (50 °C), third (75 °C), fourth (100 °C), and fifth (125 °C) temperature points respectively (shown in **Tables 3.8, 3.9, 3.10**). This has an important impact on the estimated R_{th} : by estimating R_{th} from the highest slope (1st - 2nd point) compared to the lowest slope (1st - 5th point), an R_{th} reduction of 20 - 30% is observed. The sensitivity of the extracted R_{th} on the TCR and the Y-intercept of the R_{gate} versus temperature plot is evident.

Table 3.8: TCR Results and R_{th} for Die1

Die1	Slope 1 st -5 th point	Slope 1 st -4 th point	Slope 1 st -3 rd point	Slope 1 st -2 nd point
TCR ($\Omega/^{\circ}\text{C}$)	0.074	0.0853	0.092	0.112
Y-intercept (Ω)	50.22	49.367	49.2	48.7
R_{th} (Kum/mW)	75.64	76.53	70.95	58.28

Table 3.9: TCR Results and R_{th} for Die2

Die2	Slope 1 st -5 th point	Slope 1 st -4 th point	Slope 1 st -3 rd point	Slope 1 st -2 nd point
TCR ($\Omega/^{\circ}\text{C}$)	0.073	0.0747	0.086	0.108
Y-intercept (Ω)	48.375	48.33	48.05	47.5
R_{th} (Kum/mW)	89.93	87.94	76.34	60.79

Table 3.10: TCR Results and R_{th} for Die3

Die3	Slope 1 st -5 th point	Slope 1 st -4 th point	Slope 1 st -3 rd point	Slope 1 st -2 nd point
TCR ($\Omega/^{\circ}\text{C}$)	0.076	0.08	0.09	0.108
Y-intercept (Ω)	52.2	52.1	51.85	51.4
R_{th} (Kum/mW)	94.13	89.42	79.49	66.24

3.8.3 RF Technique

With the methodology of the RF technique described previously in **Subsection 3.5.4**, the experimental findings are demonstrated here.

Experimental Results

In this work, for the RF characterization, S-parameters are measured in a frequency range from 100 kHz to 1 GHz and converted to Y parameters with dedicated open de-embedding structures. The measurements are made on an MPI TS3000-SE probe station, with the general characterization flow and high-temperature measurement aspects already discussed in **Section 2.2 of Chapter 2**. A Keysight PNA N5291A vector network analyzer and two RF $|Z|$ probes of 100 μm pitch are used for these measurements. The RF $|Z|$ probes are compatible for high-temperature measurements that shall be required for DC measurements at higher temperatures to compute I_d versus temperature slope which is essential for estimating R_{th} . DC biasing of the gate and drain is done using biasing instrument B2902A. Bias tees are used to combine the aforementioned DC bias and the RF cables to connect to the VNA. SOLT (Short-Open-Load-Thru) method is used for calibration at room temperature. For temperature measurements, the devices are measured at 25, 50, 75, 100 and 125 $^{\circ}\text{C}$, respectively. In order to have a steady temperature value while measuring, the whole system was let to steady for at least half an hour.

Figure 3.39 shows the extracted output conductance g_d versus frequency plot at V_g and V_d of 0.8 V. The transition in g_d as we go from lower to higher frequencies is clearly observed and this is the basis of the estimation of thermal resistance R_{th} . The impact of the substrate effect on the g_d transition can be visualized from the curves with V_g below the ZTC (V_g 0.4 and 0.5 V). While SH pushes down the g_d transition in these cases resulting in a monotonically decreasing plot up to around 30 MHz, the onset of substrate effect from that range is seen to push the transition upwards. In our devices, it was observed that

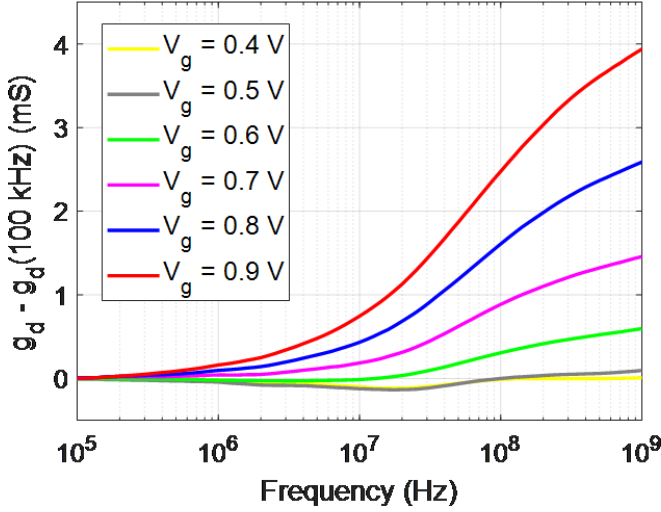


Figure 3.39: Output conductance g_d vs frequency for different V_g biases at $V_d = 0.8$ V.

the ZTC point appears at V_g 0.6 V and thus the amplitude of the g_d transition at that bias point was subtracted from the given case above to obtain the corrected g_d transition. The fact that the transition in g_d with frequency is related to the substrate and back-gate network is verified by the presence of a g_d transition at the ZTC point.

Figure 3.40 shows the variation of drain current I_d with temperature at different V_g biases, including that of the ZTC. The increase in I_d with temperature due to threshold voltage reduction for V_g biases below ZTC and the decrease in I_d with temperature above the ZTC due to mobility degradation at biases above the ZTC is evident. The slope of I_d versus T is used for the calculation of R_{th} . Note that at the ZTC ($V_g = 0.6$ V in our case), as I_d is invariant with temperature, the slope tends to zero, resulting in a very high value of R_{th} from **Equation 3.17**. Therefore, computation of R_{th} using the RF technique cannot be done close to the ZTC and it is noted in [98] that the extraction accuracy of R_{th} is best at higher V_g biases in saturation.

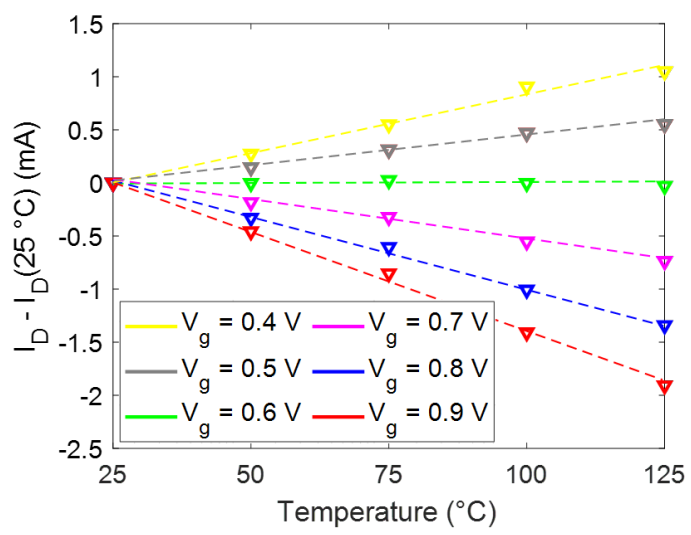


Figure 3.40: Drain current I_d vs temperature for different V_g biases at $V_d = 0.8$ V. The variations above and below ZTC of $V_g = 0.6$ V are seen.

Table 3.11: Thermal Resistance Using RF Technique at Different V_g Biases for $V_d = 0.8$ V.

Bias Condition	R_{th} without Substrate Effect Correction (Kμm/mW)	R_{th} with Substrate Effect Correction (Kμm/mW)
$V_g = 0.8\text{ V}$	221	163
$V_g = 0.9\text{ V}$	204	168

Results over Multiple Dies

The results shown have been verified over multiple dies and the results for two different bias conditions in saturation are shown below. **Table 3.12** and **Table 3.13** show the extracted results in saturation at $V_d = 0.8$ V and V_g of 0.8 V and 0.9 V, respectively. While desirable trends are obtained over all three dies, the variability across them is also as low as 4%.

Table 3.12: Thermal Resistance of 4T FET for Different Dies at $V_g = V_d = 0.8$ V.

Die	$g_{d,LF}$ (mS)	Δg_d (mS)	$\frac{\partial I_d}{\partial T}$ ($\mu\text{A K}^{-1}$)	I_d (mA)	R_{th} ($\text{K}\mu\text{m}/\text{mW}$)	ΔT ($^{\circ}\text{C}$)
Die1	3.52	1.83	-12.87	23.38	162.8	101.5
Die2	3.85	1.98	-13.44	23.95	163.5	104.4
Die3	3.46	1.69	-12.11	22.70	164.4	99.5

Table 3.13: Thermal Resistance of 4T FET for Different Dies at $V_g = 0.9$ V, $V_d = 0.8$ V.

Die	$g_{d,LF}$ (mS)	Δg_d (mS)	$\frac{\partial I_d}{\partial T}$ ($\mu\text{A K}^{-1}$)	I_d (mA)	R_{th} ($\text{K}\mu\text{m}/\text{mW}$)	ΔT ($^{\circ}\text{C}$)
Die1	4.25	3.10	18.08	27.59	166	122.1
Die2	4.70	3.26	19.07	28.16	160.7	120.6
Die3	4.25	2.94	17.30	26.90	168.3	120.7

Specifically, the trends on drain current versus temperature are demonstrated as an accurate estimation of dI_d/dT is important for the R_{th} extraction. The I_d vs temperature plots on three dies at $V_d = 0.8$ V and V_g biases of 0.8 and 0.9 V each are shown in **Figure 3.41**. Over the three dies, the averaged I_d vs temperature plot is seen in **Figure 3.42** for two different V_g biases. A good linear trend is established on all the dies.

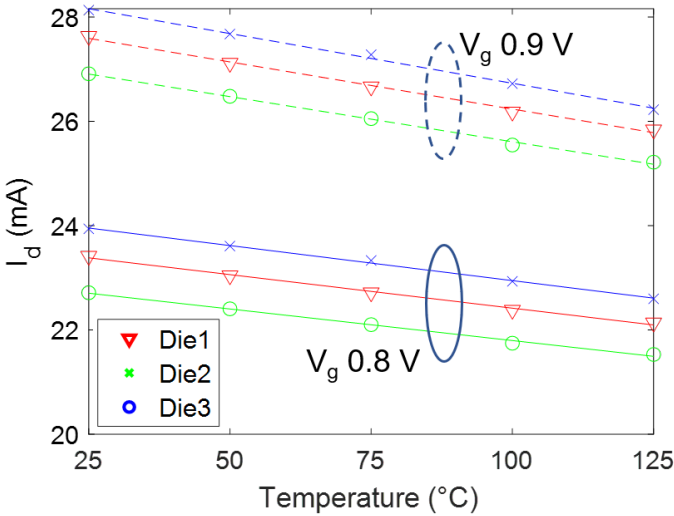


Figure 3.41: Drain current I_d vs temperature for $V_g = 0.8\text{ V}$ at $V_d = 0.8\text{ V}$.

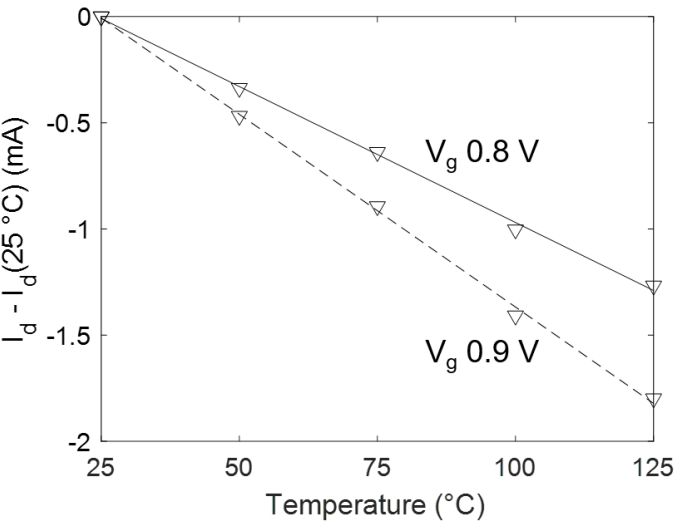


Figure 3.42: Averaged drain current I_d vs temperature over the measured dies for $V_g = 0.8, 0.9\text{ V}$ at $V_d = 0.8\text{ V}$.

3.8.4 Comparison of EXT and PLUS PDK

There are two different 22FDX[®] PDKs, namely EXT and PLUS, that model self-heating based on two different techniques. The EXT PDK uses the gate-resistance technique while the PLUS PDK uses the AC conductance technique. With the AC conductance technique having a similar methodology as the RF technique, comparing the same device on these two PDKs would give us an idea of the difference between the gate-resistance and RF techniques.

PDK Results

The device considered is the same as the one in our measurements: the gate length is 20 nm, and the total width is 30 μm for each device composed of 60 fingers, each finger having a width of 0.5 μm . On both the PDKs, the RF technique method is used to estimate the thermal resistance as in [Equation 3.17](#). The detailed PDK results on the two PDKs have been shown in [Subsection 3.7.3](#).

Computed at $V_g = V_d = 0.8\text{ V}$, around 1.34 times higher R_{th} is seen with the PLUS PDK compared to the EXT PDK, highlighting the R_{th} difference estimation from the techniques. $R_{th}\text{ EXT} = 138.05\text{ K}\mu\text{m/mW}$ and $R_{th}\text{ PLUS} : 186.07\text{ K}\mu\text{m/mW}$. The values obtained are shown below in [Table 3.14](#).

Table 3.14: R_{th} on EXT and PLUS PDKs.

PDK	$g_{d,LF}$ (mS)	$g_{d,HF}$ (mS)	Δg_d (mS)	$\frac{\partial I_d}{\partial T}$ ($\mu\text{A K}^{-1}$)	I_d (mA)	R_{th} ($\text{K}\mu\text{m/mW}$)	ΔT ($^{\circ}\text{C}$)
EXT	2.42	4.00	1.58	13.90	22.74	138	84
PLUS	2.13	4.11	1.98	13.22	22.44	186	111

Based on the study on R_{th} versus temperature on both the PDKs, a systematically higher R_{th} was observed for the PLUS PDK at different temperature points ranging from 25 to 125 $^{\circ}\text{C}$ (seen in [Figure 3.32](#) previously).

These results clearly show the difference in SH estimation using the gate-resistance and the RF techniques. An in-depth study of the quantitative difference between the cases is reserved for future works.

3.9 Discussion

3.9.1 4T Gate Resistance vs RF Technique

Table 3.15: Comparison Between Gate Resistance and RF Techniques

	Gate Resistance Tech- nique	RF Technique
Ideology	Measure the gate temperature and assumes the gate temperature to be equal to the channel temperature	Extract the thermal resistance and capacitance of the transistor after removing the dynamic self-heating effects
Simplicity of Use	Classical DC measurement setup	RF measurement setup needed
Test Structures	Special test structures with multiple contacts to the gate electrode needed	RF pads, de-embedding structures needed
Accuracy	Can be used to measure R_{th} at any bias but extractions are more sensitive at lower biases	Extraction of R_{th} around ZTC is inaccurate. Extraction of $\frac{dI_d}{dT}$ can be tricky
SH parameters measured	Can only measure thermal resistance	Can measure both thermal resistance and capacitance

Various aspects, advantages, and disadvantages of the two techniques are summarized in **Table 3.15**. We now come to a quantitative comparison of the results obtained from these two techniques. In this work, the R_{th} obtained using the RF technique of around 166 K μ m/mW is around 1.8 times that obtained using the 4T Gate resistance technique (91 K μ m/mW. This stark difference is clearly observed in this study and has also been verified by comparing results from other works in literature, as described below.

Results from Literature

In order to position the values obtained in this study quantitatively, a comparison with numbers obtained from literature is made. In [105], Takahashi demonstrated an expected thermal resistance (R_{th}) for a 21 nm BOX device of around 60 K μ m/mW for a channel length (L) of 20 nm, predicted from the

reduction of R_{th} with scaling. This is seen in **Figure 3.43**. Note that the BOX thickness is 20 nm in 22FDX[®], this can be used as the reference for comparison. The same observation is noted from the impact of BOX thinning on R_{th} in [84], where a 20 nm BOX is expected to give a R_{th} of 50 – 60 K μ m/mW for $L = 50$ nm. In [103], the R_{th} using the GR for an FDSOI MOSFET ($W = 10 \mu$ m, $L = 50$ nm, $T_{Si} = 11$ nm, and $T_{BOX} = 145$ nm) was approximately 100 K μ m/mW, in agreement with [105] and [84].

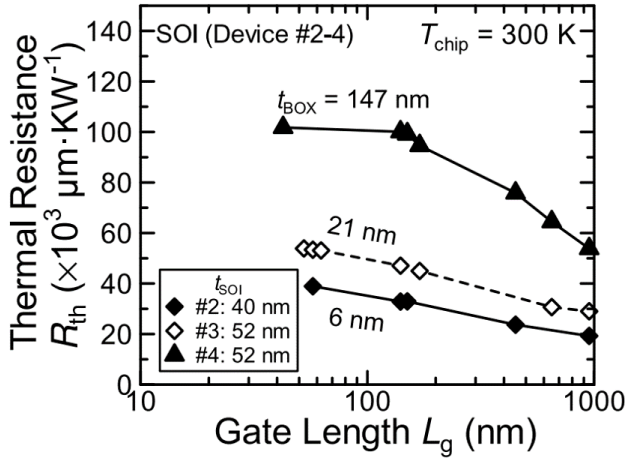


Figure 3.43: R_{th} as a function of L_g for SOI MOSFETs with a t_{BOX} of 6, 21, and 147 nm in [105]. Channel thickness t_{SOI} was approximately 50 nm.

Overall, the R_{th} values of around 80-90 K μ m/mW obtained in our measurements seem to be in the expected range as estimated from literature.

To compare the difference between techniques better too, a comparison is made with respect to bulk technology. Using the RF technique in [81] in 28 nm gate length devices, the thermal resistance was measured to be 143 K μ m/mW for FDSOI compared to 42 K μ m/mW for bulk devices. It was seen in [105], that the R_{th} for a bulk device is expected to be around 24 K μ m/mW based on the scaling trends.

In [47], a comparison of the R_{th} obtained by the two methods was made on PD-SOI technology with two different substrates (RFeSi80 and RFeSi90) with different BOX thicknesses. In both cases, a higher R_{th} was reported for the RF technique for various gate lengths as seen in **Figure 3.44**, underlying the same findings observed from our measurements in this work. The R_{th} ratio

of around 1.6 to 1.8 times for the RF technique was obtained compared with the gate resistance technique in accordance with the results seen in this current work.

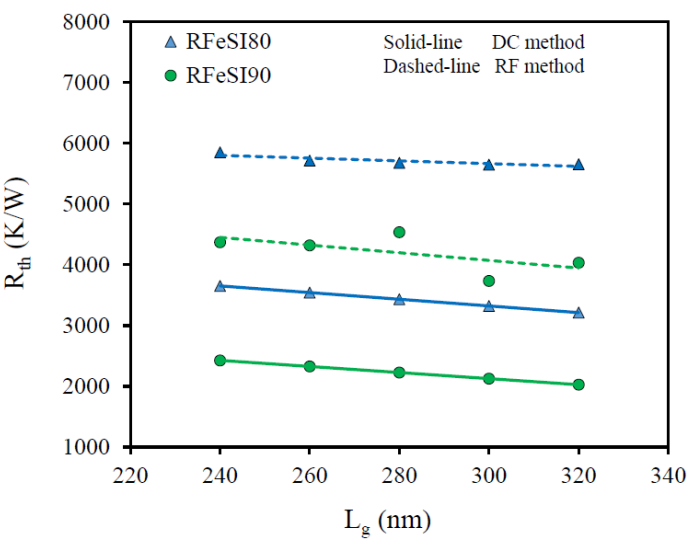


Figure 3.44: R_{th} extracted from gate-resistance and RF technique in [47].

Comparing the references above, a stark difference between the thermal resistance obtained from the gate-resistance and RF techniques on both bulk and FDSOI devices is confirmed.

Table 3.16: Comparison of R_{th} using Gate Resistance and RF Technique from [105] and [81] respectively

Technique	R_{th} in Bulk ($K\mu m/mW$)	R_{th} in FDSOI ($K\mu m/mW$)
Gate Resistance [105]	24	58
RF [81]	43	143

3.9.2 Reasons of Difference in the Techniques

The difference in thermal resistance obtained from the RF technique and the Gate Resistance technique results in a difference in the channel temperature and the gate temperature. From our measurements, under bias conditions $V_d = V_g = 0.8$ V, the corresponding temperatures at channel and gate estimated from the RF technique and the gate-resistance technique are 124 °C and 79 °C respectively, resulting in a drop of 45 °C. To assess this, we reconsider the main assumption of the Gate Resistance technique: the fact that the channel temperature is equal to that of the gate temperature. This general assumption had historically stemmed from the fact that the gate oxide is very thin and that there is good thermal coupling between the gate and the channel [104]. However, it has to be kept in mind that in advanced MOSFETs, while the equivalent oxide thickness (EOT) of the gate oxide is low, the physical thickness itself of the oxide layer is higher for high-K dielectrics used in these devices. Additionally, the gate stack is a complex entity consisting of multiple films and the thermal boundary resistance (TBR) between these films can play a significant role in determining/deteriorating the overall thermal resistance of the stack [107]. Due to the aforementioned factors, even for very thin gate oxides, the thermal resistance is not necessarily negligible. A comparison from [107] shows that thinning the Hafnium oxide from 20 nm to as low as 1 nm only manages to reduce the R_{th} by half, showing the impact the boundary resistance has in thin film materials.

In order to make a qualitative analysis of the thermal problem, we attempt to estimate the heat evacuation through the gate path. The temperature drop across the gate stack is the product of the gate stack's thermal resistance and the power dissipated through the gate path. Assuming that the channel temperature is that estimated from the RF technique and the gate temperature is that estimated from the gate resistance technique, the necessary conditions that would cause such a temperature drop across the gate are analyzed. **Figure 3.45** shows an equivalent lumped element model of this thermal problem around the gate stack region. Recalling that a temperature drop of 45 °C is observed between the gate and channel from measurements, the conditions for the same happening are looked into. For the three different gate stack R_{th} conditions representing the lowest to highest bounds, the percentage of total power that needs to be dissipated through the gate region is calculated for this temperature drop across the gate. This can be seen from **Table 3.17**.

While an accurate thermal model would require knowledge of the exact

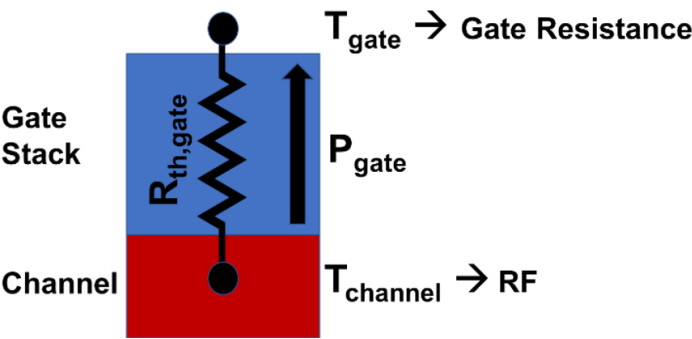


Figure 3.45: Temperature of gate and channel and the electrical representation of the thermal equivalent.

Table 3.17: Percentage of Total Power to be Dissipated Through Gate Stack for Temperature Drop Corresponding to Difference in RF and Gate Resistance Techniques for Different Gate Stack Resistance Bounds.

Thickness	1 nm (Lowest Bound)	10 nm	20 nm (Highest Bound)
R_{th} (KW ⁻¹)	16,700	21,700	33,300
P_{Gate}/P (%)	14.97	11.52	7.57

materials, thicknesses, boundaries, and geometries, a first-order qualitative analysis is made to assess the feasibility of the power dissipation through the gate path compared to the others. These aforementioned aspects of thermal analytical modelling has been elaborated in [Appendix A](#). In general, the thermal conductivity of thick film HfO₂ is around 1.2 Wm⁻¹K⁻¹ compared to 1.4 Wm⁻¹K⁻¹ for SiO₂, so both are similar from a thermal perspective [72]. The thermal resistance of the 20 nm thick BOX is thus also 33000 K/W for our device dimensions. This fact clearly brings into perspective that the gate stack thermal resistance is expected to be much lesser than that of the BOX because it should be geometrically much thinner. This makes the prospect of having the percentage heat evacuation through the gate path to facilitate the temperature drop listed in [Table 3.17](#) quite possible. For the source (drain) region, lack of precise knowledge of the raised source (drain) region prevents having reliable numbers and therefore the gate path and BOX-substrate path are the ones primarily compared here. Overall, from the primary numerical analysis above,

the possibility of heat dissipation through the gate path is established. The fact that cooling can happen through the gate region has also been verified experimentally in literature [108] [109] [110] and also stated in [105] [106], which shall be the subject of the next discussions in **Section 3.10** and **Chapter 4**. All the above points showcase a corresponding temperature drop across the gate stack thereby negating the assumption that the gate temperature and channel temperature are equal.

3.9.3 Shortcomings of the Techniques

In the course of the work, various shortcomings of both the gate resistance and the RF techniques are observed.

Gate Resistance Technique

Firstly, to find the temperature coefficient of measurements, the chuck is heated to a desired temperature to estimate the gate resistance. This means that the whole device is heated up uniformly to that temperature for the computation. However, while estimating the gate resistance due to local self-heating, just the channel region is heated up from SH. Especially for multifinger devices, this would mean that the whole gate is not at a uniform temperature with a hot-spot expected somewhere. As the two cases are not exactly the same, correlating the two remains a shortcoming of the technique.

Secondly, the absolute values of the gate resistance and the TCR play an important role in the accuracy of extraction; higher values help in estimating thermal parameters better. In our work, the gate resistance at room temperature was around $50\ \Omega$ and the TCR obtained was around $0.07\text{--}0.1\ \Omega/^{\circ}\text{C}$ range and these values are compared with some others in literature. In Tenbroek [24], a gate resistance value at room temperature of around $220\ \Omega$ and a TCR of around $0.14\ \Omega/^{\circ}\text{C}$ was observed. While the absolute value of R_{gate} was not mentioned in [105], a percentage R_{gate} increase of around 25% was reported, in contrast to around 15% increase seen in our work over the same temperature range. In both the above cases, having a gate material that has a greater dependence of R_{gate} with temperature helps extraction accuracy further.

Additionally, the variation of gate resistance with temperature is often assumed to be linear. However, studies such as [105] and [79] indicate that the temperature dependence of the resistance of a conventional polysilicon gate can be nonlinear (although with an opposite trend where R_{gate} decreases with temperature), whereas the partially nickel-silicided polysilicon gate in [105] is observed to have a linear dependence (shown in **Figure 3.46**). Therefore, the overall gate resistance versus temperature trend depends on the type of gate material used. In our study, we clearly observe that the R_{gate} vs. temperature trend shows a steeper slope at lower temperatures across multiple measurements, indicating the possibility of a nonlinear trend. The importance of accurately extracting the slope is underscored by the fact that the extracted thermal resistance (R_{th}) can decrease by up to 30% when the slope at lower temperature points is considered, compared to higher temperature points. Further studies on this

topic, in collaboration with GlobalFoundries, are required to explore this aspect in greater depth.

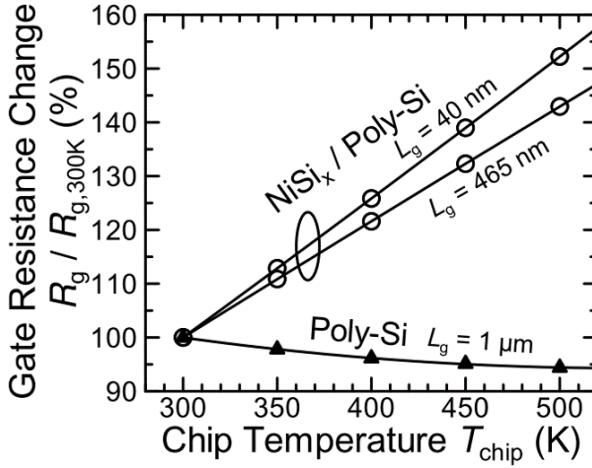


Figure 3.46: Gate Resistance vs chip temperature T_{chip} dependence of change in R_{gate} for typical devices used in [105] and conventional polysilicon gate electrode.

RF Technique

The I_d versus temperature behaviour is seen to be a crucial aspect of R_{th} extraction using the RF technique. The estimation of the slope is seen to affect the results and detailed studies on the exact trends need to be carried out. Additionally, if the trend is nonlinear, the fact that dI_d/dT varies with temperature makes it important to see the impact of these variations on estimated R_{th} .

In all studies utilizing the RF technique in the literature reviewed, the derivative dI_d/dT is typically assumed to be the linear slope of I_d with respect to temperature across a specific temperature range. It is important to note that this linear relationship is based on experimental measurements. Establishing a reliable linear I_d trend can be challenging due to the inherent variability in characterization, which is why a linear fit is often employed to extract dI_d/dT .

However, when examining the Process Design Kit (PDK) results, a nonlinear relationship between I_d and temperature is observed, indicating that dI_d/dT is not constant but varies with temperature. This variation implies that the thermal resistance (R_{th}) extracted from the data can differ significantly depending

on the temperature at which the slope is determined, unlike the case where the trend is linear. For instance, calculating dI_d/dT at 125 °C results in an R_{th} value approximately 25% higher than that obtained by taking dI_d/dT at 25 °C.

Despite the potential impact of this variation, there has been no comprehensive study in the literature addressing how inaccuracies in extracting I_d versus temperature data can affect the extracted R_{th} . This work aims to fill that gap by investigating the effect of such inaccuracies, with a comparison to trends observed in PDK models. While it is exceedingly difficult to establish a clear nonlinear trend, applying a nonlinear fit similar to that used in the PDK to our measurements shows that the nonlinear fit does not deviate significantly from a linear fit. A thorough investigation into this phenomenon would provide valuable insights and help correlate experimental measurements with model predictions and physical effects.

3.9.4 Summary

Two prominent self-heating characterization techniques, the gate-resistance technique and the RF technique are studied and compared in this section using MOSFETs in 22 nm FDSOI technology. The advantages and drawbacks of the 4T gate resistance and RF techniques are discussed qualitatively. From a quantitative analysis of characterized results on the same test device, it is found that the RF technique shows around 1.8 times as high thermal resistance as the value extracted from the gate-resistance technique. The assumption of the gate-resistance method that the channel temperature is equal to the gate temperature is brought into doubt from the difference in channel temperature value extracted by these two methods. This reinstates the fact there could be a considerable impact of the thermal insulation provided by the complex gate stack, with thermal boundary resistances between the different layers in the stack playing a role in causing a temperature drop across it. On the other hand, for the RF technique, an accurate estimation of the drain current versus temperature slope is necessary for an accurate estimation of thermal parameters.

3.10 Impact of Device Layout on Self-heating Extraction

Having looked into the pros and cons of the gate-resistance and RF techniques for SH characterization, we build further by studying layout-related impacts on SH characterization. SH parameters (thermal resistance R_{th} and channel temperature rise ΔT) extracted using characterization techniques are often compared and the difference is attributed to the inner device features itself. However, one needs to pay attention to the fact that device configuration has an important impact on the extracted features not only due to differences in the inner device configuration (and thus heating and heat evacuation) but also due to different parasitic elements and heat evacuation paths. In this work, we demonstrate this based on experimental data for four-terminal (4T) gate access (used for gate resistance technique) FET, complemented by PDK simulations of series resistance effect. This work, currently accepted as an abstract for publication, analyses the impact of device layout on SH extraction and treats it in terms of parasitic series resistance and heat evacuation.

3.10.1 Device under Test

The core FET is an nFET with total width $30\mu m$ based on 22FDX® [19]. **Figure 3.33** shows the layout of the 4T RF test structure (with additional DC pads/accesses to the gate) which allows the application of both gate resistance and RF techniques to the same device; it is the same device used in **Subsection 3.8.1**. The thermal attributes of this device are compared with a standard version of the RF device without the additional DC contacts.

3.10.2 Experimental results and Discussion

The RF technique is used for SH characterization on both the devices, with and without 4T gate accesses. The experimental setup used is the same as the one used in [Subsection 3.8.3](#) on the MPI probe station utilizing high-temperature measurements in a way described in [Section 2.2](#) of [Chapter 2](#).

The DC characteristics of the devices with 4T additional gate terminals and without them (labelled “4T” and “no 4T”, respectively) are similar in terms of threshold voltage ([Figures 3.47 and 3.48](#)), allowing for a direct comparison of their SH features. Additionally, from the above figures the fact that I_d between the two cases becomes similar in saturation (where SH becomes stronger) compared to linear (where SH is almost absent) shows the effect of heat evacuation from accesses coming into play.

[Figure 3.49](#) shows the variation of g_d with frequency (after open de-embedding) and [Figure 3.50](#) shows I_d versus temperature for these FETs. A higher value of g_d and higher absolute value of $\frac{\partial I_d}{\partial T}$ obtained for the “4T” FET suggest that it is less affected by SH compared to the “no-4T” case. [Table 3.18](#) summarizes the comparison of the devices from an SH perspective, showing around 20% lower R_{th} and ΔT in “4T” FET.

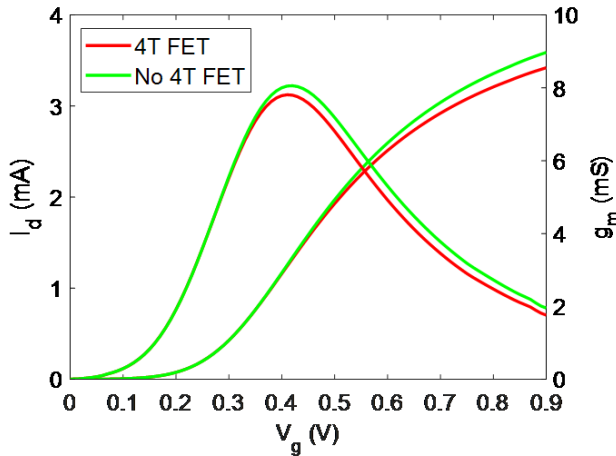


Figure 3.47: Drain current I_d and transconductance g_m vs gate voltage V_g for 4T and no 4T device in saturation at $V_d = 50$ mV.

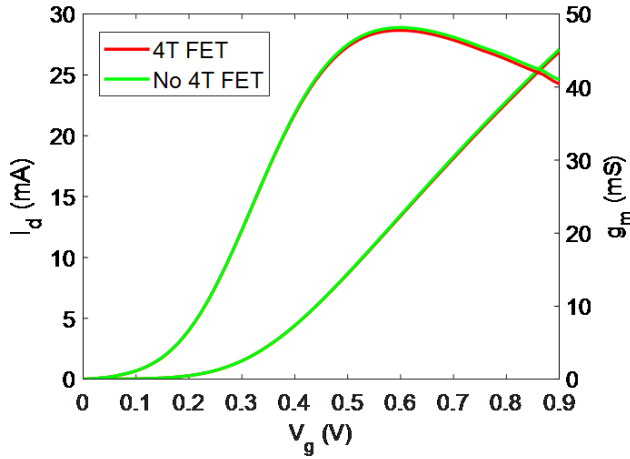


Figure 3.48: Drain current I_d and transconductance g_m vs gate voltage V_g for 4T and no 4T device in saturation at $V_d = 0.8$ V.

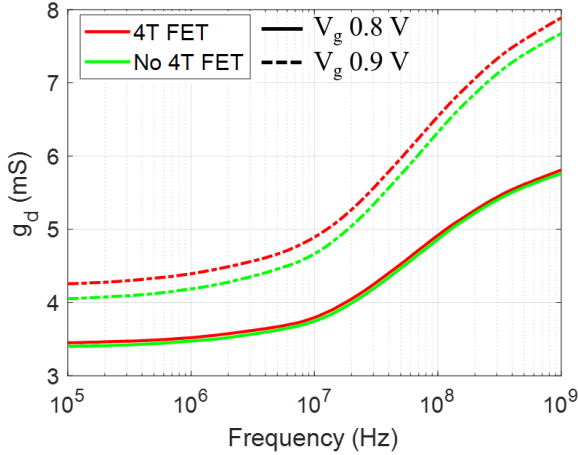


Figure 3.49: Output conductance g_d vs. frequency for 4T and non-4T devices in saturation at $V_d = 0.8$ V and $V_g = 0.8$ V and 0.9 V.

Keeping in mind that the core FET (“inner” device) is the same in both configurations, we suggest that the difference in the extracted SH features arises from the different layouts or accesses. Differences can arise from: (i) thermal

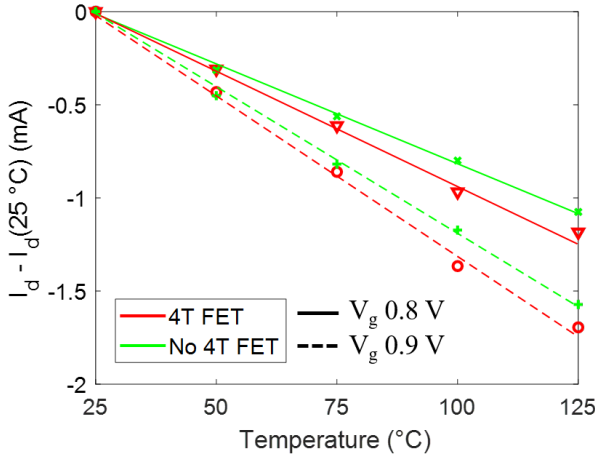


Figure 3.50: Drain current I_d vs temperature for 4T and non-4T devices in saturation at $V_d = 0.8$ V and $V_g = 0.8$ V and 0.9 V.

Table 3.18: Self-Heating Parameters. $V_g = V_d = 0.8$ V.

Device	$g_{d,LF}$ (mS)	Δg_d (mS)	$\frac{\partial I_d}{\partial T}$ ($\mu A K^{-1}$)	R_{th} ($K \mu m / mW$)	ΔT ($^{\circ}C$)
4T FET	3.46	1.69	12.11	164	99
No 4T FET	3.4	1.81	10.54	201	123

evacuation path and (ii) parasitic series resistance. Indeed, one can expect more efficient cooling from the accesses in the 4T device with a “larger”/more developed heat evacuation path. This hypothesis is in line with our works in **Chapter 4** which demonstrate that a heat sink connected to the gate of a device can reduce R_{th} [109, 110] by 8-20% depending on the sink configuration/area. From a technique point of view, the actual device R_{th} is therefore underestimated due to the gate accesses themselves acting like heat sinks. Apart from that, one can suppose different series resistances in those devices, which can be either due to variability or layout-related effects. Lower I_d attributed to the higher R_{sd} is seen in 4T FET in linear regime; the difference becomes smaller in saturation with heat evacuation difference coming into play (**Figure 3.48**). Simulations using PDK model with various series resistances added to the

FET reveal their effect on SH parameters extracted using the RF technique. R_s , R_d have a pronounced impact on both the g_d and $\frac{\partial I_d}{\partial T}$ (increasing $g_{d,LF}$ and magnitude of $\frac{\partial I_d}{\partial T}$) which is due to the difference between the external applied bias and the one seen by the inner device. The impact of R_d on the g_d transition is illustrated in **Figure 3.51** and the corresponding change in R_{th} (**Table 3.19**) is 2% (in the case of low added resistances) but can go up to 7% and higher.

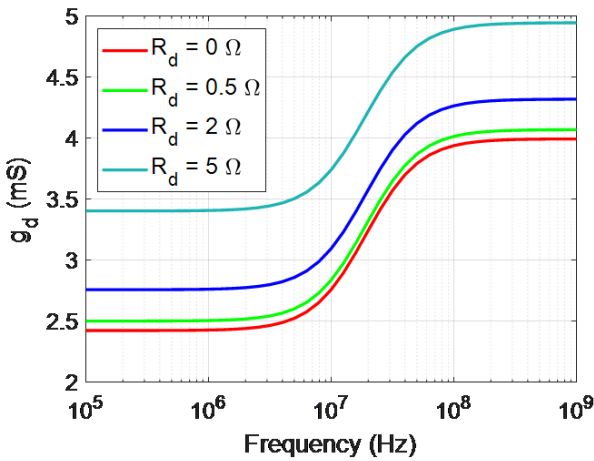


Figure 3.51: Output conductance g_d vs frequency for the device in PDK for varying R_d computed in saturation at $V_d = 0.8 \text{ V}$ and $V_g = 0.8 \text{ V}$.

Table 3.19: Measured Parameters with Different Values of R_d .

R_d	$g_{d,LF}$ (mS)	Δg_d (mS)	$\frac{\partial I_d}{\partial T}$ ($\mu\text{A K}^{-1}$)	R_{th} ($\text{K}\mu\text{m}/\text{mW}$)	ΔT ($^{\circ}\text{C}$)
0 Ω	2.42	1.57	12.8	149.12	90.43
2 Ω	2.76	1.56	12.92	145.78	88.01
5 Ω	3.4	1.54	13.12	139.85	83.76

3.10.3 Summary

This work demonstrates that special care needs to be taken when comparing different techniques and device configurations/layouts from a self-heating perspective. Observed differences should not only be attributed to the inner device but also to non-negligible layout effects. Specifically, for the 4T gate resistance characterization technique, cooling through the gate contacts leads to an underestimation of the device's thermal resistance.

3.11 Conclusion

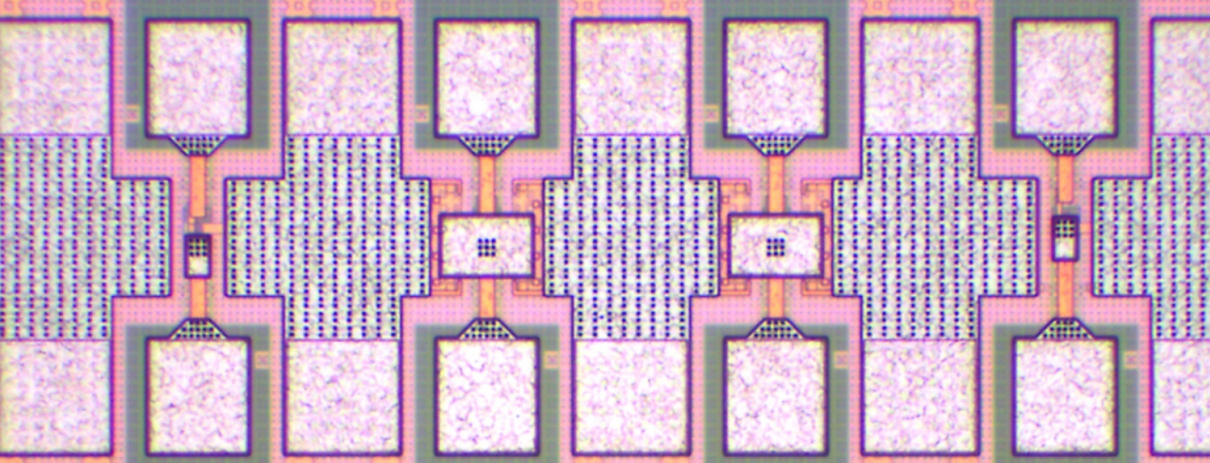
In this chapter, self-heating characterization techniques for state-of-the-art devices are looked into. Two of the most prominent techniques, Gate Resistance technique and RF technique are compared and the pros and cons of each are assessed. A comprehensive analysis of I_d versus temperature, an important parameter in the RF technique, is conducted, including adequate temperature data points to examine trends. The observed linear trend in both our data and literature is in contrast with the nonlinear trend noted in the PDK. By trying to have a similar nonlinear fitting from the PDK in our measurements, it is seen that it is possible to have such a fit, although difficult to establish precisely: this demonstrated the fine margins associated with the extraction process. A nonlinear trend results in varying dI_d/dT with temperature; this highlights the need to choose the ambient temperature point for dI_d/dT extraction. Error bars due to these variations in the slope of I_d versus temperature are shown and their impact on the extracted thermal resistance is studied in the measurements and PDK. The impact of process corners on R_{th} extraction is also studied through PDK simulation; 7-9% R_{th} variation with respect to the typical-typical corner case is observed for fast-fast or slow-slow corners. The variation of thermal resistance with ambient temperature is also investigated in measurements and PDK. Around 6% R_{th} reduction is seen on increasing temperature from 25 to 125 °C, in line with the roughly 6-8% reduction seen in the PDK models.

For the gate-resistance technique, the assumption that the gate temperature and the channel temperature are both equal is brought into question. Additionally, the linear trend assumed for R_{gate} versus temperature is looked into deeper; this is seen to be a crucial factor in SH extraction using this technique. It is seen that the R_{gate} versus temperature plot has a slightly nonlinear trend too as evident from the slope variation at different temperature points. Around 20% variation in R_{th} can be seen based on the temperature point of slope extraction, showing the sensitivity of the extraction with respect to this parameter.

From measurements on the same test structures, a 1.8 times higher thermal resistance is obtained for the RF technique compared to the gate resistance technique. The higher R_{th} for the RF technique is also verified from PDK model results. Comparing the EXT PDK (modelled using the gate resistance technique) and the PLUS PDK (modelled using the AC conductance technique), a 1.35 times higher R_{th} is obtained for the PLUS PDK. This shows that the extracted thermal attributes also depend on the type of SH characterization technique and possible reasons for the same need to be investigated. Heat

evacuation through the gate path could lead to a drop in the temperature across the gate explaining such a difference between the techniques. On exploring this aspect further, cooling through the gate contacts for the 4T gate resistance technique is established from observed lower thermal resistance values for the same MOSFET with 4T gate contacts compared to the case without the contacts. It is also observed that the differences could also partly be coming from a variation in series resistances of the devices that affect the SH extraction. Therefore device layout-related effects need to be kept in mind for accurate SH characterization.

Overall, this chapter provides an in-depth analysis and insights into self-heating extraction and the shortcomings of its techniques.



4. Self-Heating Mitigation Techniques

Having introduced the self-heating problem and the undesirable effects arising from it, we explore possibilities of reducing SH. A review of existing techniques in literature that help ameliorate SH is made. It is observed that while most SH reduction techniques focus on altering the substrate material or with sinks related to the substrate, heat evacuation through the back-end of line (BEOL) has rarely been explored. Developing on this gap in literature we demonstrate at a device level the use of a heat sink in the back-end of line (BEOL) to reduce the thermal resistance R_{th} of a device and thereby SH. Additionally, the impact of the sink size on reducing self-heating is investigated; a tradeoff is seen between SH reduction and RF performance coming from the parasitics of the sink.

4.1 Introduction: Heat Evacuation in MOSFETs

The main goal of this chapter is to look into ways of self-heating mitigation in MOSFETs. To do so, we pick up on insights obtained from **Chapter 3** where it was seen that gate contacts used for the 4T Gate Resistance technique can help in cooling. This observation shall be investigated further by focussing on the aspect of heat sinks connected to the gate to help heat evacuation. The chapter flow can be seen in **Figure 4.1**.

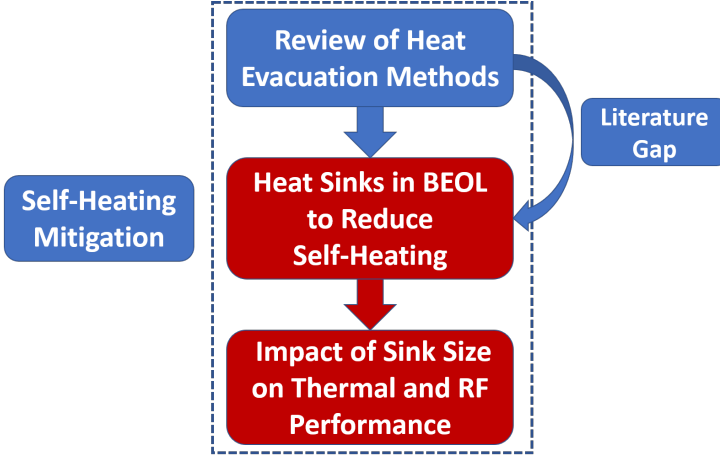


Figure 4.1: Overview of Chapter 4.

4.1.1 Heat Evacuation Paths

Looking into the possible heat evacuation paths in MOSFETs is the first step. To better understand the SH problem, a visual representation of the device geometry, materials used in the device and the heat evacuation paths is crucial. For the sake of simplicity, we shall consider a basic representation of the SOI MOSFET to comprehend the differences between them. By attributing thermal resistances to the different heat evacuation paths, insights into how the heat flows out from the channel will be looked into.

Based on a simple one-dimensional model of heat transport, the thermal resistance of each material layer/block can be expressed in **Equation 4.1** as follows:

$$R_{th} = \frac{l}{kA} \quad (4.1)$$

where l is the length of the material, k is the thermal conductivity, and A is the cross-sectional area. This is also analogous to the expression for electrical resistance computation with electrical conductivity in place of thermal conductivity.

Let us start by considering the primary heat evacuation paths as illustrated in **Figure 4.2** below. The heat generated in the channel can flow mainly through four regions: substrate, source, drain and gate.

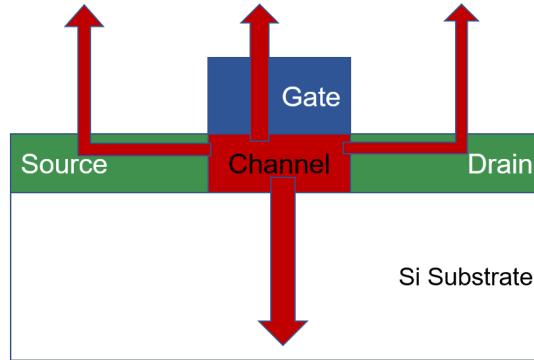


Figure 4.2: MOSFET heat evacuation paths.

Keeping the simple analysis above in mind, it is to be noted that the heat evacuation would depend on the geometry of the device: the thermal problem would differ for different values of channel length, channel thickness, BOX thickness etc. as the area of evacuation that the heat gets to flow out through different paths would be different in each case. Additionally, the geometry could affect the thermal conductivity of layers too based on their thicknesses.

4.1.2 Impact of Technology type on Heat Evacuation

Based on the previous discussion on the heat evacuation paths, we try to visualize the thermal problem in bulk and SOI technologies.

Bulk Silicon

To recall, **Figure 4.2** illustrates the heat evacuation paths in SOI MOSFET; in bulk technology just the BOX layer is absent and the downward path is directly through the substrate. There are possible heat evacuation paths upwards and downwards: with the downward path being directly to the substrate underneath and the upward path being through the gate, source and drain regions respectively. In this technology, the downward path through the bulk Si substrate turns out to be a major evacuation path as the thermal conductivity of bulk Si is relatively higher than the other regions, namely Source, Drain and Gate. This is because the lower Si thickness in the source and drain regions degrades the thermal conductivity from phonon scattering while the gate dielectric has low thermal conductivity.

PDSOI

Compare the above situation with the PDSOI technology, where a thick buried oxide (BOX) of SiO_2 is present underneath the top Si channel. The fact that the thermal conductivity of SiO_2 is two orders of magnitude lower than that of bulk Si, this BOX block impeded heat evacuation downward (thereby resulting in a greater thermal resistance in the downward path), thereby enhancing SH concerns on this technology.

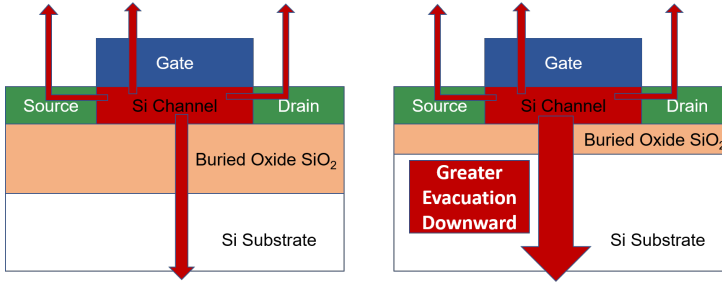


Figure 4.3: Comparison of heat evacuation in PDSOI and FDSOI

FDSOI

Thinning the BOX in FDSOI helps in reducing the thermal resistance offered by the BOX material as the thermal resistance of any material would simplistically speaking be directly proportional to the thickness of the material. While the reduction of film thickness contrarily reduces the thermal conductivity due to phonon scattering, the film thinning effect is dominant in reducing the thermal resistance of the film. This improves the evacuation downward compared to PDSOI as the thermal resistance of the downward path is reduced as seen in **Figure 4.3**.

4.1.3 Impact of Channel Dimensions on Heat Evacuation

We now take a closer look at the channel and its surroundings from an area of heat evacuation perspective. From the figure below, the top and the bottom faces of the channel (represented as a cuboid here) represent the interfaces between the gate and the substrate respectively while the left and the right faces represent the source and drain interfaces. Based on the dimensions of the device length L , device width W and channel thickness T_{Si} , the areas of heat evacuation through the different paths (via the different faces) would vary.

Having dimension L twice as high (in **Figure 4.4** (b) with respect to **Figure 4.4** (a)) would result in having twice as high area of evacuation through the gate and substrate regions. Therefore, for longer channel devices greater heat evacuation through the gate and substrate regions is expected whereas for shorter channel devices evacuation through source and drain regions could be more feasible.

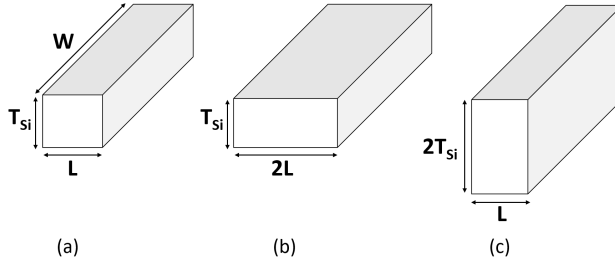


Figure 4.4: Variation of heat evacuation areas with different channel dimensions.

Alternatively, considering the case of a thicker channel device (in **Figure 4.4** (c) with respect to **Figure 4.4** (a)), the surface area of heat evacuation through the source and drain regions is increased and thereby in such a device evacuation through those regions could be more prominent.

The main message to take away here is therefore that the thermal problem varies from device based on the geometry. The impact of having different materials on the heat evacuation scenario is demonstrated next by comparing the situation in bulk and SOI technologies.

4.2 Benefits of Self-Heating Reduction

The various drawbacks due to higher device temperatures caused by SH have been listed in **Section 1.2** of **Chapter 1**. To summarize, degradation in device performance and device lifetime are the main concerns arising from the same. Finding ways to mitigate SH would help in reducing the negative effects brought about by it. By restricting the device temperature rise, performance and reliability can be improved. This is specifically of great interest in advanced nodes that face greater SH concerns and for modern applications where reliable operation over long periods is crucial.

From a reliability perspective, device lifetimes are reported to be inversely

proportional to the temperature; reducing device temperature would help improve lifetime. In **Figure 4.5**, Honeywell reports the variation of device lifetime for commercial CMOS and high-temperature SOI CMOS technologies with temperature. For Honeywell high-temperature CMOS, the device lifetime is reported to decrease from around 100 years at 150 °C to around 10 years at 200 °C. This shows the strong impact of temperature increase on reliability; using heat evacuation methods to reduce device temperatures can greatly help in this context.

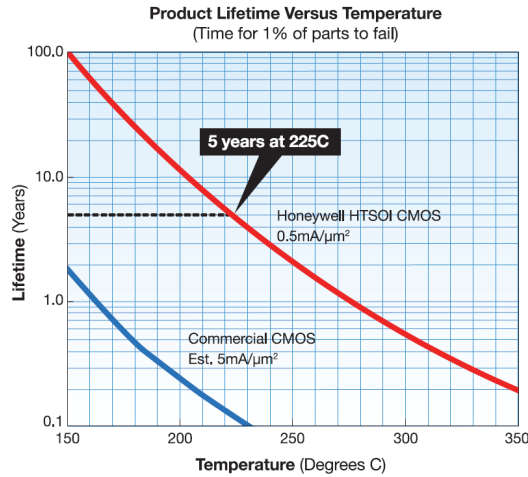


Figure 4.5: Variation of device lifetime with temperature reported by Honeywell in [43].

4.3 Different Methods of Self-Heating Reduction

With the drawbacks of SH established, possible ways of mitigating SH have been a subject of great interest. Some of the techniques from literature are listed below.

4.3.1 Substrate Engineering

Substrate engineering refers to suitably selecting or altering the properties of the substrate to have better performance. Modifying the substrate material, property or geometry could be used for different purposes in general, for example, improvement of Q factors on SOI inductors was proposed in [111].

From an SH perspective, with the fact that the SiO_2 BOX is one of the major bottlenecks in heat evacuation, reducing the thermal resistance of the BOX would help the heat evacuation process. Going back to the analytical model, with R_{th} being directly proportional to the thickness of the material and inversely proportional to the thermal conductivity of the material, two ways of reducing R_{th} would be: i) Decreasing the material thickness ii) Using a material with greater thermal conductivity

BOX Thinning

The reduction of R_{th} due to BOX thinning in PDSOI MOSFETs of different BOX thicknesses can be seen clearly in **Figure 4.6** from the work of Babak [47]. Three different BOX thicknesses of 1 μm , 0.4 μm and 0.2 μm were compared and the results were systematically lesser for the thinner BOX cases over different device lengths.

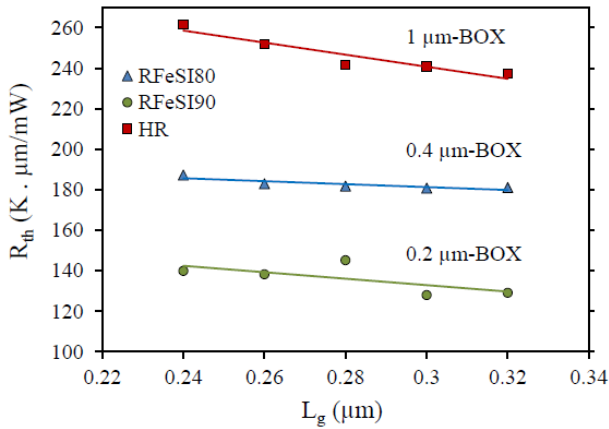


Figure 4.6: Decrease of R_{th} with BOX thinning from experimental results using RF technique by Babak in [47]. Three different BOX thicknesses were studied.

In the work from Uchida [84], the fact that BOX thinning reduces the thermal resistance was shown. It was observed that the R_{th} decreases monotonically to a possible thin t_{BOX} limit of 5 nm. The trend of decreasing R_{th} with BOX thinning was also demonstrated in simulations by Fiegna in [85].

Alternative BOX Materials

While BOX thinning has already been demonstrated to be an effective method to reduce thermal resistance, in advanced FDSOI technologies it is already

thinned down to a considerable extent. The other alternative of considering alternative BOX or even gate oxide material becomes an interesting one. Thermal conductivities of possible oxide materials are shown in **Table 4.1**. Considering some other oxides, Al_2O_3 is over 25 times thermally more conductive than SiO_2 [112]. The possibility of considering Al_2O_3 even as gate material could be worth a thought from a thermal perspective given that electrical explorations in this direction are being made [113]. Additionally, it is noteworthy that Al_2O_3 is not among rare-earth metal oxides, making it compatible with sustainable development objectives.

Previously, in 2004, using Al_2O_3 as the buried oxide was proposed by Oshima in [114] where the device temperature could be reduced by over 15–20% compared to SiO_2 BOX as seen in the **Figure 4.7**. It was shown that a demonstrated reduction in lattice temperature by around 40 °C (such as provided by the alumina BOX) enabled the mobility to increase by more than 20%. Looking at it from another perspective, this improvement in mobility aligns with the anticipated outcomes of using strained silicon films; therefore a viable method for enhancing carrier mobility involves mitigating excessive self-heating through the usage of buried alumina BOX.

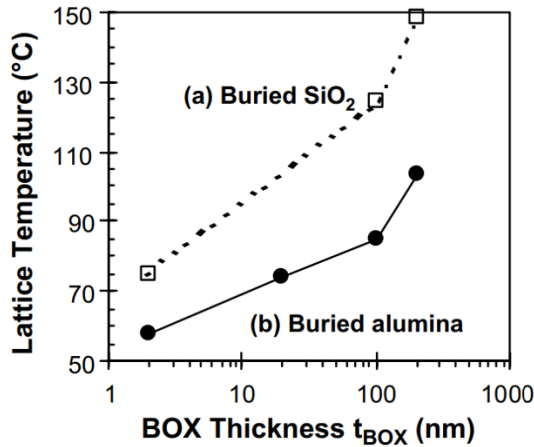


Figure 4.7: 2-D simulations of the lattice temperature versus BOX thickness in 70 nm long SOI MOSFETs with (a) SiO_2 or (b) alumina BOX ($t_{\text{Si}} = 10$ nm) [114]

In [115], the use of AlN and diamond as the BOX layer to reduce SH

was explored. AlN has a thermal conductivity around 100 times higher than SiO₂ whereas that of diamond is the best found in nature. The improvement in thermal properties using diamond instead of SiO₂ was also shown in [116].

Table 4.1: Thermal Conductivities of possible BOX Materials

Material	Thermal Conductivity (Wm ⁻¹ K ⁻¹)
SiO ₂	1.4
Al ₂ O ₃	35
AlN	136
Diamond	2400

Of course, we need to keep in mind that in thin films, due to phonon boundary scattering effects, the thermal conductivity decreases and for the most advanced devices, a comparison of the thin film values needs to be made. In Scott [107], it is reported that for very thin films, the TBRs dominate and thus while Al₂O₃ and TiO₂ films are more thermally conductive, the difference with respect to HfO₂ is lesser than the corresponding thick film numbers shown earlier.

Using polycrystalline diamond as the BOX insulator was studied in [117] and the temperature rise could be reduced 3-4 times compared to devices on oxide from both measurements and simulations. In [118], some other materials like diamond and AlN were considered in addition to Al₂O₃ which all provide thermal benefits. From an electrical perspective though, using high-*k* BOX materials could result in worsened short channel effects and thus a tradeoff can be envisioned.

4.3.2 Layout Optimization

Electrically, using multi-finger MOSFETs is done to reduce the gate resistance with the gate fingers in parallel. But from a thermal point of view, due to thermal coupling between adjacent fingers in multi-finger MOSFETs SH is more pronounced than the corresponding single-finger case. Each finger is heated by its neighbouring fingers due to heat spreading and a non-uniform temperature distribution is expected with the outer fingers being the coolest and the middle ones being the hottest. This can be seen in **Figure 4.8** demonstrated from [100].

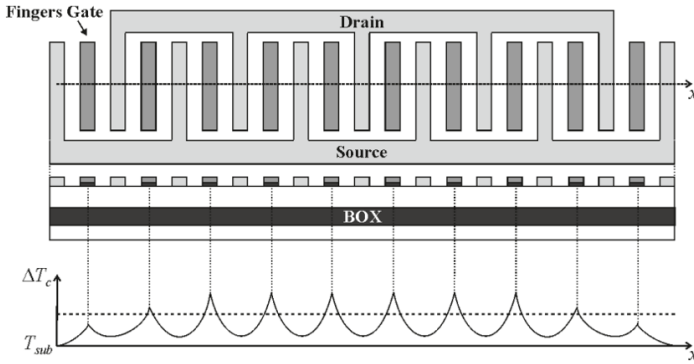


Figure 4.8: Thermal coupling in multi-finger device. Top view of transistor and schematic of the typical temperature rise in the channel, along the heat source in the x-direction, taken from [100].

Fiegna showed through simulations in [85] that R_{th} increases rapidly with the increasing number of fingers and saturates at a certain point. Thereby from a thermal point of view, having fewer fingers can help in reducing the thermal problem. A tradeoff can therefore be expected from an electrical-thermal viewpoint. On the other hand, increasing the spacing between the fingers (also referred to as pitch) can help in reducing the thermal interactions between the fingers and result in lesser heating.

The impact of improving SH at a MOSFET level helps in enhancing the performance at circuit level too. In [17], implementing a well-optimized clock-driver layout with a wider finger spacing made it possible to mitigate performance degradation caused by the self-heating effect by achieving an improvement of 1.3–1.4× in 0.09-μm bulk and SOI CMOS technologies.

4.3.3 Heat Sinks

Using heat sinks to evacuate heat is a general principle used in a variety of applications in real life and the same theory could be applied to electronics too.

As early as 1994, [119] used a buried 70 μm thick gold plated heat sink for aiding heat dissipation from the active layer. The thermal resistance was half compared to that of conventional FETs without the heat sink. More recently in 2022, in [120] Zuo simulated a highly thermally conductive diamond substrate also, with a diamond heat sink layer to reduce device temperature by 35% in

GaN HEMT devices.

In [121], the usage of polysilicon plugs through the BOX layer was made to improve thermal performance. Thermal resistance was reduced by 15% using this method. However, accommodating the heat sink took up 21% additional area compared to the standard device.

Graphene, due to its high thermal conductivity, has been of interest as a material which could aid heat removal. The thermal conductivity of suspended graphene at room temperature (RT) was found to range between 4840 and 5300 $\text{Wm}^{-1}\text{K}^{-1}$ [122]. Using graphene heat spreaders to evacuate heat using heat sink under the BOX was studied in [123]. It was discovered that integrating graphene with suitable heat sinks could significantly reduce the temperature of localized hot spots.

More recently in November 2022, OnSemi has demonstrated a series of new MOSFET devices with innovative top-side cooling to assist designers in challenging automotive applications in [124]. This has been achieved by using a 16.5 mm^2 thermal pad on the upper surface, enabling heat dissipation directly into a heat sink. Enhanced reliability with the top-cooling design contributes to an extended overall system lifespan.

Overall, most of the heat sink topologies seen in literature used have mainly explored evacuation through the substrate. Using evacuation through the BEOL has not been explored and that is what we investigate in detail in this chapter.

4.4 Heat Sink in BEOL

4.4.1 Idea and Background

Thermal optimization methods like substrate engineering using alternative materials or heat sinks in the FEOL would be trickier to implement in practice as they require significant changes in device processing. The substrate, BOX, source, drain and gate region dimensions and materials are all mostly fixed by the technology. Layout optimization might not also be possible due to a certain desired device layout from a design performance perspective. However, the BEOL path, which offers the flexibility to realize spreaders and sinks more freely, could provide a general possibility of heat evacuation that could apply to devices of different layouts or on different substrate types or technologies. With this consideration in mind, we look into the possibility of heat evacuation through the BEOL path.

Mariniello [108] experimentally demonstrated recently in 2016 the effect of heating dissipation through the gate electrode and its impact on the heating of SOI devices. In order to limit this cooling effect through the gate contacts, two gate contacts instead of four are used to measure self-heating using the gate resistance thermometry method in [106]. In this work, we go further in this concept and propose techniques of SH reduction using dedicated heat sinks implemented in the process' BEOL and explore them experimentally. The prospect of using thermal shunts in the BEOL to suppress SH was studied in [125], but only by simulations. Out of the aforementioned possible heat evacuation paths, the BEOL path above the MOSFET is of interest in this work. Our work experimentally addresses heat evacuation through the BEOL using various heat sink configurations.

In this work, published in [109], we propose a potential technique for reducing SH using dedicated heat sinks for the devices implemented in the process BEOL and explore it experimentally. Additionally, the effect of the presence of heat sinks on the performance of the devices is studied. Our conference publication [110] is extended by comparing different extraction methods, adding more measured dies and bias conditions.

4.4.2 Device under Test

The devices used in this study originate from the 22 nm FDSOI technology from GlobalFoundries [19]. The rich BEOL consisting of 11 metal layers in this technology provides ample scope for the realization of heat sinks to facilitate

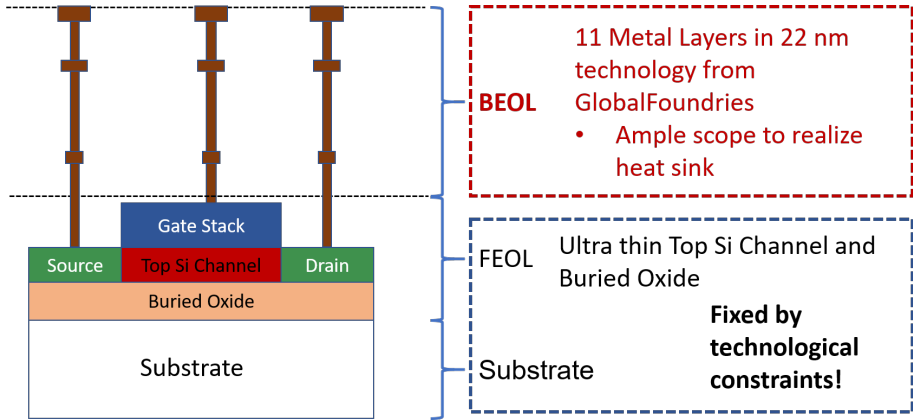


Figure 4.9: BEOL versus FEOL for sink realization.

heat dissipation (seen in **Figure 4.9**). The gate length is 20 nm, total width is $30\text{ }\mu\text{m}$ for each of these devices composed of 60 fingers, each finger having a width of $0.5\text{ }\mu\text{m}$. In this work, two identical FETs but with two different heat sink configurations are considered. One of them is connected to a heat sink through the gate (called “gate-connected sink”), while the other one includes the same heat sink, which is left floating (called “floating sink”).

The heat sink introduced in the BEOL consists of a metallic pad right above the FET, over which the passivation layer is removed. With the BEOL consisting of 11 metal layers, a metal plate of $234\text{ }\mu\text{m} \times 114\text{ }\mu\text{m}$ is used on the uppermost metal layer, connected down with vias to the fifth metal layer. **Figure 4.10** and **Figure 4.11** schematically illustrate the gate-connected sink and the floating sink configurations, respectively. The gate-connected sink (**Figure 4.10**) comprises of a similar metal plate in the top metal layer, however, it is connected by vias to the gate above the gate accesses. The floating sink is left electrically and thermally floating above the fingers of the FET in the fifth metal layer and consists of metal rectangles that continue to stack up to the metal plate in the topmost layer. Note that there are two gate accesses that lie on either side of the gate fingers of the FET that help in connecting them to the sink (only one of these gate accesses connecting the fingers is seen in **Figure 4.10** and **Figure 4.11**). The main difference between these two kinds of sinks is the electric and thermal connection to the gate with metal vias above the fifth metal layer (labelled as connected vias “V_x” in **Figure 4.10**). The

absence of these vias in case of the floating sink can also be perceived clearly in **Figure 4.11**. It is worth noting that the way of incorporation of the heat sink in the BEOL we propose in this work does not add a penalty in terms of the area occupied by the device (or circuit) on which it is implemented. Moreover, the freedom to introduce the sink in devices expected to feature greater SH is one of the advantages of this implementation.

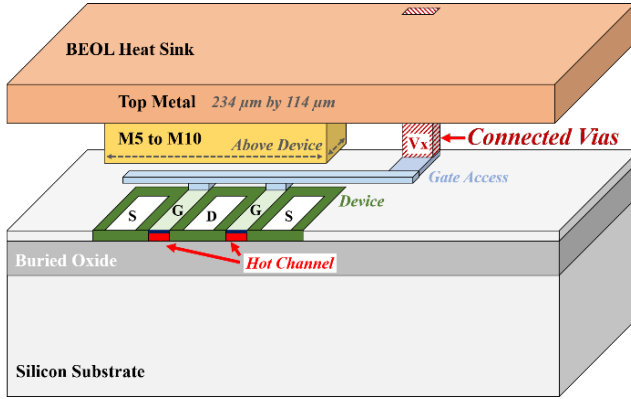


Figure 4.10: Schematic of the gate-connected sink.

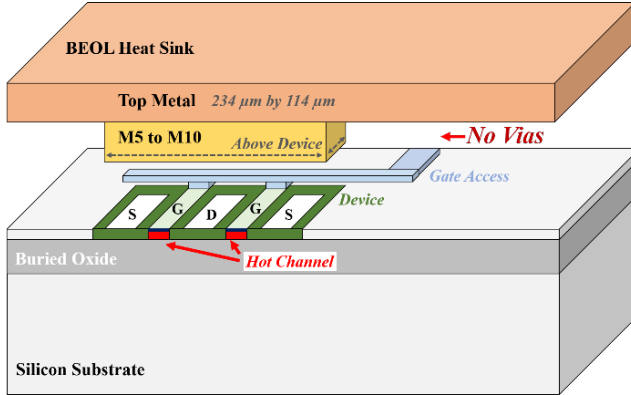


Figure 4.11: Schematic of the floating sink.

4.4.3 Measurement Setup

The RF technique for SH characterization, described in **Chapter 3**, has been used to study the SH parameters R_{th} and C_{th} in this work. For the RF characterization, S-parameters are measured in a frequency range from 100 kHz to 1 GHz and converted to Y parameters. On-wafer RF and DC measurements are made on the PM8 probe station at different temperatures, details of the high-temperature measurement process can be referred to in **Section 2.2 of Chapter 2**. An ENA vector network analyzer and two RF $|Z|$ probes of 100 μm pitch are used for these measurements. DC biasing of the gate and drain is done using a semiconductor analyzer HP 4145. Bias tees are used to combine the aforementioned DC bias and the RF cables to connect to the VNA. SOLT (Short-Open-Load-Thru) method is used for calibration at room temperature. The output conductance (g_d) is computed as the real part of Y_{dd} , transconductance (g_m) is the real part of Y_{dg} , and the drain capacitance (C_{dd}) is the imaginary part of Y_{dd} divided by ω . Both g_d versus frequency and C_{dd} versus frequency curves show transitions caused by SH, which allows assessment of SH-related features (as e.g. R_{th} and C_{th}). The transition due to source and drain coupling through the substrate is strongly attenuated by the doped back gate in our devices [82] and is neglected in this work. This is furthermore justified by the fact that the back-gate (regular threshold voltage, conventional well) and substrate network are the same in both types of devices we compare in this work.

The impact of SH causes a transition from low frequency to high frequency in Y_{dd} which can be seen in **Equation 4.2** [93] [126]:

$$Y_{dd, \text{HF}} - Y_{dd, \text{LF}} = Z_{th} \frac{\partial I_d}{\partial T} (I_d + V_d Y_{dd}) \quad (4.2)$$

Following the derivation in [126] and decomposing **Equation 4.2** into its real and imaginary parts, **Equation 4.3** and **Equation 4.4** are obtained respectively.

$$\frac{R_{th}}{1 + \omega^2 R_{th}^2 C_{th}^2} = \frac{g_d(f) - g_{d, \text{HF}}}{(I_d + V_d g_d(f)) \frac{\partial I_d}{\partial T}} \quad (4.3)$$

$$\frac{-R_{th}^2 C_{th}}{1 + \omega^2 R_{th}^2 C_{th}^2} = \frac{C_{dd}(f) - C_{dd, \text{HF}}}{(I_d + V_d g_d(f)) \frac{\partial I_d}{\partial T}} \quad (4.4)$$

I_d is the DC drain current, V_d is the drain voltage, $g_{d,\text{HF}}$ and $C_{dd,\text{HF}}$ are the output conductance g_d and drain capacitance C_{dd} , respectively, at high frequency (where dynamic self-heating effect is removed), and $\frac{\partial I_d}{\partial T}$ is the slope of the I_d versus temperature.

In this work both these extraction formulae have been used:

- Extraction Method 1 uses **Equation 4.3** and thereby computes R_{th} from the real part of Y_{dd} .
- Extraction Method 2 uses **Equation 4.4** and thereby computes R_{th} and C_{th} from the imaginary part of Y_{dd} .

In extraction Method 1, the thermal resistance R_{th} is extracted using **Equation 4.3**: at low frequency the numerator of the right-side becomes Δg_d , the difference between the output conductance g_d at low and high frequencies. In extraction Method 2, a fourth-order thermal RC network is used to fit the imaginary part of Y_{dd} measurements, similar to the procedure in [93]. For devices with different heat evacuation paths, a first-order network is usually insufficient to fit the experimental data and higher-order networks are found to be more appropriate. Similar to [93] as well as our previous observations on the same technology [98], a fourth-order network was found to be sufficient in our case. Based on this fitting, R_{th} is computed using extraction Method 2 as the equivalent low-frequency R_{th} of the fourth-order RC network ($\sum_{i=1}^4 R_{th,i}$).

C_{th} has been computed from **Equation 4.4** by using the difference in C_{dd} at low and high frequencies and plugging in the value of R_{th} obtained previously. $\partial I_d / \partial T$ is extracted from I_d - V_g curves measured in a temperature range from 300 up to 400 K. This has been achieved by a Thermo-chuck from Temptronic that allows heating up the devices to the desired temperature points with good temperature control and stabilization. The extractions have been made in saturation at a V_g and V_d of 0.8 and 0.9 V. Though the nominal V_d of this technology is 0.8 V, a value of 0.9 V has been used here to increase the power in the channel and thereby stimulate higher SH. The back gate was grounded during measurements.

4.4.4 Results and Discussion

IV characterization

Figure 4.12 shows the I_d - V_g and the g_m - V_g curves for both types of devices in saturation at $V_d = 0.9$ V. The fact that the gate connection of the sink does not affect the DC device performance is observed from the almost overlapping curves. Very similar threshold voltages V_{th} of around 0.33 V are obtained for both types of devices from the second derivative method in the linear regime, thus allowing a fair comparison between them.

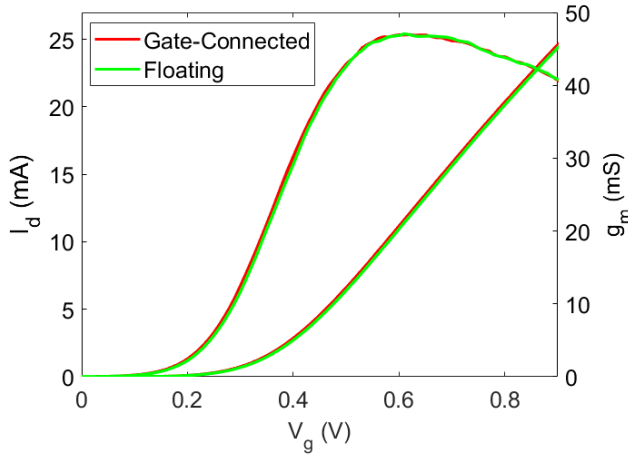


Figure 4.12: Drain current I_d and transconductance g_m vs gate voltage V_g for the “gate connected” and “floating” sinks recorded in saturation at $V_d = 0.9$ V.

By comparing the results obtained in saturation with those in linear regime, some interesting observations are made. In the linear regime (at $V_d = 50$ mV), the I_d - V_g and the g_m - V_g curves show relatively higher values for the floating sink case as seen in **Figure 4.13**. As SH does not affect this regime (due to low I_d and V_d and thus power dissipated), the fact that the gate-connected sink surpasses the floating sink in terms of I_d in saturation shows the effect of the sink coming into play.

Figure 4.14 shows the I_d - V_d curves for both types of devices for $V_g = 0.9$ V. While it is observed that the curves are mostly overlapping, the I_d and its slope g_d for the gate-connected sink are a bit larger than that for the floating sink in saturation; this correlates with observations from the I_d - V_g plot in **Figure 4.12**.

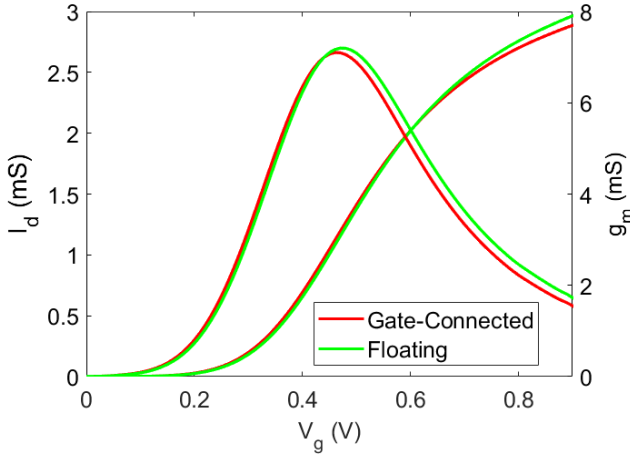


Figure 4.13: Drain current I_d and transconductance g_m vs gate voltage V_g for the “gate connected” and “floating” sinks recorded in linear at $V_d = 50$ mV.

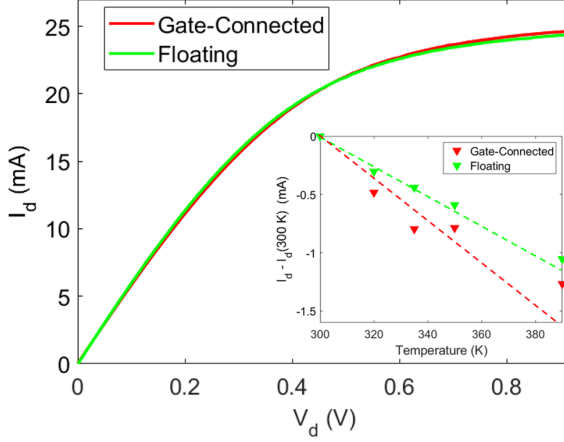


Figure 4.14: Drain current I_d vs drain voltage V_d for the “gate connected” and “floating” sinks measured at $V_g = 0.9$ V, I_d vs temperature measured shown in inset.

SH Characterization

Figure 4.15 shows the variation of output conductance g_d with frequency. From this plot, $g_{d,LF}$ (g_d at low frequency of 100 kHz), $g_{d,HF}$ (g_d at high frequency of 1 GHz), and Δg_d (the difference between $g_{d,HF}$ and $g_{d,LF}$) are extracted, as needed for the R_{th} estimation using RF method. The values of g_d at low and high frequencies represent the cases where dynamic self-heating is present and removed, respectively. Since the lowest specified frequency of operation of the bias tees is 20 kHz, the low-frequency value of 100 kHz is chosen to have reasonable results free from error. The value at 100 kHz is, in fact, verified to be a steady value. A higher value of $g_{d,LF}$ obtained for the gate-connected sink agrees well with conclusions drawn from I_d - V_d plots above and demonstrates the fact that the device with a gate-connected sink is less affected by SH compared to the floating sink counterpart. It can be noticed that there is still a difference between $g_{d,HF}$ for two configurations. This is because at HF dynamic SH is removed, but static SH remains, so that $g_{d,HF}$ for the gate-connected sink is a bit higher. The reason that the g_d curve seems to keep slightly increasing at the HF point of 1 GHz is the fact that the measurements here are not de-embedded. From measurements on similar devices with proper de-embedding structures, it is observed that $g_{d,HF}$ reaches a plateau a bit below 1 GHz. While it is true that the $g_{d,HF}$ value extracted is a bit higher than the actual value that would have been obtained had de-embedding been present, a fair comparison is maintained by the fact that the results of both the devices being compared are not de-embedded. Furthermore, extraction Method 2 is almost unaffected by this effect. Indeed, from the C_{dd} versus frequency plot in **Figure 4.16**, it has been observed that, firstly, the $C_{dd,HF}$ value at 1 GHz is close to the plateau. Secondly, SH-related variation of C_{dd} is seen to be around 3 orders of magnitude higher than $C_{dd,HF}$ and thus a small variation of $C_{dd,HF}$ almost does not affect the SH extraction.

Table 4.2 summarizes the comparison of the devices with gate-connected sink and floating sink (at $V_g = V_d = 0.9$ V) not only in terms of normalized values of R_{th} , but also various parameters involved in its extraction (using Extraction Method 1), such as output conductance g_d at low-frequency $g_{d,LF}$ and the difference between g_d at high and low frequencies Δg_d and $\frac{\partial I_d}{\partial T}$.

Higher value of $g_{d,LF}$ and lower Δg_d are obtained for the gate-connected sink suggesting lower SH in such devices. It is verified that the values of g_d at DC from the I_d - V_d plots (reported in a previous section) are very similar to the $g_{d,LF}$ values obtained at 100 kHz. The absolute value of $\frac{\partial I_d}{\partial T}$ is found to

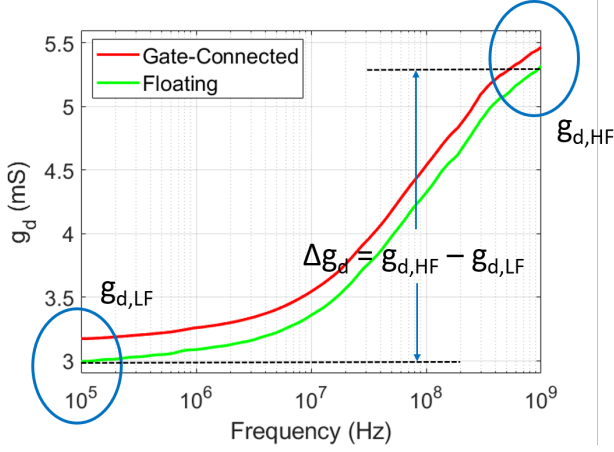


Figure 4.15: Output conductance g_d vs frequency for the “gate connected” and “floating” sinks at $V_g = V_d = 0.9$ V.

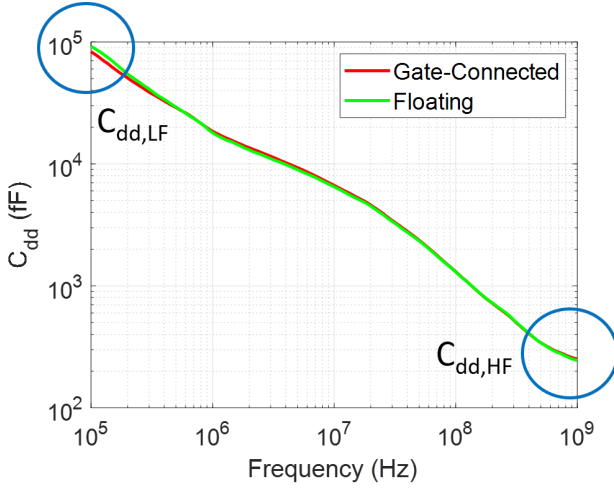


Figure 4.16: Drain capacitance C_{dd} vs frequency for the “gate connected” and “floating” sinks at $V_g = V_d = 0.9$ V.

Table 4.2: Extraction Method 1, $V_g = V_d = 0.9$ V.

Sink Type	$g_{d,LF}$ (mS)	Δg_d (mS)	$\frac{\partial I_d}{\partial T}$ (μ A/K)	R_{th} Normalized ($K\mu$ m/mW)
Connected	3.17	2.29	-9.85	254
Floating	3	2.31	-8.17	313

Table 4.3: Extraction Method 2, $V_g = V_d = 0.9$ V.

Sink Type	R_{th} Normalized ($K\mu$ m/mW)	C_{th} (pJ/K)	τ_{th} (ns)	f_{th} (MHz)
Connected	244	4.86	39.52	4
Floating	317	4.07	41.59	3.8

be higher for the gate-connected sink confirming weaker SH in this case. To better explain this difference, let us start by considering I_d variation versus temperature. At high- V_g values, I_d is expected to reduce with temperature mainly because of mobility degradation from phonon scattering given by a power law $I_d/I_{d0} \sim \mu/\mu_0 \sim (T/T_0)^{-k}$ [127]. **Figure 4.17** schematically shows I_d versus T and the slope of this variation, which is found to be more negative at lower temperatures (note that $\frac{\partial I_d}{\partial T}$ is negative in the plot as I_d is decreasing with temperature) compared to higher temperatures. It is clearly illustrated in **Figure 4.17** that with higher temperature rise coming from higher SH, a device at a lower temperature T_1 shows a higher magnitude of $\frac{\partial I_d}{\partial T}$ compared to the case where it experiences greater SH and is at a higher temperature T_2 . This shows that the magnitude of $\frac{\partial I_d}{\partial T}$ is expected to be higher for the case where lesser SH is observed, that is the gate-connected sink in this work.

A combination of the above parameters, namely the g_d values at LF and HF and the $\frac{\partial I_d}{\partial T}$, results in a lower value of R_{th} for the gate-connected sink. It is observed that the normalized R_{th} in the case of gate-connected sink is around 20% lesser than for the floating sink case.

The variation of C_{dd} with frequency is shown in **Figure 4.16**. Using the second extraction method, R_{th} and C_{th} are computed as shown in **Table 4.3** for the same devices. Additionally, τ_{th} is calculated as the product of R_{th} and C_{th} and f_{th} is given as $\frac{1}{2\pi\tau_{th}}$. It is important to emphasize that both extraction methods provide similar results in terms of R_{th} .

Measurements on multiple dies confirm this trend of lower normalized R_{th}

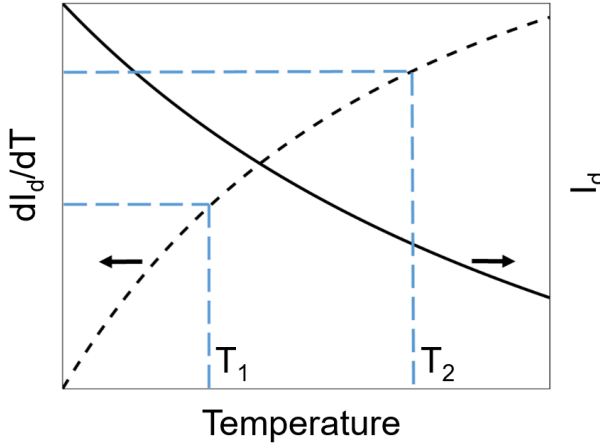


Figure 4.17: Drain current I_d vs Temperature and slope $\frac{dI_d}{dT}$ based on a power law $I_d/I_{d0} \sim \mu/\mu_0 \sim (T/T_0)^{-k}$.

in the case of the gate-connected sink (**Figure 4.18**). Furthermore, the same improvement is observed for various bias conditions (**Figure 4.18**). In the figure, we also observe good agreement in the R_{th} reduction using the two extraction techniques. The percentage reduction in R_{th} when the sink is connected is observed to vary from 15 to 35% over five dies. The variation in the magnitude of R_{th} reduction over dies arises partly from die-to-die process variability from source, drain and extensions doping, Si and oxide layer thicknesses, gate edge roughness, metal grain granularity, etc. as for any advanced process. Furthermore, possible variations in the BEOL stack layers thicknesses need to be considered (particularly in our case with different sink configurations). Of course, unavoidable measurement variability cannot be neglected. The observation of the general effect of variability can be clearly made from the earlier work of our group in [81]. However, the main point of our work is relative improvement and it can be seen that despite the variability between dies, applied bias and extraction techniques, there is always an improvement (15-35%).

The absence of the metal vias above the fifth layer of the BEOL in the case of the floating sink was expected (theoretically) to result in a greater R_{th} of that heat evacuation path. This stems from the fact that the thermal conductivity of dielectric SiO_2 is two orders of magnitude lower than that of bulk Silicon

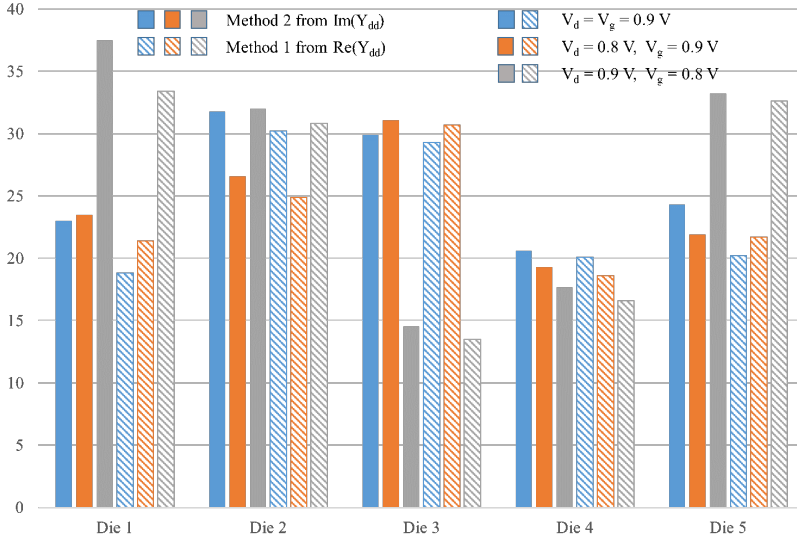


Figure 4.18: Percentage reduction in R_{th} from floating sink to gate connected sink for different bias conditions and over multiple dies.

and even lower with respect to metal [70]. Thus, the heat sink in the floating case is left thermally floating for all practical considerations, thus blocking the heat evacuation through that path. On the other hand, in the case of the gate-connected sink, connections from the FET to the heat sink in the topmost layer is expected to allow easier heat evacuation, resulting in a lower overall R_{th} . The results obtained experimentally in this work validate this theoretical hypothesis.

Results on Multiple Dies

The R_{th} reduction due to the usage of the heat sink has been demonstrated for multiple dies in **Figure 4.18**.

On each of the dies, the respective trends of I_d versus temperature are respected too; the averaged I_d vs temperature plot over all the 5 dies is shown in **Figure 4.19**. The linear trend I_d vs temperature and a steeper I_d vs temperature slope for the gate-connected sink is established from the demonstrated results.

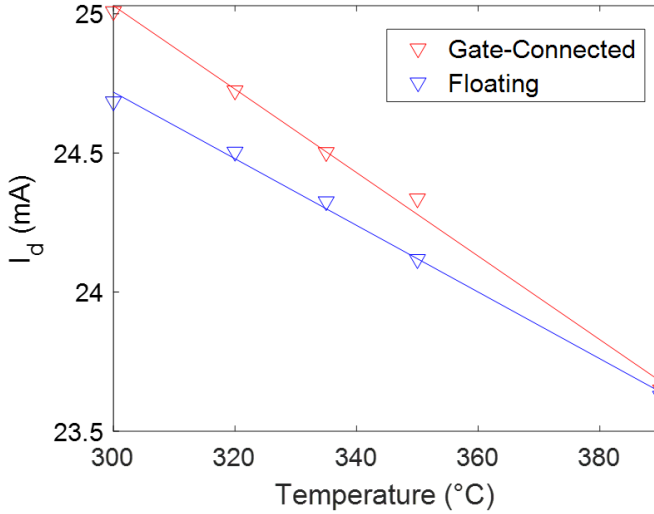


Figure 4.19: Averaged drain current I_d vs temperature over the measured dies for the gate-connected and floating sink cases at $V_g = V_d = 0.8$ V.

Discussion on the impact of heat sink parasitics on RF performance

It is worth emphasizing that in the proposed configuration, the connection of the sink creates a parallel network to the standard/usual connection of the gate access. Therefore, we do not expect to degrade the gate resistance due to the connection of the sink. The increase in gate resistance R_g due to temperature rise from SH is expected to be limited as the heat evacuation path through the gate is not the only evacuation path; the downward path through the substrate also plays an important role. However, a detailed study of R_g could not be made because of the lack of de-embedding structures for the devices.

With the main intention of the device design being to show SH reduction, it was not designed from an RF performance perspective. Also, due to the lack of de-embedding structures, precise information about the RF performance could not be demonstrated. The various parasitic capacitances between the regions where the sink and the gate access paths overlap degrade the RF performance. Based on parasitic extractions from de-embedding structures of similar devices, we predict that connecting the sink degrades the f_T by a factor of 7.5 compared to the case when the sink is not present at all for the sink geometry investigated in this work. By leaving the sink electrically floating, this degradation could be

reduced to a factor of 1.5 times. We expect that the geometry of the sink can be further optimized for better RF performance, this is studied next in [Section 4.5](#).

4.4.5 Summary

The prospect of using a BEOL heat evacuator to alleviate self-heating in advanced devices has been studied in this work. The reduction of thermal resistance (and hence temperature rise) in the case of a sink connected to the gate compared to it being left floating with respect to the gate has been experimentally verified. The fact that the DC performance of the two types of devices is similar (as seen from I_d - V_g , g_m - V_g curves) in order to make a fair comparison with respect to SH parameters has been confirmed. With the present configuration, we have achieved around 20-30% improvement in the SH parameters in the gate-connected sink devices. The observed trend was confirmed on different dies and at different bias conditions. Two extraction methods employed in this work (i.e., conductance and capacitance methods) provide consistent results, validating the gate-sink-connected approach for SH reduction in advanced devices. Thus, the possibility of using a gate-connected sink to reduce self-heating has been put forth here as a proof of concept. While this study has been conducted on FDSOI MOSFETs, the idea of using a heat sink in the BEOL can be extended to other technologies. It is worth emphasizing that the proposed configuration has two advantages: (i) it does not alter the area occupied by the devices/circuit, and (ii) it is not expected to degrade the gate resistance. The sink is mainly aimed for use in devices where SH could be a concern, and it does not affect the design of the original device. To enhance the efficiency of the heat removal by the sink and minimize the parasitic capacitance added by it, further optimization of the sink configuration is envisaged.

4.5 Comparison of Sink Efficiency with Area

Having demonstrated the impact of SH reduction by using a heat sink in the BEOL through our studies in [109] [110] described in [Section 4.4](#), our work here follows up on that by addressing heat evacuation through the BEOL using different heat sink sizes by experimental analysis. In this work, published as [128], a comparison of sinks of different dimensions in the back-end of line (BEOL) is carried out experimentally using dedicated heat sinks for the devices. Starting from the proof-of-concept done before, we now move to a more compact device and sink area with the target of still demonstrating thermal resistance reduction. The quantitative impact of the area of the sink used on helping heat evacuation through the BEOL path is experimentally explored.

4.5.1 Device under Test

The devices used in this study originate from the 22 nm FDSOI technology from GlobalFoundries [19]. The device gate length is 20 nm, total width is 30 μm for each of these devices composed of 60 fingers of 0.5 μm finger width. In this work, three devices based on the same core FET above are considered. Apart from a standard device without any heat sink, two other devices with sinks in the BEOL are designed: one with a smaller sink and the other with a larger sink dimension. With the thermal resistance expected to decrease with increasing cross-sectional area of the sink, the larger sink is expected to ease heat evacuation further through the BEOL.

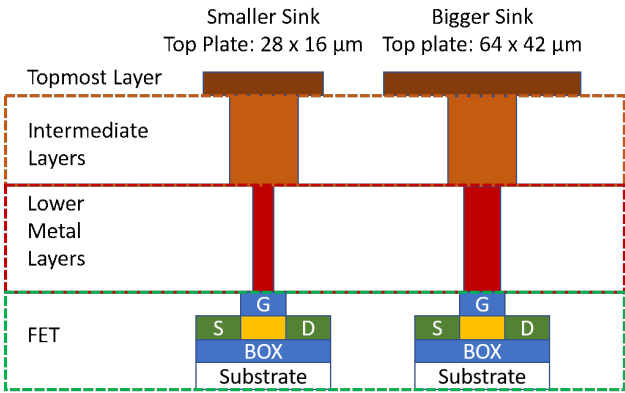


Figure 4.20: Cross-sectional schematic of the sink device in BEOL.

Figure 4.20 and **Figure 4.21** illustrate the sink configurations with just the area of the metal plate and connections being bigger for the bigger sink. The heat sink consists of a metallic pad right above the FET over which the passivation layer is removed. This top metal plate is connected down to the FET using metallic connections in the intermediate and lower metal layers below and eventually connected by vias to the gate above the gate access on the side of the FET as seen in **Figure 4.21**. The dimension of this plate on the top metal is $28\text{ }\mu\text{m}$ by $16\text{ }\mu\text{m}$ for the smaller sink device and $64\text{ }\mu\text{m}$ by $42\text{ }\mu\text{m}$ for the bigger sink device respectively. The heat sink itself is similar in configuration but much smaller than in our last work ($234\text{ }\mu\text{m}$ by $114\text{ }\mu\text{m}$) to reduce additional parasitics while having a more compact device.

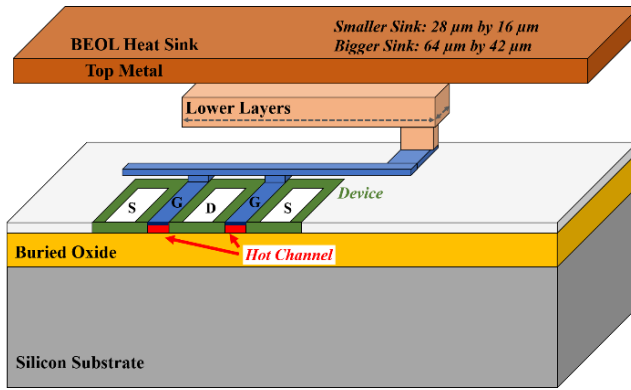


Figure 4.21: Schematic for 3D sink configuration.

4.5.2 Measurement Setup

The RF characterization technique is used again for SH characterization. S-parameters are measured in a frequency range from 100 kHz to 1 GHz, de-embedded, and converted to Y parameters. These measurements use two Ground-Signal-Ground RF $|Z|$ probes of $100\text{ }\mu\text{m}$ -pitch. The probes are compatible with high-temperature measurements up to the necessary temperature value of 125°C . The transition in g_d with frequency is caused not only due to SH but also due to the substrate and back-gate network [98] [129]. In this context, the importance of the zero-temperature coefficient (ZTC) point, where dynamic SH vanishes becomes of interest. The transition due to the substrate network is removed by considering the transition in g_d at the zero-temperature coefficient

(ZTC) point where there is no transition due to SH. R_{th} and capacitance C_{th} are then extracted like the previous case. The DC measurements in temperature are made at 25, 50, 75, 100, and 125 °C respectively. To have a steady temperature value while measuring, the whole system was let to steady for at least half an hour to ensure temperature stability. The extractions have been made in saturation at a V_d of 0.8 V. The back gate was grounded ($V_{bg} = 0$ V).

4.5.3 Results and Discussion

IV Characterization

It is verified that DC performances of the devices are similar, ensuring a fair comparison between the devices. From the I_d - V_g and g_m - V_g curve shown in **Figure 4.22**, the similarity in DC performance of the devices can be seen.

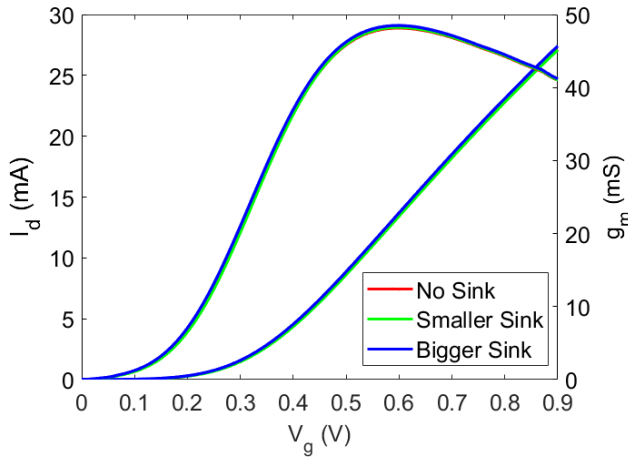


Figure 4.22: Drain current I_d and transconductance g_m vs gate voltage V_g for the different sink cases recorded in saturation at $V_d = 0.8$ V.

The second derivative method can be used to estimate the threshold voltage. From the well-overlapping curves in **Figure 4.23**, it is evident that the V_{th} of the three sink devices is also similar and found to be around 0.29 V.

From the I_d - V_d plot in **Figure 4.24**, a slight improvement in I_d in saturation is observed for the bigger sink case, suggesting weaker self-heating there.

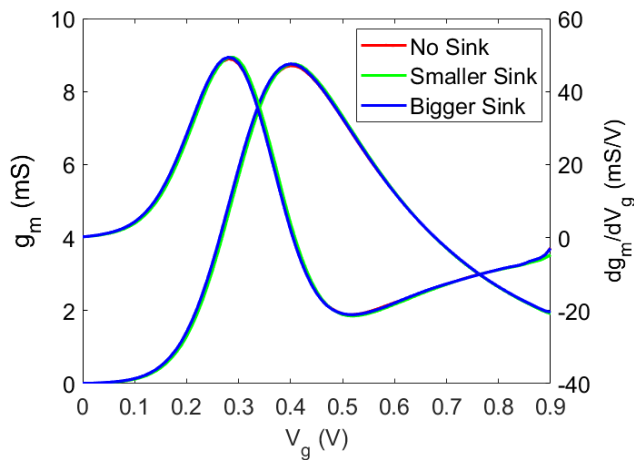


Figure 4.23: Drain current I_d and transconductance g_m vs gate voltage V_g for the different sink cases recorded in linear at $V_d = 50$ mV.

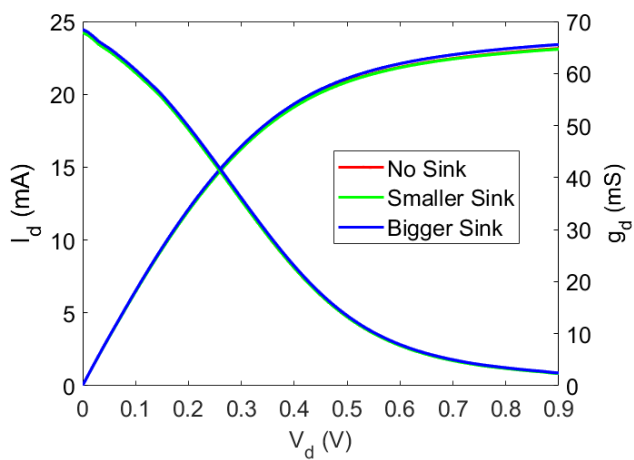


Figure 4.24: Drain current I_d and output conductance g_d vs drain voltage V_d for the different sink cases at $V_g = 0.8$ V.

SH characterization

Figure 4.25 shows the variation of output conductance g_d with frequency for the no sink and bigger sink device at $V_d = 0.8$ V and two different V_g biases of 0.8 and 0.9 V. Higher value of g_d obtained for the bigger sink for two different biases demonstrate the fact that it is less affected by self-heating compared to the other sinks. **Figure 4.26** demonstrates the variation of gain A_V (g_m/g_d) with the usage of the sinks. It is observed that A_V decreases for the case of the big sink compared to the no sink owing to improvement in g_d .

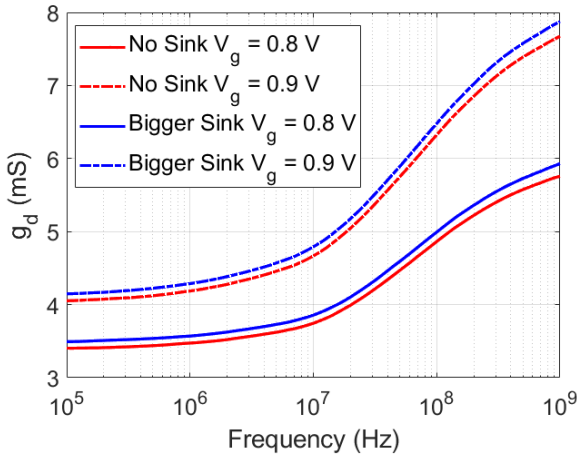


Figure 4.25: Output conductance g_d vs frequency for no sink and bigger sink cases at $V_d = 0.8$ V and $V_g = 0.8$ and 0.9 V.

In **Figure 4.27**, the variation of drain current I_d normalized with respect to the value at 25°C with temperature is shown. The fact that the bigger sink has the highest I_d versus temperature slope (having a steeper slope) demonstrates the lowest SH is observed there. The reason for the above can be seen in [109] as $\partial I_d / \partial T$ is higher at higher temperatures representative of higher SH computed from I_d versus temperature. For a V_d of 0.8 V, two different bias conditions in V_g in 0.8 V and 0.9 V are considered, and the aforementioned trends are verified for both cases. At V_g 0.9 V, a higher $\partial I_d / \partial T$ is seen as this bias point is further away from the ZTC than the V_g 0.8 V case.

The SH-related variation in drain capacitance C_{dd} is observed to be around three orders of magnitude in **Figure 4.28** similar to observations in previous work in [109].

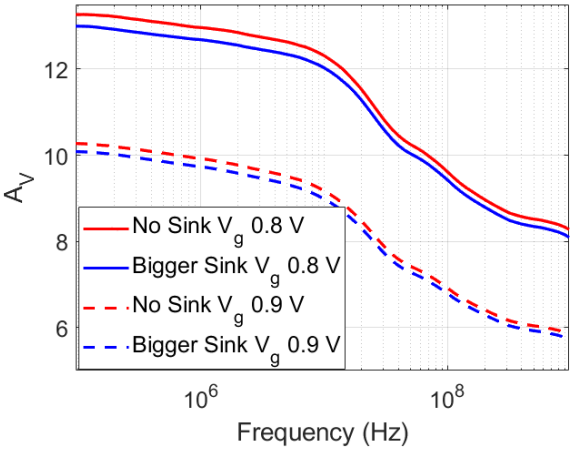


Figure 4.26: Gain A_V vs frequency for the no sink and bigger sink cases at $V_d = 0.8$ V and at V_g of 0.8 and 0.9 V.

Table 4.4 summarizes the comparison of the devices from an SH perspective. The absolute value of $\frac{\partial I_d}{\partial T}$ is found to be highest for the bigger sink and lowest for the no-sink device, confirming the weakest and the strongest SH in their cases respectively. A combination of the above parameters results in the lowest value of R_{th} for the bigger sink. An average R_{th} reduction of 4.7% and 8.9% on using the smaller and bigger sink respectively is observed over multiple dies. The C_{th} values observed are similar to the values reported in [109], slightly lower owing to the lower R_{th} observed here possibly from the substrate network impact correction.

Table 4.4: Self-Heating Parameters. $V_g = V_d = 0.8$ V.

Sink Type	$g_{d,LF}$ (mS)	Δg_d (mS)	$\frac{\partial I_d}{\partial T}$ ($\mu\text{A K}^{-1}$)	R_{th} Normalized ($\text{K}\mu\text{m/mW}$)	C_{th} (pJ K^{-1})
No Sink	3.4	1.81	−10.54	201.5	4.52
Smaller Sink	3.35	1.82	−11.12	192.5	4.7
Bigger Sink	3.49	1.87	−11.88	182.2	4.84

Table 4.5 clearly demonstrates the impact of sink size on SH reduction including comparisons with our previous work [109]. Compared to the sink in

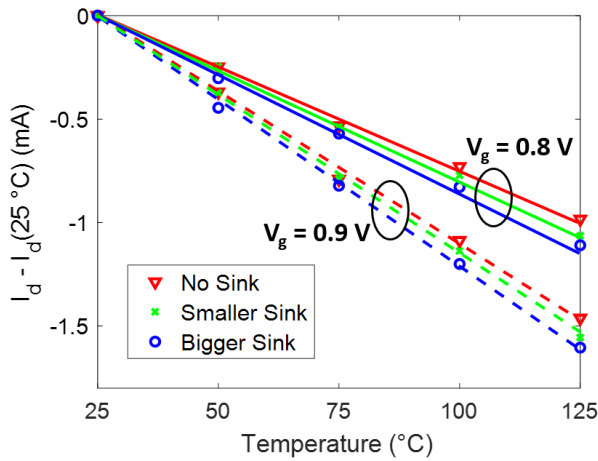


Figure 4.27: Drain current I_d vs temperature for the different sink cases at $V_d = 0.8$ V and at V_g of 0.8 and 0.9 V.

[109], shrinking sink area by a factor of 60 (bigger sink) and 10 (smaller sink) makes the percentage R_{th} reduction go down from 20% (in [109]) to 8.9% and 4.7% for bigger and smaller sink in this work.

Table 4.5: Thermal Resistance Reduction Comparison with Sink Size.

Sink Top Plate Size	Smaller Sink (28x16 μm^2)	Bigger Sink (64x42 μm^2)	Sink in [109] (234x114 μm^2)
Area Ratio w.r.t [109]	1/60	1/10	1
% R_{th} Reduction	4.7%	8.9%	~20%

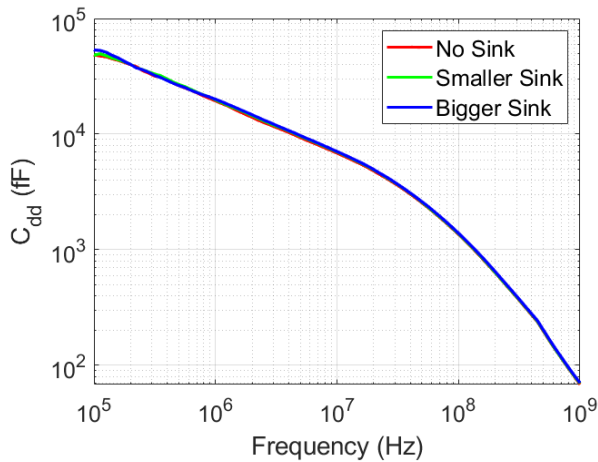


Figure 4.28: Drain capacitance C_{dd} vs frequency for the different sink cases at $V_d = V_g = 0.8\text{ V}$.

Results on Multiple Dies

The trends in the thermal resistance reduction with the sink are verified over multiple dies, with an increased reduction with sink size as seen in **Table 4.6**, **Table 4.7** and **Table 4.8**. The R_{th} reduction with the smaller sink ranges from 3.3% to 6.3% whereas with the bigger sink ranges from 7.4% to 9.7% over the three dies.

Table 4.6: Thermal Resistance Computation on Die1. $V_g = V_d = 0.8\text{ V}$.

Device	$g_{d,LF}$ (mS)	Δg_d (mS)	$\frac{\partial I_d}{\partial T}$ ($\mu\text{A K}^{-1}$)	I_d (mA)	R_{th} ($\text{K}\mu\text{m}/\text{mW}$)	ΔT ($^{\circ}\text{C}$)
No Sink	3.40	1.81	−10.54	22.85	201.5	122.8
Smaller Sink	3.35	1.82	−11.12	22.83	192.5	117.2
Bigger Sink	3.49	1.87	−11.88	23.13	182.2	112.4

In specific, the averaged I_d versus temperature plot demonstrates a linear trend for all the three sink cases as shown in **Figure 4.29** below.

Table 4.7: Thermal Resistance Computation on Die2. $V_g = V_d = 0.8$ V.

Device	$g_{d,LF}$ (mS)	Δg_d (mS)	$\frac{\partial I_d}{\partial T}$ ($\mu\text{A K}^{-1}$)	I_d (mA)	R_{th} ($\text{K}\mu\text{m}/\text{mW}$)	ΔT ($^{\circ}\text{C}$)
No Sink	3.60	1.86	-9.79	23.06	219.7	135.1
Smaller Sink	3.68	1.92	-10.6	23.45	205.9	128.7
Bigger Sink	3.64	1.91	-10.98	23.41	198.3	123.8

Table 4.8: Thermal Resistance Computation on Die3. $V_g = V_d = 0.8$ V.

Device	$g_{d,LF}$ (mS)	Δg_d (mS)	$\frac{\partial I_d}{\partial T}$ ($\mu\text{A K}^{-1}$)	I_d (mA)	R_{th} ($\text{K}\mu\text{m}/\text{mW}$)	ΔT ($^{\circ}\text{C}$)
No Sink	3.40	1.82	-10.25	22.92	207.8	127.0
Smaller Sink	3.31	1.80	-10.57	22.78	200.9	122.1
Bigger Sink	3.42	1.84	-11.13	23.04	192.4	118.2

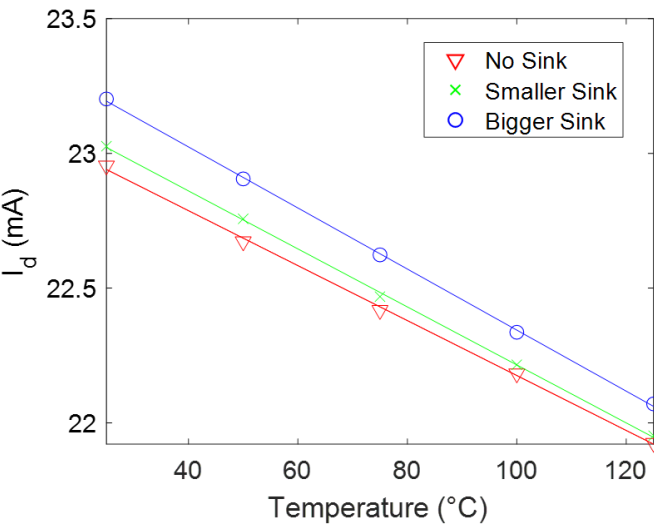


Figure 4.29: Averaged drain current I_d vs temperature over the measured dies for the three sink cases at $V_g = V_d = 0.8$ V.

Temperature Reduction by Using Sink

From **Table 4.6**, **Table 4.7** and **Table 4.8**, it is seen that using the bigger sink causes a reduction in device temperature by around 10-12 °C compared to the no sink case at bias condition $V_g = V_d = 0.8$ V. This observation is directly in line with the R_{th} reduction with sink and helps increase the device lifetime. From theoretical expectations in **Figure 4.5**, an equivalent reduction can help in increasing device lifetime by a factor of 2.

Improvement of Drain Current I_d by Using Sink

Having seen the impact of the sink on thermal resistance improvement, we now consider the improvement it brings to the drain current I_d . It is observed that the bigger sink helps improve the I_d by around 0.5 to 1.5%.

Table 4.9: Die1: Improvement of I_d with Bigger Sink at $V_d = 0.8$ V and $V_g = 0.8$ and 0.9 V

V_g (V)	I_d No Sink (mA)	I_d Bigger Sink (mA)	Improvement (%)
0.8	22.87	23.14	1.17
0.9	27.12	27.41	1.08

Table 4.10: Die2: Improvement of I_d with Bigger Sink at $V_d = 0.8$ V and $V_g = 0.8$ and 0.9 V

V_g (V)	I_d No Sink (mA)	I_d Bigger Sink (mA)	Improvement (%)
0.8	23.07	23.42	1.52
0.9	27.29	27.66	1.36

Table 4.11: Die3: Improvement of I_d with Bigger Sink at $V_d = 0.8$ V and $V_g = 0.8$ and 0.9 V

V_g (V)	I_d No Sink (mA)	I_d Bigger Sink (mA)	Improvement (%)
0.8	22.92	23.04	0.53
0.9	27.22	27.35	0.46

Improvement of Transconductance g_m by Using Sink

An improvement in transconductance is observed too: the bigger sink helps improve the g_m by around 0.4 to 0.6%.

Table 4.12: Die1: Improvement of g_m with Bigger Sink at $V_d = 0.8$ V and $V_g = 0.8$ V and 0.9 V

V_g (V)	g_m No Sink (mS)	g_m Bigger Sink (mS)	Improvement (%)
0.8	44.26	44.49	0.53
0.9	41.04	41.19	0.37

Table 4.13: Die2: Improvement of g_m with Bigger Sink at $V_d = 0.8$ V and $V_g = 0.8$ V and 0.9 V

V_g (V)	g_m No Sink (mS)	g_m Bigger Sink (mS)	Improvement (%)
0.8	43.98	44.17	0.43
0.9	40.60	40.83	0.57

Table 4.14: Die3: Improvement of g_m with Bigger Sink at $V_d = 0.8$ V and $V_g = 0.8$ V and 0.9 V

V_g (V)	g_m No Sink (mS)	g_m Bigger Sink (mS)	Improvement (%)
0.8	44.82	44.86	0.09
0.9	41.37	41.62	0.62

Impact of Sink on RF Performance

Having observed the impact of sink size on the thermal performance of the device, we consider the corresponding impact on the RF performance. To do so, the sink devices are de-embedded with dedicated no-sink device open structures; this allows us to take into account the additional parasitics from the sink compared to the no-sink case. Note that de-embedding with respect to the corresponding device de-embedding structure would not include these additional parasitics of the sink structure, therefore the no sink device de-embedding structure is used.

In **Figure 4.30**, the impact of the sink on the RF figure of merit (FoM) cutoff frequency f_T and $f_{\max}$ is demonstrated. The peak f_T and $f_{\max}$ are computed from current gain H_{21} and unilateral power gain U at V_g corresponding to $g_{m,\max}$ (0.6 V in this case). f_T is seen to degrade around 17.5% and 46%, whereas $f_{\max}$ degrades around 3.4% and 12.8% for the smaller sink and bigger sink respectively. Analytically, as previously presented in **Equation 2.38** and **Equation 2.39**, f_T is inversely proportional to $C_{gg,T}$ whereas $f_{\max}$ has a more complicated dependence on multiple parameters (like source resistance R_s , gate-to-drain capacitance $C_{gd,T}$) including gate resistance R_g which is of interest here. To understand the variation in f_T - $f_{\max}$, the trends on total gate capacitance $C_{gg,T}$ and gate resistance R_g are shown in **Figure 4.31**.

The degradation in f_T is mainly owing to increased $C_{gg,T}$ which affects f_T inversely. It is expected that due to the additional parasitics that are brought in by the sink, there would be a degradation in the RF performance, which is seen. However, the $f_{\max}$ degradation is much lesser because of a reduction in gate resistance R_g , which has an inverse proportionality with $f_{\max}$. As the sink connection is not in series with the standard gate path, we do not expect to degrade the gate resistance; in fact, a reduction is observed in measurements. A tradeoff between using the sink to improve SH performance while not degrading RF performance is therefore established. The importance of the sink still comes into play for analog and certain RF applications as the f_T - $f_{\max}$ offered by the technology is high enough to provide for them despite the degradation in RF performance owing to the sink.

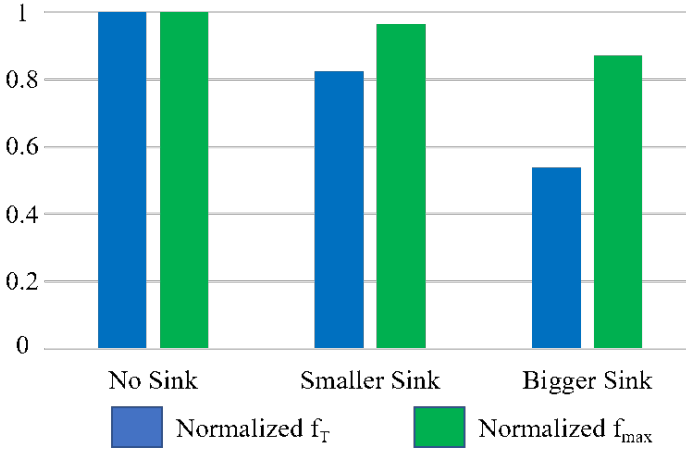


Figure 4.30: Reduction in peak cutoff frequency f_T at $V_g = 0.6$ V (corresponding to $g_{m,max}$) and $V_d = 0.8$ V. $f_T - f_{max}$ are normalized with respect to the no-sink case.

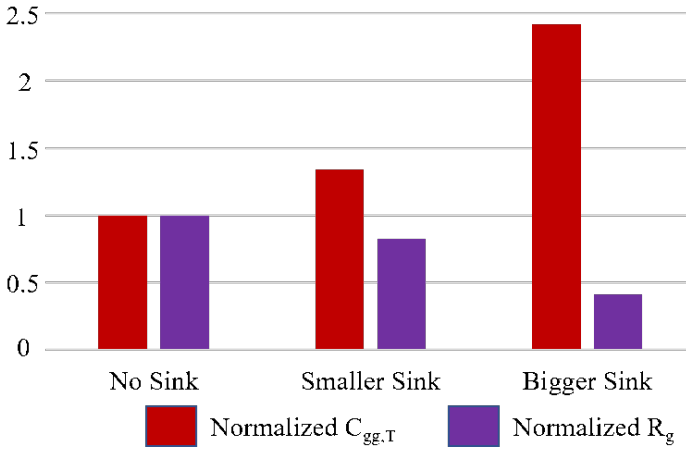


Figure 4.31: Variation in total gate capacitance $C_{gg,T}$ and gate resistance R_g , normalized with respect to the no-sink case.

4.5.4 Summary

The thermal resistance of a device using gate-connected heat sinks is observed to reduce with increasing sink size. A mean reduction of 4.7% and 8.9% in R_{th} compared to a standard no sink device is observed with the connection of a smaller and larger sink respectively, with the trends being verified over multiple dies with limited impact on C_{th} . The impact of the sink on the RF FoMs is investigated and it is observed that the cutoff frequency f_T degrades 17.5% and 46% mainly due to increased gate capacitance. The degradation on f_{max} is limited to around 3.4% and 12.8% on using the smaller and the bigger sink respectively owing to reduced gate resistance observed.

4.5.5 Impact of Device Length Variation on SH and RF FoMs

To assess the improvement in SH coming from the sink with the corresponding compromise on the RF FoMs, we compare it with the case of simply moving to longer device lengths. This would result in a similar trend as longer devices would experience lesser SH as demonstrated in literature while reducing the RF FoMs.

From the PDK model, this impact is investigated for three device lengths: 20 nm, 40 nm, and 100 nm, while keeping other dimensions the same as those of the device used in the study. It is observed that transitioning from a 20 nm to a 40 nm length device results in an R_{th} reduction of around 15.8%, with a corresponding f_T reduction of 37.3%. Moving to a longer 100 nm length can further reduce R_{th} to 40.9%, but the penalty in f_T becomes as high as 74.7% in that case.

Table 4.15: Values of Peak f_T and R_{th} with Reduction

L (nm)	Peak f_T (GHz)	% f_T Reduction	R_{th} (K μ m/mW)	% R_{th} Reduction
20	316	-	149	-
40	198	37.3%	126	15.8%
100	80	74.7%	88	40.9%

Comparing this with the heat sink in our study, we saw that in order to gain a 9% improvement in R_{th} , f_T needed to be compromised by around 46%. Contrarily, moving to a 40 nm node from a 20 nm node could bring in an effective change of 16% R_{th} reduction with a 37% f_T reduction. This could thus be an alternative SH reduction method in cases where moving to longer device lengths is possible.

However, with the need to go to smaller nodes anyway with device scaling, the possibility of using a heat sink becomes an obvious option to look into deeper. It is to be noted that despite the degradation in f_T - f_{max} with the sink, for a high enough f_T - f_{max} offered by the device technology, the possibility of using the sink is still expected for applications up to a few tens of GHz frequency range.

4.6 Conclusions

To sum up, in this chapter, heat sinks in the BEOL connected to the gate terminal of the MOSFET have been investigated, and their efficiency in heat evacuation has been demonstrated. The proposed sink design is solely in the BEOL; this makes this heat evacuation method much more flexible to implement compared to others like substrate engineering or device layout optimization. Starting from the proof-of-concept demonstration of the sink, a possibility of around 20 - 30% reduction in the thermal resistance has been demonstrated in multiple test cases. By experimentally studying sinks of different top areas, the fact that sink efficiency is directly correlated to the sink area is established; bigger sinks help greater heat evacuation. The improvement in device performance through I_d and g_m and in expected reliability based on device temperature reduction due to the usage of the sink are stressed upon as additional advantages. However, the additional parasitics from the sink result in a degradation in the RF FoMs. In fact, it is observed that in order to have an R_{th} improvement of 10%, the sink area needed would compromise the f_T by around 46%, coming from the additional parasitics of the sink. A tradeoff between SH performance and RF performance coming from the presence of the sink is therefore established. To put the impact of the sink into perspective, a comparison with the case of moving to longer device lengths is made; it is seen from PDK simulations that going to 40 nm device length from 20 nm provides a better SH betterment for f_T reduction scenario. Nevertheless, if the sink is used on a technology that provides high enough f_T - f_{max} , despite the degradation in FoMs the possibility of operation up to a certain range would be possible. Specifically, the benefit of reduced device temperature and thus increased lifetime can be very handy for modern applications requiring robust performance. Additionally, the sink can be implemented on other technologies or substrates, making it a generic thermal solution for self-heating problems in state-of-the-art devices.

From a PDK modelling perspective, the usage of first-order SH models needs to be improved as seen from the fourth-order models needed for fitting measurements. Also, it is not possible to have electro-thermal simulations along with the design itself yet. Having thermal models considering heat evacuation through the BEOL would be helpful for designers in the future.



5. Conclusion and Perspectives

5.1 Conclusion

5.1.1 Summary

In this thesis, the behaviour of advanced MOSFETs at high temperatures is investigated with a special focus on heat evacuation through the back-end of line. The pertinence of growing high-temperature electronics markets like automotive and aerospace applications, among others, pushes the need to have a thorough understanding of the thermal response of the device performance with temperatures. On the other hand, growing current and power densities in advanced MOSFETs raise self-heating effect in these devices, highlighting the need to better assess and alleviate this issue.

By mimicking high-temperature conditions in the laboratory, the way DC, analog and RF performance metrics of MOSFETs are impacted is investigated. Notably, variations in the figures-of-merit like f_T and f_{max} are also found to be bias-dependent and thus specific to the regime of operation of the devices. They are seen to be directly impacted by the variations in the SSEC parameters with temperature; specifically f_T is seen to be directly linked to transconductance g_m . Nevertheless, the temperature dependence of the metrics showcases the need to keep them in mind for applications that will have to face varying temperatures. PDK models are currently mainly limited to 125 °C whereas in literature it is quite clear that ambient temperatures can go up even higher. A comparison of measurement results with that of the PDK is made. Therefore, extending the temperature range of PDK models is deemed necessary to provide more conviction to designs for upcoming high-temperature applications.

With the self-heating problem in advanced MOSFETs established, different aspects related to the characterization of self-heating are investigated. Firstly, the impact of higher ambient temperature is studied in measurements and PDK and a thermal resistance reduction with temperature are seen in both cases. This trend is in line with theoretical findings in literature where the thermal conductivity of the SiO_2 BOX is seen to increase with temperature. Secondly, a comparison of the two most prominent self-heating characterization techniques for advanced MOSFETs, namely the RF technique and the gate-resistance technique, is made. On the same test device, the RF technique showed almost 1.8 times higher thermal resistance compared to the gate-resistance technique from measurements. From a similar study comparing PDK models which use these techniques for SH modelling, the thermal resistance using the RF technique was seen to be 1.35 times higher. From these findings, the fundamental

principle of the DC gate resistance technique that the gate temperature and channel temperature are equal due to negligible thermal isolation between the gate and the channel is brought to question. Non-negligible heat evacuation through the gate path causing a temperature drop across the gate stack could be a reason for the difference. On the other hand, the drawbacks of the RF and gate resistance techniques are looked into in detail. It is noted that the extraction of the slope of the drain current with temperature for the RF technique and the gate resistance variation with temperature for the gate-resistance technique respectively need to be accurately extracted as they can affect the estimation of thermal parameters considerably. The possible error bars in thermal resistance estimation owing to their extraction uncertainty are studied. Cross-examining different techniques could help assess SH better and help us assess the different heat evacuation paths. Additionally, it has been shown that layout-related effects could impact self-heating extraction; for example, if additional gate accesses are used as in the case of the gate-resistance technique, they could result in cooling of the device thereby underestimating thermal resistance. The underestimation of R_{th} is seen to be as high as 20% in our study case with a four-terminal gate access structure compared to the same device without these additional accesses. For the same core MOSFET, variations in the layout, interconnections and series resistances could affect SH extraction using the RF technique.

Given the self-heating concerns in advanced nodes, the mitigation of the same becomes of utmost importance. Most studies in literature on heat evacuation in MOSFETs primarily concentrate on heat dissipation through the substrate path, often overlooking the potential for heat evacuation through the BEOL. This assumption works relatively well for bulk devices, where the substrate offers a relatively straightforward path for heat to dissipate. However, in SOI devices, the presence of a highly thermally insulative SiO_2 BOX layer significantly increases the thermal impedance of the downward heat flow through the substrate. This fact makes the investigation of the highly underestimated evacuation upwards through the BEOL crucial. In our studies, we study in detail the much-ignored heat evacuation possibility through the BEOL and propose a novel heat evacuation technique for the same. One of the major findings of this work is the experimental demonstration of effective heat evacuation through the BEOL by utilizing a heat sink connected to the gate, as detailed in Chapter 4. This approach shows that depending on the size of the heat sink, a reduction in thermal resistance (R_{th}) of up to 20% can be achieved. The correlation between the size of heat sinks and the reduction in thermal resistance (R_{th}) is

demonstrated as the reduction in thermal resistance using the sink is seen to be proportional to the sink area. This is a significant improvement that challenges the traditional focus solely on substrate-mediated heat dissipation. Furthermore, this heat evacuation technique does not require any process modifications like alternate BOX materials or device geometry modification which makes it flexible to use over devices on different technologies. However, the additional parasitics coming from the sink degrade the RF performance and thus a tradeoff is seen with respect to the thermal and RF performance. The pros and cons of using the sink are summarized below.

Advantages of Using the Heat Sink

1. **Reduction in Thermal Resistance:** The use of a gate-connected heat sink can significantly reduce the thermal resistance by as much as 20%. This reduction is crucial for lowering device temperature and enhancing performance. Larger heat sink areas are significantly more effective at reducing thermal resistance, but at the cost of RF performance as seen later.
2. **Temperature Reduction:** Employing larger heat sinks decreases the device temperature by about 10-12°C for FDSOI MOSFETs in saturation ($V_g = V_d = 0.8$ V) in our study case, potentially doubling device lifetime as per device lifetime trends in literature.
3. **Improvement in Drain Current and Transconductance:** Heat sinks also contribute to improvements in drain current (I_d) by approximately 0.5% to 1.5% and in transconductance (g_m) by about 0.4% to 0.6%, leading to better device performance.

Disadvantages of Using the Heat Sink

Degradation in RF Performance: The addition of heat sinks, particularly larger ones, results in a degradation of RF performance metrics such as the cutoff frequency (f_T) and maximum oscillation frequency (f_{max}). The degradation ranges from 17.5% to 46% for f_T and from 3.4% to 12.8% for f_{max} depending on whether a smaller or a bigger sink is used, primarily due to a large increase in total gate capacitance ($C_{gg,T}$), which inversely affects f_T . While a bigger sink helps thermal evacuation, it comes at the cost of increased parasitics, degrading RF performance.

In conclusion, addressing temperature-related concerns in advanced MOSFETs is found to be critical. Some perspectives and scope for future work are mentioned in [Section 5.2](#).

5.1.2 Connection Between the Chapters

The connections between the ideas explored in this thesis are shown in **Figure 5.1**. **Chapter 2** provides the base for understanding the impact of high temperatures of devices in general, thus paving the way for studies on self-heating which also results in higher device temperatures. The reduction in thermal resistance coming from gate-connected sinks explored in **Chapter 4** is in line with the fact that gate-accesses for the gate-resistance technique in **Chapter 3** can aid in cooling. Finally, and most importantly, the bigger picture of the heat evacuation paths in the MOSFET is the underlying common link between **Chapter 3** and **Chapter 4**. Possible differences between the RF and Gate-resistance technique, heat evacuation through gate-connected sinks or accesses all help showcase the heat evacuation through the BEOL, which has been largely ignored in literature.

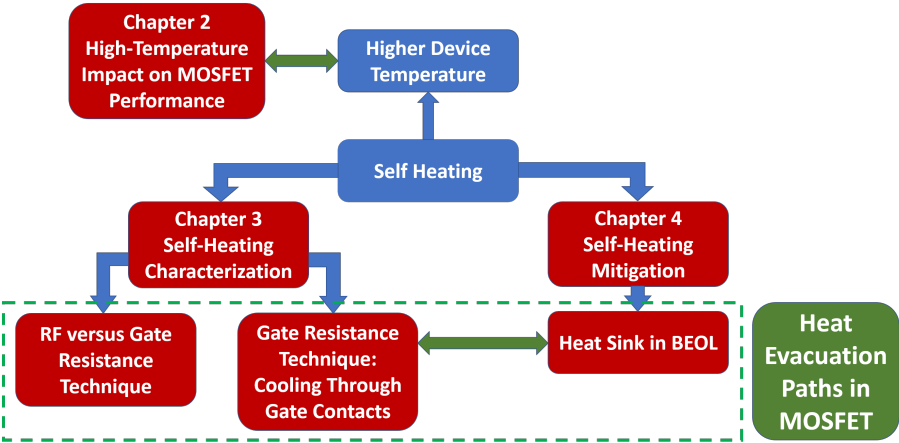


Figure 5.1: Connections between the ideas explored in the thesis.

5.2 Perspectives

The general perspectives that can be taken away from the work done in this thesis are listed below.

5.2.1 FDSOI technology for temperature applications

While the main Figures of Merit (FoMs) like peak f_T and $f_{\max}$ are reduced with temperature, the 22 nm FDSOI node offers such a high f_T and $f_{\max}$ that despite the reduction, applications up to high operation frequency ranges like 30-40 GHz are still possible for temperatures as high as 175 °C. Apart from temperature aspects, the good stability of FDSOI technology in radiation environments also establishes it as a mature technology for harsh-environment applications.

—— Back gate biasing ———

This is a crucial tuning knob offered by the FDSOI technology and can be used very effectively to cater to the impact of temperature variations on device performance. The reduction in threshold voltage with increased temperatures can be countered by adequately applying a back-gate bias and with the wider range of threshold voltage tuning in FDSOI, this can address the aforementioned problem to a much better extent. However, from an RF performance point of view, it is seen that the back-gate bias cannot counter the reduction in the main Figures of Merit (FoMs) like peak f_T and $f_{\max}$.

—— Sustainable Electronics ———

While alternative technologies like GaN or SiGe can be more effective for high-temperature applications, the fact that FDSOI technology uses readily available materials makes it more ecological. Other materials like Gallium and Germanium have a scarcer availability with more complex extraction processes.

5.2.2 Thermal Modelling and Challenges

The experimental results shown above highlight the need for a more comprehensive approach to thermal management in advanced SOI devices, taking into account not only the traditional substrate path but also the role of BEOL and device layout in heat dissipation. This understanding could lead to improved designs that better manage thermal effects, thereby enhancing device performance and reliability.

PDK Model: Missing Links

In order to strengthen the experimental assessment, thermal TCAD modelling and comparison with the PDK SH models would help understand the heat evacuation scenario better. Unfortunately, there exist quite a few missing links in this context which are highlighted below.

PDK: BEOL Impact Neglected

- **Issue:** Process Design Kits provide essential data for IC design but totally neglect the thermal impacts of the BEOL. SH modelling in the PDK is limited to a SH switch that can be turned on or off to simulate SH but this is totally independent of the BEOL.
- **Consequence:** Designers currently are unaware of the thermal impact the BEOL connections have on the thermal problem. How the heat evacuation would happen through the BEOL paths would have to be included in the future.

PDK: Inaccurate Thermal Models

- **Issue:** Thermal models in PDKs tend to be oversimplified and do not account for complex heat transfer mechanisms affected by BEOL configurations. This is evident from a first-order thermal RC fitting network used in the EXT and PLUS PDKs for 22FDX[®] technology.
- **Consequence:** Differences in the nature of fitting obtained in measurements where a fourth-order network is needed compared to the model with the first-order network.

TCAD Modelling: Lack of Information

- **Issue:** Using TCAD thermal modelling could be an excellent way of visualizing the thermal problem. However, for advanced MOSFETs, numerous issues like actual thermal conductivities of thin film materials used, thermal resistance between the boundaries of different films, lack of knowledge of exact geometry and composition of the device etc pose significant challenges in ascertaining with conviction the thermal parameters. Details of these challenges are discussed in [Appendix A](#).
- **Consequence:** Lack of solid information for TCAD modelling is a major hindrance to comparing experimental and thermal modelling results.

Different aspects of the thermal modelling of advanced FDSOI MOSFETs are discussed in [Appendix A](#). Our attempt at understanding the heat evacuation in these MOSFETs from a physical perspective is demonstrated, including the various challenges faced in the process which need to be overcome to have

better TCAD models.

Addressing the Gaps

In order to address the aforementioned gaps, the correlation between modelling and measurements needs to be done. Modelling of heat evacuation through the BEOL needs to be included in the PDK along with upgraded self-heating models used there. Reliable TCAD modelling can only happen through a strong collaboration with industrial partners with clear information about the device materials, properties and geometries.



Appendices

A Analytical Thermal Model

This appendix discusses the different aspects of the thermal modelling of advanced FDSOI MOSFETs. Previously, attempts at TCAD thermal modelling have been made in [79] [85] [130], mainly on older technology nodes. Our attempt at understanding the heat evacuation in these MOSFETs from a physical perspective is shown below, including the various challenges faced in the process which need to be overcome to have better TCAD models.

Four heat evacuation paths are established in **Chapter 4**, namely the gate, source and drain paths through the BEOL and BOX-Substrate path through the FEOL. We attempt to estimate the thermal resistance of the paths; this is calculated using the material thermal conductivities and dimensions in **Equation 4.1**, for a starting point.

A.1 Complexity of the Real Thermal Problem

Some of the major aspects and assumptions for thermal analytical and TCAD modelling are:

- i) **Boundary conditions:** The temperature at the end of each path is often assumed to be equal to that of the ambient temperature. This might not be the case; in **Chapter 4** the fact that the sinks could help in heat evacuation shows that convective or radiative heat transfer to the environment is possible. This can happen only if there is a temperature difference between the environment and the actual material boundary.
- ii) **Estimated thermal resistances:** The actual thermal evacuation is not a simple case as discussed above; the thermal resistances estimated for the different layers might not directly be related linearly to their thicknesses or areas.
- ii) **Device Geometry:** A very simplified device geometry is considered in our case. The actual device simulation should consider spacers, raised source-drain regions etc.
- iii) **Thermal conductivity values:** Accurate knowledge of the thermal conductivity of materials is crucial. Many numbers from literature are often extrapolations for thin-film materials.
- iv) **Temperature dependence of thermal conductivities:** The thermal conductivity is often assumed to be homogenous for a whole block of material but in reality, since it is a function of temperature, the values can differ based on the temperature gradient.

- v) Layout and thermal coupling: Multi-finger MOSFETs are often used in practice and there can be thermal coupling between adjacent fingers giving rise to a temperature gradient across the geometry with an expected peak temperature at the centre of the fingers with lower temperature on the edges (shown in Chapter 4).
- vi) Thermal boundary resistances: The boundary resistances at each of the interfaces need to be considered and can play a crucial role in state-of-the-art devices. Precise knowledge of the materials and interfaces is therefore necessary, especially the gate stack which consists of multiple films.

A.2 Computation of Thermal Resistances

Using a simple approach of estimating the thermal resistance of each of the material blocks, we try to have a basic idea of the thermal evacuation problem and the relative importance of the heat evacuation paths. While this approach is quantitatively not accurate, our target is to have a qualitative analysis of the problem. Comparing mainly the gate path and BOX-substrate path, we compare the thermal resistance of the two to check their relative importance. The modelling is made for the device dimensions of length 20 nm with the multi-finger case being simplified to a single finger with the same total width of $30\mu\text{m}$.

Bulk Silicon Substrate

The bulk Si substrate is one of the most thermally conductive paths for the heat in the channel to evacuate. With a bulk Si thermal conductivity of $148\text{ Wm}^{-1}\text{K}^{-1}$ [70] and a thickness of around $750\mu\text{m}$, it has the least thermal resistance because of the relatively higher thermal conductivity and also area. To start, we assume that the downward heat evacuation is dictated by the BOX thermal resistance and compute the overall thermal resistance of BOX-Substrate given below.

BOX

The BOX in 22FDX[®] technology consists of a 20 nm SiO_2 film. With the thermal conductivity of bulk SiO_2 being $1.4\text{ Wm}^{-1}\text{K}^{-1}$, which is two orders of magnitude lower than that of bulk Si, the impedance to heat evacuation due to the presence of this oxide layer is obvious. Additionally, the thermal conductivity of a 20 nm thin SiO_2 film can be further degraded compared to bulk to around $1\text{ Wm}^{-1}\text{K}^{-1}$ [73] due to phonon boundary scattering.

If a simple calculation of the BOX thermal resistance is made from a

rectangular assumption, the R_{th} turns out to be $3.33 \times 10^4 \text{ KW}^{-1}$ for our device dimensions.

Source and Drain

The thermal resistance of the source and drain regions is dependent on the device dimensions, channel extensions, and raised source-drain configuration. It is to be kept in mind that the thermal conductivity of the thin film Si (and thus that of the source and drain regions) is heavily degraded compared to its bulk counterpart; the 6 nm thin top Si channel is expected to have a thermal conductivity of $9 \text{ Wm}^{-1}\text{K}^{-1}$ compared to the bulk value of $148 \text{ Wm}^{-1}\text{K}^{-1}$ [70]. Raised Source-Drain geometry has a double thermal benefit: it improves the region's thermal conductivity by allowing a larger phonon mean free path, and it lowers its thermal resistance by offering a larger area for heat flow [131]. Thus, knowledge of the exact raised source-drain geometry is crucial to determining the thermal resistance of these paths, which is skipped for the time being.

Gate Stack

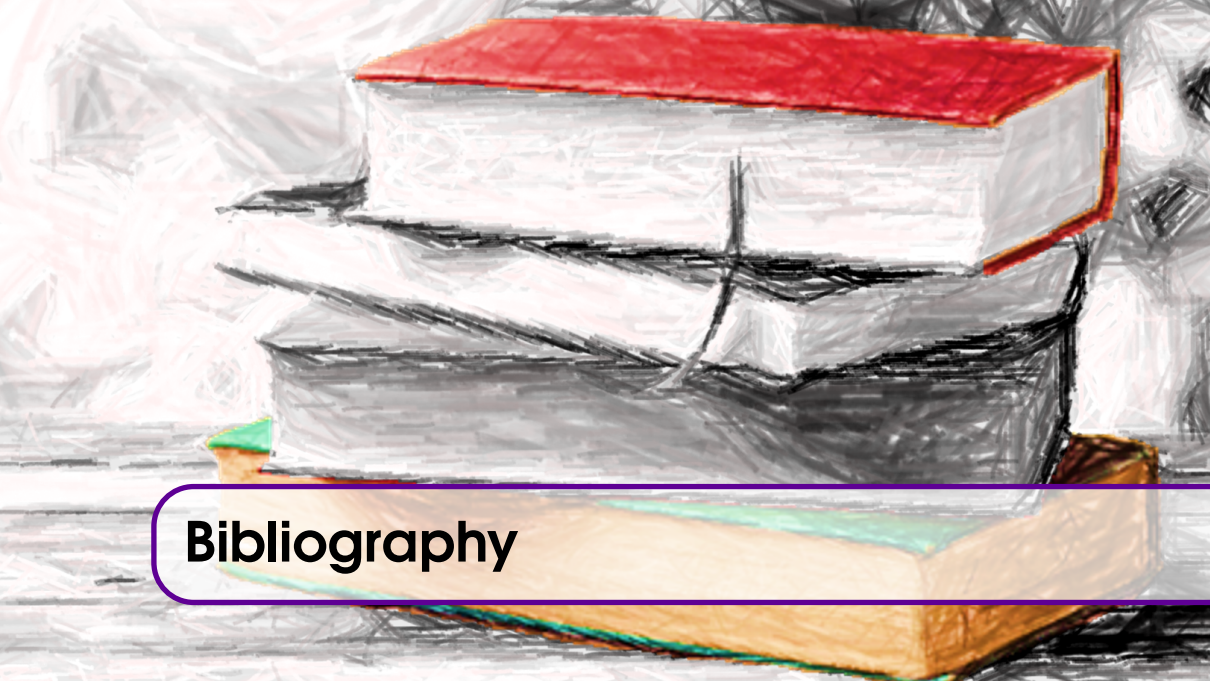
The gate stack, consisting of high-K dielectrics and gate metal, is probably the most complicated entity in the model. Nevertheless, an attempt is made to compare qualitatively the thermal resistance of the gate stack to that of the BOX to see the relative importance of these paths. In our work, we have proceeded to take a gate stack resistance based on observations in [107] to include thermal boundary resistances in the complex stack as well. As shown in **Table 3.17** in Chapter 3, the thermal resistance of the gate stack is found to be 1.67×10^4 , 2.17×10^4 , and $3.33 \times 10^4 \text{ KW}^{-1}$ for HfO_2 thicknesses of 1 nm, 10 nm, and 20 nm respectively.

The main takeaways from this are:

1. It is noted that the thermal resistance for a 20 nm HfO_2 film is similar to that of the 20 nm SiO_2 BOX computed from the rectangular geometrical formula previously (both being equal to $3.33 \times 10^4 \text{ KW}^{-1}$ for the given device dimensions).
2. With a thin gate stack reported to be used in advanced MOSFETs, the thermal resistance of the gate stack can be expected to be lesser than that of the BOX, implying that the heat evacuation path upwards through the gate stack region needs to be considered in addition to the BOX-Substrate path traditionally focused on.
3. The thermal resistance of a 1 nm HfO_2 film is around half of that of a 20 nm film when thermal boundary resistances are included. Thus

scaling down the physical thickness by a factor of 20 reduces the thermal resistance by a factor of 2! This clearly demonstrates the dominant role played by boundary resistances for thin films, and thus knowledge of thermal resistance at each boundary needs to be taken into account for proper modelling.

To have accurate thermal models in future, it is clearly seen that device materials, geometry, dimensions and interfaces need to be known. In addition to that, there is a big scope of work in the physical understanding and analysis of thermal properties in thin film materials, especially experimentally which needs to be undertaken before having a reliable analytical model or going further to TCAD simulations.



Bibliography

- [1] F. Udrea, S. Z. Ali, M. Brezeanu, V. Dumitru, O. Buiu, I. Poenaru, M. F. Chowdhury, A. De Luca, and J. W. Gardner, “SOI sensing technologies for harsh environment,” in *CAS 2012 (International Semiconductor Conference)*, ISSN: 2377-0678, vol. 1, Oct. 2012, pp. 3–10. DOI: 10.1109/SMICND.2012.6400708.
- [2] P. Dreike, D. Fleetwood, D. King, D. Sprauer, and T. Zipperian, “An overview of high-temperature electronic device technologies and potential applications,” *IEEE Transactions on Components, Packaging, and Manufacturing Technology: Part A*, vol. 17, no. 4, pp. 594–609, Dec. 1994, Conference Name: IEEE Transactions on Components, Packaging, and Manufacturing Technology: Part A, ISSN: 1558-3678. DOI: 10.1109/95.335047.
- [3] A. Hassan, Y. Savaria, and M. Sawan, “Electronics and Packaging Intended for Emerging Harsh Environment Applications: A Review,” *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 26, no. 10, pp. 2085–2098, Oct. 2018, Conference Name: IEEE Transactions on Very Large Scale Integration (VLSI) Systems, ISSN: 1557-9999. DOI: 10.1109/TVLSI.2018.2834499.
- [4] C. Claeys and E. Simoen, *Radiation Effects in Advanced Semiconductor Materials and Devices* (Springer Series in Materials Science), en, R. M.

- Osgood, R. Hull, and J. Parisi, Eds. Berlin, Heidelberg: Springer, 2002, vol. 57, ISBN: 978-3-642-07778-4 978-3-662-04974-7. DOI: 10.1007/978-3-662-04974-7.
- [5] B. Patra, R. M. Incandela, J. P. G. van Dijk, H. A. R. Homulle, L. Song, M. Shahmohammadi, R. B. Staszewski, A. Vladimirescu, M. Babaie, F. Sebastiano, and E. Charbon, "Cryo-CMOS Circuits and Systems for Quantum Computing Applications," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 1, pp. 309–321, Jan. 2018, Conference Name: IEEE Journal of Solid-State Circuits, ISSN: 1558-173X. DOI: 10.1109/JSSC.2017.2737549.
- [6] C. G. Almudever, N. Khammassi, L. Hutin, M. Vinet, M. Babaie, F. Sebastiano, E. Charbon, and K. Bertels, "Towards a scalable quantum computer," in *2018 13th International Conference on Design & Technology of Integrated Systems In Nanoscale Era (DTIS)*, Apr. 2018, pp. 1–1. DOI: 10.1109/DTIS.2018.8368579.
- [7] R. Johnson, J. Evans, P. Jacobsen, J. Thompson, and M. Christopher, "The changing automotive environment: High-temperature electronics," *IEEE Transactions on Electronics Packaging Manufacturing*, vol. 27, no. 3, pp. 164–176, Jul. 2004, Conference Name: IEEE Transactions on Electronics Packaging Manufacturing, ISSN: 1558-0822. DOI: 10.1109/TEPM.2004.843109.
- [8] M. A. Huque, S. K. Islam, B. J. Blalock, C. Su, R. Vijayaraghavan, and L. M. Tolbert, "Silicon-on-insulator based high-temperature electronics for automotive applications," in *2008 IEEE International Symposium on Industrial Electronics*, ISSN: 2163-5145, Jun. 2008, pp. 2538–2543. DOI: 10.1109/ISIE.2008.4677170.
- [9] Y. Chen, L. Del Castillo, N. Aranki, C. Assad, M. Mazzola, M. Mo-jarradi, and E. Kolawa, "Reliability assessment of high temperature electronics and packaging technologies for Venus mission," in *2008 IEEE International Reliability Physics Symposium*, ISSN: 1938-1891, Apr. 2008, pp. 641–642. DOI: 10.1109/RELPHY.2008.4558966.
- [10] J. Watson and G. Castro, "A review of high-temperature electronics technology and applications," en, *Journal of Materials Science: Materials in Electronics*, vol. 26, no. 12, pp. 9226–9235, Dec. 2015, ISSN: 1573-482X. DOI: 10.1007/s10854-015-3459-4.

- [11] R. Traeger and P. Lysne, "High temperature electronics application in well logging," *IEEE Transactions on Nuclear Science*, vol. 35, no. 1, pp. 852–854, Feb. 1988, Conference Name: IEEE Transactions on Nuclear Science, ISSN: 1558-1578. DOI: 10.1109/23.12845.
- [12] C. Prasad, "A Review of Self-Heating Effects in Advanced CMOS Technologies," *IEEE Transactions on Electron Devices*, vol. 66, no. 11, pp. 4546–4555, Nov. 2019, Conference Name: IEEE Transactions on Electron Devices, ISSN: 1557-9646. DOI: 10.1109/TED.2019.2943744.
- [13] W. Anderson, "Semiconductor device reliability in extreme high temperature space environments," in *2001 IEEE Aerospace Conference Proceedings (Cat. No.01TH8542)*, vol. 5, Mar. 2001, 2457–2462 vol.5. DOI: 10.1109/AERO.2001.931206.
- [14] C. Prasad, S. Ramey, and L. Jiang, "Self-heating in advanced CMOS technologies," in *2017 IEEE International Reliability Physics Symposium (IRPS)*, ISSN: 1938-1891, Apr. 2017, 6A–4.1–6A–4.7. DOI: 10.1109/IRPS.2017.7936336.
- [15] J.-P. Colinge, *Silicon-on-Insulator Technology: Materials to VLSI*, en. Boston, MA: Springer US, 2004, ISBN: 978-1-4613-4795-8 978-1-4419-9106-5. DOI: 10.1007/978-1-4419-9106-5.
- [16] J. Black, "Electromigration—A brief survey and some recent results," *IEEE Transactions on Electron Devices*, vol. 16, no. 4, pp. 338–347, Apr. 1969, Conference Name: IEEE Transactions on Electron Devices, ISSN: 1557-9646. DOI: 10.1109/T-ED.1969.16754.
- [17] O. Semenov, A. Vassighi, and M. Sachdev, "Impact of self-heating effect on long-term reliability and performance degradation in CMOS circuits," *IEEE Transactions on Device and Materials Reliability*, vol. 6, no. 1, pp. 17–27, Mar. 2006, Conference Name: IEEE Transactions on Device and Materials Reliability, ISSN: 1558-2574. DOI: 10.1109/TDMR.2006.870340.
- [18] Q. B. Chen and J. K. Schaeffer, "22FDX[®] Embracing IoT, 5G, and Automotive Applications - A Perspective through Global Research," en, in *2019 IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S)*, San Jose, CA, USA: IEEE, Oct. 2019, pp. 1–5, ISBN: 978-1-72813-523-6. DOI: 10.1109/S3S46989.2019.9320648.

- [19] R. Carter, J. Mazurier, L. Pirro, J.-U. Sachse, P. Baars, J. Faul, C. Grass, G. Grasshoff, P. Javorka, T. Kammler, A. Preusse, S. Nielsen, T. Heller, J. Schmidt, H. Niebojewski, P.-Y. Chou, E. Smith, E. Erben, C. Metze, C. Bao, Y. Andee, I. Aydin, S. Morvan, J. Bernard, E. Bourjot, T. Feudel, D. Harame, R. Nelluri, H.-J. Thees, L. M-Meskamp, J. Kluth, R. Mulfinger, M. Rashed, R. Taylor, C. Weintraub, J. Hoentschel, M. Vinet, J. Schaeffer, and B. Rice, "22nm FDSOI technology for emerging mobile, Internet-of-Things, and RF applications," in *2016 IEEE International Electron Devices Meeting (IEDM)*, ISSN: 2156-017X, Dec. 2016, pp. 2.2.1–2.2.4. DOI: 10.1109/IEDM.2016.7838029.
- [20] N. Planes, S. Kohler, A. Cathelin, C. Charbuillet, P. Scheer, and F. Arnaud, "28FDSOI technology for low-voltage, analog and RF applications," in *2016 13th IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT)*, Oct. 2016, pp. 10–13. DOI: 10.1109/ICSICT.2016.7998825.
- [21] S. Ong, S. Lehmann, W. Chow, C. Zhang, C. Schippel, L. Chan, Y. Andee, M. Hauschildt, K. Tan, J. Watts, C. Lim, A. Divay, J. Wong, Z. Zhao, M. Govindarajan, C. Schwan, A. Huschka, A. Bcllaouar, W. LOo, J. Mazurier, C. Grass, R. Taylor, K. Chew, S. Embabi, G. Workman, A. Pakfar, S. Morvan, K. Sundaram, M. T. Lau, B. Rice, and D. Harame, "A 22nm FDSOI Technology Optimized for RF/mmWave Applications," in *2018 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, ISSN: 2375-0995, Jun. 2018, pp. 72–75. DOI: 10.1109/RFIC.2018.8429035.
- [22] D. Jacquet, F. Hasbani, P. Flatresse, R. Wilson, F. Arnaud, G. Cesana, T. Di Gilio, C. Lecocq, T. Roy, A. Chhabra, C. Grover, O. Minez, J. Uginet, G. Durieu, C. Adobati, D. Casalotto, F. Nyer, P. Menut, A. Cathelin, I. Vongsavady, and P. Magarshack, "A 3 GHz Dual Core Processor ARM Cortex TM -A9 in 28 nm UTBB FD-SOI CMOS With Ultra-Wide Voltage Range and Energy Efficiency Optimization," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 4, pp. 812–826, Apr. 2014, Conference Name: IEEE Journal of Solid-State Circuits, ISSN: 1558-173X. DOI: 10.1109/JSSC.2013.2295977.
- [23] V. K. Khanna, *Extreme-Temperature and Harsh-Environment Electronics: Physics, technology and applications*, en. IOP Publishing, Mar. 2017, ISBN: 978-0-7503-1155-7.

- [24] B. Tenbroek, M. Lee, W. Redman-White, J. Bunyan, and M. Uren, "Self-heating effects in SOI MOSFETs and their measurement by small signal conductance techniques," *IEEE Transactions on Electron Devices*, vol. 43, no. 12, pp. 2240–2248, Dec. 1996, Conference Name: IEEE Transactions on Electron Devices, ISSN: 1557-9646. DOI: 10.1109/16.544417.
- [25] M. Emam, "Wide band and noise characterization of various MOSFETs for optimized use in RF circuits," en, Ph.D. dissertation, UCL - Université Catholique de Louvain, 2010.
- [26] Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices*, en, ISBN: 9781139195065 Publisher: Cambridge University Press, Aug. 2009. DOI: 10.1017/CB09781139195065.
- [27] G. Groeseneken, J.-P. Colinge, H. Maes, J. Alderman, and S. Holt, "Temperature dependence of threshold voltage in thin-film SOI MOSFETs," *IEEE Electron Device Letters*, vol. 11, no. 8, pp. 329–331, Aug. 1990, Conference Name: IEEE Electron Device Letters, ISSN: 1558-0563. DOI: 10.1109/55.57923.
- [28] F. Shoucair, "Design Consideration in High Temperature Analog CMOS Integrated Circuits," *IEEE Transactions on Components, Hybrids, and Manufacturing Technology*, vol. 9, no. 3, pp. 242–251, Sep. 1986, Conference Name: IEEE Transactions on Components, Hybrids, and Manufacturing Technology, ISSN: 1558-3082. DOI: 10.1109/TCHMT.1986.1136646.
- [29] J.-P. Eggermont, D. De Ceuster, D. Flandre, B. Gentinne, P. Jespers, and J.-P. Colinge, "Design of SOI CMOS operational amplifiers for applications up to 300/spl deg/C," *IEEE Journal of Solid-State Circuits*, vol. 31, no. 2, pp. 179–186, Feb. 1996, Conference Name: IEEE Journal of Solid-State Circuits, ISSN: 1558-173X. DOI: 10.1109/4.487994.
- [30] D. Fleetwood, F. Thome, S. Tsao, P. Dressendorfer, V. Dandini, and J. Schwank, "High-temperature silicon-on-insulator electronics for space nuclear power systems: Requirements and feasibility," *IEEE Transactions on Nuclear Science*, vol. 35, no. 5, pp. 1099–1112, Oct. 1988, Conference Name: IEEE Transactions on Nuclear Science, ISSN: 1558-1578. DOI: 10.1109/23.7506.

- [31] P. Neudeck, R. Okojie, and L.-Y. Chen, "High-temperature electronics - a role for wide bandgap semiconductors?" *Proceedings of the IEEE*, vol. 90, no. 6, pp. 1065–1076, Jun. 2002, Conference Name: Proceedings of the IEEE, ISSN: 1558-2256. DOI: 10.1109/JPROC.2002.1021571.
- [32] S. Cristoloveanu, "Introduction to Silicon On Insulator materials and devices," *Microelectronic Engineering*, Proceedings of the First Session "Low-Power, Low-Voltage Integrated Circuits: Technology and Design", vol. 39, no. 1, pp. 145–154, Dec. 1997, ISSN: 0167-9317. DOI: 10.1016/S0167-9317(97)00172-X.
- [33] S. Singh, S. S. Gill, and N. Kaur, "Temperature Dependence of Multi-fin FinFET for Bulk and SOI Substrate at 20 nm Channel Length," en, in *Sustainable Development Through Engineering Innovations*, H. Singh, P. P. Singh Cheema, and P. Garg, Eds., Singapore: Springer, 2021, pp. 487–494, ISBN: 9789811595547. DOI: 10.1007/978-981-15-9554-7_44.
- [34] J. Cressler, "On the Potential of SiGe HBTs for Extreme Environment Electronics," en, *Proceedings of the IEEE*, vol. 93, no. 9, pp. 1559–1582, Sep. 2005, ISSN: 0018-9219. DOI: 10.1109/JPROC.2005.852225.
- [35] D. B. Thomas, L. Najafizadeh, J. D. Cressler, K. A. Moen, and N. Lourenco, "Optimization of SiGe bandgap-based circuits for up to 300 °C operation," *Solid-State Electronics*, vol. 56, no. 1, pp. 47–55, Feb. 2011, ISSN: 0038-1101. DOI: 10.1016/j.sse.2010.11.010.
- [36] J. B. Casady and R. W. Johnson, "Status of silicon carbide (SiC) as a wide-bandgap semiconductor for high-temperature applications: A review," *Solid-State Electronics*, vol. 39, no. 10, pp. 1409–1422, Oct. 1996, ISSN: 0038-1101. DOI: 10.1016/0038-1101(96)00045-7.
- [37] A. Hassan, M. Amer, Y. Savaria, and M. Sawan, "Towards GaN500-based High Temperature ICs: Characterization and Modeling up to 600°C," in *2020 18th IEEE International New Circuits and Systems Conference (NEWCAS)*, Jun. 2020, pp. 275–278. DOI: 10.1109/NEWCAS49341.2020.9159796.
- [38] D. Flandre, "Silicon-on-insulator technology for high temperature metal oxide semiconductor devices and circuits," *Materials Science and Engineering: B*, European Materials Research Society 1994 Spring Meeting

- Symposium E: High Temperature Electronics: Materials, Devices and Applications, vol. 29, no. 1, pp. 7–12, Jan. 1995, ISSN: 0921-5107. DOI: 10.1016/0921-5107(94)04018-Y.
- [39] M. Emam, J. C. Tinoco, D. Vanhoenacker-Janvier, and J.-P. Raskin, “High-temperature DC and RF behaviors of partially-depleted SOI MOS-FET transistors,” *Solid-State Electronics*, Selected Papers from the EUROSOI '08 Conference, vol. 52, no. 12, pp. 1924–1932, Dec. 2008, ISSN: 0038-1101. DOI: 10.1016/j.sse.2008.06.058.
- [40] M. Emam and J.-P. Raskin, “Partially Depleted SOI Versus Deep N-Well Protected Bulk-Si MOSFETs: A High-Temperature RF Study for Low-Voltage Low-Power Applications,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 61, no. 4, pp. 1496–1504, Apr. 2013, Conference Name: IEEE Transactions on Microwave Theory and Techniques, ISSN: 1557-9670. DOI: 10.1109/TMTT.2013.2250513.
- [41] H. Kappert, S. Dreiner, D. Dittrich, K. Grella, A. Kelberer, M. Klusmann, N. Kordas, A. Kosfeld, A. Schmidt, U. Paschen, and R. Kokozinski, “High Temperature 0.35 Micron Silicon-on-Insulator CMOS Technology,” en, *Additional Conferences (Device Packaging, HiTEC, HiTEN, and CICMT)*, vol. 2014, no. HITEC, pp. 000 154–000 158, Jan. 2014, ISSN: 2380-4491. DOI: 10.4071/HITEC-WA14.
- [42] N. Kordas and H. Kappert, “Integrated High Temperature Electronics for Sensors in Harsh Environments,” in *Sensors and Measuring Systems; 21th ITG/GMA-Symposium*, May 2022, pp. 1–3.
- [43] “High Temperature Microelectronics.” en-US. (), URL: <https://aerospace.honeywell.com/us/en/products-and-services/product/hardware-and-systems/microelectronics/high-temperature-microelectronics>.
- [44] R. Johnson, “High temperature silicon-on-insulator pressure sensor technology,” in *HITEN 99. Third European Conference on High Temperature Electronics. (IEEE Cat. No.99EX372)*, Jul. 1999, pp. 45–48. DOI: 10.1109/HITEN.1999.827460.
- [45] S. T. Lee, A. Bellaouar, and S. Embabi, “A Low-Power, Compact 76-81GHz FMCW Transmitter for Automotive Radar in 22nm FDSOI,” in *ESSCIRC 2018 - IEEE 44th European Solid State Circuits Conference*

- (*ESSCIRC*), ISSN: 1930-8833, Sep. 2018, pp. 34–37. DOI: 10.1109/ESSCIRC.2018.8494256.
- [46] M. Sadegh Dadash, S. Bonen, U. Alakusu, D. Harame, and S. P. Voinigescu, “DC-170 GHz Characterization of 22nm FDSOI Technology for Radar Sensor Applications,” in *2018 13th European Microwave Integrated Circuits Conference (EuMIC)*, Sep. 2018, pp. 158–161. DOI: 10.23919/EuMIC.2018.8539934.
 - [47] B. Kazemi Esfeh, “RF characterization of state-of-the-art technologies,” en, Ph.D. dissertation, UCL - Université Catholique de Louvain, 2019.
 - [48] L. Nyssens, “A systemic analysis of silicon substrates toward improvements of integrated FD-SOI circuits performance at mm-wave frequencies,” en, Ph.D. dissertation, UCL - Université Catholique de Louvain, 2023.
 - [49] “|Z| Probe Family Overview.” en-US. (), URL: <https://www.formfactor.com/download/z-probe-family-overview/>.
 - [50] H. Yi, W.-H. Yu, P.-I. Mak, J. Yin, and R. P. Martins, “A 0.18-V 382-W Bluetooth Low-Energy Receiver Front-End With 1.33-nW Sleep Power for Energy-Harvesting Applications in 28-nm CMOS,” *IEEE Journal of Solid-State Circuits*, vol. 53, no. 6, pp. 1618–1627, Jun. 2018, Conference Name: IEEE Journal of Solid-State Circuits, ISSN: 1558-173X. DOI: 10.1109/JSSC.2018.2815987.
 - [51] E. Kargaran, C. Bryant, D. Manstretta, J. Strange, and R. Castello, “A Sub-0.6V, 330 μ W, 0.15 mm² Receiver Front-End for Bluetooth Low Energy (BLE) in 22 nm FD-SOI with Zero External Components,” in *2019 IEEE Asian Solid-State Circuits Conference (A-SSCC)*, Nov. 2019, pp. 169–172. DOI: 10.1109/A-SSCC47793.2019.9056899.
 - [52] O. El-Aassar and G. M. Rebeiz, “Design of Low-Power Sub-2.4 dB Mean NF 5G LNAs Using Forward Body Bias in 22 nm FDSOI,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 68, no. 10, pp. 4445–4454, Oct. 2020, Conference Name: IEEE Transactions on Microwave Theory and Techniques, ISSN: 1557-9670. DOI: 10.1109/TMTT.2020.3012538.

- [53] T. Yamauchi, H. Kondo, and K. Nii, "Automotive low power technology for IoT society," in *2015 Symposium on VLSI Circuits (VLSI Circuits)*, ISSN: 2158-5636, Jun. 2015, T80–T81. DOI: 10.1109/VLSIC.2015.7231360.
- [54] A. Halder, L. Nyssens, M. Vanbrabant, M. Rack, D. Lederer, V. Kilchytska, and J.-P. Raskin, "Impact of High Temperature Up to 175 °C on the DC and RF Performances of 22-nm FD-SOI MOSFETs," *IEEE Transactions on Electron Devices*, vol. 70, no. 10, pp. 4987–4992, Oct. 2023, Conference Name: IEEE Transactions on Electron Devices, ISSN: 1557-9646. DOI: 10.1109/TED.2023.3303150.
- [55] A. Halder, L. Nyssens, M. Rack, D. Lederer, V. Kilchytska, and J.-P. Raskin, "22 nm FD-SOI MOSFET Figures of Merit at high temperatures upto 175 °C," in *2022 IEEE 22nd Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF)*, ISSN: 2474-9761, Jan. 2022, pp. 27–30. DOI: 10.1109/SiRF53094.2022.9720052.
- [56] H.-S. Wong, M. H. White, T. J. Krutsick, and R. V. Booth, "Modeling of transconductance degradation and extraction of threshold voltage in thin oxide MOSFET's," *Solid-State Electronics*, vol. 30, no. 9, pp. 953–968, Sep. 1987, ISSN: 0038-1101. DOI: 10.1016/0038-1101(87)90132-8.
- [57] V. Kilchytska, M. K. Md Arshad, S. Makovejev, S. Olsen, F. Andrieu, T. Poiroux, O. Faynot, J. -. Raskin, and D. Flandre, "Ultra-thin body and thin-BOX SOI CMOS technology analog figures of merit," *Solid-State Electronics*, Selected Full-Length Papers from the EUROSOI 2011 Conference, vol. 70, pp. 50–58, Apr. 2012, ISSN: 0038-1101. DOI: 10.1016/j.sse.2011.11.020.
- [58] B. Kazemi Esfeh, V. Kilchytska, V. Barral, N. Planes, M. Haond, D. Flandre, and J. -. Raskin, "Assessment of 28 nm UTBB FD-SOI technology platform for RF applications: Figures of merit and effect of parasitic elements," *Solid-State Electronics*, PLANAR FULLY-DEPLETED SOI TECHNOLOGY, vol. 117, pp. 130–137, Mar. 2016, ISSN: 0038-1101. DOI: 10.1016/j.sse.2015.11.020.
- [59] D. Lovelace, J. Costa, and N. Camilleri, "Extracting small-signal model parameters of silicon MOSFET transistors," in *1994 IEEE MTT-S International Microwave Symposium Digest (Cat. No.94CH3389-4)*, ISSN:

- 0149-645X, May 1994, 865–868 vol.2. DOI: 10.1109/MWSYM.1994.335220.
- [60] R. Torres-Torres, R. S. Murphy-Arteaga, and S. Decoutere, “MOSFET bias dependent series resistance extraction from RF measurements,” en, *Electronics Letters*, vol. 39, no. 20, pp. 1476–1478, Oct. 2003, Publisher: IET Digital Library, ISSN: 1350-911X. DOI: 10.1049/e1:20030936.
- [61] A. Bracale, V. Ferlet-Cavrois, N. Fel, D. Pasquet, J. L. Gautier, J. L. Pelloie, and J. du Port de Poncharra, “A New Approach for SOI Devices Small-Signal Parameters Extraction,” en, *Analog Integrated Circuits and Signal Processing*, vol. 25, no. 2, pp. 157–169, Nov. 2000, ISSN: 1573-1979. DOI: 10.1023/A:1008332732738.
- [62] H. Bai, C. Liu, D. Majstorovic, and F. Gao, “3 - Modeling of power electronic devices,” in *Real-Time Simulation Technology for Modern Power Electronics*, H. Bai, C. Liu, D. Majstorovic, and F. Gao, Eds., Academic Press, Jan. 2023, pp. 35–72, ISBN: 978-0-323-99541-2. DOI: 10.1016/B978-0-323-99541-2.00008-9.
- [63] S. Makovejev, “Characterisation of thermal and coupling effects in advanced silicon MOSFETs,” en, Accepted: 2013-06-10T09:27:48Z, Thesis, Newcastle University, 2012.
- [64] V. Negro and L. Pannone, “Self-heating and gate leakage current in a guarded MOSFET,” *Proceedings of the IEEE*, vol. 60, no. 3, pp. 342–343, Mar. 1972, Conference Name: Proceedings of the IEEE, ISSN: 1558-2256. DOI: 10.1109/PROC.1972.8640.
- [65] P. Mautry and J. Trager, “Self-heating and Temperature Measurement in Sub-m-MOSFETs,” in *ESSDERC '89: 19th European Solid State Device Research Conference*, Sep. 1989, pp. 675–678. DOI: 10.1007/978-3-642-52314-4_141.
- [66] L. J. McDaid, S. Hall, P. H. Mellor, W. Eccleston, and J. C. Alderman, “Physical origin of negative differential resistance in SOI transistors,” en, *Electronics Letters*, vol. 25, no. 13, pp. 827–828, Jun. 1989, Publisher: IET Digital Library, ISSN: 1350-911X. DOI: 10.1049/e1:19890557.
- [67] Z. Chai and M. Berger, “The Self-Heating Effect and its Influence on the Electrical Properties of SOI MOSFETs,” in *1992 IEEE International SOI Conference*, ISSN: 1078-621X, Oct. 1992, pp. 78–79. DOI: 10.1109/SOI.1992.664803.

- [68] A. Caviglia and A. Iliadis, "A New Method for Characterizing Dynamic Self-Heating in Soi Mosfets," in *1992 IEEE International SOI Conference*, ISSN: 1078-621X, Oct. 1992, pp. 118–119. DOI: 10.1109/SOI.1992.664822.
- [69] W. Jin, S. Fung, W. Liu, P. Chan, and C. Hu, "Self-heating characterization for SOI MOSFET based on AC output conductance," in *International Electron Devices Meeting 1999. Technical Digest (Cat. No.99CH36318)*, Dec. 1999, pp. 175–178. DOI: 10.1109/IEDM.1999.823873.
- [70] E. Pop, S. Sinha, and K. Goodson, "Heat Generation and Transport in Nanometer-Scale Transistors," *Proceedings of the IEEE*, vol. 94, no. 8, pp. 1587–1601, Aug. 2006, Conference Name: Proceedings of the IEEE, ISSN: 1558-2256. DOI: 10.1109/JPROC.2006.879794.
- [71] S.-M. Lee, D. G. Cahill, and T. H. Allen, "Thermal conductivity of sputtered oxide films," *Physical Review B*, vol. 52, no. 1, pp. 253–257, Jul. 1995, Publisher: American Physical Society. DOI: 10.1103/PhysRevB.52.253.
- [72] M. A. Panzer, M. Shandalov, J. A. Rowlette, Y. Oshima, Y. W. Chen, P. C. McIntyre, and K. E. Goodson, "Thermal Properties of Ultrathin Hafnium Oxide Gate Dielectric Films," *IEEE Electron Device Letters*, vol. 30, no. 12, pp. 1269–1271, Dec. 2009, Conference Name: IEEE Electron Device Letters, ISSN: 1558-0563. DOI: 10.1109/LED.2009.2032937.
- [73] M. Burzo, P. Komarov, and P. Raad, "Thermal transport properties of gold-covered thin-film silicon dioxide," *IEEE Transactions on Components and Packaging Technologies*, vol. 26, no. 1, pp. 80–88, Mar. 2003, Conference Name: IEEE Transactions on Components and Packaging Technologies, ISSN: 1557-9972. DOI: 10.1109/TCAPT.2003.811467.
- [74] E. Pop, C. O. Chui, R. Dutton, S. Sinha, and K. Goodson, "Electro-thermal comparison and performance optimization of thin-body SOI and GOI MOSFETs," in *IEDM Technical Digest. IEEE International Electron Devices Meeting, 2004.*, Dec. 2004, pp. 411–414. DOI: 10.1109/IEDM.2004.1419172.

- [75] S.-M. Lee and D. G. Cahill, "Heat transport in thin dielectric films," *Journal of Applied Physics*, vol. 81, no. 6, pp. 2590–2595, Mar. 1997, ISSN: 0021-8979. DOI: 10.1063/1.363923.
- [76] A. Majumdar and P. Reddy, "Role of electron–phonon coupling in thermal conductance of metal–nonmetal interfaces," *Applied Physics Letters*, vol. 84, no. 23, pp. 4768–4770, Jun. 2004, ISSN: 0003-6951. DOI: 10.1063/1.1758301.
- [77] K. Wu, L. Zhang, D. Wang, F. Li, P. Zhang, L. Sang, M. Liao, K. Tang, J. Ye, and S. Gu, "A comparative study of interfacial thermal conductance between metal and semiconductor," en, *Scientific Reports*, vol. 12, no. 1, p. 19 907, Nov. 2022, Publisher: Nature Publishing Group, ISSN: 2045-2322. DOI: 10.1038/s41598-022-24379-z.
- [78] K. Triantopoulos, M. Cassé, S. Barraud, S. Haendler, E. Vincent, M. Vinet, F. Gaillard, and G. Ghibaudo, "Self-Heating Effect in FDSOI Transistors Down to Cryogenic Operation at 4.2 K," *IEEE Transactions on Electron Devices*, vol. 66, no. 8, pp. 3498–3505, Aug. 2019, Conference Name: IEEE Transactions on Electron Devices, ISSN: 1557-9646. DOI: 10.1109/TED.2019.2919924.
- [79] L. Su, J. Chung, D. Antoniadis, K. Goodson, and M. Flik, "Measurement and modeling of self-heating in SOI nMOSFET's," *IEEE Transactions on Electron Devices*, vol. 41, no. 1, pp. 69–75, Jan. 1994, Conference Name: IEEE Transactions on Electron Devices, ISSN: 1557-9646. DOI: 10.1109/16.259622.
- [80] D. Dallmann and K. Shenai, "Scaling constraints imposed by self-heating in submicron SOI MOSFET's," *IEEE Transactions on Electron Devices*, vol. 42, no. 3, pp. 489–496, Mar. 1995, Conference Name: IEEE Transactions on Electron Devices, ISSN: 1557-9646. DOI: 10.1109/16.368045.
- [81] S. Makovejev, N. Planes, M. Haond, D. Flandre, J. .-. Raskin, and V. Kilchytska, "Comparison of self-heating and its effect on analogue performance in 28 nm bulk and FDSOI," *Solid-State Electronics*, Selected papers from the EUROSOI-ULIS conference, vol. 115, pp. 219–224, Jan. 2016, ISSN: 0038-1101. DOI: 10.1016/j.sse.2015.08.022.

- [82] S. Makovejev, B. K. Esfeh, V. Barral, N. Planes, M. Haond, D. Flandre, J.-P. Raskin, and V. Kilchytska, "Wide frequency band assessment of 28 nm FDSOI technology platform for analogue and RF applications," in *2014 15th International Conference on Ultimate Integration on Silicon (ULIS)*, Apr. 2014, pp. 53–56. DOI: 10.1109/ULIS.2014.6813904.
- [83] L. Nyssens, A. Halder, B. K. Esfeh, N. Planes, M. Haond, D. Flandre, J.-P. Raskin, and V. Kilchytska, "Self-Heating in 28 FDSOI UTBB MOSFETs at Cryogenic Temperatures," in *ESSDERC 2019 - 49th European Solid-State Device Research Conference (ESSDERC)*, ISSN: 2378-6558, Sep. 2019, pp. 162–165. DOI: 10.1109/ESSDERC.2019.8901704.
- [84] K. Uchida and T. Takahashi, "Thermal-aware CMOS: Challenges for future technology and design evolutions," in *2016 46th European Solid-State Device Research Conference (ESSDERC)*, ISSN: 2378-6558, Sep. 2016, pp. 150–153. DOI: 10.1109/ESSDERC.2016.7599609.
- [85] C. Fiegna, Y. Yang, E. Sangiorgi, and A. G. O'Neill, "Analysis of Self-Heating Effects in Ultrathin-Body SOI MOSFETs by Device Simulation," *IEEE Transactions on Electron Devices*, vol. 55, no. 1, pp. 233–244, Jan. 2008, Conference Name: IEEE Transactions on Electron Devices, ISSN: 1557-9646. DOI: 10.1109/TED.2007.911354.
- [86] K. Jenkins and J.-C. Sun, "Measurement of I-V curves of silicon-on-insulator (SOI) MOSFET's without self-heating," *IEEE Electron Device Letters*, vol. 16, no. 4, pp. 145–147, Apr. 1995, Conference Name: IEEE Electron Device Letters, ISSN: 1558-0563. DOI: 10.1109/55.372496.
- [87] K. Jenkins, J.-C. Sun, and J. Gautier, "Characteristics of SOI FET's under pulsed conditions," *IEEE Transactions on Electron Devices*, vol. 44, no. 11, pp. 1923–1930, Nov. 1997, Conference Name: IEEE Transactions on Electron Devices, ISSN: 1557-9646. DOI: 10.1109/16.641362.
- [88] C. Anghel, A. Ionescu, N. Hefyene, and R. Gillon, "Self-heating characterization and extraction method for thermal resistance and capacitance in high voltage MOSFETs," in *ESSDERC '03. 33rd Conference on European Solid-State Device Research, 2003.*, Sep. 2003, pp. 449–452. DOI: 10.1109/ESSDERC.2003.1256910.

- [89] S. Makovejev, S. H. Olsen, V. Kilchytska, and J.-P. Raskin, "Time and Frequency Domain Characterization of Transistor Self-Heating," *IEEE Transactions on Electron Devices*, vol. 60, no. 6, pp. 1844–1851, Jun. 2013, Conference Name: IEEE Transactions on Electron Devices, ISSN: 1557-9646. DOI: 10.1109/TED.2013.2259174.
- [90] N. Rodriguez, C. Navarro, F. Andrieu, O. Faynot, F. Gamiz, and S. Cristoloveanu, "Self-heating effects in ultrathin FD SOI transistors," in *IEEE 2011 International SOI Conference*, ISSN: 1078-621X, Oct. 2011, pp. 1–2. DOI: 10.1109/SOI.2011.6081685.
- [91] R. Tu, C. Wann, J. King, P. Ko, and C. Hu, "An AC conductance technique for measuring self-heating in SOI MOSFET's," *IEEE Electron Device Letters*, vol. 16, no. 2, pp. 67–69, Feb. 1995, Conference Name: IEEE Electron Device Letters, ISSN: 1558-0563. DOI: 10.1109/55.386025.
- [92] N. Rinaldi, "Small-signal operation of semiconductor devices including self-heating, with application to thermal characterization and instability analysis," en, *IEEE Transactions on Electron Devices*, vol. 48, no. 2, pp. 323–331, Feb. 2001, ISSN: 00189383. DOI: 10.1109/16.902734.
- [93] A. Scholten, G. Smit, R. Pijper, L. Tiemeijer, H. Tuinhout, J.-L. van der Steen, A. Mercha, M. Braccioli, and D. Klaassen, "Experimental assessment of self-heating in SOI FinFETs," in *2009 IEEE International Electron Devices Meeting (IEDM)*, ISSN: 2156-017X, Dec. 2009, pp. 1–4. DOI: 10.1109/IEDM.2009.5424362.
- [94] L. Nyssens, A. Halder, B. K. Esfeh, N. Planes, M. Haond, D. Flandre, J.-P. Raskin, and V. Kilchytska, "Self-heating in FDSOI UTBB MOSFETs at cryogenic temperatures and its effect on analog figures of merit," *IEEE Journal of the Electron Devices Society*, vol. 8, pp. 789–796, 2020, Publisher: IEEE.
- [95] W. Jin, W. Liu, S. Fung, P. Chan, and C. Hu, "SOI thermal impedance extraction methodology and its significance for circuit simulation," *IEEE Transactions on Electron Devices*, vol. 48, no. 4, pp. 730–736, Apr. 2001, Conference Name: IEEE Transactions on Electron Devices, ISSN: 1557-9646. DOI: 10.1109/16.915707.

- [96] S. Makovejev, J.-P. Raskin, D. Flandre, S. Olsen, F. Andrieu, T. Poiroux, and V. Kilchytska, "Comparison of small-signal output conductance frequency dependence in UTBB SOI MOSFETs with and without ground plane," in *IEEE 2011 International SOI Conference*, ISSN: 1078-621X, Oct. 2011, pp. 1–2. DOI: 10.1109/SOI.2011.6081717.
- [97] S. Makovejev, V. Kilchytska, M. K. M. Arshad, D. Flandre, F. Andrieu, O. Faynot, S. Olsen, and J.-P. Raskin, "Self-heating and substrate effects in ultra-thin body ultra-thin BOX devices," in *Ulis 2011 Ultimate Integration on Silicon*, Mar. 2011, pp. 1–4. DOI: 10.1109/ULIS.2011.5758009.
- [98] L. Nyssens, M. Rack, A. Halder, J.-P. Raskin, and V. Kilchytska, "On the Separate Extraction of Self-Heating and Substrate Effects in FD-SOI MOSFET," *IEEE Electron Device Letters*, vol. 42, no. 5, pp. 665–668, May 2021, Conference Name: IEEE Electron Device Letters, ISSN: 1558-0563. DOI: 10.1109/LED.2021.3071272.
- [99] T. Chohan, Z. Zhao, S. Lehmann, W. Arfaoui, G. Bossu, J. Trommer, S. Slesazek, T. Mikolajick, and M. Siddabathula, "Implication of Self-Heating Effect on Device Reliability Characterization of Multi-Finger n-MOSFETs on 22FDSOI," *IEEE Transactions on Device and Materials Reliability*, vol. 22, no. 3, pp. 387–395, Sep. 2022, Conference Name: IEEE Transactions on Device and Materials Reliability, ISSN: 1558-2574. DOI: 10.1109/TDMR.2022.3183630.
- [100] B. González, R. Rodríguez, and A. Lázaro, "Thermal Resistance Characterization for Multifinger SOI-MOSFETs," *IEEE Transactions on Electron Devices*, vol. 65, no. 9, pp. 3626–3632, Sep. 2018, Conference Name: IEEE Transactions on Electron Devices, ISSN: 1557-9646. DOI: 10.1109/TED.2018.2853799.
- [101] S. Makovejev, S. Olsen, and J.-P. Raskin, "RF Extraction of Self-Heating Effects in FinFETs," *IEEE Transactions on Electron Devices*, vol. 58, no. 10, pp. 3335–3341, Oct. 2011, Conference Name: IEEE Transactions on Electron Devices, ISSN: 1557-9646. DOI: 10.1109/TED.2011.2162333.
- [102] J. Jomaah, G. Ghibaudo, and F. Balestra, "Analysis and modeling of self-heating effects in thin-film SOI MOSFETs as a function of temperature," *Solid-State Electronics*, vol. 38, no. 3, pp. 615–618, Mar. 1995, ISSN: 0038-1101. DOI: 10.1016/0038-1101(94)00130-8.

- [103] G. Ghibaudo, M. Cassé, F. S. di Santa Maria, C. Theodorou, and F. Balestra, “Modelling of self-heating effect in FDSOI and bulk MOSFETs operated in deep cryogenic conditions,” *Solid-State Electronics*, vol. 192, p. 108 265, Jun. 2022, ISSN: 0038-1101. DOI: 10 . 1016 / j . sse . 2022 . 108265.
- [104] P. Mautry and J. Trager, “Investigation of self-heating in VLSI and ULSI MOSFETs,” in *International Conference on Microelectronic Test Structures*, Mar. 1990, pp. 221–226. DOI: 10 . 1109 / ICMTS . 1990 . 67907.
- [105] T. Takahashi, T. Matsuki, T. Shinada, Y. Inoue, and K. Uchida, “Direct Evaluation of Self-Heating Effects in Bulk and Ultra-Thin BOX SOI MOSFETs Using Four-Terminal Gate Resistance Technique,” *IEEE Journal of the Electron Devices Society*, vol. 4, no. 5, pp. 365–373, Sep. 2016, Conference Name: IEEE Journal of the Electron Devices Society, ISSN: 2168-6734. DOI: 10 . 1109 / JEDS . 2016 . 2568261.
- [106] K. Triantopoulos, M. Cassé, L. Brunet, P. Batude, C. Fenouillet-Béranger, B. Mathieu, M. Vinet, G. Ghibaudo, and G. Reimbold, “Thermal effects in 3D sequential technology,” in *2017 IEEE International Electron Devices Meeting (IEDM)*, ISSN: 2156-017X, Dec. 2017, pp. 7.6.1–7.6.4. DOI: 10 . 1109 / IEDM . 2017 . 8268348.
- [107] E. A. Scott, J. T. Gaskins, S. W. King, and P. E. Hopkins, “Thermal conductivity and thermal boundary resistance of atomic layer deposited high-k dielectric aluminum oxide, hafnium oxide, and titanium oxide thin films on silicon,” *APL Materials*, vol. 6, no. 5, p. 058 302, May 2018, ISSN: 2166-532X. DOI: 10 . 1063 / 1 . 5021044.
- [108] G. Mariniello, M. Cassé, G. Reimbold, and M. Pavanello, “Underestimation of measured self-heating in nanowires by using gate resistance technique,” en, *Electronics Letters*, vol. 52, no. 23, pp. 1935–1937, 2016, _eprint: <https://onlinelibrary.wiley.com/doi/pdf/10.1049/el.2016.2570>, ISSN: 1350-911X. DOI: 10 . 1049 / e1 . 2016 . 2570.
- [109] A. Halder, L. Nyssens, M. Rack, D. Lederer, J.-P. Raskin, and V. Kilchytska, “Heat sink implementation in back-end of line for self-heating reduction in 22nm FDSOI MOSFETs,” *Solid-State Electronics*, vol. 184, p. 108 088, Oct. 2021, ISSN: 0038-1101. DOI: 10 . 1016 / j . sse . 2021 . 108088.

- [110] A. Halder, L. Nyssens, M. Rack, J.-P. Raskin, and V. Kilchytska, "Effect of Heat Sink in Back-End of Line on Self-Heating in 22 nm FDSOI MOSFETs," in *2020 Joint International EUROSIOI Workshop and International Conference on Ultimate Integration on Silicon (EUROSIOI-ULIS)*, ISSN: 2472-9132, Sep. 2020, pp. 1–4. DOI: 10.1109/EUROSIOI-ULIS49407.2020.9365293.
- [111] A. Bhaskar, J. Philippe, V. Avramovic, F. Braud, J.-F. Robillard, C. Durand, D. Gloria, C. Gaquiere, and E. Dubois, "Substrate Engineering of Inductors on SOI for Improvement of Q-Factor and Application in LNA," *IEEE Journal of the Electron Devices Society*, vol. 8, pp. 959–969, 2020, Conference Name: IEEE Journal of the Electron Devices Society, ISSN: 2168-6734. DOI: 10.1109/JEDS.2020.3019884.
- [112] S. H. Shin, S. -. Kim, S. Kim, H. Wu, P. D. Ye, and M. A. Alam, "Substrate and layout engineering to suppress self-heating in floating body transistors," in *2016 IEEE International Electron Devices Meeting (IEDM)*, ISSN: 2156-017X, Dec. 2016, pp. 15.7.1–15.7.4. DOI: 10.1109/IEDM.2016.7838426.
- [113] Y. Yan, V. Kilchytska, B. Wang, S. Faniel, Y. Zeng, J.-P. Raskin, and D. Flandre, "Characterization of thin Al₂O₃/SiO₂ dielectric stack for CMOS transistors," *Microelectronic Engineering*, vol. 254, p. 111 708, Feb. 2022, ISSN: 0167-9317. DOI: 10.1016/j.mee.2022.111708.
- [114] K. Oshima, S. Cristoloveanu, B. Guillaumot, H. Iwai, and S. Deleonibus, "Advanced SOI MOSFETs with buried alumina and ground plane: Self-heating and short-channel effects," *Solid-State Electronics, Silicon On Insulator Technology and Devices*, vol. 48, no. 6, pp. 907–917, Jun. 2004, ISSN: 0038-1101. DOI: 10.1016/j.sse.2003.12.026.
- [115] K. Raleva, D. Vasileska, and S. M. Goodnick, "Self-Heating Effects in High Performance Devices," en, in *ICT Innovations 2010*, M. Gusev and P. Mitrevski, Eds., Berlin, Heidelberg: Springer, 2011, pp. 114–122, ISBN: 978-3-642-19325-5. DOI: 10.1007/978-3-642-19325-5_12.
- [116] A. Aleksov, X. Li, N. Govindaraju, J. M. Gobien, S. D. Wolter, J. T. Prater, and Z. Sitar, "Silicon-on-diamond: An advanced silicon-on-insulator technology," *Diamond and Related Materials, Proceedings of Diamond 2004, the 15th European Conference on Diamond, Diamond-Like Materials, Carbon Nanotubes, Nitrides and Silicon Carbide*, vol. 14,

- no. 3, pp. 308–313, Mar. 2005, ISSN: 0925-9635. DOI: 10.1016/j.diamond.2005.01.019.
- [117] A. Soderbarg, B. Edholm, J. Olsson, S. Tiensuu, and E. Johansson, “Silicon on diamond heat sinks by bonding and etch back,” in *Proceedings of 1993 IEEE International SOI Conference*, Oct. 1993, pp. 58–59. DOI: 10.1109/SOI.1993.344593.
- [118] N. Bresson, S. Cristoloveanu, C. Mazuré, F. Letertre, and H. Iwai, “Integration of buried insulators with high thermal conductivity in SOI MOSFETs: Thermal properties and short channel effects,” *Solid-State Electronics*, Special Issue: Papers Selected from the EUROSIOI Workshop Granada, 19-21 January 2005, vol. 49, no. 9, pp. 1522–1528, Sep. 2005, ISSN: 0038-1101. DOI: 10.1016/j.sse.2005.07.015.
- [119] T. Ishikawa, K. Okaniwa, M. Komaru, K. Kosaki, and Y. Mitsui, “A high-power GaAs FET having buried plated heat sink for high-performance MMIC’s,” *IEEE Transactions on Electron Devices*, vol. 41, no. 1, pp. 3–9, Jan. 1994, Conference Name: IEEE Transactions on Electron Devices, ISSN: 1557-9646. DOI: 10.1109/16.259613.
- [120] Z. Zuo, N. Tang, and H. Chen, “Analysis and improvement of self-heating effect based on GaN HEMT devices,” in *Materials Research Express*, vol. 9, no. 7, p. 075 903, Jul. 2022, Publisher: IOP Publishing, ISSN: 2053-1591. DOI: 10.1088/2053-1591/ac82a8.
- [121] L. Yan, G. Koops, P. Steeneken, A. Heringa, R. Surdeanu, and L. van Dijk, “Integrated heat sinks for SOI power devices,” in *2013 25th International Symposium on Power Semiconductor Devices & IC’s (ISPSD)*, ISSN: 1946-0201, May 2013, pp. 285–288. DOI: 10.1109/ISPSD.2013.6694465.
- [122] A. A. Balandin, S. Ghosh, W. Bao, I. Calizo, D. Teweldebrhan, F. Miao, and C. N. Lau, “Superior Thermal Conductivity of Single-Layer Graphene,” *Nano Letters*, vol. 8, no. 3, pp. 902–907, Mar. 2008, Publisher: American Chemical Society, ISSN: 1530-6984. DOI: 10.1021/nl10731872.
- [123] S. Subrina, D. Kotchetkov, and A. A. Balandin, “Heat Removal in Silicon-on-Insulator Integrated Circuits With Graphene Lateral Heat Spreaders,” *IEEE Electron Device Letters*, vol. 30, no. 12, pp. 1281–

- 1283, Dec. 2009, Conference Name: IEEE Electron Device Letters, ISSN: 1558-0563. DOI: 10.1109/LED.2009.2034116.
- [124] “Onsemi Launches MOSFETs With Innovative Top-Cool Packaging | onsemi.” (), URL: <https://www.onsemi.com/company/news-media/press-announcements/en/onsemi-launches-mosfets-with-innovative-top-cool-packaging>.
- [125] W. Ahn, C. Jiang, J. Xu, and M. A. Alam, “A new framework of physics-based compact model predicts reliability of self-heated modern ICs: FinFET, NWFET, NSHFET comparison,” in *2017 IEEE International Electron Devices Meeting (IEDM)*, ISSN: 2156-017X, Dec. 2017, pp. 13.6.1–13.6.4. DOI: 10.1109/IEDM.2017.8268386.
- [126] U. S. Kumar and V. R. Rao, “A Novel TCAD-Based Thermal Extraction Approach for Nanoscale FinFETs,” *IEEE Transactions on Electron Devices*, vol. 64, no. 3, pp. 1404–1407, Mar. 2017, Conference Name: IEEE Transactions on Electron Devices, ISSN: 1557-9646. DOI: 10.1109/TED.2017.2657626.
- [127] S. Kasap, *Principles of Electronic Materials and Devices*, 3rd ed. USA: McGraw-Hill, Inc., Feb. 2005, ISBN: 978-0-07-310464-5.
- [128] A. Halder, L. Nyssens, D. Lederer, V. Kilchytska, and J.-P. Raskin, “Comparison of Heat Sinks in Back-End of Line to reduce Self-Heating in 22FDX® MOSFETs,” *Solid-State Electronics*, vol. 207, p. 108 706, 2023, Publisher: Elsevier.
- [129] M. Vanbrabant, L. Nyssens, V. Kilchytska, and J.-P. Raskin, “Back-Gate Lumped Resistance Effect on AC Characteristics of FD-SOI MOSFET,” *IEEE Microwave and Wireless Components Letters*, vol. 32, no. 6, pp. 704–707, Jun. 2022, Conference Name: IEEE Microwave and Wireless Components Letters, ISSN: 1558-1764. DOI: 10.1109/LMWC.2022.3162497.
- [130] K. Goodson and M. Flik, “Effect of microscale thermal conduction on the packing limit of silicon-on-insulator electronic devices,” *IEEE Transactions on Components, Hybrids, and Manufacturing Technology*, vol. 15, no. 5, pp. 715–722, Oct. 1992, Conference Name: IEEE Transactions on Components, Hybrids, and Manufacturing Technology, ISSN: 1558-3082. DOI: 10.1109/33.180035.

- [131] E. Pop, R. Dutton, and K. Goodson, “Thermal analysis of ultra-thin body device scaling [SOI and FinFet devices],” in *IEEE International Electron Devices Meeting 2003*, Dec. 2003, pp. 36.6.1–36.6.4. DOI: 10.1109/IEDM.2003.1269420.