FinFET characterization up to 110 GHz

D. Lederer[1], N. Collaert[2] and J.-P. Raskin[1]

[1]*Microwave Lab., Université catholique de Louvain, Place du Levant 3, 1348 Louvain-la-Neuve*
Tel.*: +32/10/478105,* 🖷*: +32/10/478705,* 🖃*: lederer@emic.ucl.ac.be*
[2]*IMEC, Kapeldreef 75, 3001 Heverlee*

1. INTRODUCTION: We propose in this work a detailed analysis of the analog performance of 50-nm gate length finFETs in dynamic regime up to 110 GHz.

2. DYNAMIC PERFORMANCE: The finFET dynamic performance was investigated on 50 nm-long RF devices with 2 gate fingers (N_{finger}) of 5, 15, 25 and 30 µm width (W_{finger}), a fin width W_{fin}= 55 nm and a fin spacing (S_{fin}) of 100 nm. The current ($|H_{21}|$) and maximum available gains (MAG) are plotted in Figure 1 for W_{finger} = 15 µm. It is seen that a zero-pole doublet appears in the gain curves. This effect is adequately modelled with an extended small-signal equivalent circuit (Figure 1) in which a second device (with both negligible g_{m2} and g_{d2}) is added in parallel with the active device. This second device could be associated with a parasitic channel either in the corners, at the top or the bottom of the fins. The extraction of the circuit elements was based on [1] and their values are given in [2]. The gain curves exhibit much better fitting up to 110 GHz when the parasitic device is included (Figure 1, simulation 1: classical circuit vs simulation 2: extended circuit). Extracted gate resistance values indicate too that the sheet resistivity of the polysilicon gate (R_{gres}) is very large, causing a harsh reduction of f_{max} [3]. This is due to an incomplete silicidation of the gate near the polySi/BOX interface between the fins. Silicidation must therefore be optimized in finFET processing. Reducing R_g could also be achieved by optimizing the RF structure and increasing N_{finger} (while keeping the same total device width). Figure 3 outlines the f_{max} increase obtained by: (1) N_{finger} optimization, (2) complete gate silicidation (R_{gres} = 4 Ω/sq), (3) use of a metallic gate (R_{gres} = 0.02 Ω/sq). It is seen that the increase of f_{max} saturates and is actually limited by the low value of the C_{gs}/C_{gd} and g_m/g_d ratios [2, 3]. An efficient way to increase these figures would be to decrease SCE by reducing W_{fin}. It is shown in [2] that in this case f_t and f_{max} values become higher than 200 GHz and 100 GHz, respectively.

3. CONCLUSION: RF measurements of finFETs have been presented and accurately modeled up to 110 GHz for the first time. It is shown that: (1) an additional distributed passive network must be added in the small signal circuit, (2) silicidation optimization must be considered for finFETs in order to reduce the gate resistivity and increase f_{max}..

REFERENCES

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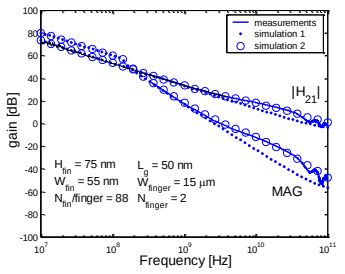

Fig.1. Measured and simulated gains for W_{finger} = 15 µm.

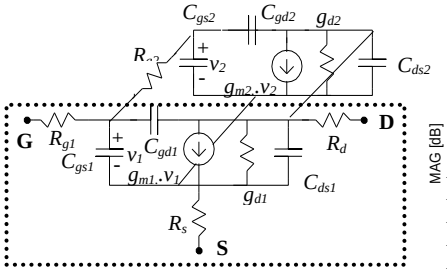

Fig.2.: Classical (inside box) and extended equivalent circuit used for finFET modelling.

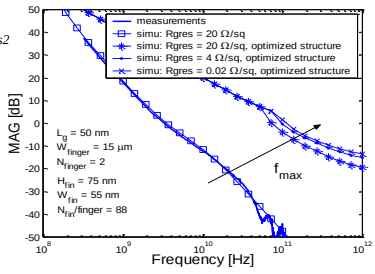

Fig.3. Measured and simulated MAG for the experimental finFET, and for optimized (N_{finger} = 76) RF finFET devices with varying R_g