Wideband characteristics of multigates MOS devices

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Invited paper

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Introduction: In the past few years, there has been much hype in the research and characterization of various forms of novel devices to overcome the short channel effects (SCE) in single gate MOSFETs, to increase current drive, integration density, reduce power consumption and to scale the device according to the International Roadmap of the Semiconductor Industry Association (ITRS). Recently, besides the Silicon-on-Insulator (SOI), strained-Si, several types of multiple-gate devices have been proposed in the literature such as Double-Gate (DG), Triple-Gate (TG), FinFET's, Pi-Gate (PG), Quadruple-Gate (QG), Omega-Gate (Ω-G), etc. Some early research demonstrated the great interest of these multiple-gate devices in the subthreshold region. In the present work, results from simulations and wideband characterizations of multiple-gate devices are deeply analyzed and compared to the prediction of the ITRS for determining the position of such devices to the roadmap. To our knowledge, the potential of multiple-gate compared to single-gate devices is demonstrated for the first time in both static and dynamic operation regimes and from subthreshold to saturation regions. The high frequency behavior of the devices are analyzed based on the following key parameters: intrinsic gate-capacitances which comprise the gate-to-source capacitances (C_{gs}) and the gate-to-drain capacitances (C_{gd}), the ratio between the gate-to-source and gate-to-drain capacitances (C_{gs}/C_{gd}), transconductance (g_m), cut-off frequency (f_T) and the current gain (H_{21}).

Description of the analyzed devices: Tridimensional (3-D) numerical software called Atlas – SILVACO was used for all of the static and dynamic simulations. The dimensions of the PG, TG, DG and SG SOI MOSFETs are: gate oxide thickness (t_{ox}) = 2 nm, silicon film thickness (W_{fin}, t_{Si}) = 20 nm and buried oxide thickness (t_{box}) = 150 nm. The doping level of the silicon film is 10^{15} cm^{-3} and the channel length (L) varies between 25 nm to 200 nm. The extension of the gate into the BOX for the PG devices was fixed to 20 nm. This length demonstrated to be sufficient for strongly reducing the short channel effects (SCE) in [3]. In order to take into account the parasitic capacitances of the transistors, the 3-D interconnection lines were introduced in the simulations. The simulations were done using the energy balance model and the gate electrode workfunction was set to 4.67 eV corresponding to Molybdenum. The physical models used for the simulations accounted for electric field dependent lifetime, transverse field dependent mobility, SRH recombination/generation, bandgap narrowing and carrier statistics. In the AC analysis, a small signal frequency from 1 MHz to 500 GHz with an amplitude of 30 mV was applied. FinFETs with L ranging from 10 μm down to 50 nm and an equivalent oxide thickness (EOT) of 2 nm built at IMEC were measured in DC up to 110 GHz.

Discussions and conclusion: In the static region, it is clear that multiple-gate devices have the edge over single-gate devices due to the advantage of the volume inversion effect. Quasi-ideal subthreshold slope, Low Drain Induced Barrier Lowering (DIBL), weak threshold voltage roll-off were simulated and measured for multigate devices with L as short as 50 nm. Multiple-gate devices operating in fully depleted mode show high Early voltage (> 100 V) translating to high intrinsic voltage gain which leads to their great interest for the 45 nm node as listed in the ITRS. The dynamic measurements and simulations have shown that moving down to the 45 nm node, the advantages of the multiple-gate structures will bring great improvement in the various analog figures of merit. It has been shown that cut-off frequency of more than 200 GHz can be reached with 50 nm FinFETs. From the simulations, it was also shown that even for the multiple-gate devices, there is a degradation of their characteristics when the gate length is reduced beyond the 25 nm node due to an increase of SCE. To benefit further beyond this node, there are mainly 2 options: i) to reduce the silicon thickness, however, this will increase the access resistances of the source and drain, and therefore the use of optimized silicidation, localized silicon epitaxy or low Schottky barrier contacts will have to be considered or ii) to decrease the equivalent oxide thickness without increasing the gate leakage current via the use of high-k materials. We have also shown that for Triple-gate/FinFET devices, the width/length per fin is an important aspect with relation to the reduction of parasitic capacitances and the increase of current density per unit area. In general, the outlook for the multiple-gate devices in the achieving the objectives listed out in the ITRS is bright because all the technological improvements presented here are already under development for deep submicron single gate MOSFETs.