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Tapeout-Oriented Strategies for Teaching Analog/Mixed-Signal IC Design and Implementation in Electrical Engineering Education

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***Abstract*—Analog and mixed-signal (AMS) integrated circuit (IC) design is essential for modern SoC development in applications such as AI, IoT, and robotics. However, AMS design remains largely manual, requiring engineers to navigate multiple abstraction levels and complex iterations. Traditional engineering education rarely equips students with the skills needed for this challenge. In this paper, we propose a set of tapeout-focused strategies for AMS education based on open-source tools and full-chip design flows. Drawing on over three years of experience at AC3E-USM in Chile, we outline an educational approach combining programmatic design, collaborative version control, and real fabrication timelines. We highlight student participation in global initiatives like the SSCS Chipathon and IHP multi-project runs, supported by resources such as the SKY130 and IHP open-source PDKs, Docker-based flows, and GitHub-based team coordination. Two case studies demonstrate how this approach enables meaningful hands-on learning and fosters a foundation for regional academic–industry collaboration in the global semiconductor ecosystem.**

***Keywords*—Engineering education, open source silicon, power management, integrated circuit, CMOS, AMS, microelectronics**

I. Introduction

It is increasingly evident that traditional approaches to integrated circuit (IC) design education in most engineering schools are insufficient to graduate engineers who are ready to perform the complex design tasks demanded by today's semiconductor industry [1], [2]. This challenge is particularly significant in the field of AMS IC design, where the required skill set is evolving rapidly due to the large complexity of modern chips.

Nowadays, AMS IC designers are expected to possess not only a solid foundation in electronics, but also strong competencies in programmatic/generator-based design methodologies [3], system-to-block specification derivation knowledge, and effective project management. These competencies are essential in the context of contemporary system-on-chip (SoC) and application-specific IC (ASIC) design workflows, which integrate analog and digital subsystems to support applications in artificial intelligence, IoT, data centers, and autonomous systems. Despite the high level of complexity in these systems, analog design processes are still often carried out in a manual, inefficient, error-prone, and non-replicable fashion [4].

Tapeout-oriented courses aim to bridge theory and practice by guiding students through real chip design using actual fabrication processes and deadlines [5], [6]. Despite their educational value, these courses have become harder to implement due to high EDA tool costs, long design cycles, logistical challenges, and the need for an experienced teaching team [1].

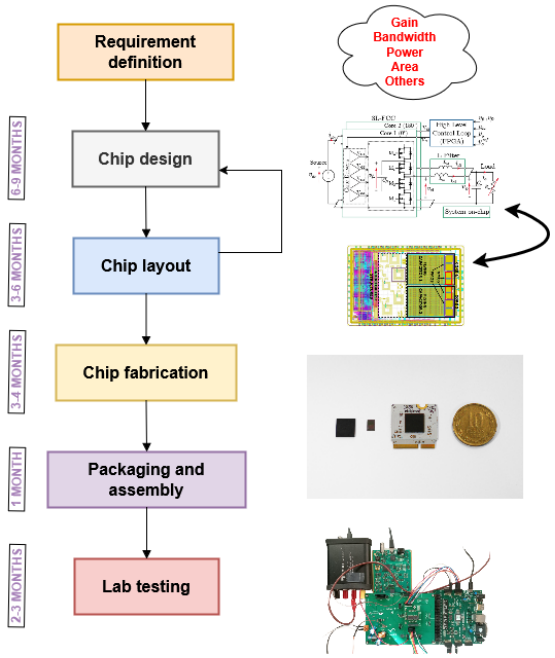


Fig. 1: Typical chip development process [1].

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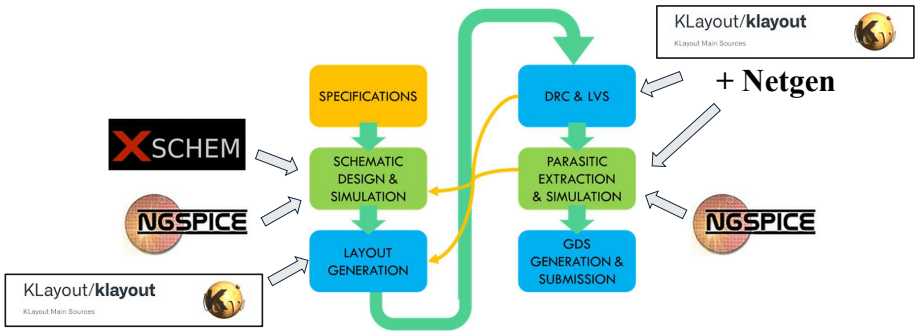


Fig. 2: AMS IC design flow block diagram (including tools used with the IHP PDK).

Still, they offer essential hands-on experience beyond textbook learning, providing a full-system design perspective crucial for real-world readiness in industrial contexts [7].

In this work, we present key strategies and lessons learned over more than three years of experience with AMS IC design education at the AC3E-USM research center in Valparaíso, Chile, where we are actively developing a microelectronics research and training ecosystem. The remainder of this article is organized as follows: Section II discusses the main challenges and emerging topics in AMS IC design education; Section III outlines the initial strategy based on open-source design tools and IEEE-sponsored educational programs; Section IV presents a case study involving the design of a power management IC test structure intended for research use; and Section V concludes the paper.

II. Requirements for Current and Future Industry-Focused Education in AMS IC Design

The growing complexity of SoCs and ASICs has amplified the importance of AMS components. Though they occupy only a small portion of the total chip area compared to the digital blocks, AMS blocks often create bottlenecks due to manual workflows and sensitivity to layout-dependent effects [8], as shown in the AMS design flow block diagram and associated tools in Fig. 2. Designers must work across all abstraction layers—system to layout—requiring multiple iterations to meet targets. Limited automation prolongs time-to-market and reduces reuse. To overcome this, design flows must enable automation, support cross-technology reuse, and remain aligned with established practices [4].

Meeting these industry demands requires a new generation of engineers equipped with a robust and modern skill set. Professionals must be fluent in programmatic and generator-based design methodologies, capable of deriving detailed block-level specifications from high-level system requirements, and proficient in automating EDA workflows through scripting. In addition to technical depth, effective project management, version control, thorough documentation, and communication skills are essential. The ability to clearly articulate and defend design decisions—whether in design reviews or in customer-facing contexts—is increasingly valued [9].

To develop such professionals, engineering education must evolve. Curricula should incorporate project-based learning that mimics real-world design cycles and emphasizes accountability, collaboration, and system thinking. Students must gain confidence in applying their engineering skills to end-to-end design challenges. Education should also leverage open-source tools and knowledge, enabling broader accessibility and transparency. Importantly, it should foster a mindset centered around full-chip flows (as presented in Fig. 1), from specification to implementation. This includes cultivating approaches based on automation paradigms that remain largely absent from the skillsets of traditionally trained AMS IC designers.

III. Existing Educational Programs, Courses and Resources Based on Opensource Silicon AMS IC Design

Since 2020, the release of the SkyWater 130nm open-source PDK (SKY130) [10]—supported by Google and hosted on the Efabless platform—has catalyzed a vibrant open collaboration ecosystem in integrated circuit design [11]. This ecosystem enables students and professionals worldwide to design, simulate, fabricate, and share AMS IC projects with unprecedented accessibility.

Building on this, the IEEE Solid-State Circuits Society (SSCS) launched the PICO program in 2021 to promote education, mentoring, and collaborative IC fabrication. A key event is the SSCS Chipathon, enabling weekly online teamwork to efficiently fill silicon area with integrated designs. The AC3E team at Universidad Técnica Federico Santa María (AC3E-USM) and Universidad del Bío-Bío (UBB, a 2021 participant) joined the 2022 Chipathon. Both teams later were awarded at the SSCS Code-a-Chip contest, which promotes reproducible design using open-source tools and notebook-driven workflows [12]. For our team, this experience led to automating the Chipathon chip design, resulting in a specification-to-GDS

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process for power stage and gate driver design, recently reported in [13].

Other educational initiatives providing fabrication access to the open-source community include IEEE CASS's UNIC-CASS program, which delivers end-to-end IC design-to-test experiential learning [14]; the Efabless Chipalooza challenge, promoting rapid design and fabrication of analog/mixed-signal blocks; and the IEEE Electron Device Society's Latinpractice program, centered on digital block design submitted via the Tiny Tapeout platform [15].

Additionally, several AMS design courses using open-source silicon flows have recently emerged, including Boris Murmann's EE628 [16], Harald Pretl's Analog Circuit Design [17], Benjamin Reyes' course [18], and Carsten Wulff's Analog Integrated Circuits [19], offering extensive learning resources for all experience levels.

A key enabler of these educational efforts is the availability of robust, integrated design toolchains. The open-source community benefits greatly from comprehensive Docker environments like IIC-OSIC-TOOLS [20], which package critical EDA tools and PDKs into accessible containers for both AMS and digital IC design. Our contribution, the usm-vlsi-tools Docker environment [21], is a streamlined version focused on AMS tapeout workflows, validated by two successful tapeouts in the IHP 130 nm open-source technology.

Together, these programs, courses, and tool environments form a foundation for accessible, project-based AMS IC education. In the next section, we present two detailed case studies that illustrate how fully open-source design flows can be effectively integrated into educational experiences.

IV. Case Studies: Educational Experiences Using Fully Open-Source AMS Design Flows

Gaining insight into the full chip design process remains uncommon in academic publications, particularly when it comes to AMS projects. In this section, we present two case studies developed entirely by the AC3E-USM team, showcasing end-to-end educational experiences—including concept, design, layout, tapeout, test setup, and lab validation—using fully open-source design flows.

Beyond the pedagogical and logistical complexities of tapeout-oriented education [1], implementing IC design projects in developing countries adds further challenges: import restrictions, limited technical infrastructure, and scarce access to test equipment and components. Yet, these constraints can also drive innovation and deepen student engagement.

Our approach incorporated basic project management practices such as GitHub-based version control, weekly design meetings, collaborative documentation (including pin lists and early-stage floorplans), and an emphasis on real-world deadlines. These experiences were also aligned with research outputs, providing students early exposure to advanced, high-impact topics.

The following subsections describe two representative examples of AMS IC educational projects, highlighting practical, reproducible strategies for accelerating student learning in open-source chip design.



Fig. 3: Chipathon 2022 AC3E-USM team.

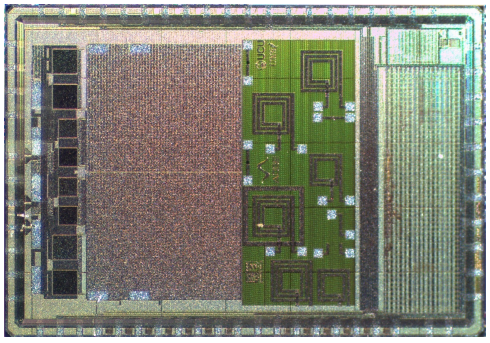


Fig. 4: Chipathon 2022 fabricated chip.

A. 3-level flying capacitor converter chip designed at Chipathon 2022

Our first hands-on chip design experience as the AC3E microelectronics team began with the 2022 edition of the SSCS Chipathon. Despite limited institutional tradition in IC design, our call for participants gathered 11 enthusiastic students, supported throughout by two academic mentors (see Fig. 3).

The chosen project addressed a relevant and modular application: power management for CubeSats. A 3-level flying capacitor converter (3LFCC) topology was selected for its research potential and manageable complexity, particularly since it allowed partial off-chip implementation: the control circuitry was implemented on an FPGA to simplify design and testing, focusing instead on integrating the power switched, gate drivers and flying capacitor on-chip (Fig. 4).

We quickly adopted a "tiny design house" model, splitting into circuit simulation and layout teams. An early lesson was the value of starting layout work even before final circuit validation, to build familiarity with physical design/verification tools and the Skywater 130nm PDK features. The weekly mentoring sessions with highly experienced designers and researchers proved invaluable, imparting design methodologies and best practices that have continued to benefit the team in all subsequent projects.

Using the Efabless Caravan platform (an analog variant of Caravel [11]) allowed us to bypass pad ring design, though it

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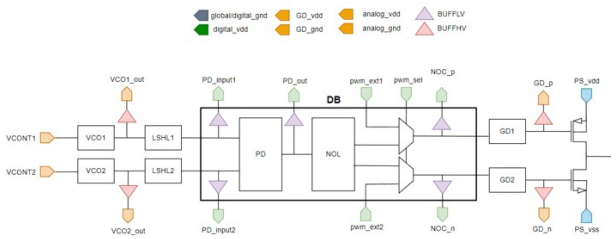


Fig. 5: IHP November 2024 tapeout time-domain DC-DC converter block diagram.

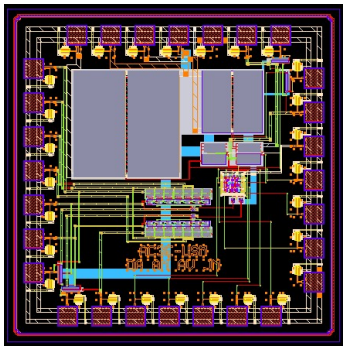


Fig. 6: IHP November 2024 tapeout time-domain DC-DC converter chip layout submitted by the AC3E-USM team.

constrained pad selection. Our design emphasized testability, planning multiple measurement points across the power path. However, the use of ESD-protected pads for connecting the flying capacitor unintentionally limited the chip's input voltage range to 3.3,V, affecting performance in ways we could not fully resolve.

Fabrication delays stretched beyond one year, disrupting our original timeline. Nevertheless, the chip was successfully brought up and validated block-by-block. Despite setbacks, the project was a valuable learning experience and yielded both simulation [22] and silicon-validated results [23].

B. Time-domain buck DC-DC converter designed and submitted to IHP November 2024 free run

A second key educational project at AC3E was the design and tapeout of a fully integrated time-domain buck DC-DC converter, submitted to the IHP November 2024 free run using its open-source CMOS technology. This more complex effort included full integration of power stage, gate drivers, and time-domain control, and lacked pre-designed pad rings. The team also had to adapt to the unfamiliar IHP PDK.

Unlike the large undergraduate team in the 2022 Chipathon, this project was executed by 3 master-level students: one member handled top-level integration (pin list, pad ring, early floorplanning, interconnection), another focused on analog layout, and a third managed analog block design and simulations. Digital blocks were synthesized using OpenLane and integrated as macros. A mentor coordinated design reviews, planning, and provided early block- and system-level simulations. Testability and modularity were enabled using isolated power domains, variable control parameters, and multiple probing points (see Fig. 5).

Improved team coordination tools were critical. Performance targets, design risks, and updates were shared through regular meetings and a shared design log. An initial prototype in SKY130 was completed during August–September 2024 [24], followed by technology migration and final implementation in October–November 2024.

The entire project was developed using the `usm-vlsi-tools` Docker environment [21], which proved to be an effective platform for team-based AMS IC design and academic tapeout preparation.

C. Next challenges

As open-source AMS IC design education matures, several key challenges remain. Standardizing packaging, breakout boards, and test infrastructure would ease lab validation and lower costs—efforts already initiated by Efabless and echoed by others. Reducing the duration of design–fabrication–test cycles is another priority, as real-world timelines often exceed the expectations provided in [1].

Strengthening the link between educational projects and research is critical for sustained mentor engagement. Open-source methods are gaining academic traction, especially for research in mature nodes like 180nm and 130nm. Industrial trust, however, remains limited. Demonstrating tool reliability and fostering collaborative development can help change this perception, especially with support from agile SMEs.

Finally, future educational strategies, such as gamification and deeper research integration, highlighted at the CICC 2025 panel "Potential of Open Source Design for Analog/Mixed Signal IC Education" [25]–[27], point toward a more innovative and engaging learning landscape.

V. Conclusion

According to the 2023 SIA report [28], the U.S. semiconductor industry will face a deficit of 27,300 engineers by 2030—a gap likely mirrored globally. We argue that Latin America, with its strong universities and adaptable academic environment, can help address this need by training engineers in AMS IC design through accessible, open-source, tapeout-driven education.

This paper outlined key educational challenges in this domain and presented two successful case studies where students with limited prior experience completed full tapeout projects. These examples show that meaningful engagement is possible, even in resource-constrained environments.

Looking ahead, we expect these initiatives to expand and mature, forming a steady pipeline of engineers with practical design experience. Beyond workforce development, we aim to foster a local ecosystem that supports academic–industry collaboration at national and regional levels—empowering Latin America not only to consume but also to design, innovate, and lead within the global semiconductor landscape.

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