Influence of Geometrical Parameters on the DC Analog Behavior of the Asymmetric Self-Cascode FD SOI nMOSFETs

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***Abstract*—This paper assesses the DC analog performance of a composite transistor named Asymmetric Self-Cascode structure, which is formed by two Fully Depleted SOI nMOSFETs connected in series with shortened gates. The influence of geometrical parameters, such as different channel widths and lengths on the transistors at source and drain sides is evaluated through three-dimensional numerical simulations, which have been firstly adjusted to the experimental measurements. The transconductance, output conductance, Early voltage and intrinsic voltage gain have been used as figures of merit to explore the advantages of the composite transistor. From the obtained results, the largest intrinsic voltage gain has been obtained by using longer channel lengths for both transistors, with narrower device close to the source and wider transistor near to the drain.**

***Index Terms*—Asymmetric Self-Cascode, FD SOI nMOSFET, Composite Transistor, Analog Performance.**

I. INTRODUCTION

Mixed-signal ICs require solutions to embed high-performance analog circuits using digital CMOS transistors [1,2]. A good alternative is to use fully-depleted (FD) Silicon-on-Insulator (SOI) technology, that presents a buried oxide layer between the active region and the substrate, featuring an intrinsic dielectric insulation between the devices and the substrate [3]. These FD MOSFETs show several analog advantages compared with the bulk Si counterparts, which are mostly linked to the reduced body factor, sharper subthreshold slope [4] and larger transconductance to drain current ratio (g_m/I_D) [5]. Despite of these advantages, degradation of the analog behavior of FD SOI transistors can occur owing to the floating body of SOI transistors. The high electric field close to the drain may cause the occurrence of parasitic bipolar effects, reducing the breakdown voltage due to the impact ionization of carriers [6].

An alternative to boost the analog characteristics of FD SOI transistors is the self-cascode structure, where two transistors are connected in series with short-circuited gates, operating as a single device [7,8]. The performance gain is related to the increase of channel length, which decreases the output conductance (g_D), and the reduction of parasitic bipolar effects, since part of the generated carriers due to the impact ionization are recombined in the intermediate N+ region between the two transistors.

In order to further reduce the output conductance while keeping the good advantages of reduced short-channel lengths, such as larger drain current (I_D) and transconductance (g_m) levels, a modification in the composite structure has been proposed in [9,10]. In general, both transistors present same channel doping concentrations. The alternative configuration is called Asymmetric Self-Cascode (A-SC) structure, depicted in Fig. 1, where L_S (W_S) and L_D (W_D) are the channel lengths (widths) of the individual transistors near the source (M_S) and the drain (M_D), respectively. The total channel length (L) of the A-SC structure is given by $L_S + L_D$. In this configuration, the transistor near the source presents higher channel doping concentration, fixing the threshold voltage (V_{TH}) of the A-SC structure, whereas the device near the drain has its channel already inverted for gate voltages close to the threshold voltage of the A-SC structure. This way, depending on the bias conditions, the effective channel length becomes equal to only L_S, increasing the drain current and transconductance levels [11]. Besides that, the presence of the M_D transistor with reduced channel doping concentration decreases the peak electric field at the channel/drain junction and, consequently, the impact ionization effect. Also, there is an improvement on the output conductance when the transistor near the drain works in saturation regime, absorbing part of the drain voltage variation applied in the overall structure [11].

The A-SC structure has been successfully implemented with planar SOI devices, by using different channel doping concentrations [9,10,11], or by using different back-gate biases to promote different threshold voltages in undoped ultra-thin body and buried oxide FD SOI transistors. According to [11], the intrinsic voltage gain ($A_V = g_m/g_D$) has been improved with a forward back-gate bias applied to the M_D transistor. Better results have been obtained by applying reverse back-gate bias to the M_S transistor [12].

The objective of this work is the study of the influence of the channel widths and lengths of the transistors near the

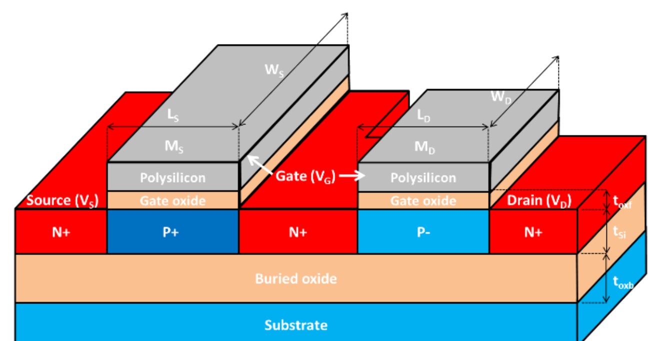

Fig. 1 Asymmetric Self-Cascode structure composed by FD SOI nMOSFETs.

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source and drain on the analog performance of the A-SC structure through three-dimensional numerical simulations, with the aim to obtain the largest intrinsic voltage gain. Section II presents the device characteristics and the measurement setup. In Section III, the DC analog study is performed through three-dimensional numerical simulations. The following figures of merit are analyzed: transconductance, output conductance, Early voltage ($V_{EA} = I_D/g_D$) and intrinsic voltage gain. In the end, Section IV summarizes the main conclusion of this paper.

II. Device Characteristics and Measurement Setup

The measured devices have been fabricated in a FD SOI CMOS technology from UCLouvain, Belgium [13]. The experimental single transistors present channel length of 2 µm and width of 20 µm. The gate oxide (t_{oxf}), silicon film (t_{Si}) and buried oxide (t_{oxb}) thicknesses are 31, 80 and 390 nm, respectively. The M_S transistor presents channel doping concentration of about 6×10^{16} cm^{-3}, whereas the M_D transistor is kept at the natural wafer doping concentration of 1×10^{15} cm^{-3}. The experimental I-V curves have been obtained using the Keithley 4200 Semiconductor Characterization System.

III. DC Analog Performance Analysis

Firstly, the model parameters of simulation files have been adjusted to fit the measured I-V curves with the three-dimensional numerical simulations, which have been performed using Sentaurus Device software [14]. Fig. 2 presents the comparison between simulated and experimental drain current and transconductance as a function of the gate voltage overdrive ($V_{GT} = V_{GS} - V_{TH}$) for the A-SC $W_S = W_D = 20$ µm; $L_S = L_D = 2$ µm structure, obtained at $V_{DS} = 50$ mV (A) and 1.5 V (B).

It is possible to see that the simulated I_D and g_m are closer to the measurements. The drain current and output conductance are presented as a function of V_{DS} in Fig. 3 for the same A-SC structure, extracted at $V_{GT} = 200$ mV. Again, one can see that the simulations fit the experimental data with good agreement, which validates the analysis of the influence of the channel widths and lengths on the analog behavior of the A-SC structure through three-dimensional numerical simulations.

A. Influence of the channel widths

Once the simulations have been adjusted, the DC characteristics of the A-SC structures have been assessed by varying the channel widths of the M_S and M_D transistors. Fig. 4 shows the I_D and g_m vs. V_{GS} curves for $W_D = 2$ µm varying W_S, extracted at $V_{DS} = 1.5$ V. One can notice that the increase of W_S increments the drain current and the transconductance in the entire V_{GS} range, since the dominant transistor in the A-SC structure is the M_S device. This way, the drain current of the A-SC structure is proportional to the channel width of the transistor near the source.

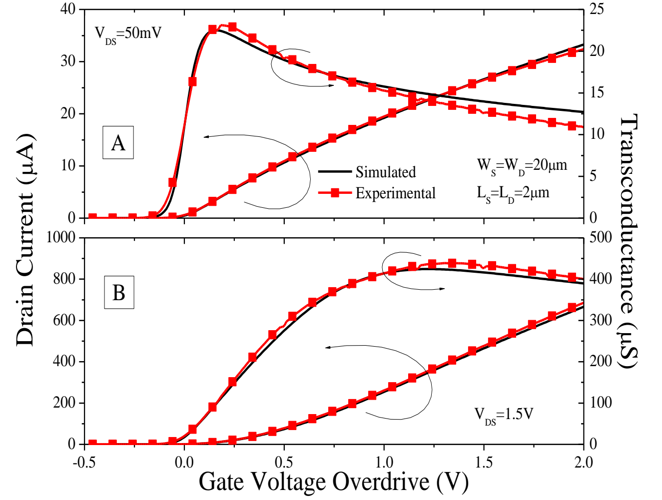

Fig. 2 Drain current and transconductance as a function of the gate voltage overdrive for the A-SC with $W_S = W_D = 20$ µm; $L_S = L_D = 2$ µm structure, extracted at $V_{DS} = 50$m V (A) and 1.5 V (B).

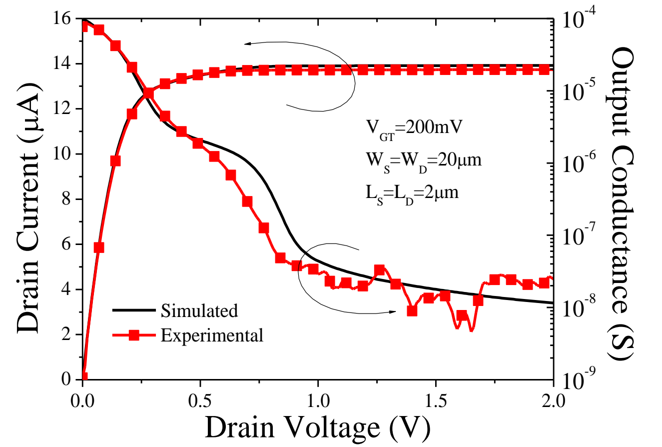

Fig. 3 Drain current and output conductance as a function of the drain voltage for the A-SC $W_S = W_D = 20$ µm; $L_S = L_D = 2$ µm structure, extracted at $V_{GT} = 200$ mV.

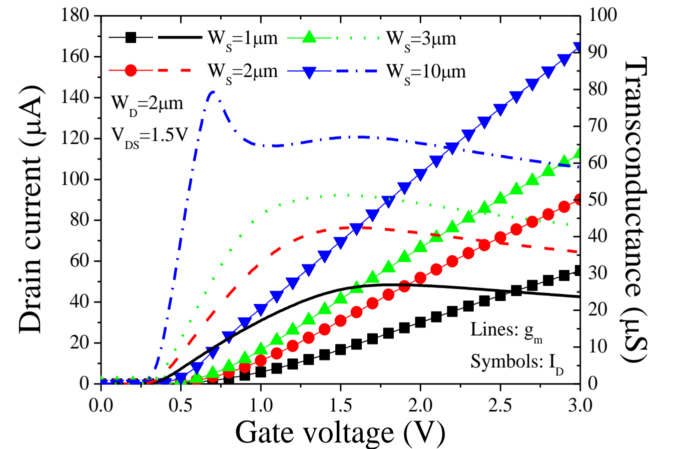

Fig. 4 Simulated drain current and transconductance as a function of the gate voltage for A-SC $W_D = 2$ µm structures varying W_S, extracted at $V_{DS} = 1.5$ V.

In Fig. 5, the influence of the channel width of the M_D transistor on I_D and g_m levels is evaluated as a function of V_{GS}, fixing $W_S = 2$ µm, biased at $V_{DS} = 1.5$ V. One can note at lower V_{GS} that the increase of W_D does not cause a significant variation on I_D and g_m levels, which is linked to

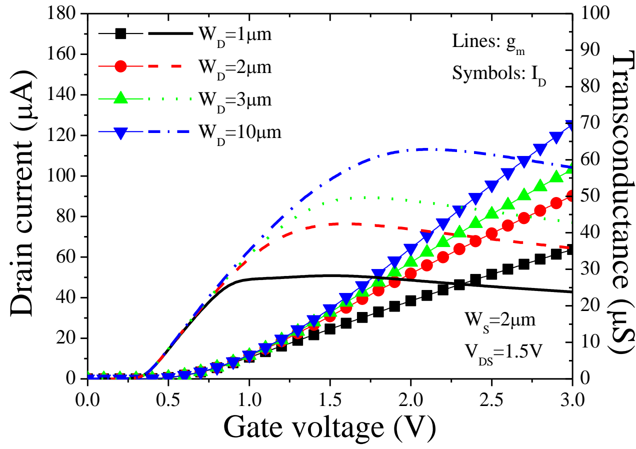

Fig. 5 Simulated drain current and transconductance as a function of gate voltage for A-SC W_S =2 μm structures varying W_D, at V_{DS} = 1.5 V.

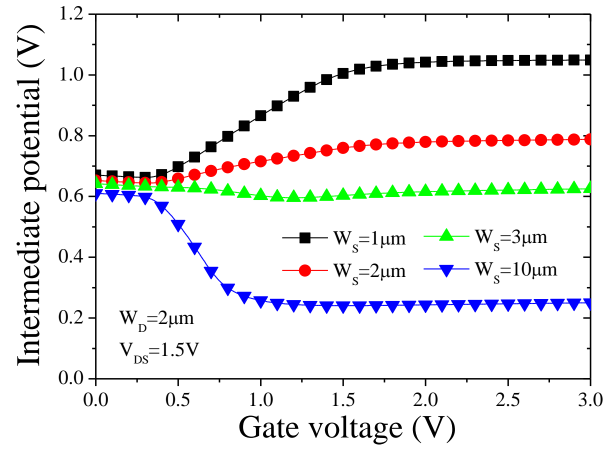

Fig. 6 Simulated intermediate potential as a function of the gate voltage for A-SC W_D = 2 μm structures varying W_S, extracted at V_{DS} = 1.5 V.

the higher electron concentration in the M_D transistor, owing to its lower threshold voltage compared to the M_S transistor. This way, the M_S transistor controls the A-SC structure at low gate voltage.

When V_{GS} increases, the M_D transistor begins to have influence on I_D and g_m, which is linked to the closer electron concentrations in both M_S and M_D transistors [15]. Thus, the M_D transistor becomes important in the current flow, and the wider the M_D transistor, the larger drain current and transconductance are obtained, since its resistance is reduced.

Looking at Fig. 4, it is possible to observe an anomalous behavior of the transconductance for A-SC structures when $W_S > W_D$. This characteristic is clearer for the A-SC W_S = 10 μm; W_D = 2 μm structure. This anomalous g_m could be of interest for non-linearities analysis when it gets rather flat, reducing the harmonic distortion, however this study is out of scope of this work.

To understand the reason of two g_m peaks, the potential at the intermediate node (V_X) between the M_S and M_D transistors is presented as a function of the gate voltage in Fig. 6 varying W_S with fixed W_D = 2 μm, obtained at V_{DS} = 1.5 V. One can see, for the previously mentioned A-SC structure, a large V_X for V_{GS} close to the threshold voltage, implying higher I_D and g_m.

By increasing V_{GS}, V_X suddenly reduces, decreasing g_m. When V_X is stabilized, there is an increase of g_m linked to the increment of V_{GS} until the moment where the mobility degradation and the similar electron concentrations between M_S and M_D transistors become important, reducing g_m again. In this case, the effective channel length of the A-SC structure is not equal to L_S, but approximates to $L_S + L_D$.

In addition, one can verify that the intermediate potential saturates for high gate voltage. In the case of the A-SC $W_S = W_D$ = 2 μm structure, the saturated V_X is close to half V_{DS}, owing to the similar resistances achieved for the M_S and M_D transistors at high gate voltage, due to the fact of presenting same aspect ratio (W/L) and being biased in strong inversion regime. In that case, the A-SC structure behaves as a uniformly doped transistor with total channel length equal to $L_S + L_D$.

With the increase of W_S, the observed reduction of V_X is related to the decrease of the resistance of the M_S transistor compared with the M_D device. Also, the V_X saturation shifts to lower V_{GS} when $W_S \geq$ 2 μm, which does not occur when W_S is lower than W_D.

Fig. 7 presents the intermediate potential as a function of V_{GS} for W_S = 2 μm changing W_D, extracted at V_{DS} = 1.5 V. Comparing with Fig. 6, the opposite occurs when W_D is incremented, since there is an increase of the intermediate potential due to the reduction of the resistance of the M_D transistor compared with the M_S device. Also, there is no variation in the gate voltage where the saturated V_X begins when $W_D \geq$ 2 μm. However, one can see for W_D lower than W_S, a displacement in the saturated V_X to smaller V_{GS}.

In order to know if I_D proportionally increases with W_S, the drain current has been normalized by W_S in Fig. 8 and plotted against V_{GS} for W_D = 2 μm varying W_S, extracted at V_{DS} = 1.5 V. One can observe that I_D/W_S reduces with the increase of W_S. As the dominant device in the A-SC structure is the M_S transistor at V_{GS} close to V_{TH}, the same normalized drain current would be expected varying W_S. However, both W_S and W_D influence the current flow in the A-SC structure. By increasing W_S and maintaining small W_D, there is a larger resistance for the M_D device compared with the M_S transistor, decreasing V_X, as indicated in Fig. 6, and consequently reducing the normalized drain current.

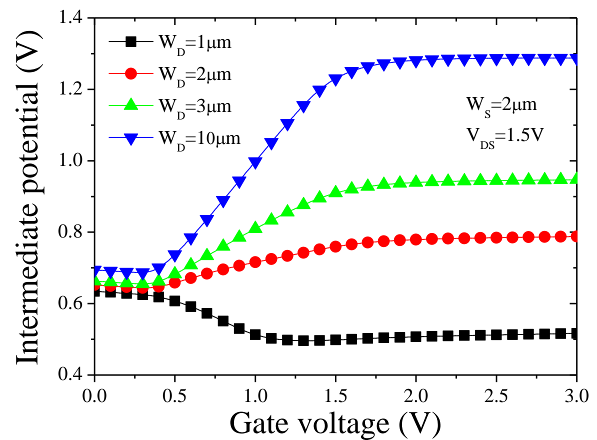

Fig. 7 Simulated intermediate potential as a function of the gate voltage for A-SC W_S = 2 μm structures varying W_D, extracted at V_{DS} = 1.5 V.

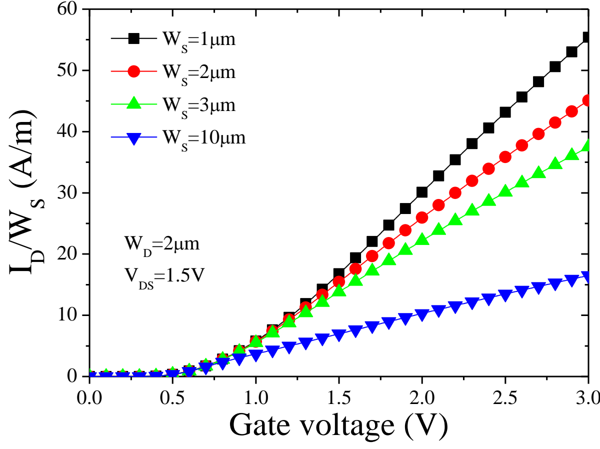

Fig. 8 Simulated drain current normalized by W_S as a function of the gate voltage for A-SC $W_D = 2$ μm structures varying W_S, at $V_{DS} = 1.5$ V.

After studying the I_D vs. V_{GS} curves, we have moved forward to the I_D vs. V_{DS} analysis. Fig. 9 exhibits the drain current and the output conductance as a function of V_{DS} for W_D = 2 μm changing W_S, obtained at $V_{GT} = 200$ mV. As mentioned before, for reduced V_{GT}, the M_S transistor is the dominant device in the A-SC structure. This way, the increment of W_S increases I_D and g_D.

In Fig. 10, the drain current and output conductance are presented as a function of the drain voltage for $W_S = 2$ μm and several W_D, extracted at $V_{GT} = 200$ mV. Opposite to the obtained results in Fig. 9, the increase of W_D practically does not influence the drain current level, however an important characteristic is observed, which is the reduction of the output conductance. This feature can be better explained by Fig. 11, where the intermediate potential and its variation with the drain voltage are presented as a function of V_{DS} for $W_D = 2$ μm changing W_S (A) and for $W_S = 2$ μm varying W_D (B), extracted at $V_{GT} = 200$ mV.

According to Fig. 11(A), there is a reduction of the intermediate potential with the increase of W_S, owing to the lower resistance of the M_S transistor. However, an increase of the intermediate potential variation with the drain voltage is obtained in the saturation regime, implying a larger output conductance. Based on Fig. 11(B), an increase of the intermediate potential with the increment of W_D is

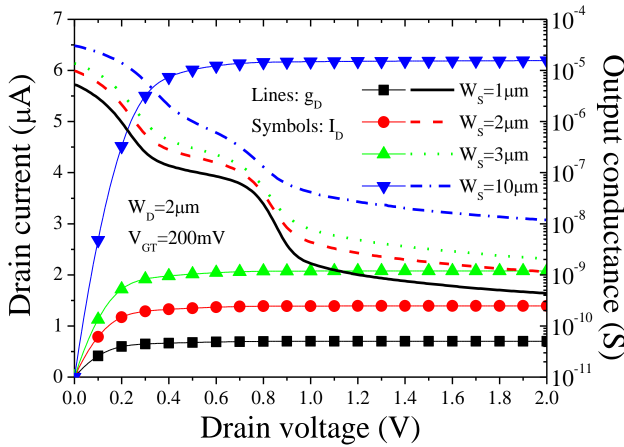

Fig. 9 Simulated drain current and output conductance as a function of the drain voltage for A-SC $W_D = 2$ μm structures varying W_S, extracted at $V_{GT} = 200$ mV.

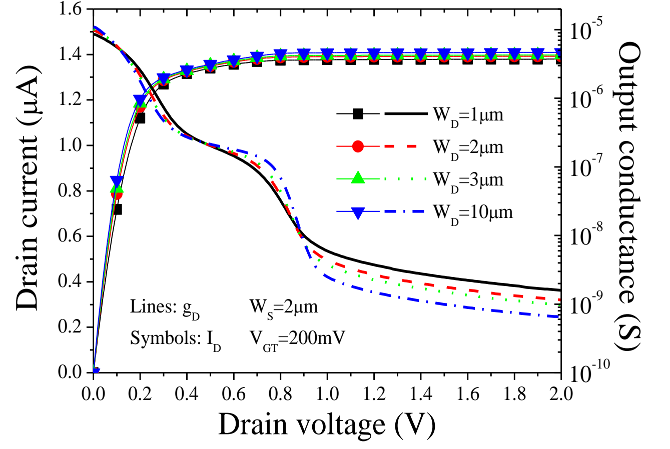

Fig. 10 Simulated drain current and output conductance as a function of the drain voltage for A-SC $W_S = 2$ μm structures varying W_D, extracted at $V_{GT} = 200$ mV.

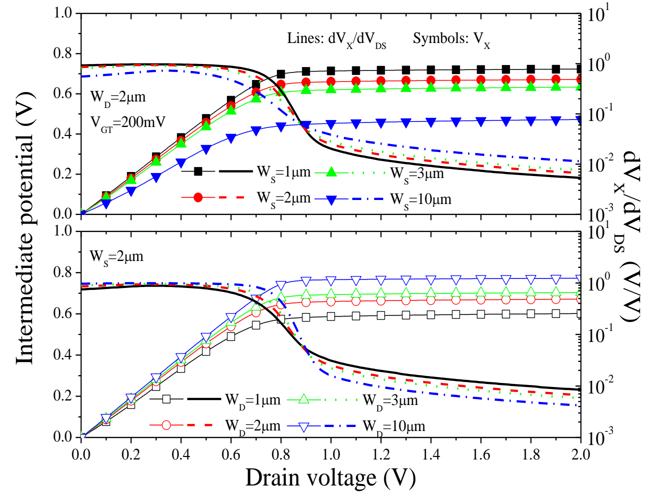

Fig. 11 Simulated intermediate potential and dV_X/dV_{DS} as a function of the drain voltage for A-SC $W_D = 2$ μm structures varying W_S (A) and for A-SC $W_S = 2$ μm structures changing W_D, extracted at $V_{GT} = 200$ mV.

noticed, linked to the lower resistance of the M_D transistor, but there is a smaller intermediate potential variation with the drain voltage in the saturation region, decreasing the output conductance.

Fig. 12 presents the transconductance (A), the output conductance (B), the intrinsic voltage gain (C) and the Early voltage (D) as a function of W_D, extracted at $V_{DS} = 1.5$ V and $V_{GT} = 200$ mV, for different values of W_S. From these results, one can note that the increment of W_D does not affect the drain current level, causes a slight increase of transconductance, but significantly reduces the output conductance, thereby raising V_{EA} and A_V.

By incrementing W_S, there is an increase of transconductance and output conductance, but the g_D rise is larger, reducing the intrinsic voltage gain and the Early voltage. According to Fig. 9, one can observe that the I_D reduction promoted by the narrower M_S transistor is less pronounced than the g_D decrease, which justifies the V_{EA} increase with W_S reduction in Fig. 12(D).

The maximum intrinsic voltage gain and Early voltage have been obtained for the A-SC structure composed by the transistor ($W_S = 1$ μm). Although the transconductance is small in this configuration, the output conductance

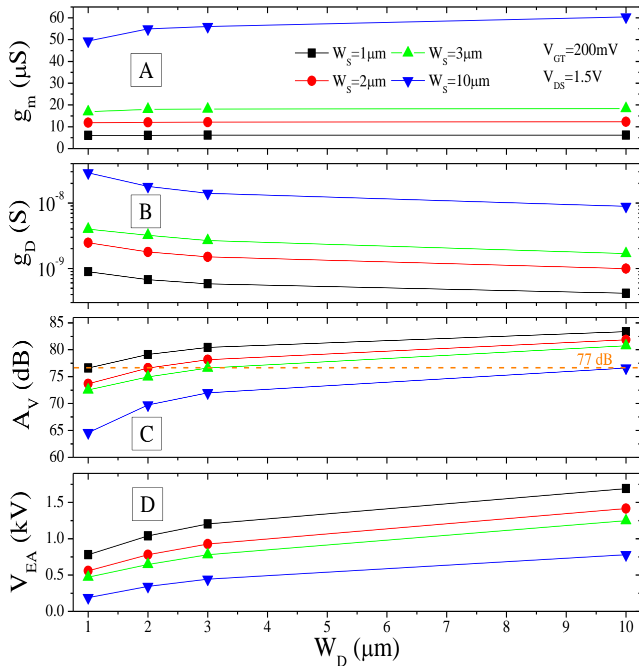

Fig. 12 Simulated transconductance (A), output conductance (B), intrinsic voltage gain (C) and Early voltage (D) as a function of W_D varying W_S, extracted at V_{DS} = 1.5 V and V_{GT} = 200 mV.

considerably reduces, increasing A_V by 7 dB and V_{EA} by a factor of 2 when compared to the A-SC with W_S = W_D = 1 µm.

Additionally, when the A-SC structures are composed by M_S and M_D transistors of same channel widths (dashed line in Fig. 12(C)), it is possible to verify the same intrinsic voltage gain of 77dB, since the intermediate potential does not vary among these A-SC structures. This way, by increasing W_S = W_D, there is a proportional increment of g_m and g_D, obtaining the same A_V.

B. Influence of the channel lengths

After analyzing the analog performance dependence on W_S and W_D, the influence of the channel lengths of each M_S and M_D transistors has been evaluated, considering W_S = W_D = 1 µm.

Fig. 13 presents the I_D and g_m vs. V_{GS} curves for L_D = 2 µm changing L_S, biased at V_{DS} = 1.5 V. In this technology, the minimum channel length to avoid short-channel effects is 2 µm. This way, the results have been plotted as a function of V_{GS}, since the threshold voltages were the same among the A-SC structures. It is possible to see that the rise of L_S reduces I_D and g_m in the whole V_{GS} range. As said before, the transistor near the source is the dominant device in the A-SC structure, controlling the drain current flow.

In Fig. 14, the I_D and g_m vs. V_{GS} curves are shown for L_S = 2 µm and several L_D, obtained at V_{DS} = 1.5 V. As observed in Fig. 5, the influence of longer L_D only impacts at higher V_{GS}, since there is a similarity between the electron concentrations of the M_S and M_D transistors [15]. The longer the L_D, the larger the M_D resistance, reducing I_D and g_m.

The anomalous behavior of g_m is also verified in Fig. 14 when L_D is incremented. This way, by using W_S > W_D or L_S

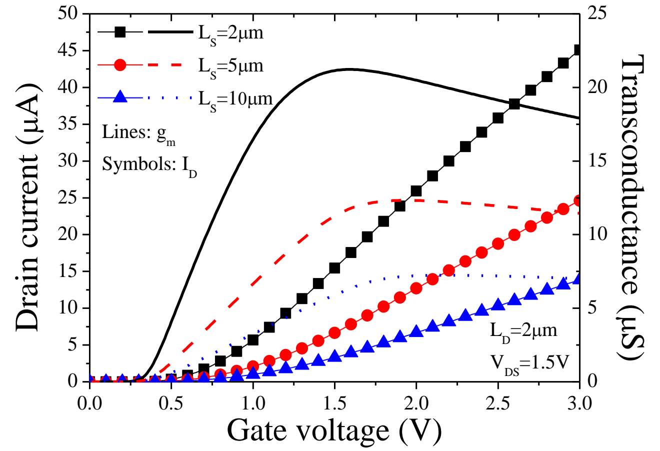

Fig. 13 Simulated drain current and transconductance as a function of the gate voltage for A-SC L_D = 2 µm structures varying L_S, with W_S = W_D = 1 µm, extracted at V_{DS} = 1.5 V.

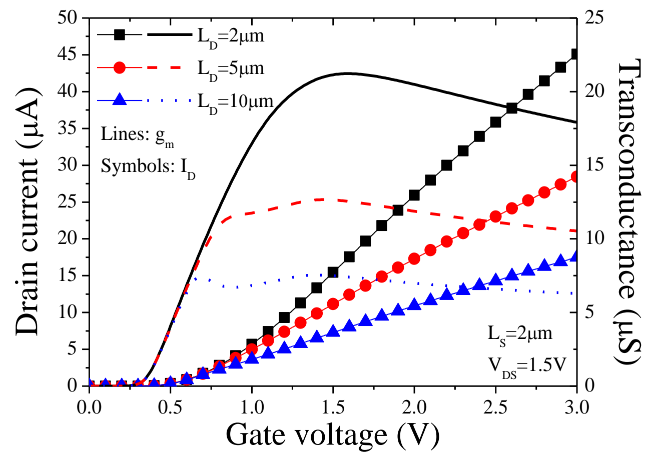

Fig. 14 Simulated drain current and transconductance as a function of the gate voltage for A-SC L_S = 2 µm structures varying L_D, with W_S = W_D = 1 µm, extracted at V_{DS} = 1.5 V.

< L_D, this g_m behavior is observed. By plotting the intermediate potential against V_{GS} in Fig. 15 varying L_S with fixed L_D = 2 µm and in Fig. 16 changing L_D with constant L_S = 2 µm, one can notice that the anomalous behavior of g_m occurs when the intermediate potential reduces with the increase of the gate voltage for V_{GS} close to V_{TH}, which corroborates with the results shown in Fig. 6 and 7.

From Fig. 15, one can see that there is an increase of the intermediate potential with the increment of L_S, since the resistance of the M_S device becomes larger compared with the M_D transistor. The opposite occurs when L_D is incremented in Fig. 16, verifying a reduction of V_X, owing to the larger resistance of the transistor near the drain.

Analyzing the I_D and g_D vs. V_{DS} curves in Fig. 17 for L_D = 2 µm and several L_S biased at V_{GT} = 200 mV, it is possible to notice that the increment of L_S significantly reduces the drain current and output conductance levels, since at lower gate voltage overdrives, the M_S transistor controls the A-SC structure.

Fig. 18 presents the I_D and g_D vs. V_{DS} curves for L_S = 2 µm varying L_D, extracted at V_{GT} = 200 mV. The increase of L_D also reduces the drain current and output conductance levels, but these decreases are slight compared with Fig. 17.

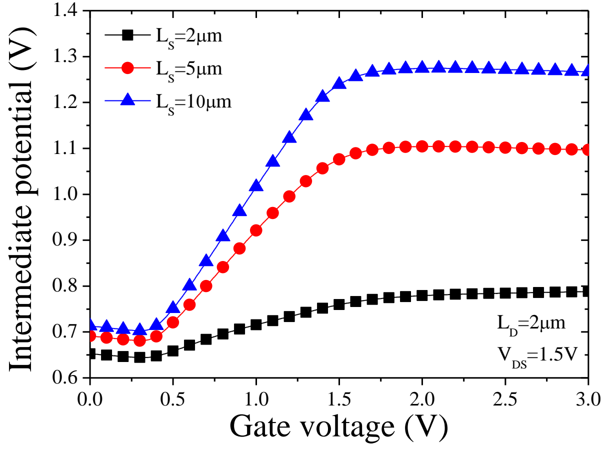

Fig. 15 Simulated intermediate potential as a function of the gate voltage for A-SC $L_D = 2$ µm structures varying L_S, with $W_S = W_D = 1$ µm, extracted at $V_{DS} = 1.5$ V.

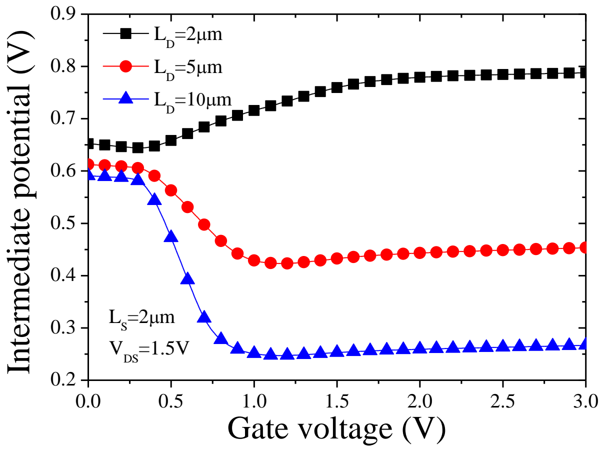

Fig. 16 Simulated intermediate potential as a function of the gate voltage for A-SC $L_S = 2$ µm structures varying L_D, with $W_S = W_D = 1$ µm, extracted at $V_{DS} = 1.5$ V.

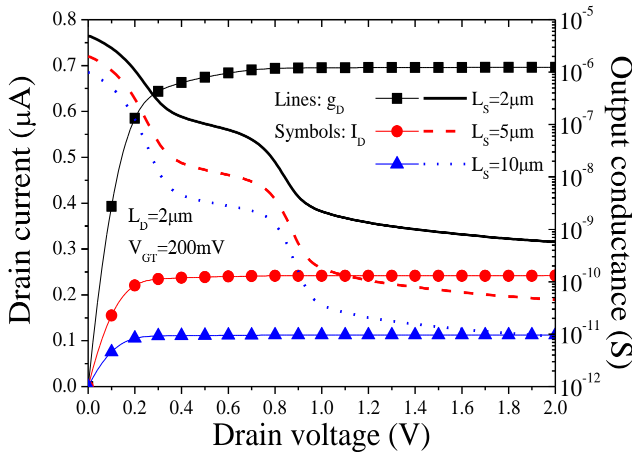

Fig. 17 Simulated drain current and output conductance as a function of the drain voltage for A-SC $L_D = 2$ µm structures varying L_S, with $W_S = W_D = 1$ µm, extracted at $V_{GT} = 200$ mV.

In Fig. 19, the intermediate potential and dV_X/dV_{DS} are plotted as a function of V_{DS} for $L_D = 2$ µm varying L_S (A) and for $L_S = 2$ µm changing L_D (B), obtained at $V_{GT} = 200$ mV. As seen in Fig. 15 and 16, the increase of L_S increments the intermediate potential V_X, whereas the rise of L_D reduces V_X. Looking at the variation of V_X with V_{DS}, one can note, in both cases, a reduction of this variation with the increase of L_S and L_D, which corroborates with the lower output conductance levels obtained in Fig. 17 and 18.

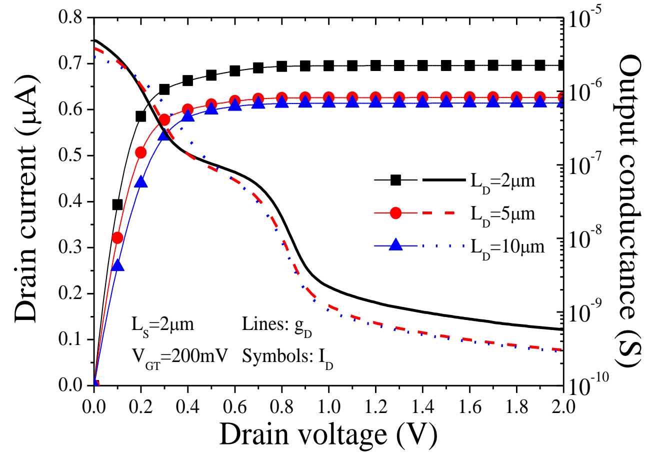

Fig. 18 Simulated drain current and output conductance as a function of the drain voltage for A-SC $L_S = 2$ µm structures varying L_D, with $W_S = W_D = 1$ µm, extracted at $V_{GT} = 200$ mV.

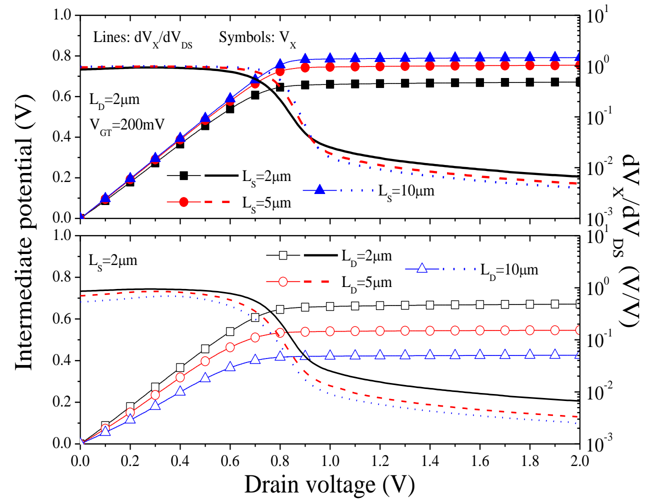

Fig. 19 Simulated intermediate potential and dV_X/dV_{DS} as a function of the drain voltage for A-SC $L_D = 2$ µm structures varying L_S (A) and for A-SC $L_S = 2$ µm changing L_D, with $W_S = W_D = 1$ µm, extracted at $V_{GT} = 200$ mV.

Once the analysis of the analog performance concerning to the influence of W_S, W_D, L_S and L_D has been completed, we have simulated some A-SC structures to achieve the best A_V. Table I presents A_V extracted at $V_{DS} = 1.5$ V and $V_{GT} = 200$ mV as well as the aspect ratio of each transistor.

According to Table I, there is an increase in the intrinsic voltage gain when L_S and/or L_D are incremented, mainly for the L_S rise. Comparing the A-SC $L_S = L_D = 2$ µm; $W_S = W_D = 1$ µm and A-SC $L_S = L_D = 10$ µm; $W_S = W_D = 1$ µm structures, the intrinsic voltage gain increases 30 dB for the longer A-SC configuration, which corroborates with the experimental results obtained in [16], where an increase of the intrinsic voltage gain is obtained when L_S and L_D are incremented.

The analog performance is even better when W_D increases, maintaining W_S lower, being observed an increment of 38 dB by comparing with the shorter and narrower A-SC structure. Concerning to the aspect ratio influence, best A_V is obtained as lower W_S/L_S when considered fixed W_D/L_D.

Table I. Intrinsic voltage gain and aspect ratios for different A-SC structures extracted at V_{DS} = 1.5 V and V_{GT} = 200 mV.

<table>
<tr><th colspan="6">A-SC structures</th><th rowspan="2">A_V (dB)</th></tr>
<tr><th>L_S (µm)</th><th>L_D (µm)</th><th>W_S (µm)</th><th>W_D (µm)</th><th>W_S/L_S</th><th>W_D/L_D</th></tr>
<tr><td rowspan="3">2</td><td>2</td><td rowspan="7">1</td><td rowspan="6">1</td><td>0.5</td><td>0.5</td><td>76.6</td></tr>
<tr><td>5</td><td>0.5</td><td>0.2</td><td>81.6</td></tr>
<tr><td>10</td><td>0.5</td><td>0.1</td><td>81.9</td></tr>
<tr><td>5</td><td rowspan="2">2</td><td>0.2</td><td>0.5</td><td>89.6</td></tr>
<tr><td rowspan="4">10</td><td>0.1</td><td>0.5</td><td>97.1</td></tr>
<tr><td rowspan="3">10</td><td>0.1</td><td>0.1</td><td>106.0</td></tr>
<tr><td rowspan="2">10</td><td>0.1</td><td>1</td><td>114.4</td></tr>
<tr><td>10</td><td>1</td><td>1</td><td>106.0</td></tr>
</table>

IV. Conclusions

This paper has evaluated the influence of geometrical parameters of the M_S and M_D transistors on the analog performance of the Asymmetric Self-Cascode structures. It has been endorsed that the transistor near the source controls the A-SC structure in all gate voltages. However, for higher V_{GS}, the transistor near the drain begins to impact on the drain current flow. It has been shown that depending on the channel widths and lengths of the M_S and M_D transistors, there is a change in the intermediate potential. The way it varies with the gate and drain voltages strongly affects the transconductance and output conductance. The increase of W_S has incremented g_m and g_D, but reducing A_V and V_{EA}, whereas the increment of W_D has slightly increased g_m, but has reduced g_D, incrementing A_V and V_{EA}. In the case of the increase of L_S and L_D, a reduction of g_m and g_D have been seen, raising A_V and V_{EA}. This way, to obtain the highest intrinsic voltage gain, one can use either longer and narrower M_S, the negative characteristic is the reduction of g_m, degrading the unit-gain frequency, or longer and wider M_D, keeping g_m at same level for low V_{GS}, however the drawback is the larger drain capacitance.

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