# DC-40 GHz SPDTs in 22 nm FD-SOI and Back-Gate Impact Study

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***Abstract*—In this paper, ultra-wideband SPDTs fabricated in the 22 nm FD-SOI process from GLOBALFOUNDRIES are presented. Three SPDT modules were implemented, each using a different type of millimeter-wave NFET, namely a conventional-well regular-$V_t$ (RVT) device, a flipped-well super-low-$V_t$ (SLVT) device and a specially treated device without back-gate well contact for decreased substrate parasitics (BFMOAT device). It is shown that using the back-gate achieves lower losses, higher isolation and better linearity for the RVT and SLVT based switches, while the reduced parasitic BFMOAT switch shows better performance at the high-end of the mm-wave spectrum.**

***Keywords*—SPDT, switch, ultra-wideband, millimeter-wave IC, 5G front-end, FD SOI, UTBB, back-gate bias, linearity, IIP3.**

## I. INTRODUCTION

In the existing generations of mobile communication (2G/3G/4G), front-end modules (FEMs) are for the most part implemented using several separate technology processes.

With the upcoming 5G network standard targeting mm-wave frequencies (and in particular 28 GHz and 39 GHz in the Ka band), a process is required to support the implementation of full FEMs (LNAs, PAs and Switches) on a single die to avoid high interface losses. Up until recently, most Ka band SPDT switch products were fabricated in GaAs or GaN technology. Such III-V compound semiconductor technologies enable ultra-fast high-electron mobility transistors (HEMTs) that have excellent performance for microwave and high-power applications. However, they are of high cost compared to silicon-based technologies for high volume production (such as required by the consumer device market). Furthermore, silicon-based technologies are attractive for high integration with analog and digital circuitry.

Over the past decade CMOS devices have become an RF technology of choice. In particular, partially-depleted (PD) silicon-on-insulator (SOI) technology has been dominating the RF switch market since around 2010 [1], and nowadays, thanks to the continuous gate length downscaling, the most advanced SOI nodes now boast speed metrics that are entirely sufficient for complete RF and mm-wave FEM applications, with $f_t$ and $f_{max}$ in the range of 300 to 400 GHz [1].

SOI transistors are isolated from the silicon bulk by a buried oxide (BOX) layer, which lends these devices characteristics well suited to FEM applications, such as reduced parasitics, improved channel control and reduced short-channel effects, smaller and more linear source and drain capacitances and lower leakage current [1].

Fully-depleted (FD) SOI with ultra-thin-body and BOX (UTBB) is the most advanced flavour of SOI today. This versatile technology offers low noise LNAs and good PAs [2] along with low loss switches towards full monolithic integration of mm-wave FEMs.

The unique architecture of UTBB-FD-SOI devices incorporates a back-gate beneath the BOX, that can be biased to further boost performance and can also be used as a tuning knob to compensate the devices against aging and variability.

In this paper, we present the design and results of ultra-wideband SPDT switches (targeting the Ka-band) fabricated using GLOBALFOUNDRIES' 22 nm UTBB-FD-SOI technology (22FDX®). Three types of SPDTs are designed, based on the three key mm-wave FET devices offered by the foundry library. The devices are compared in terms of SPDT figures of merit (FoMs), with a focus on the impact of back-gate bias.

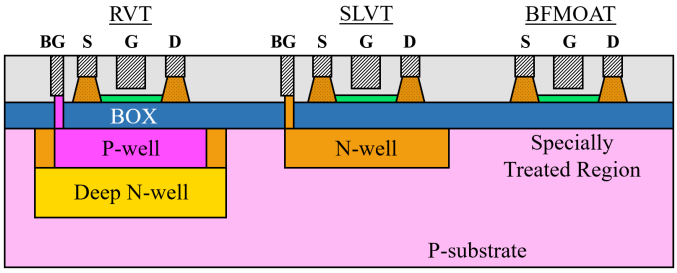


Fig. 1. Simple representation of the three different flavours of UTBB-FD-SOI devices considered for the implementation of the mm-wave SPDT switches. The source (S), drain (D), gate (G) and back-gate (BG) terminals are depicted.

We show that conventional-well devices with regular-$V_t$ (RVT) and flipped-well devices with super-low-$V_t$ (SLVT) make for the best switches below 20 GHz, thanks to the back-gate bias improving device channel resistance and reducing insertion-loss. We also show how the back-gate bias can be used to boost large-signal FoMs, such as P1dB and IIP3.

The third device, named BFMOAT, lacks the back-gate contact, as the substrate region directly beneath the BOX is specially treated in order to reduce substrate parasitics [3]. Thanks to this, we confirm that these devices are the best choice for switch applications above 40 GHz.

## II. DESIGN

The SPDT switches were designed based on a series-shunt topology, as shown in Fig. 2, for wideband functionality. The designs were made to achieve the lowest possible insertion-loss (IL) while maintaining an isolation (ISO) of 30 dB at 28 GHz. A stack of three transistors was used in each branch targeting 20 dBm of input power 1-dB compression point.

NFET devices with 20 nm nominal gate length were used to implement the SPDTs. Three SPDTs were fabricated based on the three types of transistors: RVT, SLVT and BFMOAT.

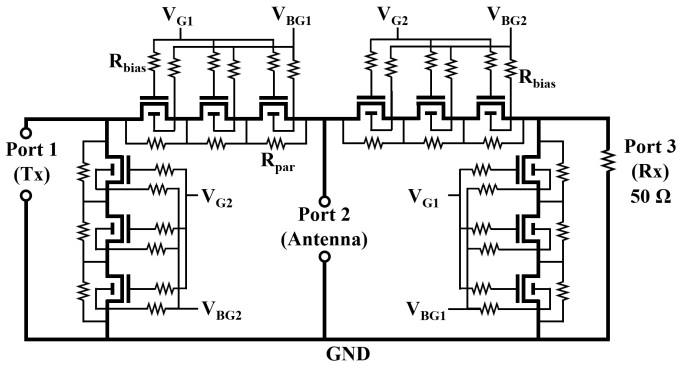


Fig. 2. Schematic of the designed SPDT switches.

The sizes chosen to achieve these specs are $W_{series}$ of 72 µm and $W_{shunt}$ of 29.4 µm. The bias resistors at the gate and back-gate terminals are 9.20 kΩ, and the resistors in parallel with the FETs are 2.45 kΩ.

The final layout of the fabricated devices is depicted in Fig. 3. The third port of the SPDT is emulated using a wideband 50 Ω resistor on-chip. The switch state is controlled by means of four DC probe pads (not shown), corresponding to the DC bias points depicted in Fig. 2, i.e. $V_{g1}$, $V_{bg1}$, $V_{g2}$ and $V_{bg2}$.

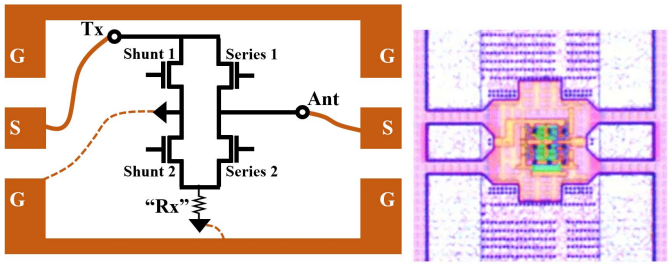


Fig. 3. Layout and photograph of the fabricated SPDT switches (without matching inductors).

SPDTs with and without matching circuits are considered in this work. To reduce return loss, inductors of 150 pH can be added as series elements at all three ports. With improved matching comes a decrease in the overall IL in the DC-40 GHz band of interest. However, these inductors come at the price of significantly increasing the overall area of the SPDTs.

## III. Measurement Results

The SPDTs were fully characterized under both small- and large-signal conditions using an on-wafer set-up employing a pair of GSG Infinity probes from Cascade Microtech and a 67 GHz PNA-X vector network analyzer.

In this section, the impact of matching, of applied back-gate bias and of transistor choice will be discussed and analyzed with respect to the measured switch FoMs.

Throughout this paper, when in the switches are in the on-state, the gate voltages are set to $V_{g1}$ = 0.9 V and $V_{g2}$ = -0.9 V. In the off-state, they are set to $V_{g1}$ = -0.9 V and $V_{g2}$ = 0.9 V.

### A. Impact of Matching

Fig. 4 plots the measured S-parameter results of the SPDTs under 0 V of back-gate bias, and highlights the benefits of improving the matching. It is shown that, at 28GHz, the IL is improved by 0.5 dB for the BFMOAT SPDT and by 0.7 dB for the SLVT and RVT SPDTs by including the series matching inductors, as the return loss at 28 GHz is improved from around -10 dB to less than -20 dB for all SPDTs.

There is little effect of the matching inductors on the isolation. At 28 GHz, the ISO is around 29.1 dB for the RVT and BFMOAT SPDTs, and 31.1 dB for the SLVT SPDT.

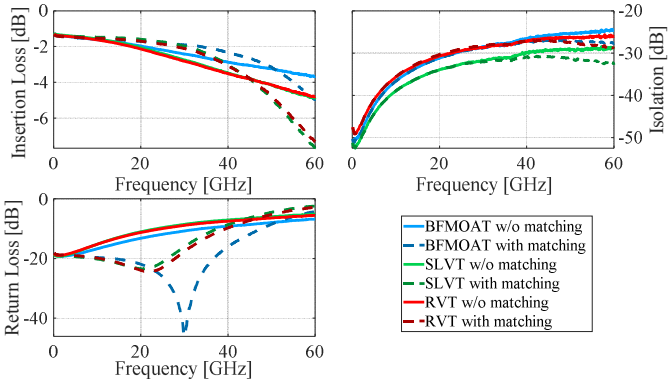


Fig. 4. Measured Insertion Loss and Return Loss in On-State, and measured Isolation in Off-state for the three SPDT switches. All back-gate bias are 0 V for the RVT and SLVT switches.

Large-signal measurements were also performed on-wafer at 900 MHz and up to 25 dB of input power in order to characterize the SPDT power handling, i.e. the 1-dB compression point (P1dB), and its linearity, i.e. the third order intercept point (IIP3). A plot of the power-sweep results is given in Fig. 5 for the case of the BFMOAT SPDT, which presents a P1dB of 19.6 dBm and an IIP3 of 33.1 dBm. There is almost no impact of the matching circuits on these FoMs.

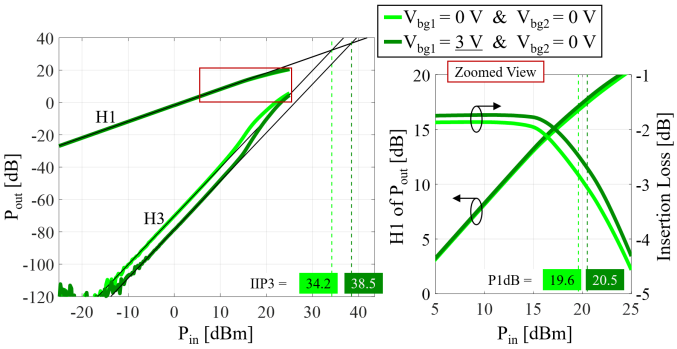


Fig. 5. Large Signal FoM measurement at 900 MHz of the SLVT SPDT at two back-gate bias conditions.

When the signal is large enough the overdrive voltage $V_{OV}$ in the conducting branches becomes very low at each positive cycle of the RF / mm-wave signal. This has the effect of severely modulating the output conductance $g_d$, which translates directly into a degradation of $R_{on}$ at low $V_{OV}$ and to an increase in IL. In the isolating branches, large amplitude negative cycles threaten to drive the transistors into a state of conduction, thereby degrading their isolation, which also causes IL increase. These are the origins of the 1-dB compression point under large amplitude excitations, and justifies the stacking design of 3 FETs in each branch in order to attain a P1dB point close to 20 dBm.

### B. *Impact of Back-Gate Bias*

Both the RVT and SLVT devices include a back-gate terminal beneath the BOX (see Fig. 1) that can serve to tune the transistor threshold voltage ($V_t$) by applying a DC bias, and this feature can serve to improve the FoMs of the RVT and SLVT switches.

#### 1) *Impact of Back-Gate on the On-State Insertion Loss*

In the on-state, sweeping the back-gate of the conducting branches, i.e. $V_{bg1}$, reveals an improvement of 0.2 dB in the insertion loss at 28 GHz, mainly because higher $V_{bg1}$ results in a lower $R_{on}$ if the conducting series branch. This is highlighted in the measurement results of Fig. 6 and Fig. 7 (a).

Sweeping $V_{bg2}$ in the on-state has little impact on the IL, because the $C_{off}$ elements have almost no dependency on $V_{bg}$.

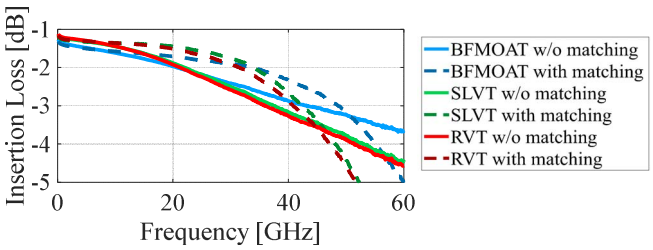


Fig. 6. Measured Insertion Loss for the three SPDT switches. The applied back-gate bias is $V_{bg1}$ = 3 V and $V_{bg2}$ = 0 V for the RVT and SLVT switches. Please observe an approximate 0.2 dB shift in the IL curves of RVT and SLVT as compared to the curves given in Fig. 4.

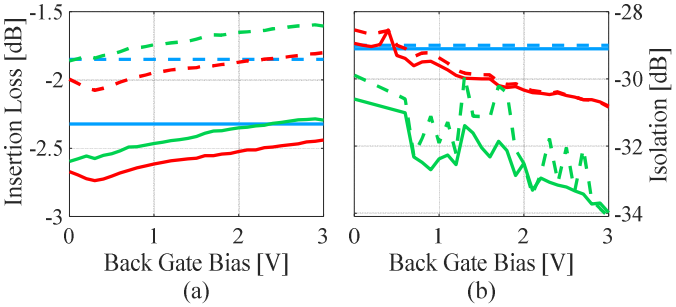


Fig. 7. (a) IL vs. $V_{bg1}$ at 28 GHz ($V_{bg2}$ = 0 V). (b) ISO vs. $V_{bg2}$ at 28 GHz ($V_{bg1}$ = 0 V).

Table 1. Summary of the Impact of Input Matching and Back-Gate Bias on SPDT Insertion Loss / Isolation, given in dB, at 28 GHz.

| | **Without Matching** | | **With Matching** | |
|---|---|---|---|---|
| **Back Gate ($V_{bg1}$ = $V_{bg2}$)** | **0 V** | **3 V** | **0 V** | **3 V** |
| RVT | 2.67 / 29.0 | 2.44 / 30.8 | 1.99 / 28.7 | 1.80 / 30.8 |
| SLVT | 2.60 / 30.8 | 2.29 / 33.5 | 1.85 / 31.2 | 1.66 / 33.3 |
| BFMOAT | 2.32 / 29.1 | n/a | 1.85 / 29.0 | n/a |

#### 2) *Impact of Back-Gate on the Off-State Isolation*

In the off-state, sweeping the back-gate potential $V_{bg1}$ reveals little impact on the isolation. Once again, this is because the $C_{off}$ elements have almost no dependency on $V_{bg}$.

Sweeping $V_{bg2}$ reveals a slight improvement in the isolation for RVT and SLVT SPDTs, of the order of 2 dB at 28 GHz, mainly because a higher $V_{bg2}$ results in a lower $R_{on}$ of the conducting shunt branch. This is highlighted in the measurement results of Fig. 7 (b).

Table 1. recaps the small-signal performance of the SPDTs, and highlights the impact of matching and back-gate biasing.

#### 3) *Impact of Back-Gate on P1dB and IIP3*

As discussed above, the compression point and non-linearities associated to the active devices originate mainly from the large-amplitude signals doing two things:

- Pulling the conducting FETs (biased to $V_g$ = 0.9 V) out of a regime of strong positive $V_{OV}$ and reducing the overall $R_{on}$ in these branches.
- Pulling the isolating FETs (biased to $V_g$ = -0.9 V) out of a regime of strong negative $V_{OV}$, thereby reducing $C_{off}$ and even contributing to an $R_{off}$ term in these branches.

Therefore, the P1dB and IIP3 metrics of the RVT and SLVT switches can be boosted by: 1) applying forward voltages to the back-gates of the conducting branches to reduce transistor $V_t$ which increases the good operation range of $V_{OV}$ in the conducting FETs, and 2) by applying reverse biases to the back-gates (only applicable to RVTs) of the isolating branches to increase transistor $V_t$ which increases the good operation range of $V_{OV}$ in the isolating FETs.

Table 2 recaps the large-signal performance of the SPDTs, and highlights the impact of the back-gate biasing. There is no trade-off with IL, as the optimum back-gate bias point for reduced IL coincides with the optimum back-gate bias point for the highest P1dB and IIP3.

Table 2. Summary of the Impact of Back-Gate Bias on the SPDT Switches' Large-Signal FoMs: P1dB / IIP3 given in dBm.

| **Back Gate** | **$V_{bg1}$ = 0 V, $V_{bg2}$ = 0 V** | **$V_{bg1}$ = 3 V, $V_{bg2}$ = 0 V** | **$V_{bg1}$ = 3 V, $V_{bg2}$ = -3 V** |
|---|---|---|---|
| RVT | 19.1 / 32.5 | 20.2 / 36.3 | 20.4 / 37.2 |
| SLVT | 19.6 / 34.2 | 20.5 / 38.5 | n/a |
| BFMOAT | 19.6 / 33.1 | n/a | n/a |

### C. *Impact of Device*

So far, all devices have been compared at 28 GHz under both small- and large-signal analysis. At 28 GHz, the SLVT device outperforms both the RVT and BFMOAT in all small- and large-signal FoMs. This is because the SLVT can attain the lowest threshold voltage, which has the simultaneous impact of lowering IL and increasing P1dB and IIP3.

However, the IL curves from Figs. 4 and 6 show that the BFMOAT device has slower IL roll off versus frequency, thanks to its lower parasitics. This is supported by the conclusions from [3], and marks the BFMOAT device as the preferred choice over SLVT and RVT for mm-wave switches in the 40-100 GHz range. In the lower frequency range RVT and SLVT switches outperform the BFMOAT ones thanks to an applied back gate bias, that enables them to achieve approximately 0.2 dB advantage in IL from DC to 20 GHz. The IL of SLVT with back-gate biasing is lower than that of

Table 3. State-of-the-art mm-wave SPDT modules in SOI technology.

| | | [4] 2011 | [5] 2014 | | [6] 2017 | [7] 2017 | [8] 2018 | [9] 2019 | This Work 2020 | |
|---|---|---|---|---|---|---|---|---|---|---|
| Technology | | 45-RFSOI | 180nm SOI | | 130nm SOI | 40nm SOI | 45-RFSOI | 22FDX | **22FDX** | |
| $R_{on}C_{off}$ | [fs] | / | / | | / | / | 90 | 98 | **103** | |
| Substrate | | 13.5 Ωcm | > 1 kΩcm | | > 1 kΩcm | / | > 1 kΩcm | 10 Ωcm | **10 Ωcm** | |
| Switch Type | | SPDT | SPDT | | SPDT | SPDT | SPDT | SPDT | **SPDT** | |
| Topology | | Series-Shunt with matching | Series-Shunt with matching | | Series-Shunt with matching | Series-Shunt | Series-Shunt | | **Series-Shunt with matching** | **Series-Shunt** |
| Band | [GHz] | DC-60 | DC-40 | | DC-50 | DC-50 | DC-50 | 26.5-29.5 | **DC-40** | |
| IL(28 GHz) | [dB] | 1.4 | 1.1 | 2.1 | 1.0 | 1.4 | 0.7 | 1.6 | **1.66** | **2.29** |
| ISO(28 GHz) | [dB] | 30 | 16.5 | 17.5 | 32 | 33 | 24 | 22 | **33.4** | |
| P1dB | [dBm] | 7.1 | 11 | 15 | 14 | 21 | 29.5 | / | **20.5** | |
| IIP3 | [dBm] | 18.2 | 25.8 | / | 27 | / | 46 | / | **38.5** | |
| Switching time | [ns] | 0.35 | / | / | 10 | / | / | / | **0.25** | |
| Size | [$10^{-3}$ mm²] | 39 | 25 | / | 40 | / | 4 | 150 | **34** | **1.8** |

BFMOAT up to around 34 GHz for our designs with matching, and up to around 26 GHz for our unmatched design.

The applied bias that improves IL also simultaneously improves P1dB and IIP3, by 1 dBm and 4 dBm respectively.

## IV. Conclusion

In this paper, SPDT switches were implemented in 22 nm FD-SOI technology for Ka band operation. With matching inductors, the small footprint SPDT presents 1.66 dB of insertion loss and 33.3 dB of isolation at 28 GHz. The large-signal P1dB and IIP3 FoMs are 20.5 dBm and 38.5 dBm respectively. In terms of response time, simulation data reveals a 250 ps switching time (without ESD protection), that is very low thanks to small gate lengths employed. Table 3 benchmarks our results against state-of-the-art mm-wave SPDT modules in SOI, and shows our designs to be competitive. It also highlights that by forgoing the inductor matching circuits, a drastic reduction in SPDT area is achievable at the price of a degraded IL (2.29 dB at 28 GHz).

Through small- and large-signal on-wafer measurements, we demonstrated boosts in SPDT FoMs by careful control of back-gate biasing, improving IL by 0.2 dB and ISO by 2.0 dB at 28 GHz, along with P1dB by 1 dBm and IIP3 by 4 dBm.

Finally, by comparing different flavors of FD-SOI FETs, we can advise that the back-gate functionality be sacrificed when designing switches above 40 GHz, through the use of the BFMOAT device option that reduces substrate parasitics that have a strong impact on the IL at high frequencies.


## Acknowledgment

The authors would like to thank GlobalFoundries for chip fabrication and research support.


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