Sub-6 GHz RF SPDT Switches Designed in an Advanced 28 nm Fully-Depleted Silicon-on-Insulator Technology with a High Resistivity Substrate

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***Abstract* — In this paper two RF switches named as 3-stack and 12-stack are studied. They are designed to have the same overall R_{ON} and built using a 28 nm FD-SOI technology atop of different substrate resistivities. A new *advanced passivation technique* is also used in order to boost the switches' performance. The 3-stack switch atop of standard Process of Reference (POR) substrate (~15 Ωcm) shows an insertion loss 1.2 dB higher than the same switch atop of high-resistivity (>1 k Ωcm) with *advanced passivation technique.* Moreover, the 12-stack switch with *advanced passivation technique* demonstrates 2.5 dB improvement in the insertion loss compared to the same one built on a standard substrate while the isolation remains lower than 20 dB.**

***Keywords* — RF switches, fully depleted silicon-on-insulator (FD-SOI), high power switches, advanced passivation technique, substrate effect, parasitic surface conduction (PSC), stacked RF switches, high resistivity (HR) substrate.**

I. INTRODUCTION

The popularity of today's versatile mobile phones has led to a need for very small RF front-end modules (FEMs) placed between the antenna and the multi-mode multi-band RF transceiver system-on-chip (SoC) [1]. Single Pole Double Throw (SPDT) switches are commonly used in order to connect the antenna to the power amplifier (PA) in a TX mode, or to the low-noise amplifier (LNA) in a RX mode. Since the switches are used for mobile communications, they need to provide low insertion loss, high isolation between the transmit and receive path, high linearity, and high-power handling capability [2]. In the past, advanced RF switch design typically relied on III–V semiconductor-based processes or silicon-on-sapphire (SOS) technology [3]. However, III–V semiconductor-based materials like Gallium Arsenide (GaAs) and Indium Phosphide (InP), as well as Silicon-on-Sapphire (SOS) technology, have drawbacks such as costly substrates and limited ability to work well with digital circuits [4]. The silicon-on-insulator (SOI) technology has shown its capability in terms of integration and low cost. However, high insertion loss and low linearity levels are observed when using standard substrates having a resistivity of around 10-15 Ωcm. This is because the RF signal unavoidably couples to the substrate in unshielded passive devices such as inductors and specific transmission lines like coplanar waveguides (CPW). High-resistivity (HR) substrates (>1 k Ωcm) demonstrate better RF performance compared to standard resistivity substrates (10-15 Ωcm) by suffering from lower substrate losses. Using HR substrate for RF switches has previously shown its in [5] in the case of a partially-depleted (PD) 0.25 µm SOI process. However, due to the positive oxide charges in the buried oxide (BOX), electrons are attracted near the BOX-silicon interface in the substrate creating a conductive layer called *parasitic surface conduction* (PSC). This makes the substrate non-uniform by having a thin low resistivity layer at the interface and high resistivity region in the bulk. This not only creates unexpected additional losses but also increases substrate-induced non-linearities. In order to build better RF switches, the Trap-Rich (TR) substrate has been developed by introducing a blanket (ie, covering the entire wafer surface) thin polysilicon (between 300 nm and 2 µm) layer between the BOX and the HR substrate. This solution overcomes the PSC effect by capturing the free electrons coming from the silicon bulk leading to Fermi level pinning near the silicon mid-gap [6],[7]. The TR substrate has demonstrated its excellent RF performance not only for passive devices (CPW lines, inductors, filters, etc.) but also for different front-end module parts such as switches [8], PAs [9] and LNAs [10]. The TR substrate made the integration of the whole T/R front end in the same chip possible using the PD-SOI technology in [11]. Nowadays, the TR interface passivation is uniquely compatible with PD-SOI technology and is widely regarded as the state-of-the-art benchmark silicon-based RF substrate solution. However, the blanket trap rich solution presents implementation challenges when moving to the fully-depleted (FD)-SOI, in which below-BOX functionalities are required for proper device operation (back-gate contacts, isolation wells, substrate diodes, etc.). In particular, compatibility issues are foreseen when implementing these in a defect-rich polysilicon layer [12]. For instance, it is expected that the reverse current of a biased back-gate formed in such a polysilicon layer will be orders of magnitude higher than in a crystalline Si material. This motivates the interest for the development of a local passivation technology that can be used with advanced FD-SOI technologies based on HR substrates. We have developed such technique and refer to it in this paper as *advanced passivation technique*. As we show here, our *advanced passivation* technique is successful and leads to a significant reduction of insertion losses RF switches. Our study is based on a DC-6 GHz

SPDT 12-stack switch intended for high power applications and a similar 3-stack switch used for comparison. Both switches are built on several substrates of various nominal resistivities.

II. RF Circuit Design

In this paper two switches were designed: one 3-stack and one 12-stack having the same topology and identical transistor type. The mainstream series-shunt topology is used because of its simplicity and can cover low frequencies with less chip area [13]. The transistors employed are called GO2 (EGV-LVT-N-FET) and implement a thick gate oxide recommended by the foundry for RF switches. Gate lengths of 100 nm and finger width of 2.5 µm are chosen. Each transistor can either be biased in an ON state using front- and back-gate voltages of V_g=1.8 V and V_{bg}= 3 V, or to an OFF state using V_g=-1.8 V and V_{bg}=0 V. The gate and back-gate nodes of all transistors are biased through 10 kΩ resistors. Moreover, a 10 kΩ drain source resistor is connected to each FET (not shown) in both the series and shunt branches, this is done in order to ensure that the voltage across each FET in OFF state is evenly distributed [14].

A. 3- and 12- Stack Switches

Both switches are designed to have the same $R_{on}\times C_{off}$ metric. The 12-stack was designed from the 3-stack as depicted in Fig. 1.

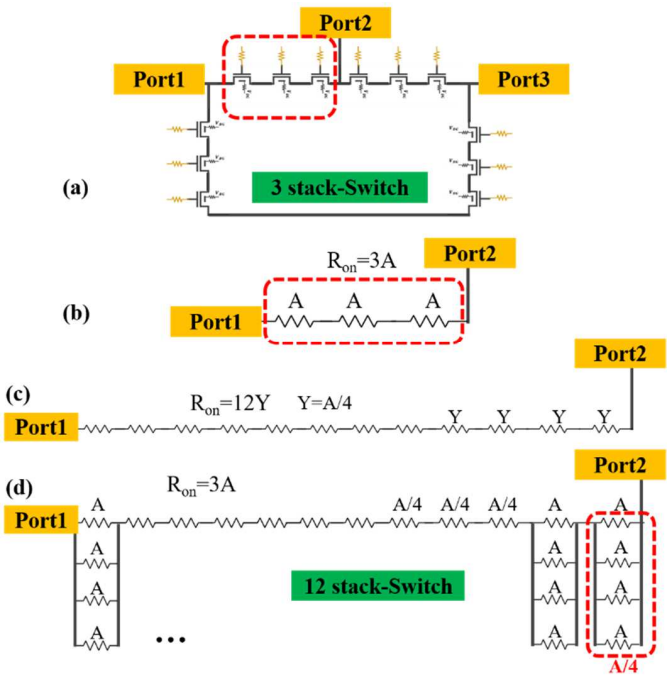

Fig. 1: Description of the 12-stack switch series branch design starting from a 3-stack switch.

In Fig.1a, the 3-stack switch is a conventional SPDT having the PORT2 serves as pole while PORTS 1 and 3 are the throws. The switch has 3 series FETs and 3 shunt FETs. Considering the stacked series transistors in the ON state, depicted in a red circle of Fig 1b., the total branch resistance (R_{on}) is 3A, where A is the ON-series resistance of a single FET. In order to build the 12-stack series branch with the same total R_{on} (and hence similar insertion losses as the 3-stack switch if we neglect the losses in the metallic interconnections), its FETs are designed to have an ON-series resistance of A/4 (see Fig.1c). This is achieved by using 4 parallel FETs having the same geometry as those used in the 3-stack switch (see Figure.1d).

The dimensions of each FET for the two switches are listed in Table 1.

Due to these design choices, the 3-stack and 12-stack switches are expected to yield similar small-signal performances (S-parameters) if substrate parasitics are negligible. In terms of large-signal performance, the 3-stack design targets above 30 dBm of power handling, while the 12-stack targets close to 40 dBm.

Table 1. Transistors Dimensions in the Branch of the Two RF Switches

	3-stack	12-stack
N	3	12
W_{ser} [µm]	562.5	2250
W_{sh} [µm]	62.5	250

III. RF Measurements

Small-signal S-parameter measurements were performed using an Agilent 4-port Performance Network Analyzer (PNA)-X, three ground signal ground (GSG) infinity probes with 100 µm pitch and 4-point DC probe as depicted in Fig. 2

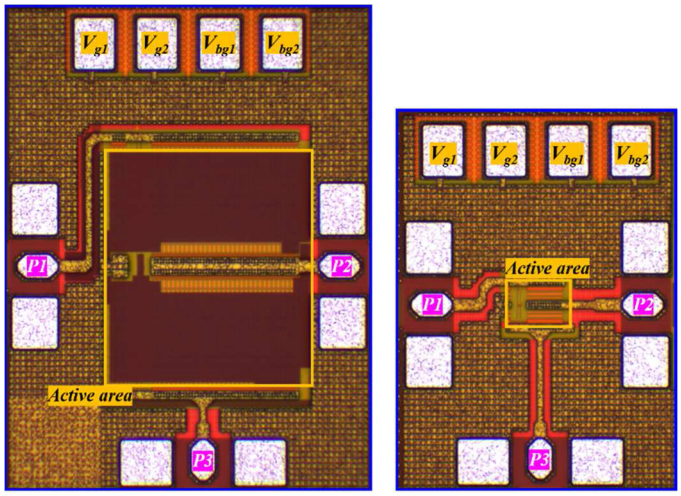

Fig. 2. Photograph of the designed RF switches (a): 12- and (b): 3 -stack. The active area of the 12-stack is 0.152 mm², for the 3-stack is around: 0.005 mm².

The switches were built on three different substrate types termed as: *standard substrate* (bulk resistivity at 10-15 Ωcm), *high resistivity* (HR) *substrate* (bulk resistivity above 1 kΩcm) without passivation and HR substrate with *advanced passivation*. Each circuit on every substrate was measured three times to reduce measurement errors and remove uncertainties. The impact of the substrate on the switch performance is described in the next subsections.

A. Advanced Passivation Technique Placement

The advanced passivation technique used in this paper is similar to the implanted PN junctions described in [15] by the fact that it provides interface passivation the substrate *locally*.

Fig. 3 shows a top left zoom of the active area from the 12-stack switch of Fig. 2a. It presents the position of the first 6 series and shunt transistors in pink color. Those transistors are surrounded by the advanced passivation in blue color. The remaining orange area is not passivated, and therefore has an underlying layer of PSC. The minimum vertical distance between the series transistors and the PSC is around 5 µm. Meanwhile, the PSC is suppressed between the vertical shunt transistors. The minimum lateral distance between the transistors and the PSC is round 3.7 µm. The ideal way to implement this advanced technique passivation is to recoat all the PSC by the advanced passivation technique. However, the passivation cannot be employed below the transistors and the technology's design rules limit its implementation over the entire area continuously. For these reasons, the passivation layout depicted in Fig. 3 was implemented.

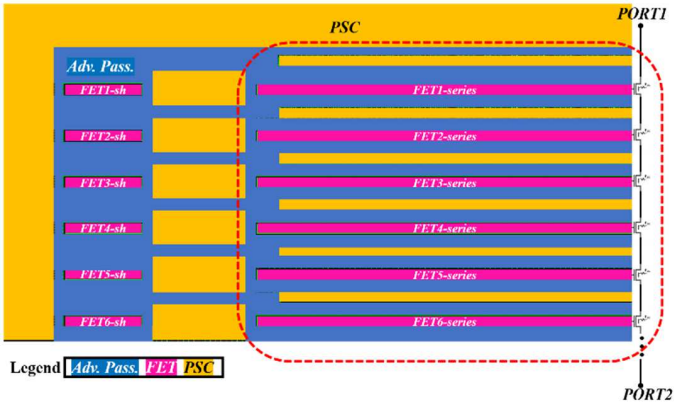

Fig. 3. Implementation of the advanced passivation technique in the 12-stack switch layout. The PSC is in orange, the transistors active area is in pink and the advanced passivation is in blue color. The dashed red line represents the series branch shown in Fig. 1d.

B. Substrate Effect on the Designed 3-Stack Switch

Fig. 4 shows the S_{21} (left) and S_{13}/S_{23} (right) for the 3-satck switch designed on different substrates.

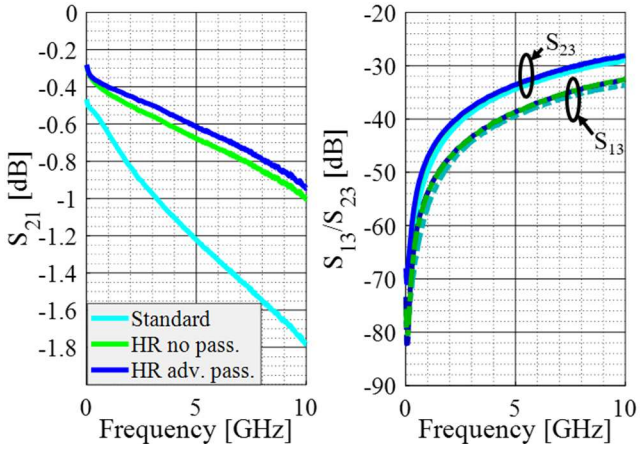

Fig. 4. Measured S-parameters for the 3-stack switch built on top on standard, high resistivity substrate without passivation and high resistivity with advanced passivation.

The 3-stack switch on standard substrate demonstrates 1.22 dB insertion loss at 5 GHz. The same circuit atop of HR substrate without passivation shows 0.68 dB insertion loss at 5 GHz. However, even if the HR substrate reduces substrate losses, the PSC remains around the transistors. This is why using the HR substrate with the advanced passivation technique further reducing losses by 0.07 dB at 5 GHz, while maintaining high isolation between all the ports (i.e., below 20 dB).

C. Substrate Effect on the Designed 12-Stack Switch

Fig. 5 shows the S_{21} (left) and S_{13}/S_{23} (right) for the 12-stack switch designed on the previously described substrates.

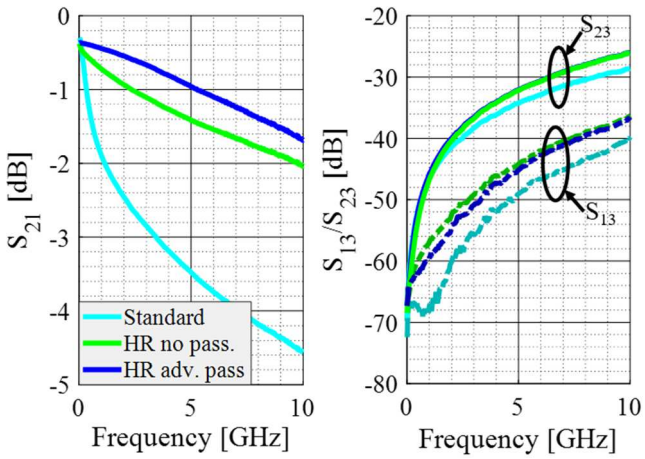

Fig. 5. Measured S-parameters for the 12-stack switch manufactured on top of standard, high resistivity substrate without passivation and high resistivity with advanced passivation.

The 12-stack switch on the standard resistivity substrate shows around 3.5 dB insertion loss at 5 GHz. Changing from standard to HR without passivation improves the insertion loss to 1.36 dB at 5 GHz. Using the advanced passivation technique, the 12-stack switch insertion loss are 0.91 dB at 5 GHz. The isolation between the non-connected ports remains lower than 20 dB for all the described substrates.

The substrate effect is more pronounced in the 12-stack compared to the 3-stack, and this effect is caused by the much larger surface occupied by the FETs of the 12-stack switch. Due to its higher power handling, it should be noted that the 12-stack switch is a more appropriate circuit for mobile communications.

D. 12- and 3-Stack Comparison

Fig. 6 shows the insertion loss comparison of the 3- and 12-stack switches on each substrate. It is shown that the gap between the two switches gradually decreases as the interface is well passivated going from a gap of 2.29 dB for standard substrate, to 0.69 dB for HR without passivation and then finally to a gap of only 0.3 dB for the HR with advanced passivation. Theoretically, the 3-stack and 12-stack switches are expected to have very similar performance if there are no substrate parasitics or associated losses at all. This is achieved at 2 GHz but not at 5 GHz, where a (modest) gap of 0.3 dB is present.

For any substrate, the FETs in 12-stack switch will always be expected to suffer from higher substrate-parasitics than those in the 3-stack design, since the area occupied by the FETs in the

12-stack is more than 30 times larger than that occupied by the FETs in the 3-stack.

The gap in the S-parameter results between the two designs could theoretically be reduced to zero if substrate parasitics could be totally removed. The fact that the substrate-parasitics' influence reduces down to 0.3 dB at 5 GHz when comparing the two designs highlights that a high effective resistivity is well achieved for the effective substrate material around the FETs of the fabricated switches.

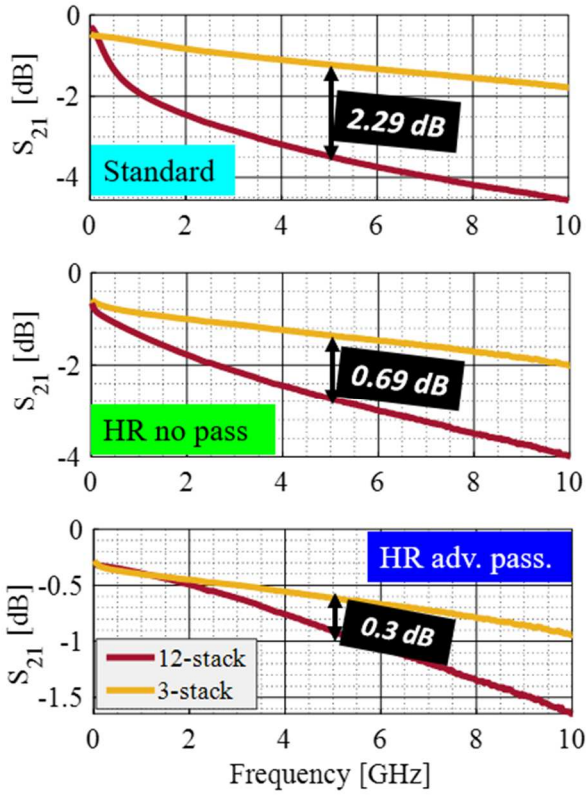

Fig. 6. Comparison of the S21 between 3- and 12-stack switches on (a): standard substrate, (b): HR substrate without passivation and (c): HR with advanced passivation.

IV. Conclusion

In this paper, a local, advanced passivation technique is proposed for a 28 nm FD-SOI technology using high resistivity substrates. It is demonstrated that for high power 12-stack SPDT switches it is possible to gain more then 2 dB insertion loss by changing the substrate from a standard to a high-resistivity substrate. On top of that, this insertion loss can be further improved by around 0.5 dB through the addition of an advanced passivation technique, which locally suppresses parasitic surface conduction effects and further improves substrate isolation. It has been shown that the 12-stack switch is more sensitive to substrate effects due to its considerably larger active area compared to the 3-stack. This highlights the significance of advanced passivation techniques in reducing substrate coupling, particularly for high-area circuits.

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