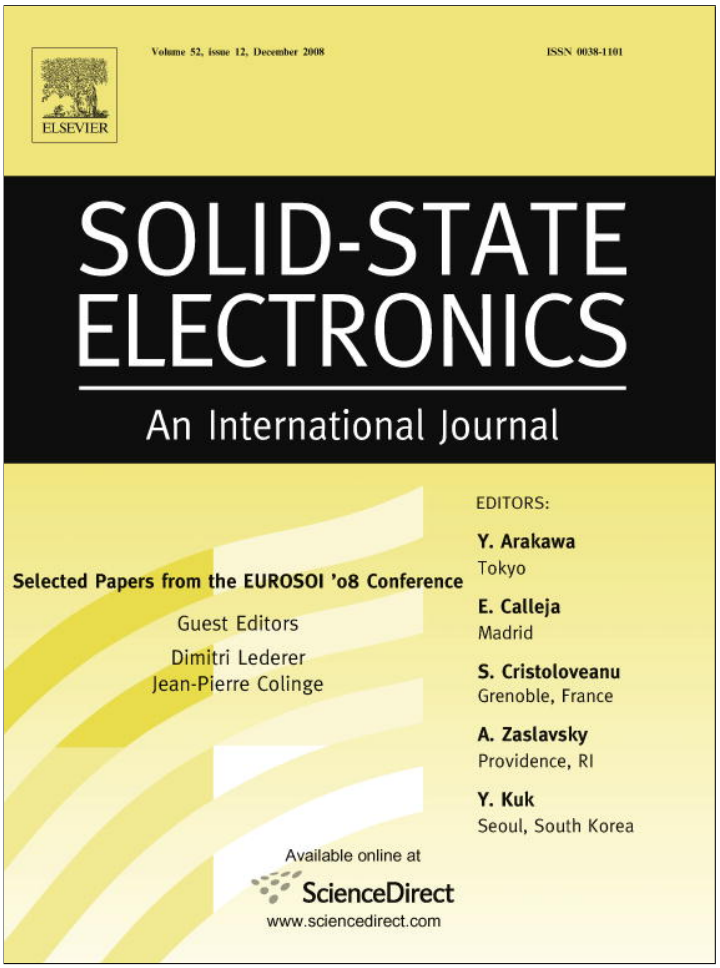

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High-temperature DC and RF behaviors of partially-depleted SOI MOSFET transistors

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ABSTRACT

This work presents the high-temperature DC and RF behaviors of partially-depleted SOI MOSFETs. DC and RF figures of merit are deeply investigated, both analytically and experimentally, to provide a complete study of high-temperature performance and a comparison between floating-body and body-tied transistors. A highly stable RF performance is noticed especially for cutoff frequency and intrinsic elements for temperature as high as 250 °C.

1. Introduction

High temperature is a large value market that has been difficult to serve up till now. In automotive electronics, on-engine and on-transmission applications are projected to require maximum temperatures of up to 200 °C with the wheel-mounted applications going even higher. Further high-temperature application areas include aerospace and environmental monitoring, such as mining and well logging.

Silicon-on-Insulator (SOI) technology is emerging as the most mature solution for high-temperature applications in MOS technology area. Indeed, SOI MOSFETs present lower leakage currents than bulk devices at high temperature, as well as a smaller variation of threshold voltage with temperature [1]. They are also immune to temperature-induced latchup. As a result, SOI circuits can operate at temperatures above 300 °C, while bulk CMOS is usually limited to 150 °C [2,3].

In previous published work [1–5], high-temperature DC behavior has been considered, while RF high temperature behavior has rarely been discussed [6]. This work presents a detailed investigation of DC and RF high temperature behaviors of partially-depleted SOI MOSFETs. Starting from DC and *S*-parameters measurements, important figures of merit for both DC and RF behaviors are investigated in depth and compared for two types of Partially-Depleted (PD) SOI transistors, which are Floating-Body (FB) transistor; where the body is not connected to any terminal and Body-Tied (BT) transistor; where body and source are shorted together by a silicided contact. In addition, parameters extraction of a small-signal equivalent circuit is presented for temperatures ranging from 25 to 250 °C and frequencies ranging from 40 MHz to 40 GHz. Characterized transistors feature 30 gate fingers of 2 μm wide each connected in parallel, on a 130 nm high-resistivity SOI CMOS technology with a gate oxide thickness, film thickness and buried oxide thickness of 2.6, 150 and 400 nm, respectively.

2. High-temperature DC behavior

2.1. Threshold voltage V_{th}

The threshold voltage of an n-channel MOSFET is given by

$$V_{th} \cong \Phi_{MS} + 2\Phi_F - \frac{Q_{ox}}{C_{ox}} - \frac{Q_D}{C_{ox}} \quad (1)$$

where Φ_{MS}, Φ_F, Q_{ox}, Q_D and C_{ox} are the metal–semiconductor work-function difference, the Fermi potential, the charge density in the gate oxide, the depletion charge controlled by the gate and the gate oxide capacitance, respectively. Eq. (1) is valid for PD devices where

$$Q_D = qN_aW_{max} \quad (2)$$

where W_{max} is the maximum depletion width and is given by

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$$W_{max} = \sqrt{\frac{4\epsilon_{si}\Phi_F}{qN_a}} \tag{3}$$

where ϵ_{si} is the permitivity of the silicon, N_a is the doping concentration and q is the charge of electron.

If an N^+-polysilicon is assumed, the value of the work-function difference is given by

$$\Phi_{MS} = -\frac{E_g}{2} - \Phi_F \tag{4}$$

with

$$\Phi_F = \frac{kT}{q}\ln(N_a/n_i) \tag{5}$$

where E_g, T and n_i are the silicon bandgap, the temperature and the silicon intrinsic carrier concentration, respectively.

The temperature dependence of the intrinsic carrier concentration, n_i, is given by [8]

$$n_i = 3.9 \times 10^{16} T^{3/2} e^{-E_g/2kT} \tag{6}$$

The temperature dependence of the threshold voltage can be obtained from (1) and (5). Q_{ox} is assumed to have no temperature dependence over the temperature range under consideration 25–250 °C. The same applies to E_g, which varies by only 0.3% for this temperature range [9]. Therefore, for bulk and thick-film SOI devices [7],

$$\frac{dV_{th}}{dT} = \frac{d\Phi_F}{dT}\left[1 + \frac{q}{C_{ox}}\sqrt{\frac{\epsilon_{si}N_a}{kT\ln(N_a/n_i)}}\right] \tag{7}$$

with

$$\frac{d\Phi_F}{dT} = 8.63 \times 10^{-5}\left[\ln(N_a) - 38.2 - \frac{3}{2}\{1 + \ln(T)\}\right] \tag{8}$$

In the case of thin-film, Fully-Depleted (FD) devices, Q_D has a value which can range between qN_at_{si} and qN_at_{si}/n, with t_{si} the silicon film thickness, which is independent of temperature, and the value of n ranges between 1 and 2, depending on oxide charge and back-gate bias conditions. If n is assumed independent of temperature, therefore Q_D is independent of temperature. And since Q_{ox} and E_g were assumed independent of temperature too, therefore, from (1)

$$\frac{dV_{th}}{dT} = \frac{d\Phi_F}{dT} \tag{9}$$

From (7) to (9), it can be seen that dV_{th}/dT is larger in bulk and thick-film SOI devices than in thin-film SOI devices by a ratio given by the bracket term of (7) which typically ranges from 2 to 3, depending on the gate oxide thickness and the channel doping concentration. In other words, it depends on C_D and C_{ox}, depletion capacitance and oxide capacitance, per unit area, respectively. Typical values of dV_{th}/dT range between −0.7 and −0.8 mV/K in thin-film SOI MOSFET's and between −2.4 and −3 mV/K in bulk and thick-film SOI MOSFET's (with N_a of $\sim 1.6 \times 10^{17}$ cm^{-3}) depending on oxide thickness and temperature range [7].

Fig. 1 shows the degradation of threshold voltage V_{th} with temperature measured for FB and BT PD SOI devices in linear region. Both FB and BT transistors show a dV_{th}/dT of −0.7 mV/K over the temperature range from 25 to 250 °C. Although the film thickness in our case is not very thin (150 nm), the high channel doping ($N_a \sim 10^{18}$ cm^{-3}) results in higher C_D and hence smaller dV_{th}/dT (as depicted from Eq. 7) compared to reported values for thick-film devices, putting it rather near of dV_{th}/dT of thin-film transistors. In a recent publication, using FD (50 and 4.5 nm of film thickness and gate oxide thickness, respectively), low-V_{th} (low-doping) devices, a very small dV_{th}/dT of −0.44 mV/K was achieved [10].

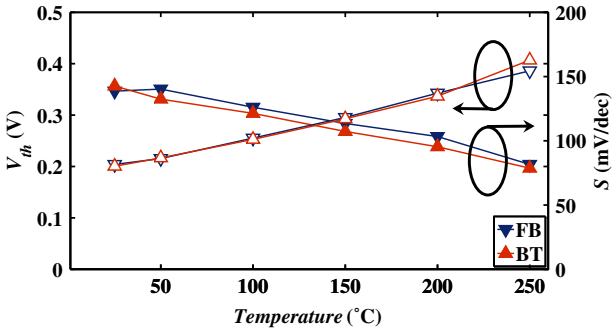

Fig. 1. Variation of threshold voltage V_{th} and subthreshold slope S with temperature in linear region.

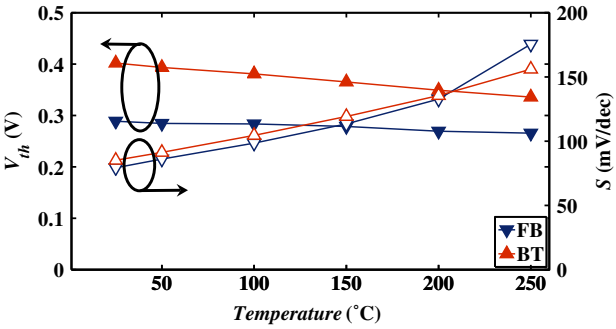

Fig. 2. Variation of threshold voltage V_{th} and subthreshold slope S with temperature in saturation region.

In saturation region, on the other hand, a difference in V_{th} between FB and BT is noticed, as shown in Fig. 2. Also dV_{th}/dT differs, with −0.1 and −0.3 mV/K for FB and BT transistors, respectively. Both differences, in V_{th} and dV_{th}/dT, are due to the floating-body effects which, in saturation, cause the drain current to be higher than corresponding current in BT transistor, and this is translated into a lower V_{th} values, compared to linear region. This difference was also reported for PD devices in [11].

2.2. Subthreshold slope S

Normally, for bulk and PD SOI transistors (if the interface traps are neglected), subthreshold slope is given by [12]

$$S = \frac{kT}{q}\ln(10)\left(1 + \frac{C_D}{C_{ox}}\right) \tag{10}$$

$$C_D = \frac{dQ_D}{d\psi_S} \tag{11}$$

$$Q_D = qN_aW_{max} \tag{12}$$

where ψ_S is the surface potential. As W_{max} varies with temperature, C_D depends on temperature as well and so does the subthreshold slope. This variation is usually linear, as shown in Figs. 1 and 2.

A severe degradation of subthreshold slope S from 25 to 250 °C can be seen from the logarithmic scaled IDVG curves shown in Figs. 3 and 4. Measured values of S for both FB and BT transistors are approximately 80 and 160 mV/dec at 25 and 250 °C, respectively, in both linear and saturation regions, as shown in Figs. 1 and 2. This is very critical for digital circuit designers. This degradation is linear in nature which is in conformity with theoretical and experimental behavior for bulk and partially-depleted SOI devices as reported in [2,12], where similar values of degradation were

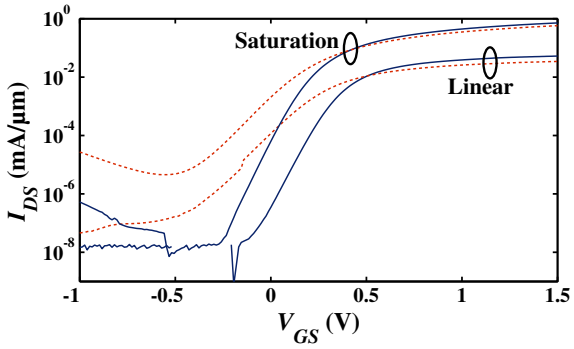

Fig. 3. IDVG in logarithmic scale for FB device at 25 °C (solid line) and 250 °C (dotted line).

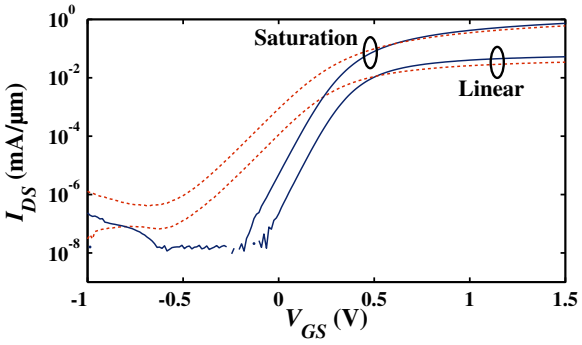

Fig. 4. IDVG in logarithmic scale for BT device at 25 °C (solid line) and 250 °C (dotted line).

shown. Still, this should be considered as an advantage compared to a non-linear degradation scheme in the case of FD devices, where the value of S at 250 °C could reach four times its value at room temperature [2,12].

2.3. Leakage current

The increase of junction leakage current is one of the main causes of failure in circuits operating at high temperature. The junction leakage current is proportional to the area of the junction. The strongest leakage component found in bulk CMOS operating at high temperatures originates from the "huge" well junctions. This causes loss of functionality in CMOS circuits at temperature above 180 °C while the same SOI CMOS circuits can operate up to 300 °C.

The leakage current in SOI MOSFET transistors is basically composed of two parts, a generation and a diffusion components, both related to the N^+–P junction (body–drain junction). The sum of these two components describes the leakage current as follows [2]

$$I_{\text{leak}} = qA\left(\frac{D_n}{\tau_n}\right)^{1/2}\frac{n_i^2}{N_a} + qA\frac{n_i W}{\tau_e} \tag{13}$$

where A is the junction area, D_n is the electron diffusion coefficient, τ_n is the electron lifetime in p-type neutral silicon, W is the depletion width, and $\tau_e = (\tau_n + \tau_p)/2$ is the effective lifetime related to the thermal generation process in the depletion region. The temperature dependence of leakage current is based on the temperature dependence of n_i which is given in Eq. (6).

The first term in Eq. (13) (the diffusion component) is proportional to n_i^2, and the second term (the generation component) is proportional to n_i. It has been experimentally observed [13] that the leakage current of SOI MOSFETs and reverse-biased diodes varies as n_i below a temperature of 100–150 °C and varies as n_i^2 above those temperatures, which implies that the diffusion component is more effective at higher temperatures while at lower temperatures it is the generation component which is more effective. It is also worth noticing that A, the area of the junction, and $A \cdot W$, the volume of the space-charge region associated with the diode, are both much smaller in SOI transistors than in bulk devices. Therefore, extremely low leakage current can be obtained in SOI devices.

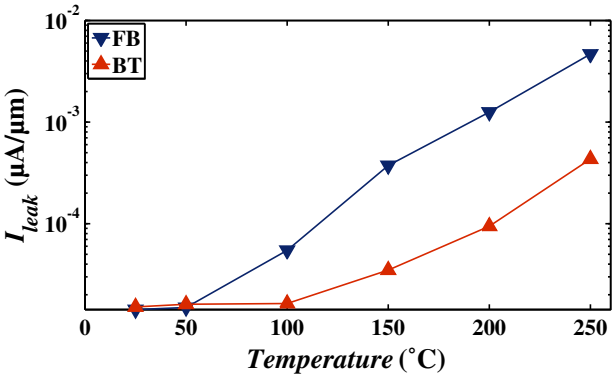

Fig. 5. Variation of leakage current I_{leak} with temperature.

In FB transistors, this diffusion component becomes more important due to the presence of the floating charge reservoir in the body. And as temperature increases, this reservoir becomes more and more important with charges thermally generated and accumulated inside it, hence the diffusion component is highly magnified. On the other hand, in BT transistors, the connection between the body and the source limits the diffusion component as no accumulation of charges takes place in the body. This behavior is manifested in Fig. 5 where the measured leakage current for the FB and BT transistors as a function of temperature is shown. Leakage current is measured when the transistor is in deep depletion region, which in this case is taken for small negative values of V_{GS} and for $V_{DS} = 1.2$ V. Under this biasing condition, the drain current is characterized by a plateau, and as V_{GS} becomes more negative the transistor turns into accumulation regime and the channel current starts to increase again. Therefore, the current at the plateau region is due only to junction leakage current.

It can be observed from Fig. 5 that up to 100 °C the difference between the two transistors is not very large, since not enough charges are accumulated in the body of FB transistors, so both devices are basically acting the same. But above 150 °C, thermally generated charges accumulated in the floating reservoir have high enough energy to overcome the barrier between the body and the source, therefore the floating-body transistor starts to show much higher leakage current and at 250 °C. FB transistor shows a leakage current of 4.7 nA/μm while BT transistor shows a leakage current of 0.43 nA/μm only, which is one order of magnitude lower than FB transistor (at 25 °C both transistors have only 15 pA/μm of leakage current).

2.4. I_{ON}-to-I_{OFF} ratio

This figure of merit is very important for digital circuit designers. It is well known that SOI devices provide much higher I_{ON}-to-I_{OFF} ratio than bulk devices, and this is related to the much smaller area of source and drain junctions in SOI compared to bulk (by a factor of 15 to 100, depending on the design rules) [2], and more important, the largest of all junctions, the well junctions, are totally absent from SOI CMOS. This contributes to a drastic reduction in the overall standby current consumption of SOI circuits compared to bulk ones.

In highly-doped devices, in which I_{OFF} corresponds to leakage current I_{leak}, the evaluation of the I_{ON}-to-I_{OFF} ratio with temperature is determined by the variations with temperature of threshold voltage, subthreshold slope and leakage current. On the other hand, in lowly-doped devices, it is dependent on threshold voltage and subthreshold variations only. Usually, we can expect to have stronger temperature dependence of the I_{ON}-to-I_{OFF} ratio in devices with higher threshold voltages.

The measured I_{ON}-to-I_{OFF} ratio for FB and BT transistors is shown in Fig. 6. Measurements of I_{OFF} are taken at $V_{GS} = 0$ V and of I_{ON} at $V_{GS} = 1.2$ V with $V_{DS} = 1.2$ V in both cases. As expected, BT transistor shows better I_{ON}-to-I_{OFF} ratio, thanks to its lower leakage current. It should also be noticed that the I_{ON}-to-I_{OFF} of BT transistors degrades faster with temperature. This is related to a higher degradation scheme of OFF current for BT transistor, as it can be seen from the OFF current shown in Fig. 6. The relatively large difference between OFF currents at room temperature (about one decade) tends to diminish at 250 °C, which explains the tendency to have close values of I_{ON}-to-I_{OFF} ratios for FB and BT transistors at 250 °C of about 362 and 888, respectively. These values are very close to the values obtained for a 0.15 μm fully-depleted low-V_{th} devices published in [14]. These values are also very large compared to the I_{ON}-to-I_{OFF} ratio of bulk transistors, which are in the order of 40 at 250 °C [2].

2.5. ZTC point and kink effect

The so called Zero Temperature Coefficient (ZTC) point has been identified for bulk CMOS by Shoucair [15] and Prijic et al. [16] in both the linear and the saturation regions for temperatures between 27 and 200 °C. According to Shoucair, the ZTC drain current is usually well defined up to approximately 200 °C, whereas at higher temperatures, drain-to-body leakage currents typically cause the characteristics to shift upwards on a linear scale of microamperes. Later, Groeseneken et al. [7] and Jeon and Burk [17] demonstrated the existence of the ZTC point experimentally for thin and thick-film SOI MOSFETs, respectively. The analytical formulation for ZTC in SOI devices has been introduced by Osman et al. [18]. ZTC point is device-geometry-independent for a given process [15] but it depends on the bias of the body for body-contacted SOI devices [19].

Basically, there are two ZTC points for a transistor, one for the drain current and the other for the transconductance, and in general they have different values in linear and saturation regions. These ZTC points are defined as the points at which the drain current or the transconductance remains constant as temperature varies, i.e., $\partial I_{DS}(T)/\partial T \approx 0$ or $\partial g_m(T)/\partial T \approx 0$, respectively. This can be explained as follows. The ZTC points, are values of V_{GS} at which the reduction of the threshold voltage is counter-balanced by the reduction of the mobility, and as a result, the value of the drain current or the value of the transconductance remains constant as the temperature varies. For gate voltages lower than ZTC, the decrease of threshold voltage is dominant and so drain current increases with temperature, while for gate voltages higher than ZTC, the mobility degradation predominates and drain current decreases with temperature. The ZTC is a very important bias point for analog designers as it corresponds to a gate voltage at which the device DC performance remains constant with temperature [20,21].

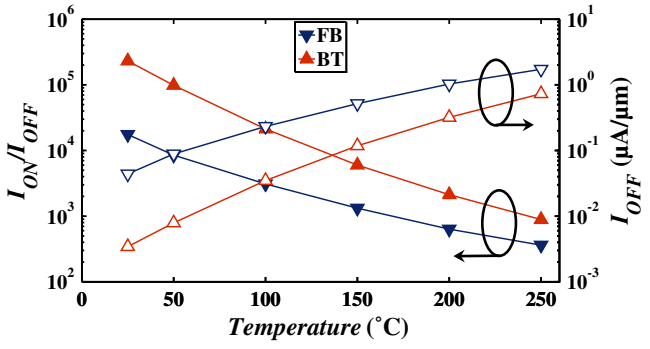

Fig. 6. Variation of I_{ON}-to-I_{OFF} ratio and I_{OFF} current with temperature.

Figs. 7 and 8 present the normalized I_{DS}–V_{GS} characteristics of both FB and BT transistors in addition to the normalized transconductance calculated from DC measurements by

$$g_m = \left.\frac{\partial I_{DS}}{\partial V_{GS}}\right|_{V_{DS}} \tag{14}$$

A very interesting advantage of BT transistor over FB transistor is shown in Figs. 7 and 8 where the ZTC points are noticed at higher V_{GS} for BT transistor for both drain current and transconductance measured at $V_{DS} = 1.2$ V . For BT transistor, ZTC_{IDS} and ZTC_{gm} take place at $V_{GS} = 0.6$ and 0.4 V, respectively, while for FB transistor they take place at $V_{GS} = 0.43$ and 0.25 V, respectively. This ensures, for BT transistor rather than FB transistor, an operation in ON mode at the ZTC point, giving higher drive current and higher overdrive voltage which is quite important for analog circuit designers working at varying temperature environments. It can also be noticed that, contrary to what Shoucair noticed for Bulk transistors [15], the ZTC point for both FB and BT transistors are well defined even up to 250 °C (and up to 300 °C for the work of Osman et al. [18]) thanks to the suppression of leakage currents by the insulating layer between the body and substrate; i.e., the buried oxide (BOX). For Bulk transistors, Shoucair reported a ZTC_{IDS} of 2 and 1.5 V in saturation and non-saturation regions, respectively.

On the other hand, Fig. 9 shows the output conductance of the FB transistor calculated from DC measurements using

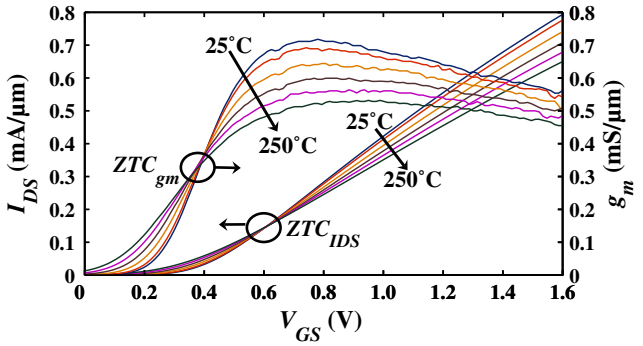

Fig. 7. I_{DS} and g_m versus V_{GS} at various temperatures for BT transistor at $V_{DS} = 1.2$ V.

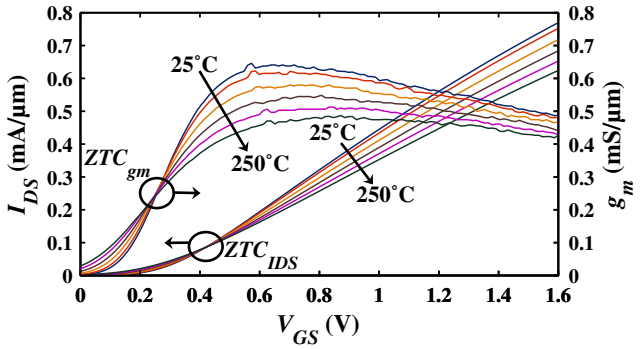

Fig. 8. I_{DS} and g_m versus V_{GS} at various temperatures for FB transistor at $V_{DS} = 1.2$ V.

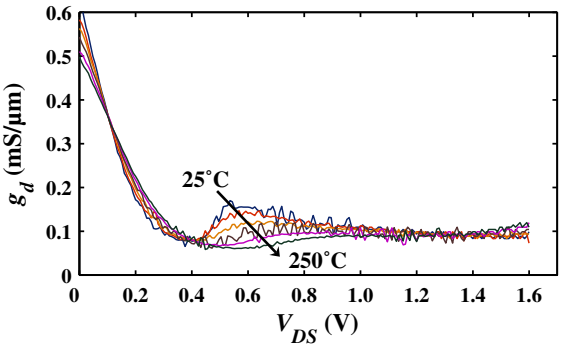

Fig. 9. Variation of g_d with temperature for FB transistor.

$$g_d = \left.\frac{\partial I_{DS}}{\partial V_{DS}}\right|_{V_{GS}} \tag{15}$$

where a suppression of the kink effect at higher temperatures is evident. This promotes FB transistors to work at harsh environments without problems arising from floating-body effects. Several factors can explain this improved performance for FB transistor. First, this can be due to the enhanced generation processes at high temperatures which leads to more efficient excess carrier extraction from the floating body. Also due to the attenuation of the impact ionization up to total disappearance at high temperatures (due to decrease of carrier mean free path) which also leads to the increase of Early voltage at elevated temperatures [22]. It can also be related to the reduction of the excess minority carrier concentration in the device body through increased recombination. And also, the reduction of the body potential variations owing to an increase of the saturation current of the source junction [2].

3. High-temperature RF behavior

The high-temperature RF behavior of SOI MOSFETs has not received the same attention as the high-temperature DC behavior. In the following subsections, the high-temperature RF behavior is investigated in details based on measured data. The Anritsu 37369A two-port vector network analyzer VNA operating up to 40 GHz and a 100 μm-pitch ground-signal-ground (GSG) high-frequency high-temperature Z-probes are used for RF signal measurements while DC biasing is achieved using HP 4145B device parameter analyzer. A temperature controlled 200 mm chuck is used to obtain measurements from room temperature up to 250 °C. An OPEN dummy structure is measured to perform a one-step de-embedding and hence removing the effects of the pad capacitances C_{pg} and C_{pd}. The effect of the access inductances L_g, L_d and L_s was found to be negligible due to the short access lines and the relatively low frequencies at which the extraction was performed (between 1 and 4 GHz). Therefore, the reference plan could be put at the dashed box in the small-signal equivalent circuit shown in Fig. 10.

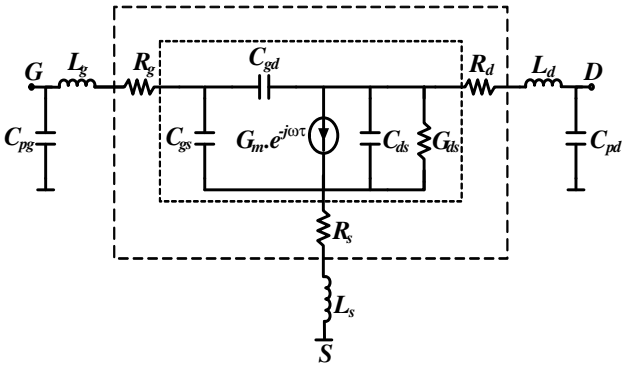

Fig. 10. Small-signal equivalent circuit of MOSFET.

3.1. Cutoff frequency

The cutoff frequency of a transistor (also known as the transition frequency) which characterizes the point at which the current gain of the transistor vanishes, and hence characterizes the high-frequency behavior of the transistor, can be obtained from

$$f_T = \frac{\mathrm{Re}(Y_{21})}{2\pi \mathrm{Im}(Y_{11})/\omega} \tag{16}$$

where $\mathrm{Re}(Y_{21})$ is mainly a function of the gate transconductance and $\mathrm{Im}(Y_{11})/\omega$ is directly related to the total gate capacitance.

The cutoff frequency extracted from de-embedded measured data is shown in Fig. 11 as a function of temperature for both FB and BT transistors, under the condition of maximum transconductance biasing, i.e., $V_{DS} = 1.2$ V and $V_{GS} = V_{GS}@g_{m_{max}}$. It is clear that as the temperature increases, the cutoff frequency f_T of both FB and BT transistors decreases with slightly different slopes. From 25 to 250 °C, the cutoff frequency degrades by 26% and 27% for FB and BT transisotrs, respectively. From Eq. (16), this degradation of f_T can be related to either a degradation with temperature in the behavior of $\mathrm{Re}(Y_{21})$, thus the transconductance, or $\mathrm{Im}(Y_{11})/\omega$, thus total gate capacitance, or both. This can be further investigated when looking at the intrinsic parameters presented in Section 3.4.

3.2. Extrinsic resistances

In Fig. 10, the dotted box differentiates between the intrinsic (inside) and extrinsic (outside) elements of a typical equivalent circuit for a SOI MOSFET. It was found that the extraction of intrinsic elements from measured *S*-parameters is very sensitive to the values of the extracted extrinsic resistances R_g, R_d and R_s. The extraction of these extrinsic resistances is performed using the cold FET method proposed by Bracale et al. in [23] and applying the $\omega^2\mathrm{Re}(Z_{ij})$ versus ω^2 method proposed by Crupi et al. in [24] to minimize the frequency dependence of $\mathrm{Re}(Z_{ij})$ associated to an incomplete capacitance de-embedding and/or intrinsic capacitive effects.

Fig. 12 shows the results of the extraction. R_d and R_s are quite similar for both FB and BT transistors. However, the difference in values between R_d and R_s is related to a slight dissymmetry between the two sides of the transistor. Between room temperature and 250 °C, both R_d and R_s show an increase of nearly 100% going from ~ 2 to ~ 4 Ω for R_d and from ~ 1.5 to ~ 3 Ω for R_s. Resistivity of doped silicon is calculated from [8]

$$\rho(T) = \frac{1}{qN_a\mu_p(T)} \tag{17}$$

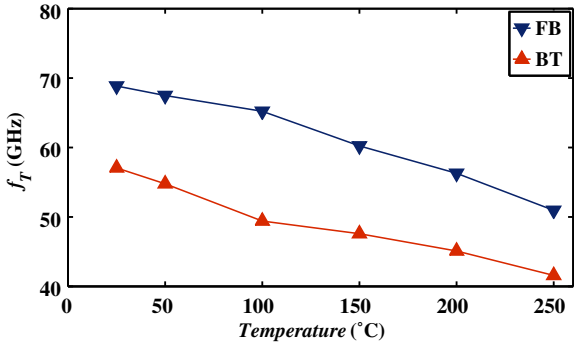

Fig. 11. Variation of cutoff frequency f_T with temperatures at max g_m condition.

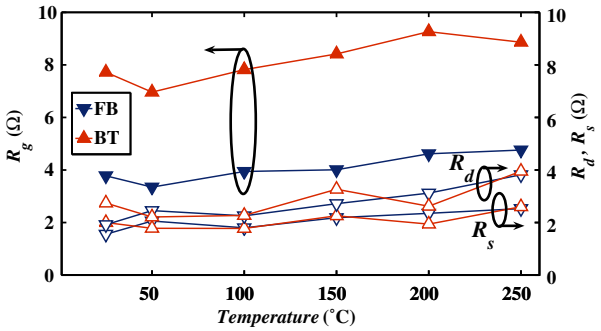

Fig. 12. Extrinsic resistances variation with temperature.

where $\mu_p(T)$ is the hole mobility as a function of temperature which can be calculated using Arora's mobility model [25]. For highly-doped silicon (as in the case of source and drain regions), only a 25% increase in resistivity is obtained for the considered temperature range. In our case, the classical Bracale method, used to extract the extrinsic resistances, does not consider the mobility degradation. This produces an over estimation of R_d and R_s [26], giving the high percentages of increase shown in Fig. 12.

3.3. Capacitances in OFF state

The values of extrinsic resistances extracted in the previous section are subtracted from the measured Z-parameters (Z_{ext}) to get the intrinsic Z-parameters (Z_{int}) using the following equation:

$$[Z_{int}] = [Z_{ext}] - \begin{bmatrix} R_g + R_s & R_s \\ R_s & R_d + R_s \end{bmatrix} \quad (18)$$

At this point, the reference plan is moved to the dotted box in Fig. 10. This represents the intrinsic part of the small-signal equivalent circuit of the MOSFET transistor. Besides the transconductance and the output conductance (presented in next section), the intrinsic part contains three capacitances; C_{gs}, C_{gd} and C_{ds}. It is of interest to extract these capacitances when the transistor is operated in ON (inversion) and OFF (depletion) states. This will give more insight for circuit designers, instead of the conventional definition of intrinsic and extrinsic capacitances. To extract the capacitances in OFF state, transistors are biased in deep depletion mode, i.e., negative values of V_{GS} and zero V_{DS}. The direct extraction method introduced by Raskin et al. in [27] is then applied. V_{GS} is set to −0.5 V where the capacitances showed a minimum when plotted as a function of V_{GS}. The results of the extraction are shown in Figs. 13 and 14. C_{gs} and C_{gd} in OFF state contain the contribution of three capacitances, as shown in Fig. 15; the fringing capacitances, the overlap capacitances and the body depletion capacitances. The later has a high sensitivity to temperature variation as it depends on the intrinsic carrier density n_i, which is sensitive to temperature changes as shown earlier in Eq. (6). This explains the variation of capacitances in deep depletion with temperature as summarized in Table 1.

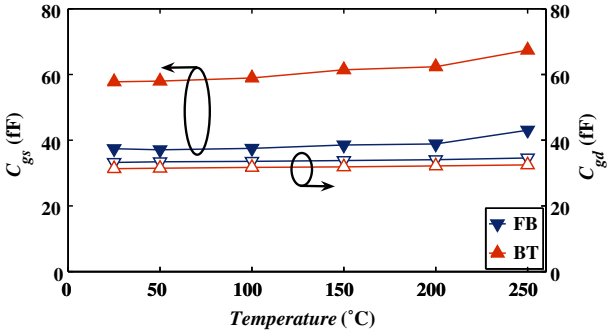

Fig. 13. C_{gs} and C_{gd} variation with temperature in OFF state.

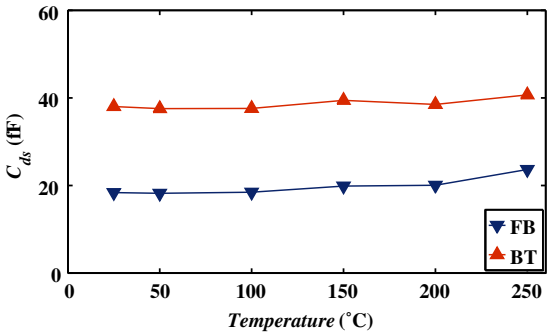

Fig. 14. C_{ds} variation with temperature in OFF state.

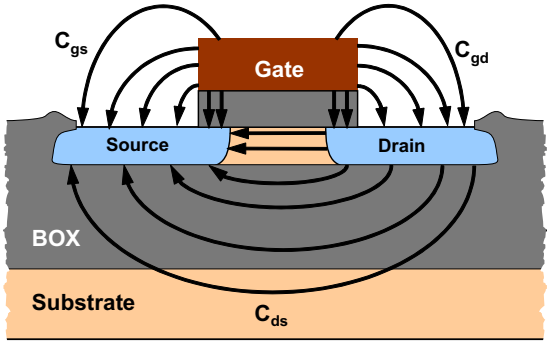

Fig. 15. Capacitances of MOSFETs.

Theoretically, C_{ds} in BT should be double that in FB, due to the absence of one of the two series capacitances because of the short connection between the body and the source, as shown in Fig. 16. Fig. 14 shows that this is rather correct, as BT transistor shows nearly double the value of C_{ds} compared to FB transistor. On the other hand, FB transistor shows double the variation of C_{ds} with temperature compared to BT transistor, as shown in Table 1, for the same reason; in FB transistor, two capacitors in series vary with temperature, while in BT transistor one of these series capacitances is removed.

This connection between the body and the source also affects the gate-source capacitance C_{gs}, where again it is higher in the case of BT transistor as shown in Fig. 13, due to the metal layers connections which adds to C_{gs} and varies according to the layout implemented. Fig. 17 shows an illustration of the layout used in this work. Therefore, a good layout optimization technique can highly reduce this capacitance. It is worth mentioning here that the capacitance related to the body node in BT transistors is very small compared to capacitances related to metal layers connections. Values for extracted body node capacitances for the same technology used in this work was published by Lederer and Raskin in [29]. The layout variations also affect the amount of difference between C_{gs} and C_{gd} in OFF state for the same transistor, whether FB or BT, thus affecting the theoretical symmetry of the transistor assumed at zero V_{DS}. Fig. 13 shows a small difference between C_{gs} and C_{gd} in

Table 1
Variation of capacitances from 25 to 250° for FB and BT transistors in deep depletion

	C_{gs}	C_{gd}	C_{ds}
FB (%)	↑ 6.1	↑ 3.8	↑ 14.2
BT (%)	↑ 11.4	↑ 3.5	↑ 6.9

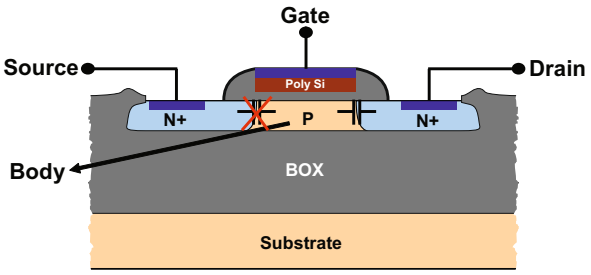

Fig. 16. Difference in C_{ds} between FB and BT transistors.

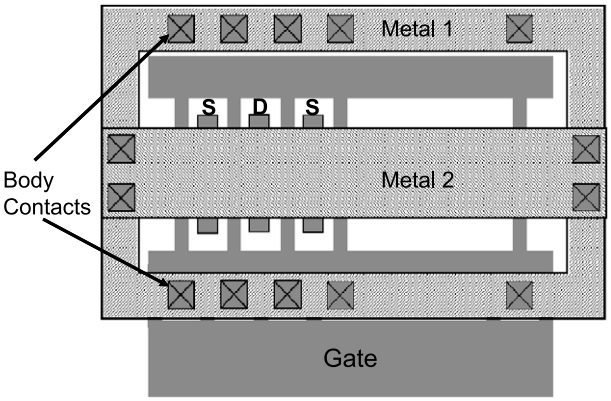

Fig. 17. An illustration of the layout showing the metal layers connection between the body and the source.

the case of FB (nearly symmetric) while large difference (nearly the double) in the case of BT transistor.

3.4. Intrinsic elements in ON state

As in the case of the extraction of capacitances in deep depletion, the extraction of intrinsic elements in ON state is performed using the intrinsic Z-parameters (Z_{int}) (obtained from Eq. (18)) and the direct extraction method [27] under saturation and strong inversion bias conditions; i.e., $V_{DS} = 1.2$ V and $V_{GS} = 1.5$ V. The results of the extraction are shown in Figs. 18–20. Percentages of variation of intrinsic elements with temperature are shown in Table 2. All percentages are relative to the room temperature values.

C_{gs} in ON state shows higher values for BT transistor compared to FB transistor, for the same reason of metal layers connections explained in previous section. Also a higher difference (compared to the OFF state case) is shown in Fig. 18 between C_{gs} and C_{gd} for the same transistor due to the presence of the inversion layer in

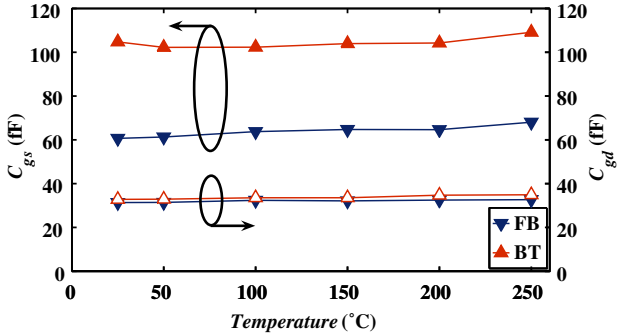

Fig. 18. Variation of C_{gs} and C_{gd} with temperature extracted in saturation region under strong inversion.

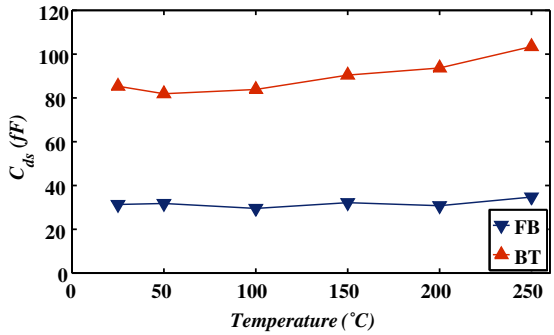

Fig. 19. Variation of C_{ds} with temperature extracted in saturation region under strong inversion.

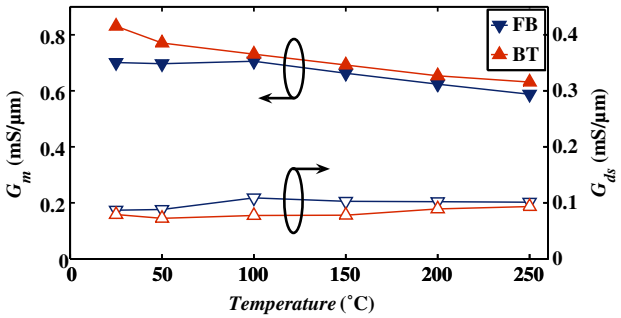

Fig. 20. Intrinsic transconductance G_m and intrinsic output conductance G_{ds} variation with temperature extracted in saturation region under strong inversion.

saturation region, i.e., the transistor is no more symmetric. C_{gs} and C_{gd} show relatively stable behavior with temperature, as can be seen from Table 2, while C_{ds} shows higher degradation (increase) with temperature reaching nearly 7.77% and 23.4% for FB and BT transistors, respectively. This degradation in C_{ds} is related to the increase in generation and recombination rates in the channel with temperature.

Output conductance G_{ds}, shows a relatively stable behavior with temperature, where BT transistor shows an increase of 24.1% at 250 °C and FB transistor shows an increase of 15.6% which is less than that for the BT transistor due to the supression of the kink effect as explained in Section 2.5. As a result, both transistors show stable output performance at high temperatures, hence the matching with next stages is not affected by the increase in temperature.

Transconductance G_m, on the other hand, shows some degradation with temperature. A decrease of 16.3% and 20.5% for FB and BT transistors, respectively, can be noticed. This can be explained by the degradation of surface mobility with temperature, an effect that has been measured and modeled by Reichert et al. [28]. These transconductances are extracted from intrinsic Z-parameters (Z_{int}) in saturation region, thus away from the ZTC point of G_m and also from the maximum value of G_m. Therefore, this degradation will directly affect the intrinsic gain of the transistor at elevated temperatures.

To complete the study of the intrinsic behavior of the FB and BT transistors, an extraction of the intrinsic cutoff frequency f_c is nec-

Table 2
Variation of intrinsic elements from 25 to 250° for FB and BT transistors in strong inversion

	C_{gs}	C_{gd}	C_{ds}	G_m	G_{ds}	f_c
FB (%)	↑ 10.9	↑ 0.4	↑ 7.77	↓ 16.3	↑ 15.6	↓ 21.6
BT (%)	↑ 4.3	↑ 6.4	↑ 23.4	↓ 20.5	↑ 24.1	↓ 23.9

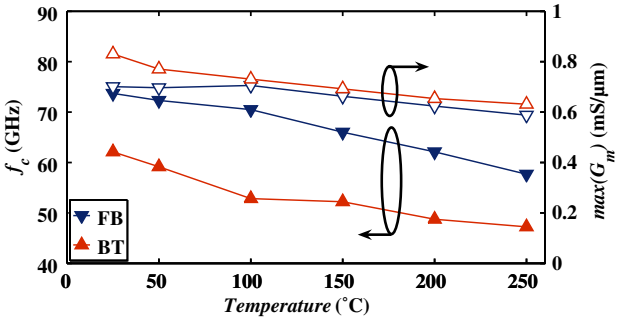

Fig. 21. Variation of intrinsic cutoff frequency f_c and max(G_m) with temperature.

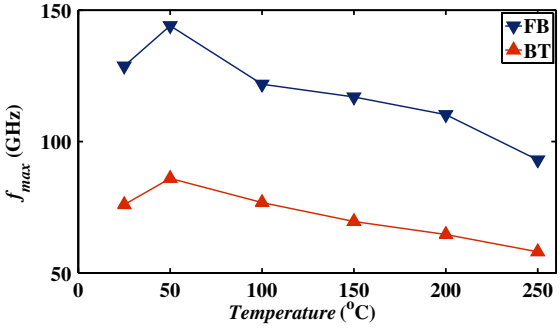

Fig. 22. Variation of f_{max} with temperature under maximum g_m bias condition.

essary. The effect of transconductance G_m is very important on f_c since it is defined by:

$$f_c = \frac{G_m}{2\pi C_{gs}} \tag{19}$$

Therefore, the extraction is performed at maximum G_m bias condition and using intrinsic measured Z- and S-parameters (Eq. (18)). Results of extraction are shown in Fig. 21. The degradation in max(G_m) is nearly the same as for G_m in saturation, with a decrease of 16.3% and 18.1% for FB and BT transistors, respectively. On the other hand, f_c degrades by 21.6% and 23.9% for FB and BT transistors, respectively. It is clear from these results that the difference in degradation schemes for f_c between FB and BT transistors (about 2% of difference) comes from the G_m component in Eq. (19). The transconductance G_m is interpreted to be more dominant in affecting the behavior of the intrinsic cutoff frequency than C_{gs}.

It is also of interest to check the behavior of f_{max} with temperature. f_{max} is defined as the frequency at which unilateral gain (ULG) is equal to 1 (i.e., 0 dB). ULG is defined by Mason [30] as the maximum available gain when a lossless feedback is used to cancel the transmission of power from the output to the input of the device. Thus, ULG is given by

$$\mathrm{ULG} = \frac{|Y_{21} - Y_{12}|^2}{4[\mathrm{Re}(Y_{11})\mathrm{Re}(Y_{22}) - \mathrm{Re}(Y_{12})\mathrm{Re}(Y_{21})]} \tag{20}$$

Fig. 22 shows f_{max} as it varies with temperature, extracted from measurements made at maximum G_m bias condition. A similar degradation scheme is noticed for both transistors with 29.6% decrease and 28.1% decrease for FB and BT transistors, respectively.

4. Conclusions

The DC and RF high temperature behaviors have been investigated in details and presented in this paper in order to provide insights to the RF designers for high temperature applications with the required information needed to achieve a stable performance, both in DC and RF. It was shown that although some of the small-signal equivalent circuit elements do not show a high degradation with temperature (like C_{gs} and C_{gd}), some other RF figures of merit suffer from relatively high degradation with temperature, like the cutoff frequency and the intrinsic transconductance. However, the degradation shown in cutoff frequency should not be very effective for the recent technologies where f_T reaches hundreds of GHz. The FB transistor outperforms the BT transistor regarding the temperature stability especially for intrinsic transconductance which, besides the suppression of the kink effect in output conductance, promotes it as a good candidate for high-temperature RF applications. On the other hand, FB transistor shows poorer DC performance at higher temperatures, especially when leakage current and I_{ON}-to-I_{OFF} ratio are concerned. It also demonstrates lower ZTC point than BT transistor for both drain current and transconductance. So in conclusion, a designer should optimize the different features of FB and BT transistors in order to reach the most stable performance for a certain application.

Acknowledgement

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References

[1] Fleetwood DM et al. High-temperature silion-on-insulator electronics for space nuclear power systems: requirements and feasibility. IEEE Trans Nucl Sci 1988;35:1099–112.
[2] Colinge Jean-Pierre. Silicon-on-insulator technology: materials to VLSI. 3rd ed. Kluwer Academic Publishers; 2004.
[3] Flandre D, Nazarov AN, Hemment PLF. Science and technology of semiconductor-on-insulator structures and devices operating in a harsh environment. Kluwer Academic Publisher; 2005.
[4] Li Y, Niu G, Cressler I JD, Patel J, Liu M, Reed RA et al. Operating SOI CMOS technology in extreme environments. In: Silicon monolithic IC in RF system; 2003. p. 37–40.
[5] Francis P, Terao A, Gentinne B, Flandre D, Colinge JP. SOI technology for high-temperature applications. Tech Dig IEDM 1992:353–7.
[6] Emam M, Tinoco JC, Vanhoenacker-Janvier D, Raskin J-P. High-temperature RF behavior of partially-depleted SOI MOSFET transistors. In: Proceedings EUROSOI'08, Cork Ireland, 23–25 January; 2008.
[7] Guido Groeseneken, Jean-Pierre Colinge, Maes Herman E, Alderman JC, Holt S. Temperature dependence of threshold voltage in thin-film SOI MOSFET's. IEEE Electron Dev Lett 1990;11(8):329–31.
[8] Yuan Taur, Ning Tak H. Fundamentals of modern VLSI devices. Berlin: Cambridge University Press; 1998.
[9] Muller RS, Kamins TI. Device electronics for integrated circuits. 2nd ed. New York: Wiley; 1986 [p. 56].
[10] Delatte P, Picún G, Demeûs L, Vancaillie L, Kilchytska V, Flandre D et al. On the potential 0.2 μm fully-depleted SOI for low-power mixed and digital circuits for applications up to 225C. In: Proceedings of HITEN Conference, Oxford (UK), July 8–10; 2003.
[11] Yeh Wen-Kuan, Huang Chiutsung, Chen Mao-Chieh. Temperature dependency of 0.1 μm partially depleted SOI CMOSFET. IEEE Electron Dev Lett 2001;22(7):339–41.
[12] Rudenko T, Kylchytska V, Colinge JP, Dessard V, Flandre D. On the high-temperature subthreshold slope of thin-film SOI MOSFETs. IEEE Electron Dev Lett 2002;23(3):148–51.
[13] Vu DP, Boden MJ, Henderson WR, Cheong NK, Zavracky PM, et al. Proc IEEE SOS/SOI Technol Conf 1989:165–6.
[14] Vancaillie L, Kilchytska V, Delatte P, Matsuhashi H, Ichikawa F, Flandre D. 0.15 μm Fully depleted SOI for mixed-signal applications up to 250C: are we approaching the limits of device scaling for high-temperature electronics? In: Procceedings of HITEN Conference, Oxford (UK), July 8–10; 2003.
[15] Shoucair FS. Analytical and experimental methods for zero-temperature-coefficient biasing of MOS transistors. Electron Lett 1989;25:1196–8.
[16] Prijic Z, Dimitrijev SS, Stojadinovic N. The determination of zero temperature coefficient point in CMOS transistors. Microelectron Reliab 1992;32(6):769–73.
[17] Jeon DS, Burk DE. A temperature-dependent SOI MOSFET model for high-temperature applications (27–300 °C). IEEE Trans Electron Dev 1991;38(9):2101–10.

[18] Osman Ashraf A, Osman Mohamed A, Dogan Numan S, Imam Mohamed A. Zero-temperature-coefficient biasing point of partially depleted SOI MOSFET's. IEEE Trans Electron Dev 1995;42(9):1709–11.
[19] Kaamouchi El, Dambrine G, Si Moussa M, Emam M, Vanhoenacker-Janvier D, Raskin J-P. Body-biasing control on zero-temperature-coefficient in partially depleted SOI MOSFET. In: Proceedings of Silicon Monolithic Integrated Circuits in RF Systems SiRF; 23–25 January 2008. p. 114–17.
[20] Gentinne B, Eggermont JP, Colinge JP. Performances of SOI CMOS OTA combining ZTC and gain-boosting techniques. Electron Lett 1995;31(24):2092–3.
[21] El Kaamouchi M, Si Moussa M, Raskin J-P, Vanhoenacker-Janvier D. Zero-temperature-coefficient biasing point of 2.4-GHz LNA in PD SOI CMOS technology. In: Proceedings of European Microwave Conference; 9–12 October 2007. p. 1101–4.
[22] Kilchytska V, de Meyer K, Flandre D. In-depth investigation of 0.13 m SOI MOSFETs for high-temperature applications. In: Proceedings of ultimate integration silicon (ULIS 2004), Leuven, Belgium, March 11–12; 2004. p. 163–6.
[23] Bracale A, Ferlet-Cavrois V, Fel N, Pasquet D, Gautier JL, Pelloie JL, et al. A new approach for soi devices small-signal parameters extraction. Analog Integr Circ Signal Process 2000;25:157–69.
[24] Crupi G, Schreurs D, Parvais B, Caddemi A, Mercha A, Decoutere S. Scalable and multibias high frequency modeling of multi-fin FETs. Solid State Electron 2006;50:1780–6.
[25] Arora ND, Hauser JR, Roulston DJ. Electron and hole mobilities in silicon as a function of concentration and temperature. IEEE Trans Electron Dev 1982;29(2):292–5.
[26] Tinoco JC, Raskin J-P. Revised RF Extraction Methods for Deep Submicron MOSFETs. European Microwave Week EuMW-2008, Amsterdam, Netherlands, October 27–31; 2008.
[27] Raskin J-P, Gillon R, Chen J, Vanhoenacker-Janvier D, Colinge J-P. Accurate SOI MOSFET characterization at microwave frequencies for device performance optimization and analog modeling. IEEE Trans Electron Dev 1998;45(5):1017–25.
[28] Reichert G, Ouisse T, Pelloie JL, Cristoloveanu S. Surface mobility of SOI MOSFET's in the high temperature range: modeling and experiment. In: Proceedings of IEEE SOI conference; 1995. p. 42–3.
[29] Dimitri Lederer, Jean-Pierre Raskin. Characterization of the body node in PD SOI MOSFETs using multiport VNA measurements. IEEE Trans Electron Dev 2007;54(11):3030–9.
[30] Mason SJ. Power gain feedback amplifier. IRE Trans Circ Theor 1954;CT-1(2):20–5.