SOI Devices and Substrates towards RF and Millimeter Wave ICs

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Abstract— **In this paper, an overview of SOI technology for high-frequency telecommunication applications is presented. At the transistor level, thanks to SOI's low-parasitic architecture and good electrostatics, high oscillation and cut-off frequencies in the range of 400 GHz are achieved. At the RF-IC level, a review is made to reveal the position of SOI for key RF and millimeter wave circuits (switches, LNAs and PAs). Finally, substrate impact is described at RF frequencies. The existing flavors of SOI substrates are reviewed, highlighting substrate requirements at RF, as it seriously impacts parasitic coupling, RF losses, passive quality factor, and non-linear signal distortion. Overall, SOI is shown to be a prime candidate for high-performance millimeter wave and 5G applications, and also for low-power RF IoT.**

Keywords—SOI, Radio-Frequency, Trap-Rich, Low-Loss Substrate, Substrate Non-Linearity, FD-SOI, Front-End-Module

I. Introduction

Silicon-on-Insulator (SOI) technology has taken the radio-frequency (RF) world by storm in the past decade. By offering high performance at low cost it has steadily displaced Gallium-Arsenide and Silicon-on-Sapphire technologies to become the mainstream technology for RF switch banks in mobile applications. This success of SOI in today's RF market is not only due to significant technological improvements at the transistor level, but also to optimizations made at the substrate and back-end of line levels to enable high performance RF applications.

With the circuit complexity of RF front-end modules (FEMs) in smart devices ever increasing as the next generations of telecommunication standards emerge (4G-LTE, 5G), more and more RF content is required in each device [1]. This strong growth in the RF industry, expected to be led by 5G and Internet-of-Things (IoT) products, must be supported by a technology with a high-volume manufacturing capability. This requirement leads to a strong interest in silicon-based technology for RF applications, as it is a mature technology fully enabled on 300-mm-diameter wafers for high throughput. Today, SOI is a strong candidate for a variety of RF circuit blocks, beyond RF switches where it has already made a name for itself over the past decade. Indeed, advanced partially depleted (PD) SOI nodes (sub-100 nm) as well as the most advanced fully depleted (FD) SOI nodes (28 and 22 nm) are demonstrating their potential for all kinds of RF and millimeter wave front-end circuit modules.

This paper aims to present the overall RF performance of SOI technologies, at the device, circuit and substrate levels, for telecommunications and FEM applications.

II. State-of-the-Art SOI Devices and RF-ICs

A. SOI Devices

Aggressive gate-length downscaling of MOSFETs has been the main stimulus for the growth of the integrated circuit industry. It is primarily the result of the need for improved circuit performance and cost reduction and has resulted in tremendous increase in MOSFET transconductance and decrease in total gate capacitance, thereby resulting in very high cut-off frequencies [2]. It is only in recent decades that CMOS has been considered as an RF technology of choice. Indeed, the most advanced SOI nodes are now boasting speed performances that rival the established ultra-fast high-electron mobility transistors. Nowadays, the most advanced PD- (45 nm) and FD-SOI (28 nm and 22 nm) nodes are boasting speed metrics that are entirely sufficient for RF and even mm-wave applications, with cut-off frequencies f_t and f_{max} in the 300 to 400 GHz range, opening SOI to RF and mm-wave markets beyond switches.

For FD-SOI, 5G is not the only RF sector of opportunity. Indeed, thanks to its below-BOX back-gate electrodes, FD-SOI devices can achieve very low threshold voltage V_T [3]. This enables low-power capabilities, making FD-SOI a prime candidate for Internet-of-Things (IoT) applications, that will for the most part require low throughput, but in which low power is essential, as well as large volume manufacturing capabilities.

B. SOI RF and mm-wave ICs

The FEM complexity increases with each new generation of communication standard, due to the existence of a larger number of bands and modulation techniques. An FEM supporting state-of-the-art telecommunication standards is composed of at least one transmit and receive module per standard, with switches, filters and amplifiers associated to each frequency band and/or sub-band. Higher data-rate generation standards therefore lead to a higher amount of RF content in a single smartphone device, which has grown from approximately $1 for 2G cellular handsets, to $3 for the first generation of 3G enabled smartphones, up to $13 in today's (2019) 4G-TLE-advanced technology, and is predicted to reach $25 of RF content in 5G enabled devices.

To support this growth in the RF industry, a technology with high-volume manufacturing capability is required for each element of the FEM. SOI technology fits the bill, leading to the development of a wide range of high-frequency SOI circuit modules, supported by the impressive RF characteristics of advanced SOI FETs. Tremendous research effort has been dedicated to RF-SOI, driven by large volume applications requiring inexpensive single-chip transceivers (switches, LNAs, PA, etc.), both at the base-band and the RF front-ends. To highlight this, Fig. 1 presents a historical literature review of SOI technologies for RF applications.

Switch modules were the first RF applications for SOI, hitting the market around 2007 and dominating it for handsets by 2012. In 2019, almost every single RF switch in modern smartphones is implemented in a PD-SOI node (typically 180 nm or 130 nm node) on a engineered "trap-rich" substrate.

Significant research interest and industry development pushed the RF SOI nodes even further, down to the 45 nm PD-SOI node, truly optimized for RF performance, and beyond, to sub-30 nm FD-SOI nodes, at which cutoff and oscillation frequencies reach the range of 400 GHz. With these performances other key RF circuit elements emerged in

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the literature, starting from around 2010 for low-noise amplifiers (LNA) and power amplifiers (PA).

Notably, the GlobalFoundries PD 45 nm RF-SOI process has demonstrated its strong potential for RF and mm-wave circuits. Fig. 1 shows its emergence around 2012, implementing RF functions such as VCOs, LNAs, PAs and switches at millimeter wave frequencies up to 100 GHz. This process combines very fast transistors on top of low-loss and highly linear trap-rich substrates that are truly optimized for RF purposes, that allow for high-quality interconnects, transmission lines and passives (inductors, transformers, etc.) along with strong substrate isolation and linearity.

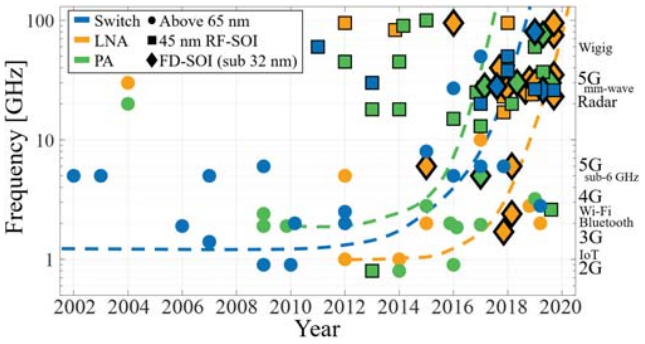

Fig. 1. Literature review over time of SOI technologies for RF and millimeter wave circuit elements of FEMs.

Around 2015, IC demonstrator circuits in 22 nm and 28 nm FD-SOI were developed, and interest in these nodes for high frequency applications has increased significantly since then. In particular, Fig. 1 clearly reveals a focus at 28 GHz.

While 45 nm RF-SOI has a strong application focus at the millimeter wave bands, FD-SOI nodes also find applications at lower frequencies (sub-6 GHz) where their RF performances can be tuned down (threshold voltage and back-gate control) to remain sufficient for IoT type RF applications at ultra-low power consumption.

III. Silicon-Based RF-Substrates

The electrical properties of the physical substrate have a strong impact on device and circuit performance, and this is especially true at RF and mm-wave frequencies. Indeed, at high-frequencies the thin dielectric layer isolating the metal interconnects, passives, and transistors from the substrate becomes transparent by their capacitive nature, and significant electric fields from these devices penetrate into the silicon substrate, inducing losses and strongly impacting the values of parasitic coupling elements. In this section, we overview the substrate impact on RF integrated circuits (RF-ICs), and present the major different flavors of SOI substrates found in today's foundry options.

A. Substrate Impact on Coplanar Technology

In the field of RF-ICs electrical signals propagate in a conductive metal layer atop an insulator-semiconductor stack. A coplanar waveguide (CPW) is depicted in Fig. 2 atop such a stack of materials. To avoid losses in such lines, and also to mitigate coupling between them, it is important for the underlying substrate to have a high effective resistivity. Furthermore, it is required that the substrate be as linear as possible to minimize distortion of the electrical signals. For these reasons the standard-doped (~10 Ωcm) silicon substrate –that is widespread among digital applications– is unsuited to wireless systems, RF devices and power circuits due to its high conductivity, high RF losses and low linearity. Low-doped silicon is then favoured with high nominal resistivity (ρ_{nom}) above 1 kΩcm. The resistivity of semiconductors is by nature dependent on the local electric field. Low-doped high-resistivity (HR) substrates are particularly field-sensitive, and it is typical for the semiconductor volume beneath the insulator to be in a conductive state due to (even low-level) parasitic fields present in the multilayer. The most common parasitic fields originate from fixed charges (usually positive in Si/SiO_2 heterostructures) that are present at the insulator - semiconductor interface. Then, a highly conductive channel-like layer is induced beneath the insulator, as depicted in Fig. 2, for the case of a low-doped HR substrate. These charges (represented "+" symbols in Fig. 2), are inevitable in the IC fabrication process, and induce free electrons at the interface in very high concentrations, locally lowering the resistivity by a factor of 10^3 to 10^6. This in turn lowers the sensed resistivity by a factor of 10 to 10^4, to values as low as 1 Ωcm. This is referred to as the parasitic surface conduction (PSC) effect that renders the use of a HR substrate ineffective for improving the performance of overlying RF-ICs as compared to standard-doped silicon (ρ_{nom} ~10 Ωcm) [4].

A breakthrough on this matter was made in the early 2000's with the introduction of a thin polysilicon layer rich in defects (traps) beneath the buried oxide in SOI technology [5]. This layer effectively mitigates the PSC effect by pinning the Fermi-level near mid-gap at the interface in a highly resistive state, enabling ρ_{eff} values of over 1 kΩcm.

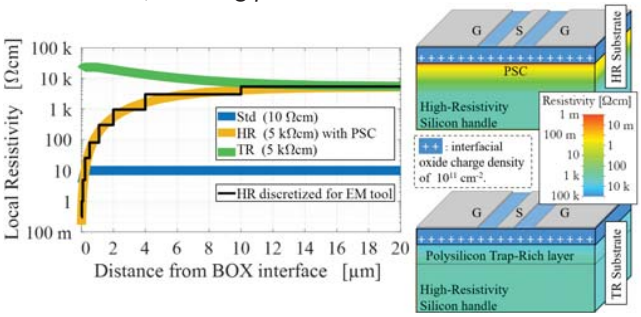

Fig. 2. Resistivity profiles in the semiconductor volume beneath the BOX layer for a Std, HR and TR SOI substrates. All profiles include the presence of interfacial oxide charges with a density of 10^{11} cm^{-2}.

High-resistivity wafers suffering from the PSC effect have highly non-uniform resistivity profiles beneath the BOX.

The green curve in Fig. 2 represents the resistivity profile beneath the BOX in a high-quality TR-SOI substrate, while the blue curve illustrates the profile in a standard resistivity (~10 Ωcm) substrate (Std).

The results of Fig. 2 were obtained using the finite element semiconductor simulation tool ATLAS from Silvaco which solves for Poisson's and semiconductor equations in the Si-based substrates and at the Si/SiO_2 interfaces, allowing for physical parameters such as fixed oxide charges, interface and volume traps, to be accurately simulated along with their impact on the free carrier distributions in the semiconductor regions. In all simulated substrates an interfacial oxide charge density of 10^{11} cm^{-2} was defined. For the TR sample tail-type distributions for the acceptor and donor traps were used to model the polysilicon layers according to [6].

Three reference SOI substrates, a standard-resistivity (Std), a high-resistivity (HR) and a trap-rich (TR) were fabricated with passive RF devices defined above a 200 nm

BOX in order to compare the RF measurements of the various devices. Both the HR and TR samples were fabricated starting from high-resistivity float-zone wafers characterized by a nominal resistivity above 5 kΩcm, while a 10 Ωcm silicon wafer was used for the Std sample. A 500 nm-thick polysilicon layer was deposited for the TR sample. Finally, a 500 nm-thick oxide was deposited by PECVD for all three samples, followed by a 1 µm aluminium metallization and front-side lithography and etch to pattern the RF structures. The dimensions of the CPWs are a signal line width of 26 µm, a spacing of 12 µm and ground line widths of 155 µm.

B. *Small-Signal Substrate Performance*

RF measurements and simulations of CPW lines enable the extraction of effective substrate electrical parameters. Indeed, RF engineers require accurate values for substrate permittivity and resistivity to perform robust designs of RF circuits. However, because the substrate is a heterostructure, made up of several materials, and because the semiconducting materials present non-uniform properties, the concepts of effective resistivity (ρ_{eff}) and permittivity (ε_{eff}) are employed to electrically describe it [7].

CPW lines are measured and simulated on the considered SOI wafers. The RF measurements were performed on-wafer using a wideband VNA and a pair of GSG microwave probes. Calibration and de-embedding techniques are described in [7, 8]. Both the measurements and the simulations yield the S-parameters of the CPWs, and these are converted into the substrate's ρ_{eff} according to [7]. The computed ρ_{eff} of the three substrates are plotted in Fig. 3.

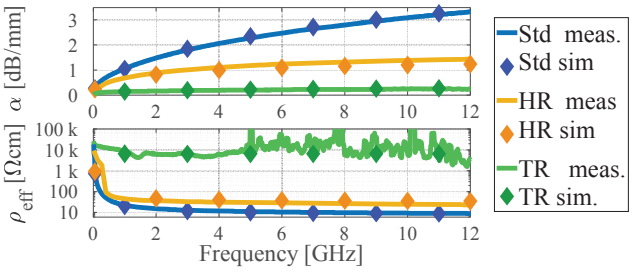

Fig. 3. Line losses (α) and effective substrate resistivity (ρ_{eff}) extracted from CPW-lines S-parameters, measured and simulated.

The CPW lines on standard resistivity (Std) SOI substrates present an effective resistivity in the range of 10 Ωcm. As a consequence, the lineic RF losses of the lines on Std substrates are in the range of 3.0 dB/mm at 10 GHz.

The effective resistivity and RF losses of the CPWs on a high-resistivity (HR) substrate are of similarly poor performance. The extracted value of around 30 Ωcm for HR is due to the PSC effect induced by fixed charges in the BOX [4, 7], by which the high nominal resistivity of the HR substrate is counteracted by a thin, high carrier density, highly conductive region formed at the Si/SiO_2 interface (see Fig. 2). Consequently, the lineic RF losses of the CPWs on HR are in the range of 1.4 dB/mm at 10 GHz.

Trap-rich (TR) substrates eliminate the PSC effect with the addition of a thin polysilicon layer, rich in defects, beneath the BOX and above a high nominal resistivity silicon bulk [5]. These defects, or traps, capture the large number of induced carriers present in the PSC layer and effectively pin the Fermi-level near mid-gap at the BOX interface, ensuring a state of strong depletion and high resistivity. The extraction of the effective parameters from the CPW line measurements show a substantial increase of the effective resistivity to values of the order of 5 to 10 kΩcm, and as a consequence the RF line losses at 10 GHz are at the low value of 0.24 dB/mm. Most of these losses are due to the finite conductivity of the metal lines, and not to dissipations within the substrate.

C. *Large-Signal Substrate Performance*

The latest communication standards demand high performance metrics from FEMs. Carrier aggregation techniques in particular impose more stringent requirements in terms of isolation and linearity [9], both of which are sources of spectral cross-contamination between adjacent bands. The linearity burden is increased at all levels of RF chip: from system design and RF circuit modules down to the engineered substrate [1].

Semiconductor materials are non-linear by nature, as their local electrical properties depend on the electric field that penetrates them. Indeed, in an IC block, a significant amount of the overall distortion can originate from the silicon-substrate itself rather than from the active devices [10].

In order to evaluate harmonic distortion (HD) originating from the substrate large-signal measurements of the 2.1 mm-long CPW lines are performed on-wafer using a dedicated setup [11]. A single 900 MHz (f_0) tone is injected into one port of the CPW, and its power is swept (-30 to +25 dBm). Due to the non-linear substrate behavior the output is multi-tone, with a fundamental component H1 (900 MHz) along with harmonic components at all integer multiples of f_0. The second harmonics H2 (1.8 GHz), measurement on the three SOI substrates, are plotted in Fig. 4 versus the H1 at output.

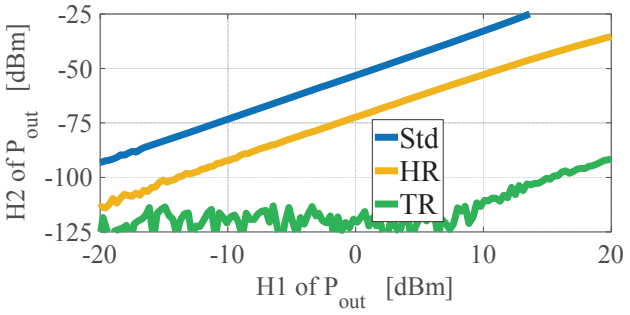

Fig. 4. Second harmonic H2 plotted versus fundamental component H1 of the output signal of a 2.1 mm CPW line implemented on the SOI substrates.

The electrical characteristics of Std and HR substrates are strongly voltage-dependent [12], and consequently high levels of harmonic distortion are observed. This occurs as the substrate impedance associated to these substrates varies as a function of the applied signal. Wide amplitude voltage signals modify the free carrier distributions in the underlying silicon substrate, as it is pulsed through inversion/depletion/accumulation states over time in response to the large signal. This leads to relatively high harmonic distortion at the output of the CPW line.

The introduction of the polysilicon trap-rich layer beneath the BOX of a nominally high resistivity substrate brings reductions of up to 60 dB in the total distortion over

the measured power range [13]. The traps at the Si/SiO_2 interface effectively pin the Fermi-level (E_F) near mid-gap. Contained to a narrow energy range by these traps, the position of E_F is rendered much less voltage-sensitive, improving the linearity of the substrate and reducing the substrate-induced distortion in signals propagating through overlying transmission lines. For this reason, trap-rich (TR) SOI substrates provided by Soitec are also named "eSI™", which stands for "enhanced Signal-Integrity" [1].

In today's market (2019), 300-mm diameter TR wafers are commercially available for the most advanced PD-SOI nodes (180 nm to 45 nm) and are truly optimized with their high linearity (and low losses) for RF applications.

IV. RF Modelling of Silicon Substrates

A. Small-Signal Linear Substrate Modelling

Superimposed on the small-signal measurement curves of Fig. 3 are plotted simulation results for each SOI substrate.

The simulation method is based on an electromagnetic (EM) field solver using Maxwell's equations. Popular EM tools are Momentum ADS from Keysight and HFSS from Ansys. However, to account for semiconductor effect in the silicon volume, a TCAD solver is employed first, in order to determine an accurate electrical description (resistivities) of the semiconductor regions to be defined in the EM solver.

TCAD software solves for semiconductor transport equations, calculating the induced band-bending potential at each finite element substrate node, taking into account oxide charges, traps, and other physical parameters.

The TCAD tool (Atlas from Silvaco in this case) is used first to obtain the resistivity profiles in the silicon volume. An example of such a curve is given in Fig. 2 for the case of the HR substrate suffering from the PSC effect, and the curve is discretized to be used in the EM solver.

The full-wave 3D EM solver is then employed to compute the overall S-parameters. The substrate parameters used in these simulations are based on the resistivity profiles obtained from TCAD (such as those given in Fig. 2). Silicon layers and blocks with various (uniform) resistivity values are placed in the HFSS simulated structure to account for the HR bulk and the PSC region. Their resistivities and thicknesses are determined by the fitting of the discretized curve to the continuous TCAD results (see Fig 2).

B. Large-Signal Non-Linear Substrate Modelling

Large-signal modelling of semiconductor substrates is a challenge at RF frequencies. At lower frequencies, the substrate can be modelled classically as voltage dependent elements C(V) and G(V). Such a modelling approach is valid while the substrate remains in equilibrium. However, if the large signal V varies too fast, the substrate's carriers only have the time to partially respond, and the substrate is always out of equilibrium. This stems from the physical fact that carriers have a finite inertia and response time. This response time depends on a number of material parameters, but for typical HR substrates it is usually longer than 1 ns [12]. This means that for RF frequencies in the RF and mm-wave range, carrier response will seriously lag behind the large-signal, and seriously affect the substrate-induced signal distortion.

As a consequence, the C(V) and G(V) formulation is no longer valid, as the C-V and G-V curves then present a hysteresis, and are no longer injective functions of V. The loss of injectivity poses serious problems for frequency-domain analysis (harmonic balance for example), and time-domain types of large-signal simulations seem unavoidable under these conditions [12].

V. Conclusion

The high-volume production capabilities offered by the silicon industry has motivated the development of RF- PD-SOI and FD-SOI nodes, that are now demonstrating their potential for all kinds of RF and millimeter wave functional blocks towards full SOI front-end module integration.

The success of SOI as an RF platform is due to significant technological improvements made at both the transistor level as well as at the level of the substrate.

At the transistor level, high speed metrics –f_t and f_{max} in the 400 GHz range– and low parasitics are attained by the SOI FET architecture, making SOI a promising technology for 5G and mm-wave applications, while at the same time providing advanced digital processing capabilities on the same technological platform. Furthermore, FD-SOI's ultra-low power capabilities are of significant interest toward RF-IoT types of applications.

Below the BOX, substrate engineering has enabled the development of a range of high-quality silicon-based solutions optimized for RF applications, that guarantee low losses, high isolation and strong linearity, while being manufacturable on a large scale (300 mm diameter wafers).

Overall, SOI is expected to be a big contender as a technological platform to enable mass production of millimeter wave 5G and ultra-low power RF IoT devices and products in the near future.

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