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C-V characterization of the trap-rich layer in a novel Double-BOX structure

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ABSTRACT

A new Double-BOX structure is introduced to explore the electrical properties of the trap-rich layer used to enhance the performance of radio frequency Silicon-on-Insulator substrates. Capacitance-voltage (C-V) measurements reveal anomalous behavior with a "shoulder" emerging in the electron accumulation region and a shift towards negative gate voltage in hysteresis. TCAD simulation shows that these features are related to trap states at the grain boundary in the trap-rich polycrystalline silicon (polysilicon) layer. These traps form a potential barrier and affect the C-V curves. To determine the traps density in polysilicon, a three-element circuit model is used. The effective density of fast traps is evaluated from the corrected C-V curve, while the hysteresis of double-sweep C-V measurement yields the slow traps density at the grain boundary in polysilicon.

1. Introduction

High-resistivity Silicon-on-Insulator (HR-SOI) substrates are massively used for radio frequency (RF) integrated circuits and mixed-signal applications due to their superior performance and low cost. However, a well-known issue arises from the parasitic surface conduction (PSC) effect caused by fixed charges present in the buried oxide layer (BOX) [1–3]. The PSC effect leads to resistivity degradation near the BOX/substrate interface, and thus increases the substrate loss. To solve this problem, a trap-rich layer is introduced beneath the BOX and on top of the high resistivity silicon substrate [1,4]. Typically, this layer is formed with polycrystalline silicon (polysilicon) or amorphous silicon, which effectively captures free carriers and eliminates the formation of parasitic channels at the BOX/substrate interface. In principle, the substrate is thus able to maintain its high nominal resistivity, resulting in reduced losses and improved linearity [1,4].

Nonetheless, partial re-crystallization and impurity contamination of the trap-rich layer, caused by the direct contact with the silicon substrate, may affect the local resistivity and, hence the RF performance. These effects are responsible for a tenfold reduction in effective resistivity and a drastic degradation in linearity [5]. To address these issues, a new structure named double-buried-oxide (D-BOX) trap-rich substrate was proposed by UCLouvain and SOITEC [6]. As shown in Fig. 1, this structure incorporates a second thin buried oxide (BOX2) between the trap-rich layer and the silicon substrate, thereby preventing direct contact between them. The parasitic channel at the substrate/BOX2 interface, caused by fixed charges in the BOX2 layer, can be effectively passivated with the trap-rich layer as long as the BOX2 thickness is thinner than 10 nm [6]. Thus, the high resistivity (>10 kΩ•cm) of the substrate can be maintained. In addition, the D-BOX structure also facilitates the compatibility of the trap-rich interface passivation solution with the fully-depleted (FD) SOI technology nodes.

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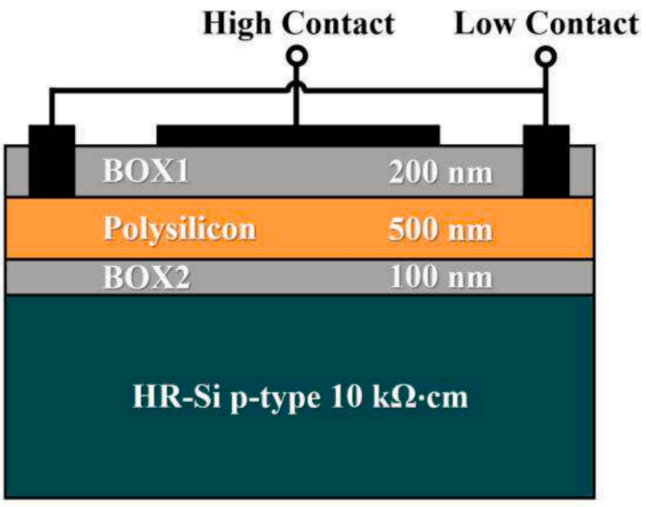

Fig. 1. Cross-section of the trap-rich D-BOX structure.

The presence of the BOX2 layer eliminates significant leakage current that may occur between the ground-planes (doped polysilicon utilized as back-gate) and the HR Si substrate. Consequently, the simultaneous achievement of a back-gate configuration and a high RF performance is attainable.

As we all know, the electrical properties of polysilicon are significantly influenced by the density of traps, as a higher density leads to better RF performance [7]. Therefore, the traps density in polysilicon and at the interfaces is a critical parameter that enhances the RF merits of the substrate. Traps inspection by applying the capacitance–voltage (C-V) method to the standard vertical MOS structure of trap-rich SOI wafers is inappropriate due to depletion layer effects in silicon substrate. This depletion capacitance in series with the trap-rich layer's capacitance makes the traps analysis complex. To address this, we utilized a lateral MOS structure based on the D-BOX structure for the electrical characterization of trap-rich layer at wafer level [8]. This lateral MOS structure eliminates the impact of bulk depletion layer on C-V curves, simplifying analysis and enabling successful characterization.

Preliminary results for the inspection of the polysilicon trap-rich layer in a D-BOX structure using C-V measurements have been exposed in [8]. In this extended paper, we provide additional experimental results (Section 3) and simulations (Section 4) together with an enriched discussion of the methodology for the traps extraction (Section 5). We introduce a TCAD simulation model to explain the anomalous C-V behavior and reveal the impact of traps distributions on C-V response as well as the mechanism behind the negative shift of C-V hysteresis. Subsequently, equivalent RC circuits are developed for different gate biases based on TCAD simulation analysis. To enhance accuracy, a three-element circuit model is utilized to correct the capacitance and conductance measurements. Finally, the effective traps density of the polysilicon layer is evaluated from both C-V hysteresis and corrected C-V curve.

2. Device fabrication and experimental setup

The D-BOX stack (metal/oxide/polysilicon/oxide/silicon, Fig. 1) is fabricated in the clean room facilities at UCLouvain. The process involves the thermal growth of a 100 nm-thick silicon dioxide (BOX2) layer at 900℃ on top of a high-resistivity silicon substrate, followed by the deposition of a 500 nm-thick polysilicon layer through low-pressure chemical-vapor deposition (LPCVD) at 625℃. The capacitive structure is completed with a 200 nm-thick silicon dioxide (BOX1) formed on the polysilicon film by plasma-enhanced chemical-vapor deposition (PECVD). Finally, an aluminum layer is deposited on BOX1 to define the gate and the lateral contacts with the polysilicon film. The polysilicon layer is left undoped, while the silicon substrate is lightly p-doped with a resistivity of 10 kΩ•cm. The area of the metal gate is 8.76 mm^2.

The capacitance is measured at frequencies ranging from 1 kHz to 100 kHz with a Keysight B1500A semiconductor parameter analyzer under dark and at room temperature. The High and Low electrodes are connected to the front gate and the polysilicon, respectively. For C-V hysteresis responses, all the measurements are conducted by sweeping from negative voltage to positive voltages, and then sweeping back. To ensure accurate and reliable results, the hold time and delay time are set to 120 s and 0.1 s, respectively.

3. Experimental results and discussion

Fig. 2 shows typical C-V characteristics of the trap-rich D-BOX structure measured for frequencies ranging from 1 kHz to 100 kHz. The C-V characteristics exhibit anomalies attributed to the substantial density of traps present in polysilicon. Without traps, the C-V curve should have a "V" shape, with the depletion regime occurring at the minimum capacitance value, which aligns with the flat band voltage (V_{FB}). Here, the value of V_{FB} is determined as −6 V due to positive fixed charges in the oxide. Interestingly, a "shoulder" is observed in the electron accumulation region near flat band voltage ($V_{FB} < V_G < 4$ V) for all measured curves. According to $C = \Delta Q/\Delta V$, the lower capacitance in the shoulder regime reflects a reduction of free charge carriers in polysilicon. In other words, a portion of the charge carriers induced by the gate voltage becomes trapped within the slow traps present in polysilicon. The time constants of these slow traps exceed the period of the applied ac signal, thereby impeding the overall capacitance to increase normally with V_G. Moreover, a large frequency dispersion is observed as a result of the large value of series resistance and the time constant dispersion of traps in polysilicon [9].

Fig. 3 illustrates the C-V hysteresis response recorded at 1 kHz. A clear hysteresis effect is observed between forward and reverse gate voltage sweeps. It is well known that the hysteresis effect is caused by the charge trapping and de-trapping in the oxide layer or at the semiconductor-oxide interface. Previous studies have reported a shift towards positive gate voltage due to oxide traps near the interface [10,11]. However, in Fig. 3, a shift towards negative gate voltage is detected. The observed phenomenon can be attributed to a higher density of traps present in polysilicon near the interface compared with the one in the oxide. To further investigate and understand the origin of the C-V "shoulder" and hysteresis, we conducted simulations using TCAD tool (Atlas from Silvaco).

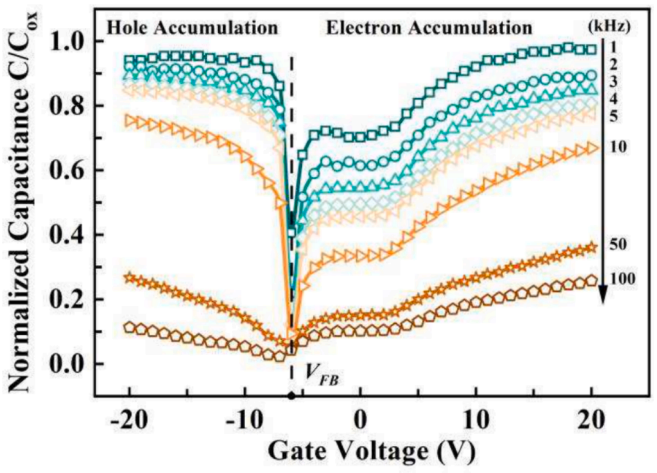

Fig. 2. Measured C-V curves of the trap-rich D-BOX structure for a frequency range from 1 kHz to 100 kHz.

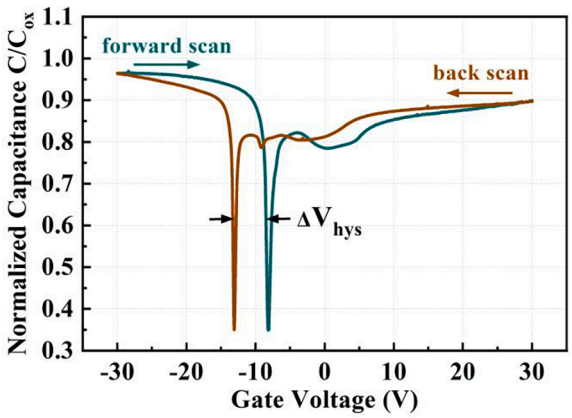

Fig. 3. Measured C-V hysteresis response in trap-rich D-BOX SOI wafer at 1 kHz.

4. TCAD simulations and analysis

In this section, the C-V "shoulder" and hysteresis effect are analyzed through TCAD simulation. Initially, the polysilicon is assumed to be a homogeneous material such as to evaluate the impact of trap-energy distributions on C-V behavior. It is then divided into columnar grains to investigate the influence of grain boundaries on total capacitance and hysteresis behavior.

4.1. "Shoulder" in C-V characteristics

Firstly, the polysilicon is considered as a homogeneous layer with traps uniformly distributed throughout its structure. This simplification allows for easier mathematical modeling and analysis of C-V curves under different conditions.

To further simplify the simulation, we developed a structural model with only half of this structure, as shown in Fig. 4. The thickness of each layer corresponds to that depicted in Fig. 1. A fixed charge density ($N_{BOX1} = 8 \times 10^{11}$ cm^{-2}) is introduced at the BOX1/polysilicon interface. The polysilicon is modeled using a continuum of trap states consisting of donor-like ($g_D(E)$) and/or acceptor-like ($g_A(E)$) states distributed across the energy band gap. The electron and hole mobilities (μ_n and μ_p) in polysilicon are set to 300 cm^2/(V•s) and 30 cm^2/(V•s), respectively, while their lifetimes (τ_n and τ_p) are both equal to 1 ns. These data have been verified in [12].

The simulated C-V curves for a variety of traps distributions in polysilicon are shown in Fig. 5 and Fig. 6, respectively. As depicted in Fig. 5 (a), in the absence of traps in both the BOX1 and polysilicon layers, the C-V curve exhibits a regular "V" shape, as expected, with a V_{FB} value of 0 V. Upon introducing traps within these two layers, the entire curve shifts

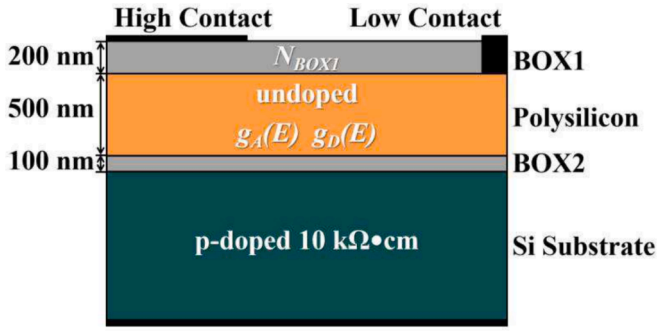

Fig. 4. Cross-section of the device structure used in TCAD simulation. Parameters: $N_{BOX1} = 8 \times 10^{11}$ cm^{-2}, $\mu_n = 300$ cm^2/(V•s), $\mu_p = 30$ cm^2/(V•s), $\tau_n = \tau_p = 1$ ns.

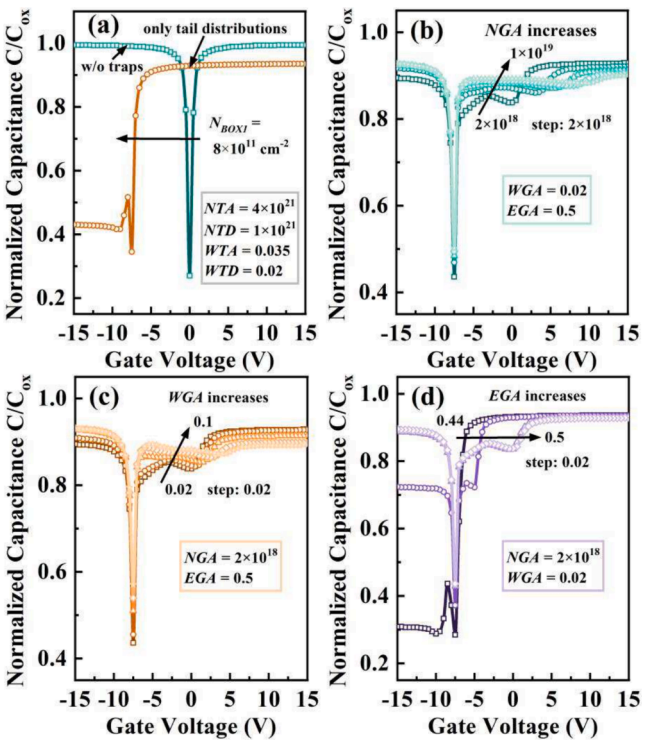

Fig. 5. Simulated C-V curves at 1 kHz for different traps distributions in polysilicon. (a) Only tail distributions with both acceptor-like and donor-like traps, (b) only Gaussian distribution with different acceptor-like traps densities, (c) only Gaussian distribution with different characteristic decay energy values of acceptor-like traps, and (d) only Gaussian distribution with different peak energy values of acceptor-like traps.

towards negative gate voltages. However, the expected "shoulder" in the electron accumulation region is not observed when considering only tail distributions for donor-like and acceptor-like traps (see Fig. 6(a)) in polysilicon. This observation suggests that the presence of a "shoulder" does not originate from shallow traps near the band edges, but rather from deep traps located close to the mid-gap region. For checking that hypothesis, we consider only acceptor-like trap with a Gaussian distribution near the mid-gap, as the "shoulder" is exclusively observed within the electron accumulation region. The formula used to describe a Gaussian distribution for acceptor-like traps in Atlas is given as:

$$g_{GA}(E) = NGA \exp\left[-\left(\frac{EGA - E}{WGA} \right)^2 \right] \quad (1)$$

where *NGA*, *WGA*, and *EGA* are the total density of states, characteristic decay energy, and peak energy of acceptor-like trap, respectively. To study the effect of polysilicon trap states, we vary one individual polysilicon trap state parameter while keeping the others constant. The simulation results are reproduced in Fig. 5(b)–(d); the corresponding trap profiles are indicated in Fig. 6(b)–(d). It can be seen that the introduction of deep traps leads to the emergence of a distinct "shoulder" in the electron accumulation region. Notably, the characteristics of this "shoulder" exhibit variations corresponding to the distribution patterns of deep trap states. Increased values of *NGA*, *WGA*, and *EGA*, indicating a broader and deeper distribution of a higher density of deep trap states, result in an augmentation and lateral extension of the "shoulder" capacitance. We can conclude that the "shoulder" is a signature of a large density of acceptor-like trap states located near the mid-gap. These deep traps exhibit longer time constants compared with shallow trap states.

We now consider a more realistic scenario where the polysilicon is composed of a multitude of grains. Previous research [13] has indicated

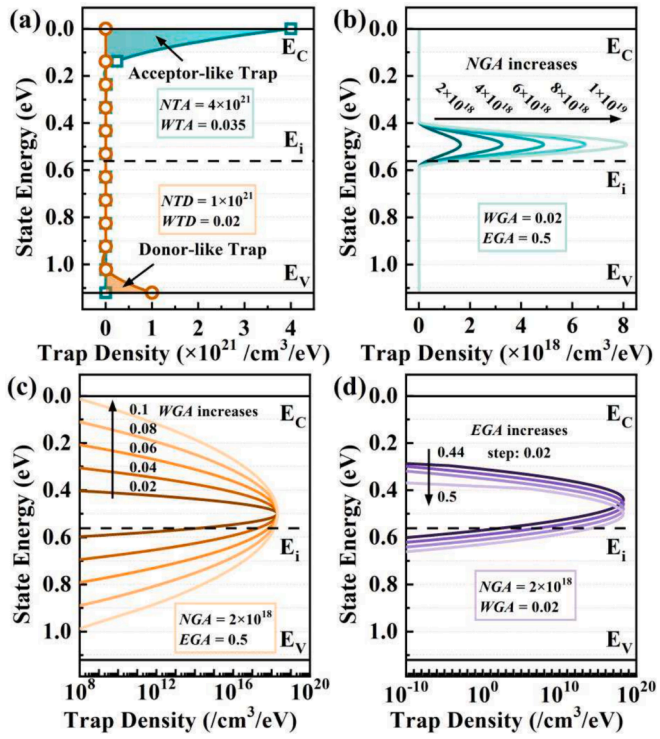

Fig. 6. Traps distributions in polysilicon assumed to compute Fig. 5. (a) Only tail distributions with both acceptor-like and donor-like traps similar to those reported in [5], (b) only Gaussian distribution with different acceptor-like traps densities, (c) only Gaussian distribution with different characteristic decay energy values of acceptor-like traps, and (d) only Gaussian distribution with different peak energy values of acceptor-like traps.

that there are minimal trap states within the grains themselves, while a high density of traps exists at both oxide interfaces and grain boundaries. The scanning electron microscopy (SEM) image presented in Fig. 7, as well as in [14], illustrates a columnar grain structure with grain boundaries nearly parallel to the growth direction. Additionally, we can also observe the presence of small grains near the bottom polysilicon/BOX2 interface, which gradually enlarge when approaching to the polysilicon/BOX1 interface. Since the C-V measurement in this paper only characterizes the trap states near the polysilicon/BOX1 interface, henceforth, the influence of these small grains can be ignored.

It follows that the polysilicon layer in D-BOX structure can be described by a model consisting of multiple columnar grains, as shown in Fig. 8(a). In this model, traps are only located near the front/back interfaces and along the grain boundaries, while the volume of the grain is considered to be intrinsic monocrystalline silicon. A similar structure model of polysilicon film has been proposed in the literature [13]. This model is implemented in TCAD simulation to analyze the influence of grain boundaries on the observed "shoulder" phenomenon in C-V curves, as depicted in Fig. 8(b). To simplify the simulation, only vertical grain boundaries are taken into consideration; indeed, no "shoulder" is observed when there is solely trap states near the front interface. According to [15,16], the distribution of trap states at the grain boundary includes both exponential tail and Gaussian distributions for acceptor-like and donor-like trap states.

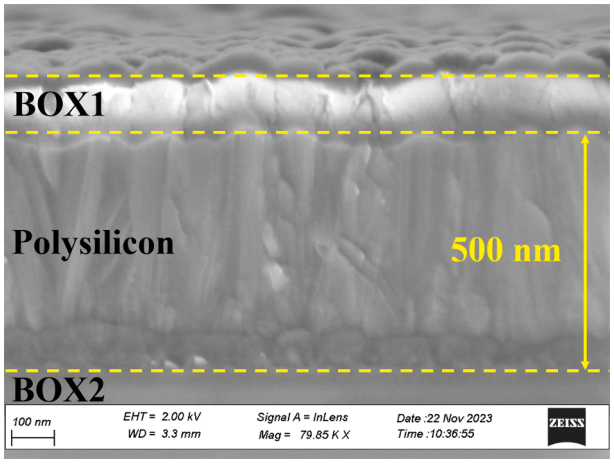

Fig. 7. SEM image of the D-BOX structure.

The simulated C-V curve is presented in Fig. 9(a), exhibiting good agreement with the experiment. In the absence of a positive oxide charge, V_{FB} is shifted back to 0 V. To gain deeper insight into the impact of vertical grain boundaries on C-V behavior, Fig. 9(b)–(f) depict the energy band diagrams and the equivalent RC circuits of the polysilicon layer for distinct gate biases. The gate controls the carrier density in the grains under the "High Contact", resulting in the modulation of the grain boundary barrier height, and consequently affecting the total capacitance. The key bias points identified in Fig. 9(a) are described next.

Point (b) – At high negative bias (V_G = -15 V, Fig. 9(b)), holes are accumulated under the gate ("High Contact"). Since the polysilicon also features a p-type behavior at the grain boundary [15,17,18], the region nearby is in accumulation or in weak depletion mode with negligible contribution. The total capacitance is the oxide capacitance C_{ox} in series with the interface trap capacitance C_{it}.

Point (c) – At V_G = 0 V (Fig. 9(c)), the polysilicon underneath the gate is fully depleted. The depletion capacitance (C_{dep}) in series with C_{ox} leads to the decrease of the total capacitance to a minimum value.

Point (d) – At V_G = +1 V (Fig. 9(d)), electrons start accumulating under the gate. Given the p-type behavior of the grain boundary, a depletion region with capacitance C_{gb} forms at the grain boundary. The existence of C_{gb} explains the smaller value of the total capacitance compared with that measured for hole accumulation (V_G = -15 V). This is why a "shoulder" appears on the C-V curve.

Point (e) – At higher positive voltage (V_G = +4 V, Fig. 9(e)), the surface concentration of electrons increases and causes the depletion region at the grain boundary to shrink. The values of C_{gb} and total capacitance are expected to increase, but instead both experiments and simulations indicate a reduced (or constant) value of the total capacitance. This can be attributed to the expansion of the electron

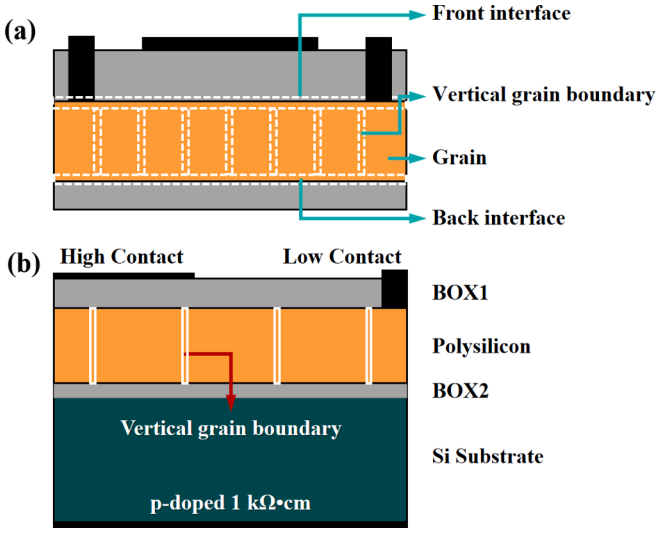

Fig. 8. (a) Structure model of the polysilicon film with oxide interfaces and grain boundaries; (b) Cross-section of the simplified half-structure used in TCAD simulation.

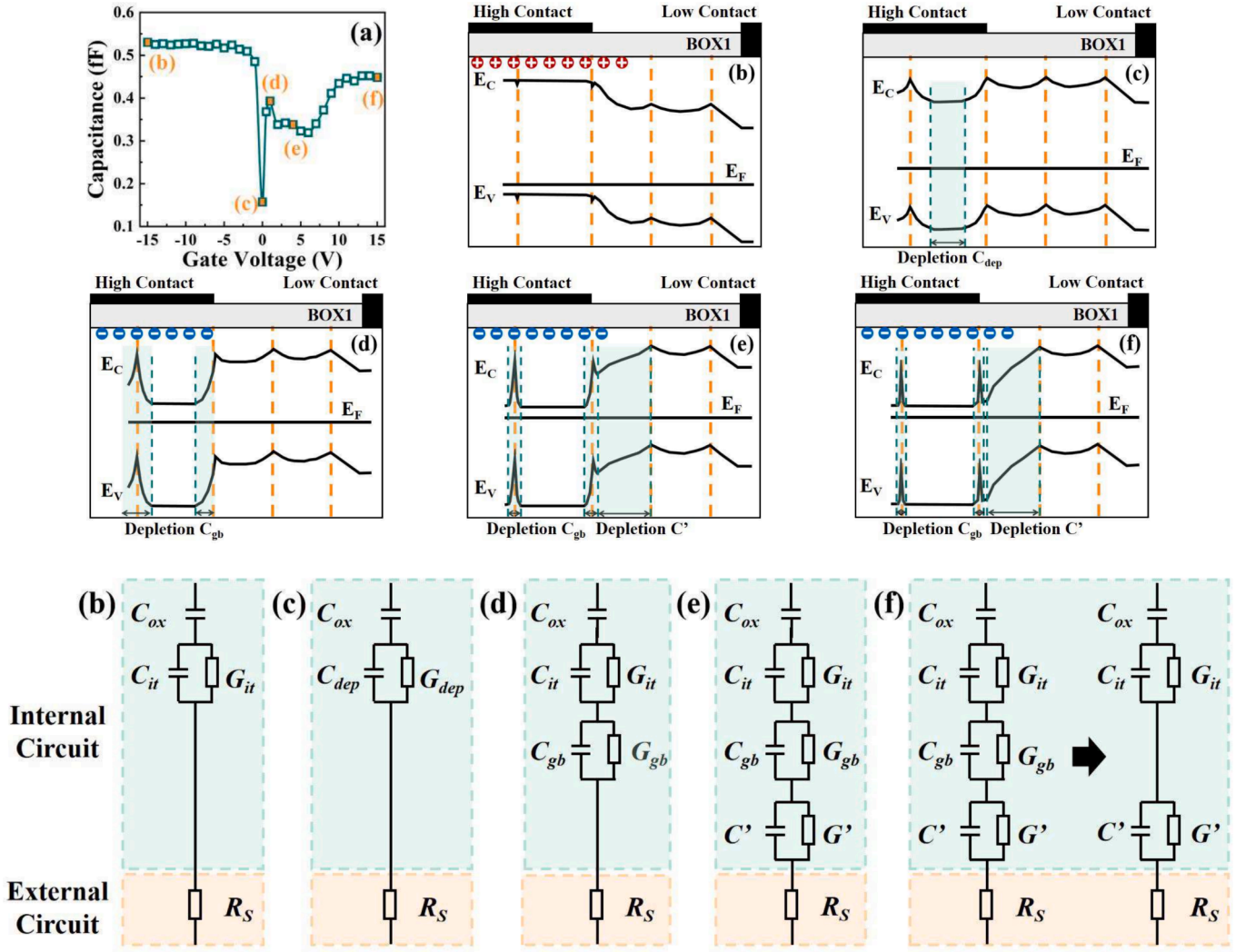

Fig. 9. (a) Simulated C-V curve at 1 kHz. Energy band diagrams and equivalent RC circuits of the polysilicon layer for (b) V_G = -15 V, (c) 0 V, (d) 1 V, (e) 4 V, and (f) 15 V. C_{ox} is the capacitance of BOX1. C_{it} and G_{it} are the capacitance and conductance of the interface traps, respectively. R_S is the series resistance. C_{dep} and G_{dep} are the total capacitance and conductance of the depletion region in polysilicon under the "High Contact", respectively. C_{gb} and G_{gb} are the total capacitance and conductance of the depletion region formed at the grain boundary. C' and G' are the capacitance and conductance of the additional depletion region near the edge of "High Contact".

accumulation layer caused by the intensified electric field from the gate, which in turn enlarges the depletion width.

Point (f) – At $V_G = +15$ V (Fig. 9(f)), the depletion width is further reduced, leading to a higher total capacitance. When the depletion width at the grain boundary becomes small enough, the contribution of C_{gb} can be ignored and the equivalent RC circuit is simpler.

In summary, the traps around the mid-gap affect the C-V characteristics, leading to a "shoulder" revealed in experiments. These deep traps, mainly located at the grain boundary, create a potential barrier and subsequently influence the overall capacitance.

4.2. C-V hysteresis effect

It is well documented that the presence of oxide traps near the interface typically results in a shift of the C-V curve towards positive gate voltages [10,11]. Hence, the occurrence of an unusual negative shift in the C-V curve is likely to originate from a high density of traps located within the polysilicon near the front interface, which we refer to as parallel grain boundary here. The impact of this parallel grain boundary on C-V hysteresis is investigated using energy band diagrams at different gate biases, as depicted in Fig. 10. Consistent with our previous model, the trap states are assumed to be located only at the parallel grain boundary.

- *Forward scan* (see Fig. 10(a)): Under negative gate bias, an accumulation of holes occurs at the front interface, leading to a hole trapping process where trap states capture the holes. This results in a shift of the Fermi level at the parallel grain boundary (E_{FB}) towards the valence band (E_V), causing band bending towards the conduction band (E_C) at the front interface and consequently inducing a positive shift in the C-V curve.
- *Back scan* (see Fig. 10(b)): Under positive gate bias, electrons accumulate at the front interface, triggering the release of the trapped holes (referred to as hole de-trapping process) and resulting in a shift of the Fermi level towards E_C in the parallel grain boundary. Consequently, this leads to a band bending towards E_V at the front interface, causing a negative shift in the C-V curve.

We conclude that the trapping/de-trapping of carriers along the parallel grain boundary changes the potential barrier at the front interface and leads to a negative shift of C-V curve. The traps density at the parallel grain boundary is much larger than that in the oxide near the

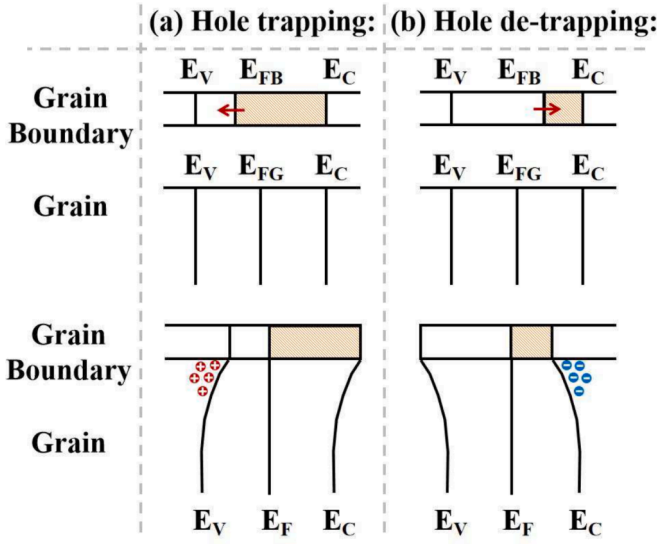

Fig. 10. Energy band structures in polysilicon at the front interface under different gate biases.

front interface. Thus, it is primarily the trap states located within the parallel grain boundaries that dictate the direction of the C-V shift.

To validate the theoretical assumptions mentioned above, a 5 nm-thick polysilicon region with a high traps density is implemented at the front interface in the simulation. Since the Heiman's model in Silvaco is exclusively used for simulating the hysteresis induced by insulator traps, we introduced p- and n-type doping in the parallel grain boundary to mimic changes in Fermi level caused by trapping and de-trapping processes. Here, the p- and n-type doping correspond to the hole trapping and de-trapping, respectively. The simulation results in Fig. 11 confirm a shift of the C-V curve towards negative gate voltage, which is in agreement with the experimental findings.

5. Traps extraction method and results

In this section, we describe two methods for experimentally estimating the traps density in polysilicon.

Firstly, the hysteresis effect serves to evaluate the deep traps density at the grain boundaries. The hysteresis and shift in C-V characteristics are related to changes in traps occupancy near the interface. These changes depend on both the magnitude of the applied gate voltage and the direction of gate voltage sweep [11]. The larger the magnitude of the applied gate voltage, the more pronounced the alterations in traps occupancy. Our experiments indicate that the shift in C-V characteristics saturates when gate voltages exceed 25 V. The deep traps density is calculated from the shift ΔV_{hys} of the C-V characteristics using the relationship, $\Delta N_{dt} = C_{ox} \times \Delta V_{hys}/q$, where ΔN_{dt} is the deep traps density. Since the traps in the parallel grain boundaries dominate the hysteresis effect, the deep traps density is estimated to be $\Delta N_{dt} \approx 5.4 \times 10^{11}$ $cm^{-2}\bullet eV^{-1}$ ($\Delta V_{hys} = 5.6$ V in Fig. 3).

Secondly, the proposed equivalent RC circuit model in Fig. 9 is used to calculate the traps density in polysilicon. To ensure more accurate capacitance and conductance characteristics of the device, it is necessary to de-embed the series resistance R_S caused by high-resistivity polysilicon between two contacts from measurement data. Here, we use a three-element circuit model to correct the C-V curve, as shown in Fig. 12. Fig. 12(a) gives the two-element parallel circuit model serving for typical admittance characterization, where C_m and G_m are, respectively, the measured capacitance and conductance. Fig. 12(b) presents the three-element circuit model with C_c and G_c being the corrected capacitance and conductance, respectively. By equating the real part of the total impedance in Fig. 12(a) and (b), we obtain:

$$\frac{G_m}{G_m^2 + (\omega C_m)^2} = \frac{G_C}{G_C^2 + (\omega C_C)^2} + R_S \tag{2}$$

where ω is the angular frequency. With $D = G/\omega$, Equation (2) can be rewritten as:

$$\frac{D_m}{\omega(D_m^2 + C_m^2)} = \frac{D_C}{D_C^2 + C_C^2} \times \left(\frac{1}{\omega}\right) + R_S \tag{3}$$

Fig. 13 shows the variation of $D_m/[\omega(D_m^2 + C_m^2)]$ with the reciprocal frequency $1/\omega$. The intercept with the Y-axis yields the value of the series resistance R_S. However, due to the potential barrier formed at the grain boundary under the "High Contact", the value of R_S changes with gate bias and frequency. In hole accumulation region (at high negative V_G), the potential barrier is low or even completely vanished. Thus, the plot in Fig. 13(a) is linear as a function of $1/\omega$, which means that the value of R_S is independent on frequency and can safely be extracted from the intercept with the Y-axis. In electron accumulation region, the potential barrier is high at the grain boundary and alters the total R_S: the plot in Fig. 13(b) is no longer a linear function of $1/\omega$. The value of R_S depends on frequency and is determined by the intercept of the tangent line with the Y-axis.

Fig. 14 shows the bias-dependent series resistance at 1 kHz. During hole accumulation, R_S is nearly constant (4 kΩ). The peak point corresponds to a maximum barrier width at the grain boundary. As the gate bias increases, the width of the barrier region decreases and so does the value of R_S. It is worth noting that this curve exhibits a similar pattern to the effective resistivity measured in a trap-rich substrate [4].

After eliminating the contribution of R_S, we obtain corrected capacitance C_C and conductance G_C curves. The classical equivalent

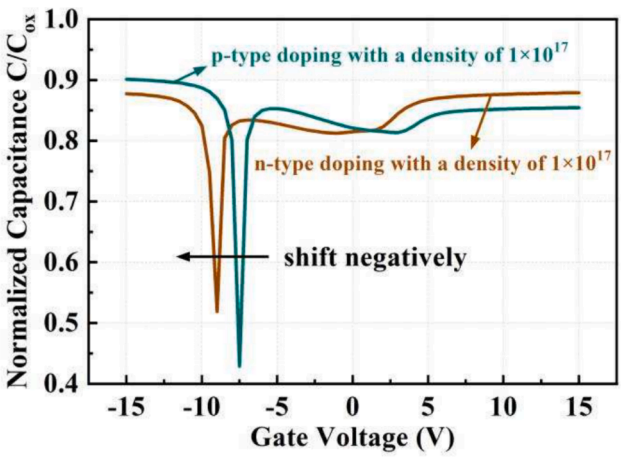

Fig. 11. Simulation results of the C-V hysteresis in polysilicon due to the influence of the parallel grain boundaries.

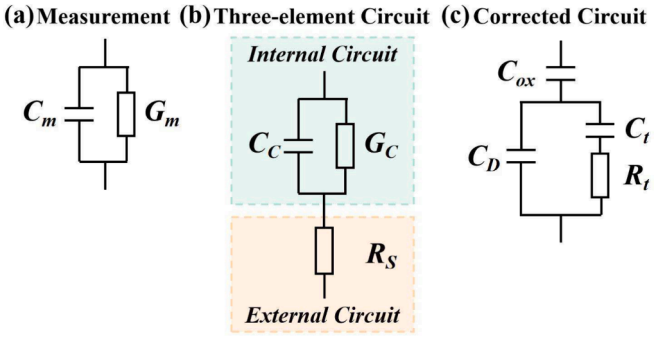

Fig. 12. Small-signal equivalent circuit models of MOS capacitors: (a) parallel circuit model, (b) three-element circuit model, and (c) series RC model.

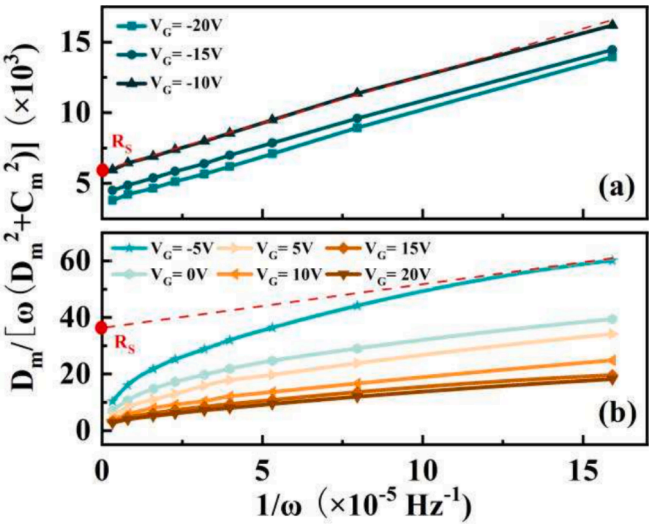

Fig. 13. Variation of $D_m/[\omega(D_m^2 + C_m^2)]$ as a function of $1/\omega$ to extract the series resistance R_S. (a) Hole accumulation at high negative gate voltage, (b) depletion or electron accumulation.

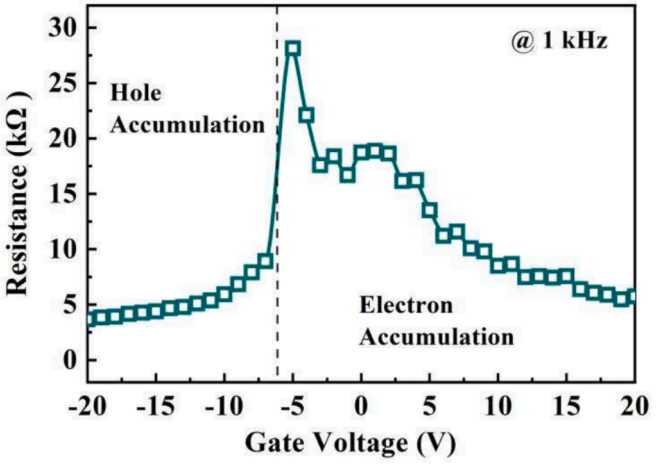

Fig. 14. Series resistance R_S extracted from measurements as a function of gate bias at 1 kHz.

circuit for the MOS capacitor (Fig. 12(c)) [19,20] is used to determine the effective traps density in polysilicon. Here, C_D is the depletion layer capacitance while C_t and R_t form the series RC network of the effective trap states in polysilicon, including interface traps and grain boundary traps. Since the oxide capacitance C_{ox} is known from the geometry of the capacitor and C_D is negligible in hole/electron accumulation region, the numerical values for C_t and R_t can be extracted. The trap capacitance is converted to traps density by dividing by the electronic charge and the capacitor area. Fig. 15 shows the calculated effective traps densities in polysilicon as a function of gate bias for a frequency range from 1 kHz to 5 kHz. It has been observed that the defect states in polysilicon have a U-shaped distribution with shallow exponential tail states near the conduction/valence band and deep states in the form of narrow peak near the mid-gap. Similar defect states distribution in polysilicon was reported in [9] and [15]. In addition, a frequency dispersion is obvious over the whole range of V_G, which points on a wide distribution of time constants at the Fermi level in polysilicon. This means that the trap states at a given surface potential have multiple time constants. It follows that the traps concentration computed with a single RC series circuit represents the average of all the states with their various time constants. Lower frequency measurements would make all the trap states respond to the ac signal.

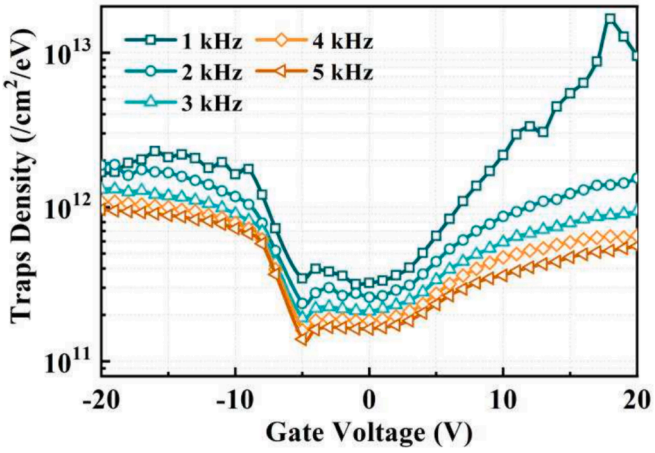

Fig. 15. Effective traps densities in polysilicon as a function of gate bias for a frequency range from 1 kHz to 5 kHz. These curves are derived from measurements using Eq. (3).

6. Conclusions

The D-BOX structure offers a simple and straightforward characterization approach for evaluating the quality of trap-rich layers at the wafer-level without involving complex device fabrication processes. An original methodology is proposed for D-BOX SOI to characterize the traps density in the trap-rich layer using the C-V method. Unusual C-V behavior, including the emergence of a "shoulder" in the electron accumulation region and a shift towards negative gate voltage in hysteresis, is observed in undoped polysilicon MOS structure. To clarify these phenomena, TCAD simulation models are developed considering both vertical and parallel grain boundaries. Our results demonstrate that the "shoulder" is caused by the potential barrier formed at the vertical polysilicon grain boundaries, leading to a decrease in total capacitance. Additionally, we find that the negative shift in hysteresis is attributed to trapping/de-trapping processes occurring in deep trap states located at parallel grain boundaries, which alter the potential barrier at the front interface.

To determine the traps density in polysilicon, two methods are employed in this study. Firstly, the C-V hysteresis window indicates that the deep traps density within grain boundary is approximately 5.4×10^{11} $cm^{-2}\bullet eV^{-1}$. Secondly, we develop a three-element circuit model to correct capacitance and conductance measurements by accounting for the high series resistance in undoped polysilicon. This correction helps recovering the true material properties from measured C-V curves and obtaining the effective density and energy distribution of traps.

However, it is noted that these two methods yield results representing trap states with different time constants. Since our measurements were performed at frequencies above 1 kHz, RC equivalent circuit analysis can only determine fast-trap states densities but cannot reveal traps with much longer time constants [21]. In contrast, the C-V hysteresis method only captures the density of slow trap states with response times comparable to or greater than the C-V measurement time [22].

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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