CHAPTER 3

RF MODELING AND CHARACTERIZATION OF SUB-MICRON MOSFET

3.1 Introduction

The evolution of CMOS technologies in the microwave domain has required to develop specific characterization techniques. Methods have been developed to determine a correct model of transistors, based on the measurement of their true S-parameters.

Models for high frequency transistors are basically of two kinds:

- Polynomial models: They are obtain easily from measurement. They described the behavior of devices, as black boxes. They can be easily introduced in simulators. But no information about the device physic can be deduced from these models.

- Physical small signal equivalent circuits: These circuits are usually close to the device physic. The circuit elements have a known origin. But they are not easily extracted from the S-parameters.

Along this chapter, techniques used to extract physical equivalent circuits of MOSFETs are presented. They are using transistor measurements at different bias to extract all the elements of its equivalent circuit, and they are called “direct extraction techniques”.

The knowledge of the equivalent circuit elements is interesting to develop circuit design methodologies, or to determine which parameters have strong influences on the performances of MOSFETs.

In the following sections, a general equivalent circuit of MOSFET transistor is presented. It is created based on the device physics, and its 3D structure.

Then various techniques are presented to extract the physical equivalent circuit of sub-micron SOI MOSFET transistors.

3.2 Small signal model of integrated SOI MOSFET

One of the advantages of SOI transistors compared to bulk device, is that at microwave frequency, the substrate does not influence significantly the behavior of transistors. Thanks to the thickness of the buried oxide, the body effect can be neglected at high frequency [1]. There is no significant parasitic effects related to the substrate occurring at microwave frequency. Then it is not necessary to develop a four terminal model for the SOI transistor used at microwave frequency.

In the next sections, a general equivalent circuit of SOI MOSFETs is built, taking into account its intrinsic behavior and its physical structure.

3.2.1 Useful effect

The useful effect of a MOSFET is its ability to control its output current (I_{ds}) when a voltage is applied to the gate (V_{gs}). This behavior can be easily modeled using a voltage controlled current source connected between the device source and drain. The gate voltage will be applied between the gate and the source. A preliminary equivalent circuit, modeling the useful effect of the device, can then be drawn (Figure 3.1). The transconductance (g_{m_i}) is qualified as *intrinsic* element, because it is a simple representation of the physical phenomenon, that occurs inside of the transistor channel. The transconductance is defined as follow

$$g_{m_i} = \frac{\partial i_{ds}}{\partial v_{gs}}\Big|_{v_d=v_s=0} \tag{3.1}$$

where i_{ds} is the small variation of the drain current when a small variation of potential (v_{gs}) is applied to the gate. The sub-index “i” means that it is an intrinsic element.

Even if it denotes the useful effect of the MOSFET, the equivalent circuit of Figure 3.1 is not efficent enough to describe the behavior of the device if the

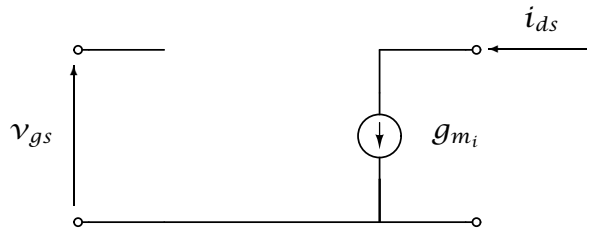


Figure 3.1: Modeling of the useful effect of a MOSFET.

operating frequency is raised, as no parasitic elements are taken into account.

3.2.2 Quasi-static model

Because of transistors physics, there are influencies from each device terminals on the others. These influences can be modeled by capacitances added in the equivalent circuit (Figure 3.2). As explained in [2], all these components are bias dependent and are related to variations of charges or currents when a small signal is applied around equilibrium on a terminal. The capacitances between the source, drain and gate are defined by

$$C_{gd_i} = -\frac{\partial q_g}{\partial v_d}\Big|_{v_s=v_g=0} \quad C_{dg_i} = -\frac{\partial q_d}{\partial v_g}\Big|_{v_s=v_d=0} \tag{3.2}$$

$$C_{gs_i} = -\frac{\partial q_g}{\partial v_s}\Big|_{v_d=v_g=0} \quad C_{sg_i} = -\frac{\partial q_s}{\partial v_g}\Big|_{v_s=v_d=0} \tag{3.3}$$

$$C_{ds_i} = -\frac{\partial q_d}{\partial v_s}\Big|_{v_d=v_g=0} \quad C_{sd_i} = -\frac{\partial q_s}{\partial v_d}\Big|_{v_s=v_g=0} \tag{3.4}$$

These relations can be used only in quasi-static operation. The applied small signal is varying sufficiently slowly such as the charges respond instantaneously to the applied signal.

Moreover, MOSFETs being inperfect current sources, an output conductance must be added in the model. It is defined by

$$g_{ds_i} = \frac{\partial i_{ds}}{\partial v_{ds}}\Big|_{v_g=v_s=0} \tag{3.5}$$

The capacitances are not linked to any physical capacitor-like structure. They are representations of the influence of a voltage applied on a terminal

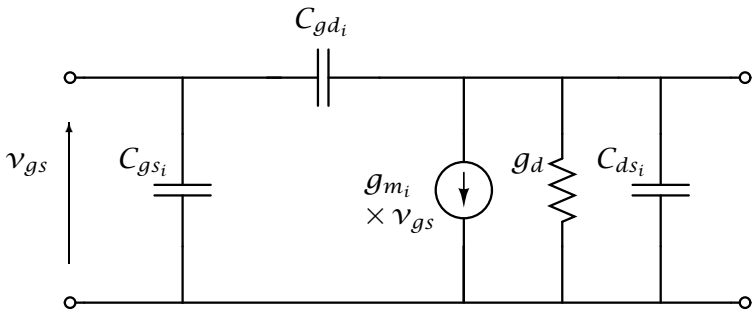


Figure 3.2: Intrinsic quasi-static model of a MOSFET.

on the charges being at another, with regards to the MOSFET physic. They are called *intrinsic* capacitances.

These intrinsic capacitances may not be reciprocal. Indeed, considering an ideal MOSFET in saturation, any variation of the drain voltage will not introduce any variation of the output current and of the gate charges because of pinch off. Hence the drain to gate capacitance must be equal to zero. But if the gate voltage is changed, a variation of the current will occur, inducing a variation of drain charges. The gate to drain capacitance will then be higher than zero, and is different than the drain to gate capacitance.

This non-reciprocal effect can be modeled adding a parasitic element to the transconductance, defining a new one. The new "effective" transconductance (g'_{m_i}) can be defined by

$$\begin{aligned} g'_{m_i} &= g_{m_i} - j\omega C_{m_i} \\ \text{where } C_{m_i} &= C_{dg_i} - C_{gd_i} \end{aligned} \tag{3.6}$$

Usually the non-reciprocity of capacitances is neglected when the device is studied at microwave frequency. It is not necessary to take it into account to model correctly MOSFET transistors up to several tens of GHz. But recently, some authors [3] proposed a method to extract non-reciprocal capacitances for bulk MOSFET using measurement up to 10 GHz and a extremely simplified equivalent circuit.

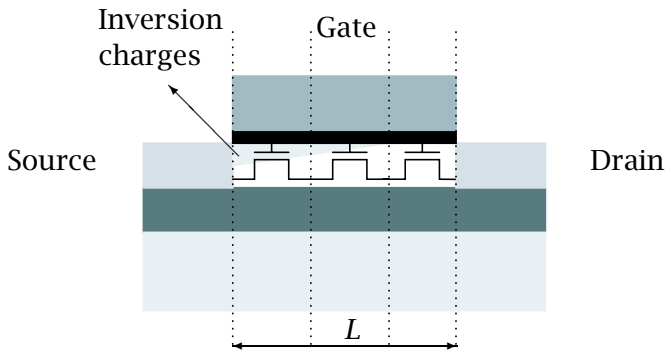


Figure 3.3: Non-quasi-static modeling of a MOSFET using several quasi-static transistors connected together

3.2.3 Non-quasi-static model

In the previous section, an equivalent circuit of MOSFETs has been presented, considering that charges respond without delay to the applied signal. But when the frequency becomes higher, the charges are not able to follow the signal instantaneously. This phenomenon can be observed more easily for long devices. According to TSIVIDIS, the upper limit of the quasi-static model is proportional to $1/L^2$, L being the channel length of the transistor [2] (Figure 3.3).

To model the non-quasi-static effects, the MOSFET channel can be divided into several small transistors connected together as presented in Figure 3.3. Then, quasi-static models are used for all sub-transistors. This solution is used when the values of different intrinsic elements are obtained using formulae from physical model. If they must be extracted from measurement, this method cannot be used, because the number of unknowns increases drastically.

Instead of dividing the MOSFET into several small transistors, the non-quasi-static effects can be modeled by introducing new elements in the equivalent circuit (Figure 3.4) [2]. These elements introduce a delay between the signal and its effects. They are of two kinds: intrinsic resistances (R_{gd_i}, R_{gs_i}) that are in series with intrinsic capacitances, and a time delay (τ) affecting the transconductance. The command of the voltage controlled current source is still the potential "v" applied to the intrinsic capacitance C_{gs_i}.

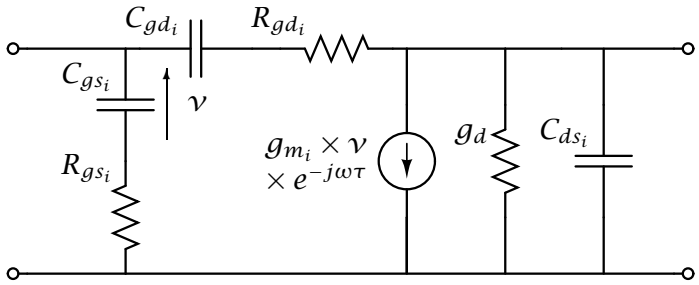


Figure 3.4: Intrinsic non-quasi-static model of a MOSFET

The Y-matrix of the new equivalent circuit of Figure 3.4 is given by

$$Y_i = \begin{bmatrix} j\omega\left(\frac{C_{gs_i}}{1+j\omega R_{gs_i}C_{gs_i}} + \frac{C_{gd_i}}{1+j\omega R_{gd_i}C_{gd_i}}\right) & -j\omega\frac{C_{gd_i}}{1+j\omega R_{gd_i}C_{gd_i}} \\ \frac{g_{m_i}e^{j\omega\tau}}{1+j\omega R_{gs_i}C_{gs_i}} - j\omega\frac{C_{gd_i}}{1+j\omega R_{gd_i}C_{gd_i}} & g_d + j\omega\left(C_{sd_i} + \frac{C_{gd_i}}{1+j\omega R_{gd_i}C_{gd_i}}\right) \end{bmatrix} \quad (3.7)$$

3.2.4 Extrinsic model and access elements

In the previous sections, equivalent circuits have been defined only considering the physical properties of the MOSFET channel. They were composed of several intrinsic elements which depend on the device dimension and on the applied bias. But, the physical structure of the MOSFET is more complex. Because of its geometry, some parasitic elements are surrounding the active part of the device. And they are mainly bias independent.

In the following paragraphs, these parasitic elements are described. They will be defined from the closest to the intrinsic to the furthest, filling the gap between the intrinsic part of the device and the reference planes defined by the calibration. It would lead to an astonishing and extremely complex equivalent circuit, which could be simplified depending on the device layout.

3.2.4.1 Extrinsic capacitances

Several parasitic capacitances are located around the channel of the transistors as presented in Figure 3.5. They are bias indepedent, and proportional to the

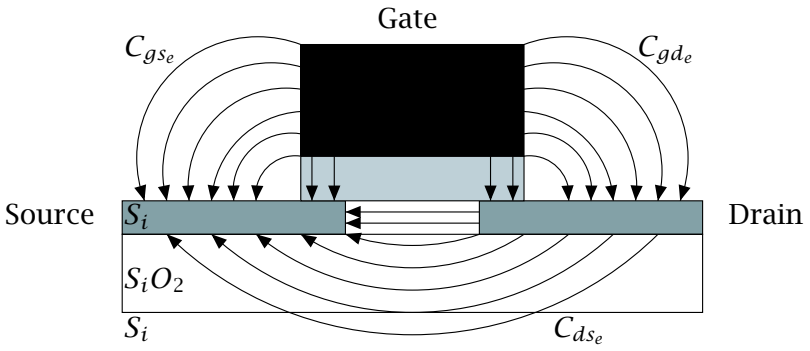


Figure 3.5: Location of the extrinsic capacitances in the physical structure of the MOSFET

transistor width. They are named *extrinsic* capacitances and noted with an index "e".

The extrinsic gate to source (C_{gs_e}) and gate to drain (C_{gd_e}) capacitances are composed of two different elements. They include overlap capacitances, located between the gate oxide and the diffusion of the source and the drain under the gate, and fringing capacitances from the gate sides to the source and drain implants.

The capacitance C_{ds_e} is completely different from the two other extrinsic capacitances. It is the expression of the coupling between source and drain through the film of silicon, the buried oxide, and the substrate. The capacitance C_{ds_e} is the simple high frequency model of a complex capacitive network.

The extrinsic capacitances are added to the previous equivalent circuit. A new one is obtained (Figure 3.6). Its Y-matrix is given by

$$\mathsf{Y}_\pi = \mathsf{Y}_\mathsf{i} + \mathsf{Y}_\mathsf{e} \tag{3.8}$$

$$\text{where } \mathsf{Y}_\mathsf{e} = \begin{bmatrix} j\omega(C_{gd_e} + C_{gs_e}) & -j\omega C_{gd_e} \\ -j\omega C_{gd_e} & j\omega(C_{ds_e} + C_{gs_e}) \end{bmatrix} \tag{3.9}$$

3.2.4.2 Extrinsic resistances and inductances

The intrinsic gate, source and drain are connected to the "outside world" by gate, source and drain fingers. These fingers having a given resistivity, they are

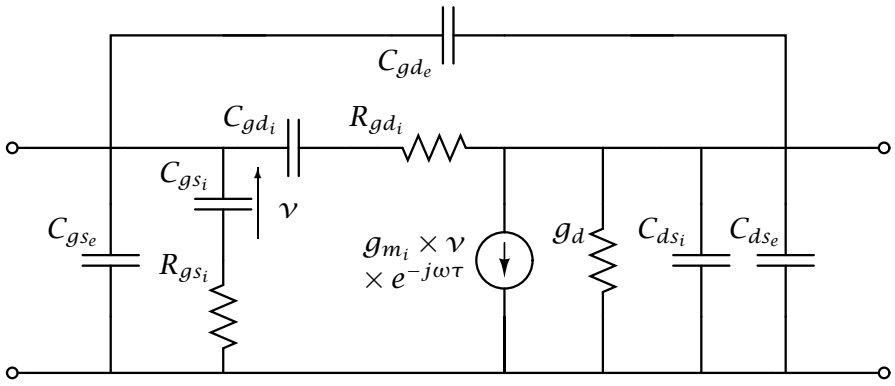


Figure 3.6: Intrinsic model of a MOSFET with extrinsic capacitances

distributed resistances (Figure 3.7).

These distributed elements are modeled by using lumped resistances called R_{g_e} , R_{s_e} and R_{d_e} , since the transistor is generally small compared to the wave length. They are connected to the gate, the source, and the drain respectively.

The resistances R_{d_e} and R_{s_e} include the metallic losses and the contact resistances between the metal and the source and drain implants. They are proportional to the inverse of the transistor width. The resistance R_{g_e} includes the resistance of the gate fingers, which is proportional to the transistor width, and the resistance of some metallic lines. These lines connect the gate fingers together and to the reference plane. In most of the cases, the resistance of the gate finger is much higher than the others. It is usually considered as the only contribution to the extrinsic gate resistance R_{g_e} .

Using the same approach, parasitic inductances can be defined. They are called L_{g_e} , L_{d_e} and L_{s_e} . But, nowadays, for sub-micron MOSFETs, these inductances are usually a few pico-Henry and are nearly negligible within the frequency band of operation.

The equivalent circuit including these extrinsic elements are presented in Figure 3.8. The Z-matrix of this circuit is defined by

$$\mathsf{Z}_\Sigma = \mathsf{Z}_e + \mathsf{Y}_\pi^{-1} \tag{3.10}$$

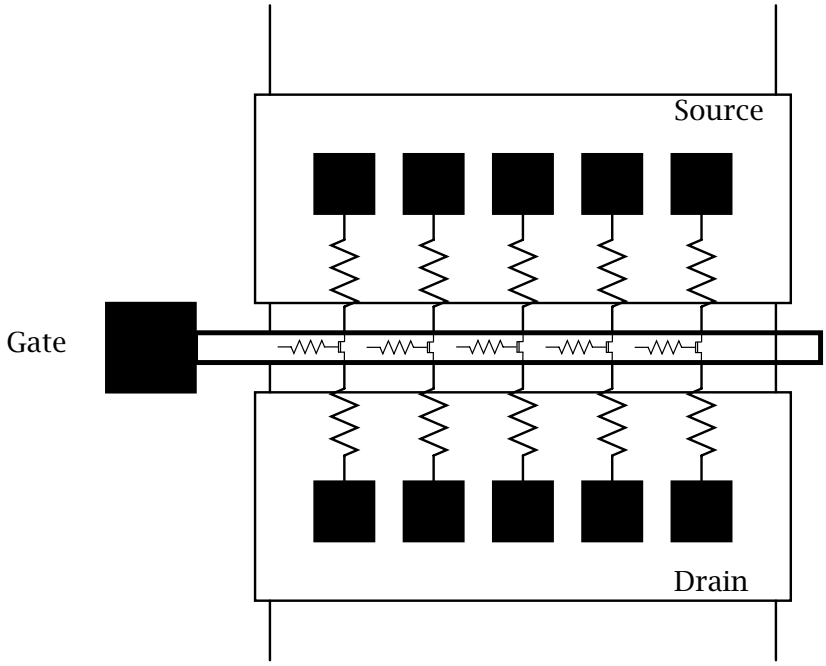


Figure 3.7: Distributed resistances along the fingers in the physical structure of a MOSFET

$$\text{where } \mathsf{Z}_e = \begin{bmatrix} R_{g_e} + R_{s_e} + j\omega\left(L_{g_e} + L_{s_e}\right) & R_{s_e} + j\omega L_{g_e} \\ R_{s_e} + j\omega L_{g_e} & R_{d_e} + R_{s_e} + j\omega\left(L_{d_e} + L_{s_e}\right) \end{bmatrix} \tag{3.11}$$

3.2.4.3 Extrinsic-Extrinsic capacitances

Since the dimensions of MOSFETs are shrinking, some parasitic couplings, which were negligible for larger devices, cannot be longer neglected. Considering the structure of modern MOSFETs presented in Figure 3.9, GOFFIOUL [4] has proposed to model the coupling between metal lines outside the active zone by new capacitances. These capacitances ($C_{gs_{ee}}$, $C_{gd_{ee}}$, and $C_{ds_{ee}}$) are connected directly between the three terminals of the previous equivalent circuit (Figure 3.10). Since they are bias independent and proportional to the transistor width, they are called “extrinsic-extrinsic” and noted by the index “ee” (Figure 3.10).

The Y-matrix of the new circuit is defined by

$$\mathsf{Y}_\Pi = \mathsf{Z}_\Sigma^{-1} + \mathsf{Y}_{ee} \tag{3.12}$$

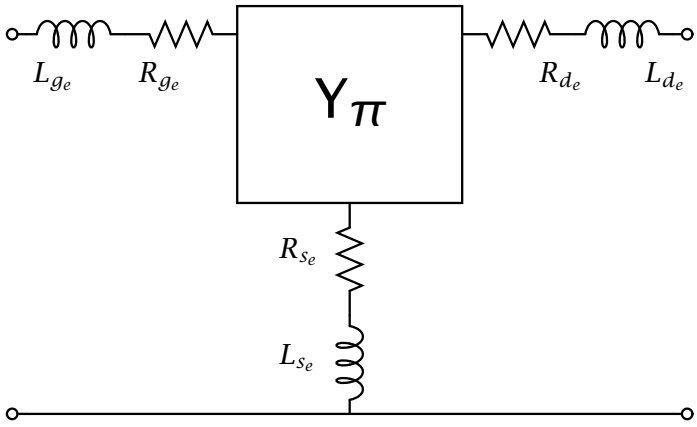


Figure 3.8: Equivalent circuit of a MOSFET including parasitic extrinsic resistances and inductances.

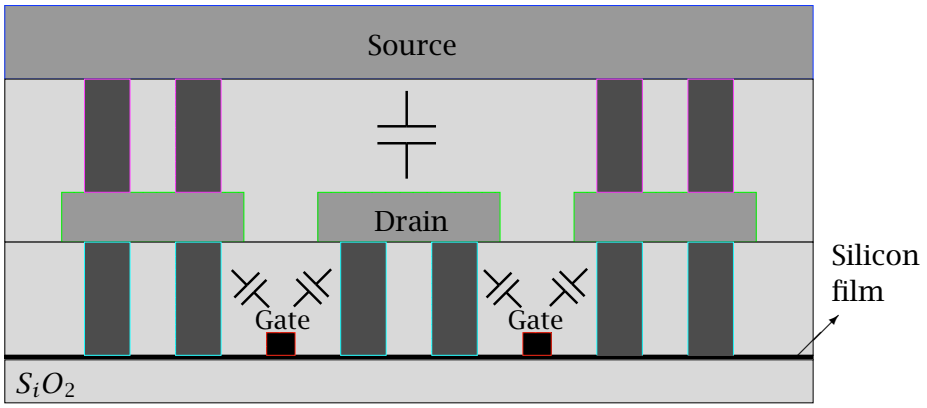


Figure 3.9: Cross section of sub-micron MOSFET using several metal layers.

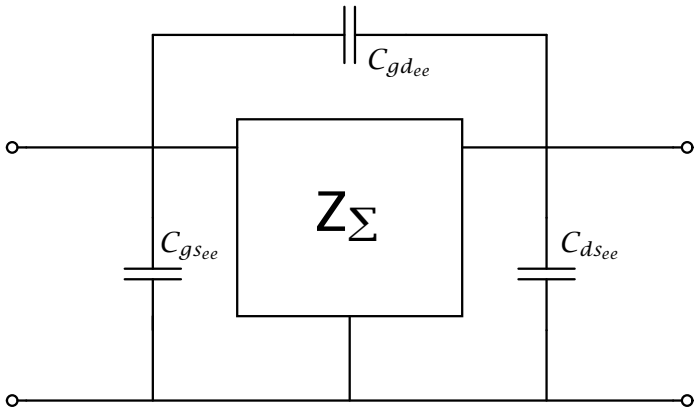
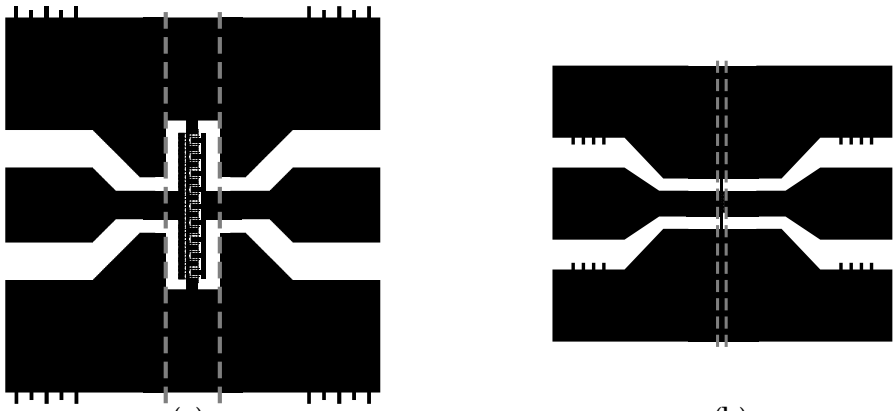


Figure 3.10: Equivalent circuit of a MOSFET including all extrinsic parasitic elements.



(a) (b)

Figure 3.11: Top view of two MOSFET's, with a gate length of $0.75\ \mu m$ (a) and $0.25\ \mu m$ (b) with the same W/L ratio, embedded in CPW lines. The measurement reference planes are represented by dashed lines

$$\text{where } Y_{ee} = \begin{bmatrix} j\omega(C_{gd_{ee}} + C_{gs_{ee}}) & -j\omega C_{gd_{ee}} \\ -j\omega C_{gd_{ee}} & j\omega(C_{ds_{ee}} + C_{gs_{ee}}) \end{bmatrix} \tag{3.13}$$

3.2.4.4 Access parameters

Depending on the device size and the measurement method, the reference planes after the calibration, might not be located at the edge of the active zone. Thus metal interconnections remain at the input and at the output of the transistor, which were not cancelled by the calibration. Also, when huge devices are measured, the ground planes of the CPW line around the transistor are cut (Figure 3.11). Several parasitics are then introduced, and are independent of the transistor dimension.

The parasitic effects of metallic interconnections are usually modeled by inductances and capacitances. These elements are considered lossless because their losses are negligible compared to those introduced by the extrinsic resistances in SOI technologies.

Since they are bias independent and not directly proportional to the device width, these elements are called “access", and noted by an index “a".

The general equivalent circuit of an integrated MOSFET embedded in a CPW line can finally be built (Figure 3.12).

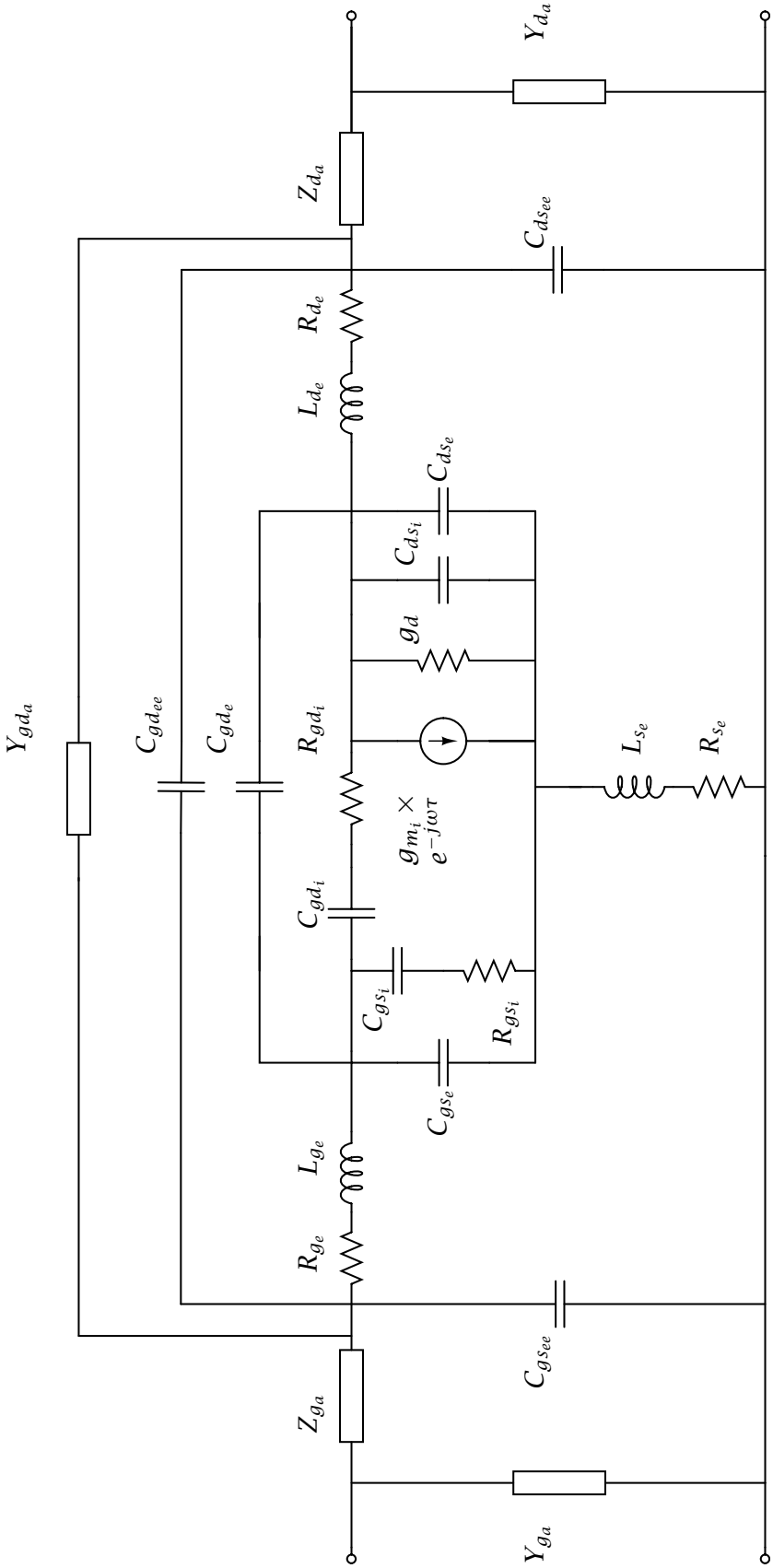


Figure 3.12: General equivalent circuit of an integrated MOSFET embedded in a CPW line

3.3 Extraction procedure of the small signal model

The purpose of this part is to develop a systematic characterization scheme allowing us to determine correct equivalent circuits of MOSFET transistors. Based on the general equivalent circuit proposed previously, assumptions are made in order to simplify the equivalent circuit.

Various measurements are used to describe the different steps of the method. In order to cover all cases that can be encounter.

The method is also applied in its entirety to a Fully Depleted, a Partially Depleted, and a Bulk MOSFET with gate length $L = 0.13\mu m$ and total width $W = 10\mu m$. Only the results of the FD are presented at each step of the method, but the transistors results obtained for the other devices are compared and briefly discussed at the end of this section.

The transistors are embedded in CPW structure, and are measured from 40 MHz up to 40 GHz by using a VNA. The two-steps calibration technique presented in section 2.3.2 is used to obtain the true s-parameters of the transistors. The influence of the measurement pads is then canceled. After calibration, the reference planes are defined at the edges of the transistors (Figure 3.11b).

Along the following sections, the intrinsic part of the transistors is de-embedded of all parasitic elements. Different methods are proposed to determine the values of extrinsic components. Their advantages and drawbacks are explained.

3.3.1 Parasitic access elements

Methods description The first step of the scheme is to decide if it is necessary to take into account access elements in the extraction. As explained in section 3.2.4, these elements are necessary to model metallic interconnections connecting the active zone of the transistor to the reference planes.

Some years ago, when the gate length of MOSFETs were in the range of $0.75\mu m$, the area of an efficient RF MOSFET was so huge that the ground plane of the CPW was cut, and a taper was used to connect the gate fingers to the central conductor of the CPW (Figure 3.11a). The reference plane cannot be defined close to the active zone, because of the non-uniformity of the access lines.

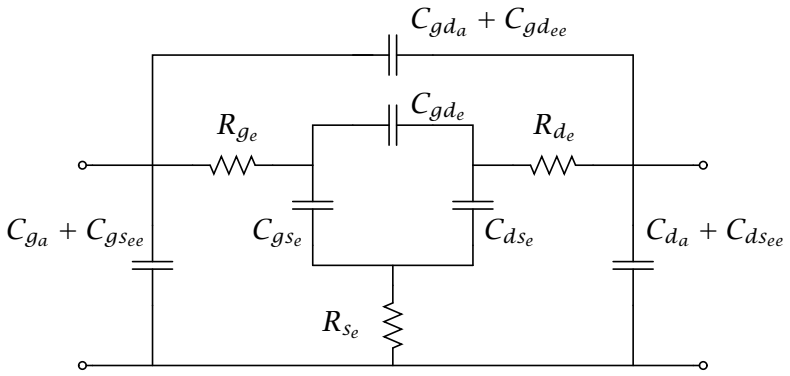


Figure 3.13: Considered equivalent circuit of a MOSFET to extract the access parameters.

Complex model had to be used for access elements.

Nowadays, since the size of efficient MOSFETs is smaller, the ground plane of CPW lines does not require to be cut (Figure 3.11b). The influence of access elements is then extremely small and mainly capacitive [1][4][5][6].

The usual techniques used to determine the access capacitance are based on the depletion assumption. The transistor is biased with V_{gs} below threshold ($V_{gs} << V_{th}$) and $V_{ds} = 0V$. Its intrinsic part is neglected. The general equivalent circuit can then be simplified. The considered equivalent circuit is shown in Figure 3.13.

In most of the cases (Figure 3.13), the imaginary part of the Y-parameters is strictly proportional to the frequency, and is approximated by the following relations

$$\Im\{Y_{11}\} \approx \omega\left(C_{g_a} + C_{gd_a} + C_{gd} + C_{gs}\right) \tag{3.14}$$

$$\Im\{Y_{12}\} \approx -\omega\left(C_{gd_a} + C_{gd}\right) \tag{3.15}$$

$$\Im\{Y_{22}\} \approx \omega\left(C_{d_a} + C_{gd_a} + C_{gd} + C_{ds}\right) \tag{3.16}$$

where $C_{gd} = C_{gd_e} + C_{gd_{ee}}$

$C_{gs} = C_{gs_e} + C_{gs_{ee}}$

$C_{ds} = C_{ds_e} + C_{ds_{ee}}$

Equations (3.14)-(3.16) are not sufficient to determine the access capacitances (C_{gd_a}, C_{d_a}, C_{g_a}). Indeed, only their sum with the extrinsic capacitances can be

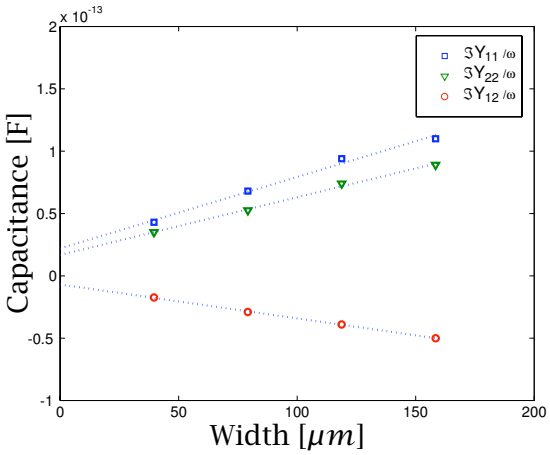


Figure 3.14: Evolution of the capacitances measured in deep depletion at $V_{ds} = 0$ for various width of Partially Depleted MOSFETs with a gate length $L = 0.25\mu m$

deduced directly.

To solve that problem, two different techniques can be used, depending on the number of available devices:

1. When several devices having the same gate length and number of fingers, but different width, are available, a linear regression between the effective capacitances ($\Im(Y_{ij})/\omega$) and the transistors widths is used to extract rigorously the access capacitances. Since the extrinsic capacitances are proportional to the device width, the intersections between the lines formed by the effective capacitances and the y-axis provide the access capacitances values. Figure 3.14 shows the regression for PD SOI transistors with a gate length $L = 0.25\mu m$. The extracted values of C_{g_a}, C_{d_a}, and C_{gd_a} are equal to 15, 11, and 7fF respectively.

2. If only one device is available, three other assumptions must be made to extract access capacitances:

   (a) The coupling between the gate and drain is negligible ($C_{gd_a} \approx 0$)

   (b) The transistor is symmetrical ($C_{gs} \approx C_{gd}$)

   (c) C_{ds} is small compared to C_{d_a}

   The access capacitances are renamed C'_{g_a} and C'_{d_a}. The imaginary parts of

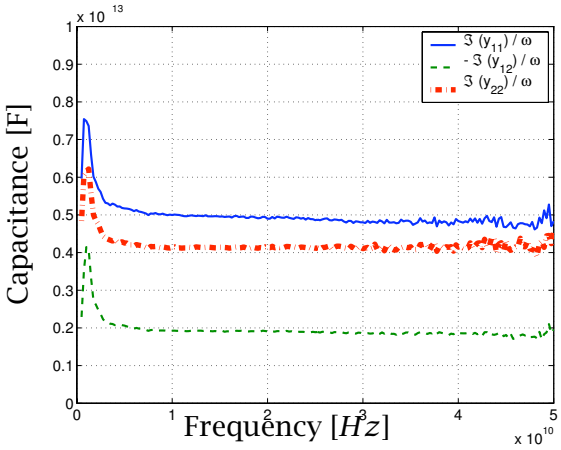


Figure 3.15: Effective capacitances of a SOI PD MOSFET with a gate length $L = 0.25\mu m$ and a total width $W = 80\mu m$. The transistor is biased at $V_{gs} = -1V$ and $V_{ds} = 0$

the Y-parameters are given by

$$\Im\{Y_{11}\} \approx \omega\left(C'_{g_a} + C_{gs} + C_{gd}\right) \tag{3.17}$$

$$\Im\{Y_{12}\} \approx -\omega\left(C_{gd}\right) \tag{3.18}$$

$$\Im\{Y_{22}\} \approx \omega\left(C'_{d_a} + C_{gd}\right) \tag{3.19}$$

$$\text{where} \quad C_{gd} = C_{gd_e} + C_{gd_{ee}}$$

$$C_{gs} = C_{gs_e} + C_{gs_{ee}}$$

The extraction of the access capacitances is then straightforward

$$C'_{g_a} = \Im\left\{\frac{Y_{11} + 2Y_{12}}{\omega}\right\} \qquad C'_{d_a} = \Im\left\{\frac{Y_{22} + Y_{12}}{\omega}\right\} \tag{3.20}$$

The access capacitances are deduced from the measurement shown in Figure 3.15. The extracted values of C'_{g_a} and C'_{d_a} are equal to 10fF and 22fF respectively.

The single transistor method induces errors depending on the physical values of C_{gd_a} and C_{ds}. The access gate capacitance is always underestimated ($C'_{g_a} = C_{g_a} - C_{gd_a}$), and the access drain capacitance is overestimated ($C'_{d_a} = C_{d_a} + C_{ds}$).

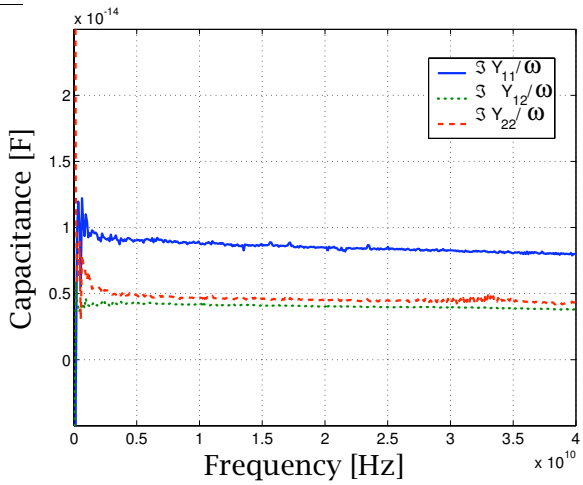


Figure 3.16: Effective capacitances of a FD SOI MOSFET with a gate length $L = 0.13\mu m$ and a total width $W = 10\mu m$ at $V_{gs} = -1V$ and $V_{ds} = 0V$

Once the access capacitances are known, they can be de-embedded from the transistor measurements (Y_{meas}), using the following relations

$$Y_{\Pi} = Y_{meas} - Y_a \tag{3.21}$$

$$\text{where } Y_a = \begin{bmatrix} j\omega(C_{gd_a} + C_{g_a}) & -j\omega C_{gd_a} \\ -j\omega C_{gd_a} & j\omega(C_{d_a} + C_{gd_a}) \end{bmatrix} \tag{3.22}$$

Experimental results The FD MOSFET transistor has been biased at $V_{gs} = -1$ and $V_{ds} = 0$. The access capacitances are extracted from the imaginary part of the measured Y-parameters, using the single transistor method (Figure 3.16). The extracted capacitances C_{gd_a}, C_{g_a}, and C_{d_a} are equal to $0fF$, $0.5fF$, and $0.5fF$ respectively.

These capacitances have been de-embedded from measurements using Equations (3.21)-(3.22).

3.3.2 Extrinsic-extrinsic capacitances

Method description The origin of the extrinsic-extrinsic capacitances ($C_{gd_{ee}}$, $C_{gs_{ee}}$, and $C_{ds_{ee}}$) is the capacitive coupling between the metallic interconnection lines outside the transistor active zone. These capacitances exist in all transistors, but can usually be neglected. Because they are usually small, and their effects are not often in the frequency band of measurement.

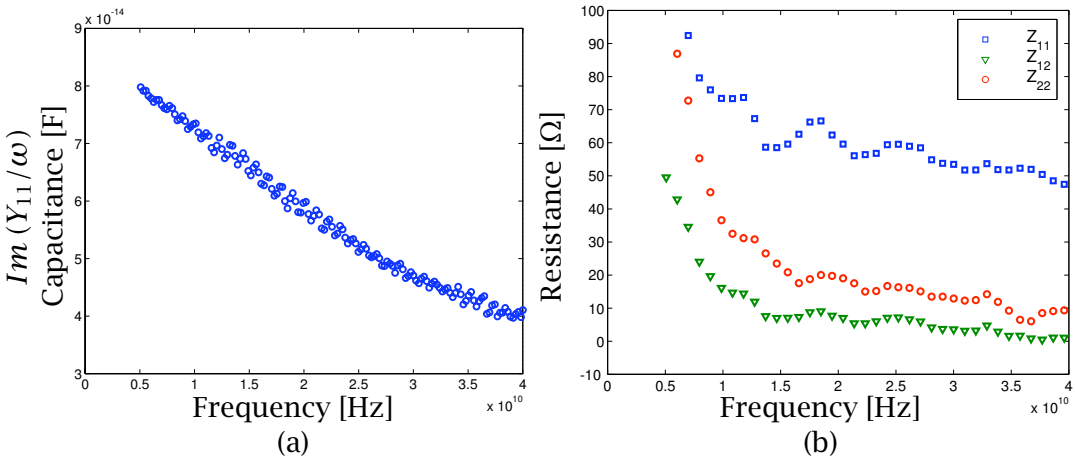


Figure 3.17: Measurement of MOSFET with a gate length $L = 0.25\mu m$ and a total width $W = 120\mu m$ requiring "extrinsic-extrinsic" capacitances. (a) Input capacitances of a MOSFET in deep depletion, (b) real part of the Z-parameters

If they cannot be neglected, the following behaviors are observed in the MOSFET measurement in deep depletion:

- The effective capacitances $(\Im(Y_{\Pi_{ij}})/\omega)$ exhibit a strong variation versus frequency, as shown in Figure 3.17a.

- The real parts of the Z-parameters are extremely small. They can even be lower than zero (Figure 3.17b). This behavior is confirmed using the corresponding relations deduced from the equivalent circuit.

In order to extract these "extrinsic-extrinsic" capacitances, some authors [4] have proposed to use electrostatic simulators to estimate their value. This technique necessitates the exact knowledge of the 3D structure of the transistor. But usually, the complete transistor structure is not known accurately. As a consequence, this technique is difficult to use.

A new method has been developed to deduce the capacitances value directly from measurements [5]. The measurements made by GOFFIOUL in [4] and its simulated results have been used to validate the proposed method.

The expression of the effective capacitance is approximated by the following equation

$$\Im\left\{\frac{Y_{ij}}{\omega}\right\} \approx C_{ee} + \frac{C_e}{1+\tau^2\omega^2} \tag{3.23}$$

where τ^2 is function of all of the equivalent circuit parameters and does not depend on frequency.

The coefficients C_{ee}, C_e and τ^2 are determined using a mean square method. Indeed, if we call $c_\iota = Y_{ij}(\omega = \omega_\iota)/\omega_\iota$ and $d_\iota = 1/(1 + \tau^2\omega_\iota^2)$, the coefficients C_{ee}, C_e, and τ^2 are found to minimize the following expression:

$$\sum_{\iota=1}^{N} (c_\iota - C_{ee} - C_e d_\iota)^2 \tag{3.24}$$

The sum is made over the whole frequency range.

After differentiating this equation for each of the unknowns, and after some basic manipulations (Appendix B), the following equations are obtained

$$C_{ee} = \overline{y} - C_e\overline{d} \tag{3.25}$$

$$C_e = \left(\frac{1}{N}\sum_{\iota=1}^{N} d_\iota^2 - \overline{d}^2\right)^{-1}\left(\left(\frac{1}{N}\sum_{\iota=1}^{N} c_\iota d_\iota\right) - \overline{y}\overline{d}\right) \tag{3.26}$$

$$\mathrm{cor}[c, d^2] = \mathrm{cor}[c, d]\mathrm{cor}[d, d^2] \tag{3.27}$$

where $\mathrm{cor}[a, b]$ is the correlation coefficient between a and b and the overline represents the mean.

Equation (3.27) has to be solved numerically, by finding the roots of the following function

$$\mathcal{F}(\tau^2) = \mathrm{cor}[y, d^2] - \mathrm{cor}[y, d]\mathrm{cor}[d, d^2] \text{ where } d_\iota = 1/(1 + \tau^2\omega_\iota^2) \tag{3.28}$$

Figure 3.18 shows the function ($\mathcal{F}$) versus τ^2, using measurements shown in Figure 3.17a. Two roots can be determined. The first one, which corresponds to $\tau = 0$, must be rejected. It means that the two capacitances are just connected in parallel. The second one is used to solve the Equations (3.26) and (3.25).

Table 3.1 compares the values of the extrinsic-extrinsic capacitances extracted using Equations (3.25)-(3.27) with the values obtained from simulations. No big differences are observed, validating the efficiency of the method.

Since the “extrinsic-extrinsic” capacitances are determined, they are de-embedded

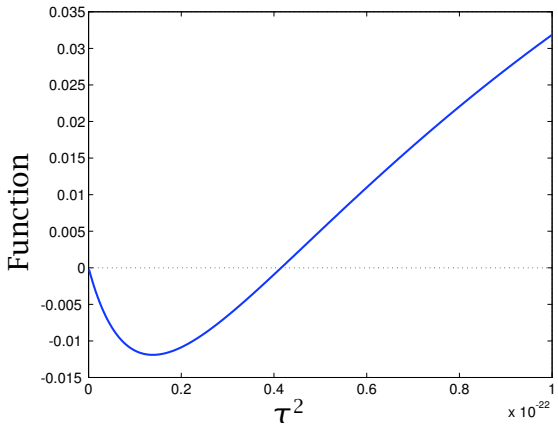


Figure 3.18: Determination of the roots of equation 3.27 for a MOSFET with a gate length $L = 0.25\mu m$ and a total width $W = 144\mu m$

	$C_{gs_{ee}}$ (fF)	$C_{gd_{ee}}$ (fF)	$C_{gd_{ee}}$ (fF)
Simulated Values	10	10	20
Extracted Values	11	13	35

Table 3.1: Extracted and simulated values of extrinsic-extrinsic capacitances of a MOSFET with a gate length $L = 0.25\mu m$ and a total width $W = 144\mu m$

from the measurement (Y_Π), using the following relation

$$Z_\Sigma^{-1} = Y_\Pi - Y_{ee} \tag{3.29}$$

$$\text{where } Y_{ee} = \begin{bmatrix} j\omega(C_{gd_{ee}} + C_{gs_{ee}}) & -j\omega C_{gd_{ee}} \\ -j\omega C_{gd_{ee}} & j\omega(C_{ds_{ee}} + C_{gs_{ee}}) \end{bmatrix} \tag{3.30}$$

Experimental results The FD transistor measured exhibits nearly flat effective capacitances (Figure 3.16) over the whole frequency band, then no extrinsic-extrinsic capacitances are required in its equivalent circuit. Neither the PD nor the Bulk MOSFET require the use of extrinsic-extrinsic capacitances in their equivalent circuit.

3.3.3 Extrinsic resistances and inductances

Methods description Extractions of parasitic resistances and inductances are classical topics in the field of RF characterization of integrated components. Various methodologies have been developed to extract these parasitic elements.

In the following paragraphs, some methods, which can be used for SOI MOSFETs, are described . They are divided into three categories:

- The depletion methods. The extrinsic resistances and inductances are extracted from one measurement made in deep depletion.
- The inversion methods, also called cold-FET methods. The extrinsic resistances and inductances are extracted from several measurements made in strong inversion ($V_{gs} >> V_{th}$) with $V_{ds} = 0V$.
- The saturation methods. The extrinsic resistances and inductances are extracted from one measurement made in saturation.

Depletion method : In this method, the MOSFET is put in depletion ($V_{gs} \ll V_{th}$). The intrinsic part of the device is neglected. The Z- parameters, defined by Equation (3.10), are used to extract the resistances and the inductances using relationships given by LOVELACE in [7]

$$Z_{\Sigma_{11}} - Z_{\Sigma_{12}} \approx R_{g_e} + j\omega L_{g_e} + \frac{1}{j\omega C_1} \tag{3.31}$$

$$Z_{\Sigma_{12}} \approx R_{s_e} + j\omega L_{s_e} + \frac{1}{j\omega C_2} \tag{3.32}$$

$$Z_{\Sigma_{22}} - Z_{\Sigma_{12}} \approx R_{d_e} + j\omega L_{d_e} + \frac{1}{j\omega C_3} \tag{3.33}$$

where $\frac{1}{j\omega C_1} = (\mathsf{Y}_e^{-1})_{11} - (\mathsf{Y}_e^{-1})_{12}$, $\frac{1}{j\omega C_2} = (\mathsf{Y}_e^{-1})_{12}$, and $\frac{1}{j\omega C_1} = (\mathsf{Y}_e^{-1})_{22} - (\mathsf{Y}_e^{-1})_{12}$.

The capacitances are extracted using the mathematical expressions of the Y-parameters

$$(Z_\Sigma^{-1})_{11} \approx j\omega(C_{gd_e} + C_{gs_e}) + \epsilon_{11}\,\omega^2 \tag{3.34}$$

$$(Z_\Sigma^{-1})_{12} \approx j\omega C_{gd_e} + \epsilon_{12}\,\omega^2 \tag{3.35}$$

$$(Z_\Sigma^{-1})_{21} \approx j\omega(C_{gd_e} + C_{ds_e}) + \epsilon_{22}\,\omega^2 \tag{3.36}$$

where ϵ_{ij} is function of all parameters of the equivalent circuit.

The accuracy of this method is poor for small integrated devices [1]. Practically, the real part of the Z-parameters are frequency dependent, because even in deep depletion, the gate transconductance g_{m_i} and the output conductance g_d have a value different from zero. The imaginary parts of the Z-parameters are affected. Few μS for g_{m_i} and g_d are sufficient to degrade the validity of Equation (3.31)-(3.34) [8].

Saturation method : The transistor is biased in the saturation regime. The entire equivalent circuit is considered, but the non-quasi-static resistances and the source inductance are neglected.

The expressions of the Z-parameters become complicated but can be summarized as follow

$$\Re\{Z_{12}\} = R_{s_e} + \frac{A_s}{B+\omega^2} \quad (3.37)$$

$$\Re\{Z_{22} - Z_{12}\} = R_{d_e} + \frac{A_d}{B+\omega^2} \quad (3.38)$$

$$\Re\{Z_{11} - Z_{12}\} = R_{g_e} + \frac{A_g}{B+\omega^2} \quad (3.39)$$

$$\Im\left\{\frac{Z_{12}}{\omega}\right\} = L_{s_e} - \frac{E_s}{B+\omega^2} \quad (3.40)$$

$$\Im\left\{\frac{Z_{22} - Z_{12}}{\omega}\right\} = L_{d_e} - \frac{E_d}{B+\omega^2} \quad (3.41)$$

$$\Im\left\{\frac{Z_{11} - Z_{12}}{\omega}\right\} = L_{g_e} - \frac{E_g}{B+\omega^2} - \frac{F_g}{\omega^2(B+\omega^2)} \quad (3.42)$$

where all the coefficients are frequency independent.

To find the solution of this set of equations, some authors use an optimizer [9], or some relationships between different Z-parameters [1].

For example, for the extrinsic resistances, the parametric curves defined in a two-dimensional plane by $[\Re\{Z_{ij}\}, \Re\{Z_{kl}\}]$ where $ij \neq kl$ are straight lines. The slope and the intercept at the origin of that line are function of the resistances.

$V_{gs}\backslash V_{ds}$	$0.75V$	$0.9V$	$1.05V$	$1.2V$
$0.6V$	9.8Ω	10Ω	10.1Ω	
$0.75V$		7.9Ω	8.3Ω	8.4Ω
$0.9V$			6.4Ω	6.8Ω
$1.05V$				4.75Ω

Table 3.2: Extracted gate resistances for a $12\times(12.6/0.5)\mu m$ MOSFET at different polarization, using a saturation method.

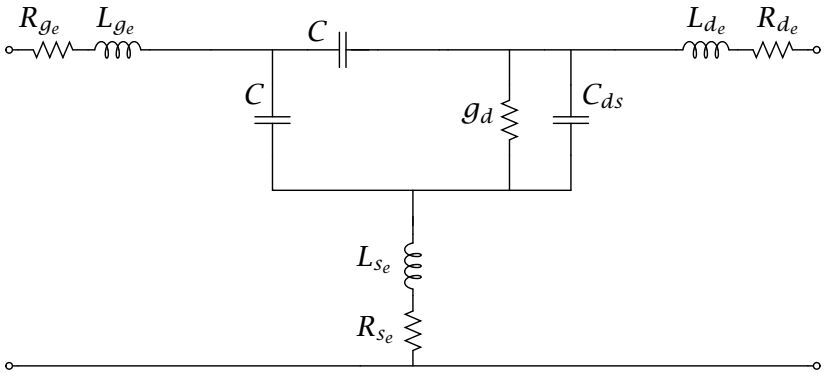


Figure 3.19: Equivalent circuit of the MOSFET used in strong inversion.

This method has shown strong dependancies to the applied bias [5]. Table 3.2 shows the extracted gate resistances of a SOS MOSFET, with a gate length of $.5\mu m$ and a total width of $120\mu m$, for various applied bias. Large variations of the extracted values are observed, which is clearly a strong limitation of this method.

Moreover, this method neglects the non-quasi-static effect of the intrinsic part of the MOSFET. These simplifications can introduce significant errors [10].

To increase the method accuracy, RASKIN [1] proposes to use optimization steps after introducing the non-quasi-static resistance in the model. Then, this method becomes much more complicated.

Inversion method : The transistor is biased with V_{ds} equal to zero. Several measurements of the transistor with different gate voltages are required [6]. As the transistor is working in the linear regime, the equivalent circuit of the transistor is simplified

(Figure 3.19).

Assuming that $C_{gd} \approx C_{gs} = C$, the expressions of the Z-parameters can be approximated by

$$\Re\{Z_{22} - Z_{12}\} = R_{d_e} + \frac{1}{2g_d} \quad (3.43)$$

$$\Re\{Z_{12}\} = R_{s_e} + \frac{1}{2g_d} \quad (3.44)$$

$$\Re\{Z_{11} - Z_{12}\} = R_{g_e} - \frac{1}{4g_d} \quad (3.45)$$

$$\Im\left\{\frac{Z_{22} - Z_{12}}{\omega}\right\} = L_{d_e} + \frac{C + 2C_{ds}}{4g_d^2} \quad (3.46)$$

$$\Im\left\{\frac{Z_{12}}{\omega}\right\} = L_{s_e} + \frac{C + 2C_{ds}}{4g_d^2} \quad (3.47)$$

$$\Im\left\{\frac{Z_{11} - Z_{12}}{\omega}\right\} = L_{g_e} - \frac{C_{ds}(C + 2C_{ds})}{4gd^2C} - \frac{1}{2C\omega} \quad (3.48)$$

$$\text{when } \left(\frac{-C^2 - 2CC_{ds}}{4g_d^2C^2}\omega^2\right) \ll 1 \quad (3.49)$$

Practically, this condition is reached when the applied gate voltage is at least two times bigger than the threshold voltage ($V_{gs} \gg V_{th}$).

In the MOSFET theory, the drain to source conductance is proportional to the gate voltage in linear regime. The output conductance is given by

$$g_d = \frac{\mu W C_{ox}}{L}(V_{gs} - V_{th} - nV_{ds}) \quad (3.50)$$

Then, the values of the real and imaginary part of the Z-parameters are proportional to the inverse of the gate voltage overdrive ($1/GVO = 1/(V_{gs} - V_{th})$). The resistances and the inductances are extracted using linear regression of the real and imaginary part of the Z-parameters versus $1/(V_{gs} - V_{th})$ for the resistances and $1/(V_{gs} - V_{th})^2$ for the inductances.

In order to evaluate the accuracy of the presented methods, the intrinsic part

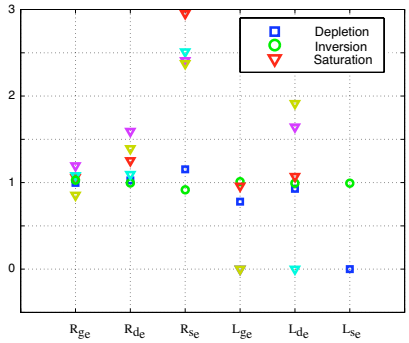


Figure 3.20: Relative errors in the extraction of extrinsic elements of MOSFET with a gate length $L = 0.25\ \mu m$ and a total width $W = 108\ \mu m$. The different triangles are for different biases in saturation.

of the MOSFET has been simulated using Atlas from Silvaco [11] for several polarizations and frequencies. The transistor is a fully depleted SOI MOSFET with a gate length $L = 0.25\mu m$. The simulated 2-ports have been embedded with extrinsic elements using several values taken from the literature. Then, a random variable following a Gaussian law has been added to the corresponding S-parameters in order to generate realistic noisy data, to evaluate the robustness of the different methods against measurement noise.

The relative error in the extraction of the extrinsic elements, defined as the ratio between the fixed value and the extracted value, is shown in Figure 3.20.

The inversion method seems to be the most accurate one for the dimensions of interest, which are in the submicron range. The depletion method can give good results but it is extremely case dependent. It is also the same for the saturation method, but this one exhibits also a strong dependence on the applied bias.

After the determination of the extrinsic resistances and inductances, these parasitic elements can be de-embedded from the data using the following equations

$$\mathsf{Y}_{\pi}^{-1} = \mathsf{Z}_{\Sigma} - \mathsf{Z}_{e} \tag{3.51}$$

$$\text{where } \mathsf{Z}_{e} = \begin{bmatrix} R_{g_e} + R_{s_e} + j\omega\left(L_{g_e} + L_{s_e}\right) & R_{s_e} + j\omega L_{g_e} \\ R_{s_e} + j\omega L_{g_e} & R_{d_e} + R_{s_e} + j\omega\left(L_{d_e} + L_{s_e}\right) \end{bmatrix} \tag{3.52}$$

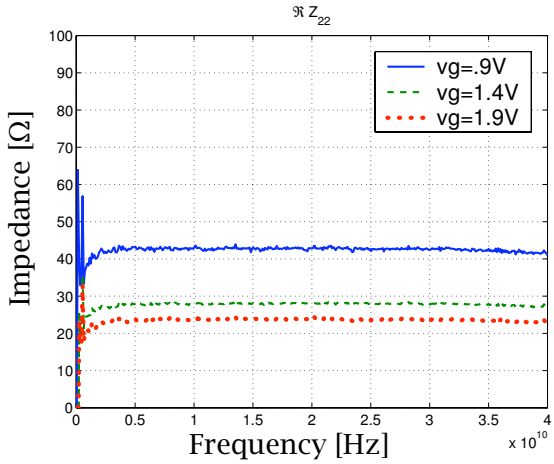


Figure 3.21: Real part of measured Z_{22} of a FD SOI MOSFET ($L = 0.13\ \mu m$, $W = 10\ \mu m$)

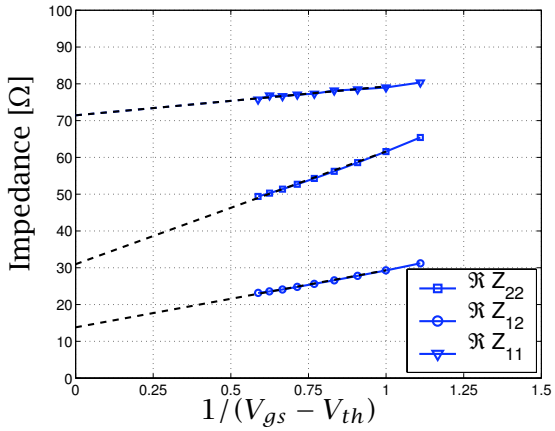


Figure 3.22: Real part of measured Z-parameters versus gate voltage overdrive of a FD SOI MOSFET ($L = 0.13\ \mu m$, $W = 10\ \mu m$)

Experimental results Since the inversion method seems to be the most accurate one, it is used to determine extrinsic resistance values of the transistors. We did not extract directly extrinsic inductances, because no significant variations of the imaginary part of the Z-parameters were observed when the gate voltage was changed.

To apply the inversion method, the real part of the Z-parameters must reach a plateau at a few GHz (Figure 3.21). If no plateau is observed, there must be errors in the de-embedding of the access or extrinsic-extrinsic capacitances. The mean values of each plateau are calculated, then they are plotted versus $1/(V_{gs} - V_{th})$ as shown in Figure 3.22. Then linear regressions are made. The extracted resistances R_{g_e} , R_{s_e} , and R_{d_e} are equal to 57Ω, 14Ω, and 16Ω respectively.

3.3.4 Extrinsic capacitances

Method description The extrinsic capacitances are usually considered bias independent, and can be deduced directly from the imaginary part of the parameters of Y_π in deep depletion using the following equations

$$C_{gs_e} = \Im\left\{\frac{Y_{11} + Y_{12}}{\omega}\right\} \tag{3.53}$$

$$C_{gd_e} = \Im\left\{\frac{-Y_{12}}{\omega}\right\} \tag{3.54}$$

$$C_{ds_e} = \Im\left\{\frac{Y_{22} + Y_{12}}{\omega}\right\} \tag{3.55}$$

Only a few authors [1][4] are considering these capacitances in their extraction procedure for MOSFETs. The others assume that they are part of the intrinsic. They concider implicitly that these capacitances are bias dependent, or that they are negligible compared to the active capacitances.

The extrinsic capacitances are de-embedded from measurements (Y_π), using the following relation

$$\mathsf{Y}_i = \mathsf{Y}_\pi - \mathsf{Y}_e \tag{3.56}$$

$$\text{where } \mathsf{Y}_e = \begin{bmatrix} j\omega(C_{gd_e} + C_{gs_e}) & -j\omega C_{gd_e} \\ -j\omega C_{gd_e} & j\omega(C_{ds_e} + C_{gs_e}) \end{bmatrix} \tag{3.57}$$

Experimental results The extrinsic capacitances are extracted from the imaginary part of the measured Y-parameters. The extracted capacitances C_{gs_e} , C_{gd_e} , and C_{ds_e} are equal to $4fF$, $4fF$, and $0fF$ respectively.

The extracted extrinsic capacitance C_{ds_e} is always close to zero when the single transistor method is used to determine the access capacitances (Section 3.3.1). Indeed, the effect of this physical capacitance is compensated by the capacitance C_{d_a}.

3.3.5 Intrinsic elements

Method description After all the previous steps, the intrinsic part of the MOSFET is obtained (Y_i). Based on the expression of the Y-parameters of the non-quasi-static model shown by the Equation (3.7), the values of the intrinsic ele-

ments are given by

$$g_{m_i} = -\left|\frac{Y_{i_{21}} - Y_{i_{12}}}{Y_{i_{11}} + Y_{i_{12}}}\right| \frac{1}{\Im\left\{\frac{1}{Y_{i_{11}}+Y_{i_{12}}}\right\}} \tag{3.58}$$

$$g_d = \Re\left\{Y_{i_{22}} + Y_{i_{12}}\right\} \tag{3.59}$$

$$C_{gs_i} = -\frac{1}{\omega\ \Im\left\{\frac{1}{Y_{i_{11}}+Y_{i_{12}}}\right\}} \tag{3.60}$$

$$C_{gd_i} = \frac{1}{\omega\ \Im\left\{\frac{1}{Y_{i_{12}}}\right\}} \tag{3.61}$$

$$C_{ds_i} = \frac{\Im\left\{Y_{i_{22}} + Y_{i_{12}}\right\}}{\omega} \tag{3.62}$$

$$R_{gd_i} = -\Re\left\{\frac{1}{Y_{i_{12}}}\right\} \tag{3.63}$$

$$R_{gs_i} = \Re\left\{\frac{1}{Y_{i_{11}} + Y_{i_{12}}}\right\} \tag{3.64}$$

$$\tau = \frac{1}{\omega}\text{atan}\left\{\frac{\Im\left\{(Y_{i_{21}} - Y_{i_{12}})/(1 + j\omega R_{gs_i} C_{gs_i})\right\}}{\Re\left\{(Y_{i_{21}} - Y_{i_{12}})/(1 + j\omega R_{gs_i} C_{gs_i})\right\}}\right\} \tag{3.65}$$

Experimental results Equations (3.58)-(3.64) are applied to the de-embedded measurement, the different extracted elements are shown in Figure 3.23. Relatively flat curves are obtained above a few GHz for almost all components, except the non-quasi-static resistances. In fact, the frequency band is not wide enough to allow determining accurately the non-quasi-static elements. Their effects on the behavior of a deep sub-micron MOSFET are extremely small in the frequency band of measurement. It is then extremely difficult to extract their values.

Values for the intrinsic components have been deduced from these curves. Then, by using the previously determined extrinsic components, the complete model of the MOSFET has been built. The values of the equivalent circuit elements are summarized in Table 3.3.

The model is compared with measurement in Figure 3.24. Relatively good agreement is obtained between simulation and measurement. The methodology used is then correct for such device.

Access capacitances		
$C_{g_a} = 0.5fF$	$C_{d_a} = 0.5fF$	$C_{gd_a} = 0fF$
Extrinsic resistances		
$R_{g_e} = 57\Omega$	$R_{d_e} = 16\Omega$	$R_{s_e} = 14\Omega$
Extrinsic capacitances		
$C_{gs_e} = 4fF$	$C_{ds_e} = 0fF$	$C_{gd_e} = 4fF$
Intrinsic components		
$g_{m_i} = 7.6mS$	$g_d = .72mS$	
$C_{gs_i} = 4.5fF$	$C_{gd_i} = 0.26fF$	$C_{ds_i} = 0.3fF$
$R_{gs_i} = 49\Omega$	$R_{gdi} = 0\Omega$	$\tau \approx .3ps$

Table 3.3: Extracted parameters of the equivalent circuit of a FD SOI MOSFET ($L = 0.13\ \mu m$, $W = 10\ \mu m$) biased at $V_{gs} = 0.7\ V$ and $V_{ds} = 1.2\ V$

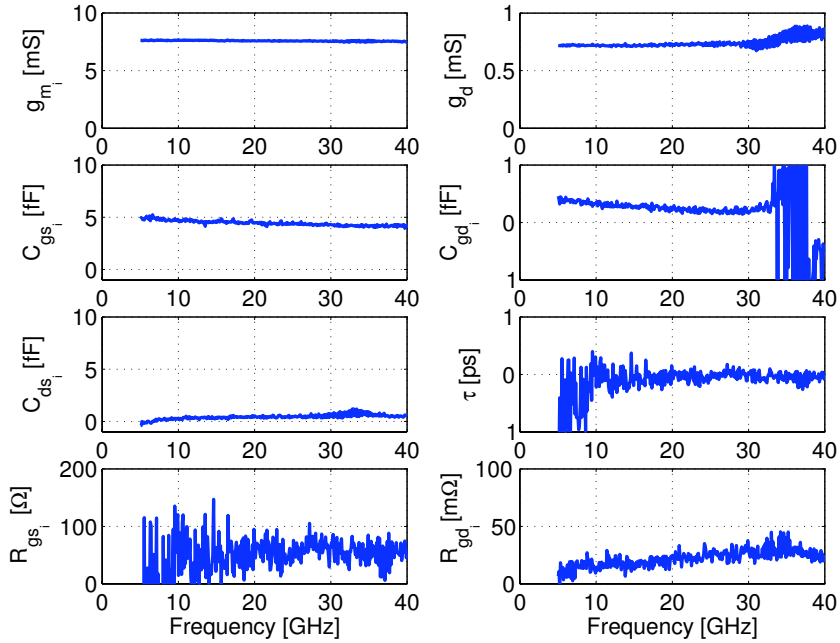


Figure 3.23: Parameters extracted using Equation (3.58)-(3.64) of a FD SOI MOSFET ($L = 0.13\ \mu m$, $W = 10\ \mu m$) biased at $V_{gs} = 0.7$ and $V_{ds} = 1.2\ V$

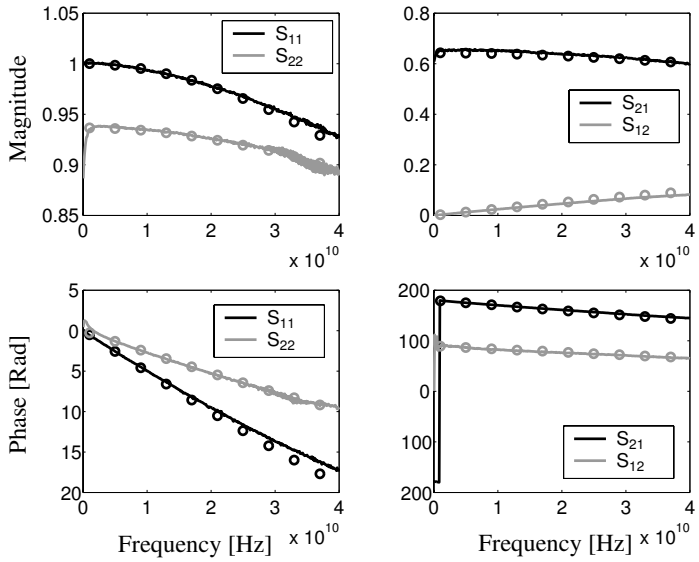


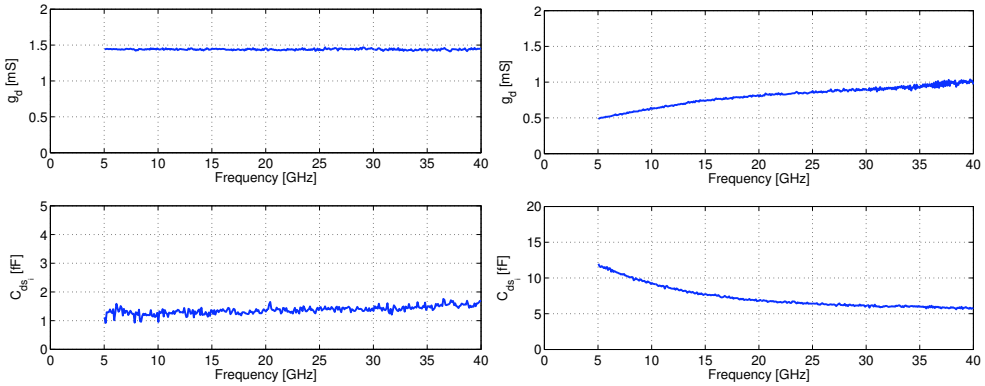
Figure 3.24: Simulated (o) and measured (-) S-parameters of a FD SOI MOSFET ($L = 0.13\ \mu m$, $W = 10\ \mu m$) biased at $V_{gs} = 0.7$ and $V_{ds} = 1.2\ V$

3.3.6 Comparison between FD, PD, and Bulk MOSFET

One of the main differences between FD and PD or Bulk MOSFET, is that there is a part of the substrate, located between the source and the drain, which is not depleted. Then, the coupling between drain and source may not be accurately model using only the capacitance C_{ds}. In that case, the intrinsic output conductance (g_d) and drain to source capacitance (C_{ds_i}), extracted using Equation (3.59) and (3.62), will not be constant versus frequency.

By applying the extraction scheme to the PD and Bulk MOSFETs, the intrinsic part of their equivalent circuit has been extracted. The output conductance (g_d) and drain to source capacitance (C_{ds_i}) are given in Figure 3.25. The parameters extracted from the PD are relatively flat over the whole frequency range as for a FD transistor. The equivalent circuit is then correct to model deep sub-micron PD transistor at high frequency. But in the case of bulk transistor, huge variations are observed.

Thus, the equivalent circuit is not adequate to model deep sub-micron Bulk MOSFET. It has to be completed by adding new elements between source and drain to model the influence of the substrate.



(a) (b)

Figure 3.25: Output conductance and drain to source intrinsic capacitances of a PD (a) and a Bulk MOSFET (grounded body) with a gate length $L = 0.13\ \mu m$ and a total width $W = 10\ \mu m$ biased at $V_{gs} = 0.7\ V$ and $V_{ds} = 1.2\ V$

3.4 Conclusion

Along this chapter, an equivalent circuit of integrated SOI MOSFETs has been defined. Different methods have been proposed to simplify the equivalent circuit, and to determine the values of its components.

The described procedure has been successfully applied to deep sub-micron FD and PD SOI MOSFETs. The influence of the substrate has been found negligible for both FD and PD transistor, compared to what it is observed for Bulk transistors.

But direct extraction techniques have exhibited some of their limits. Indeed, the non-quasi-static elements are difficult to extract with accuracy for sub-micron MOSFETs as their effects is less important, in the measurement frequency band (section 3.2.3). The extracted values allow us to obtain a model that fit correctly the measurements, but they cannot be directly linked to the device physic.

Usually, the non-quasi-static elements are easily extracted when frequency is sufficiently high so that intrinsic capacitances are almost short-circuited. But this condition cannot be achieved in deep sub-micron transistors for frequencies under 40 GHz. Higher frequency measurements will be helpful if we want to use direct extraction techniques for next generations of integrated MOSFETs.

Otherwise, optimization should be used to determine correct equivalent circuit of transistors.

Furthermore, the equivalent circuit considered for the intrinsic part of the MOSFET might be not appropriate for future generations of MOSFET transistors. Indeed, as the dimensions of the transistors are reduced, new parasitics will be required to model the transistor. Then all the extraction methods used should be adapted.

However, extraction techniques are still the most practical method to determine the parameters limiting the device performances, if the correct equivalent circuit is used. When the aim of extraction is to do a technological study, and not a modeling of MOSFET for circuit designer, MOSFET should be designed to facilitate the extraction of the extrinsic parameters.

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