A Low-Power 42 to 67 GHz Variable-Gain LNA in 22FDX® on Standard- and High-Resistivity Substrates with 3.4 dB Noise Figure

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***Abstract* — This paper describes the design and implementation of a 42-67 GHz LNA using GlobalFoundries' 22 nm FD-SOI technology, that was fabricated on standard-resistivity as well as on high-resistivity substrate wafers. On the conventional standard-resistivity substrate, the proposed design achieves 3.8 dB of minimal noise-figure for a peak gain of 21.0 dB at its nominal bias under 13.7 mW of power-consumption. The LNA makes use of the unique back-gate bias node of the 22FDX® technology to offer 10 dB of gain-control over a 2 V bias range at the back-gates, and takes up an area of 0.17 mm². On the high-resistivity silicon substrate, improvements of 0.9 dB in gain and 0.4 dB in noise-figure are achieved for this LNA, and these improvements are attributed to the increased quality factors of the integrated spiral inductors present in the design.**

***Keywords* — Low-noise amplifier (LNA), variable gain, high-resistivity silicon substrate, mm-wave, FD-SOI, noise-figure (NF).**

I. Introduction

New generations of wireless technologies face spectrum scarcity issues in the sub-6 GHz frequency band, due to the ever-increasing number of users and connected devices in today's ever-growing electronics consumer landscape.

To meet the demands of these emerging applications, wider operational bandwidths are being targeted at mm-wave frequencies (ranging from 24 to 100 GHz).

In particular, the 60 GHz band is of high interest since it provides a license-free, wide frequency spectrum across many parts of the world [1]. Compared to Wi-Fi networks that can support maximum data rates between 50 Mbps and 300 Mbps, protocols at 60 GHz can support rates up to several Gbps.

At the receiver (Rx) node, these applications require high sensitivity along with wide dynamic range. Indeed, according to wireless personal area network (WPAN) standard [2], Rx terminals are required to accept input power levels ranging from -70 dBm to -10 dBm. To help cope with that wide range, it is of high interest that the Rx chain implement *variable-gain* to adapt to the received power level.

In this work, we propose a variable-gain LNA design in GlobalFoundries' 22FDX® technology node, being fabricated in the reference process on standard-resistivity (10 Ωcm) as well as in an exploratory research process using high-resistivity (>1 kΩcm) substrates, targeting higher-quality passives and hence an overall higher performance LNA. The 22FDX® technology offers excellent RF-performance metrics with transit frequencies (f_t) and maximum oscillation frequencies (f_{max}) of above 300 GHz [3], along with low noise performance at low power, making such nodes strong candidates for mm-wave and sub-THz front-end circuitry. The proposed LNA makes use of FD-SOI's unique back-gate terminals for the control of the gain, with the advantage of the design consuming less DC power in the lower-gain modes.

In this paper, the design and measurements of a wideband 42 to 67 GHz LNA with 10 dB variable-gain in the 22 nm FD-SOI node are presented. At its nominal bias, the LNA consumes 13.7 mW under a 1.1 V supply and achieves 21.0 (21.8) dB of peak gain for 3.8 (3.4) dB of minimum noise figure on the standard-resistivity (high-resistivity) substrate.

II. Circuit Design

The overall schematic along with the core layout of the 3-stage LNA is presented in Fig. 1, with each stage being a cascode topology with degenerated source inductor (L_s) with a transformer load (L_g and L_d).

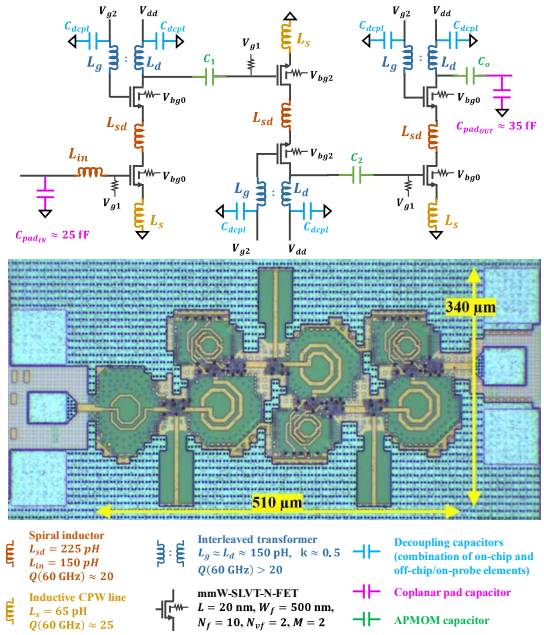

Fig. 1. Schematic of the 3-stage LNA and corresponding layout photograph. Note that the second stage is flipped for layout area reduction. Circuit parameter values are given, and the Q-factor values of the inductors correspond to those achieved on the standard-resistivity.

The multistage cascode architecture is chosen to achieve high gain while maintaining a low power consumption in this

technology, and the transformer-loaded technique is used to boost the gain and trade-off gain for bandwidth [4].

A. Transistors

All transistors in the LNA are SLVT N-FETs of 20 nm gate length, and are sized with 500 nm finger width, which provides a good trade-off point between available minimal noise figure (NF_{min}) and available gain. Each transistor is made up of four transistor cells of 5 µm width each, using 10 fingers, for a total width per transistor of 20 µm.

A source to drain voltage (V_{ds}) bias condition of 0.55 V is chosen for each FET of the design (therefore a V_{dd} of 1.1 V). The gate bias points were set to V_{gs} = 0.37 V for all devices in the LNA. The back-gate voltages V_{bg} (stages 1 and 3) and V_{bg2} (stage 2) are nominally set to 2.0 V, and V_{bg2} can be varied to implement the LNA's variable gain function.

The nominal V_{bg2} value of 2.0 V was chosen in order to implement a flexible design, capable of reducing its performance metrics (gain and NF) by decreasing the overdrive voltage on the devices in the second stage through the lowering of the high-valued V_{bg2} from the nominal 2.0 V down to -0.3 V. This leads to an LNA design that can efficiently trade-off power for performance, targeting around 10 dB of gain control through the V_{bg2} tuning of the 2nd stage.

The bias of the first stage is kept un-modified so as to maintain approximately the same noise-performance (dominated by the input stage) in all states of the overall LNA.

Similarly, the bias of the third stage is kept un-modified so as to maintain approximately the same linearity (OIP3 and P1dB) performance (dominated by the output stage) in all states of the overall LNA.

B. Degeneration Inductors and Input Matching

The degeneration inductors L_s at the common-source (CS) FETs are included to help stabilize the amplification stages and to tune the input impedance of the first stage such that matching can be achieved using a single series input spiral inductor L_{in}. This approach minimizes the complexity of the input matching network prior to the first stage, thereby minimizing the impact of that network on the overall NF of the LNA. The first stage is sourced-matched close to Γ_{opt} in order to achieve close to minimal noise-figure performance.

C. CG to CS Noise Isolation

Inductors L_{sd} are placed in between the CS and common-gate (CG) transistors in each amplification stage to resonate-out capacitive parasitics at the node between these FETs and to suppress the noise contribution of the CG transistor.

D. Transformer Load: Gain-Peaking and Bandwidth Increase

Inductors L_d are included at the drain nodes of the CG devices to resonate-out the drain capacitances and peak the gain, while inductors L_g are included at the gate node to increase the cascode gain of each stage. However, large values of L_g tend to render the CG stage unstable, but this is compensated for by introducing coupling between L_g and L_d. During the design, L_g is introduced to boost the gain, and then coupling (k) is introduced with L_d to achieve stability [4].

Furthermore, L_g and k (the coupling factor of the transformer) can be tuned to trade-off peak gain at a single frequency versus a flatter and wider-band response of the gain. This was exploited in this work, where it was determined that using values of L_g and L_d of 150 pH along with a coupling factor of 0.5 between them achieved a wideband response for the amplifier, from 42 to 67 GHz.

E. Substrate Impact on Inductor Quality Factor

Beyond the entire LNA being fabricated on different substrates (results to be discussed in Section III.D), standalone two-port inductor devices were also fabricated and measured. One such device is depicted in Fig. 2. It is a 1.5 turn spiral inductor (190 pH) implemented in the topmost copper metal layers of the technology. It has a very similar topology, layout, inductance value and operation frequency as the 1.5 turn input inductor L_{in} (150 pH) of the 42-67 GHz LNA.

The inductor's measurements were performed on all wafers and deembedded using dedicated open and short structures. The self-inductance and overall quality factor values were extracted from the two-port data from the Y_{11} parameter, and the results are plotted in Fig. 2. The data demonstrates an appreciable increase in the inductor quality factor on the high resistivity substrate option, achieving a peak value close to 30, compared to a peak value just above 20 on the standard substate, with little impact on the inductor value.

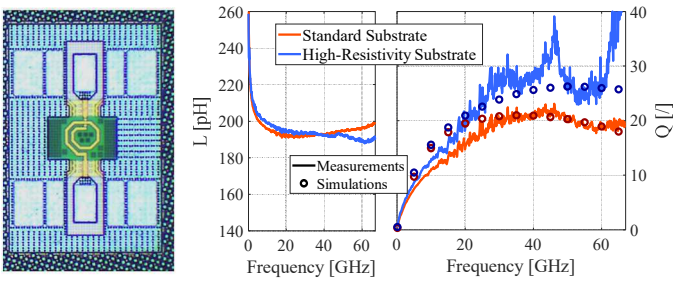

Fig. 2. Photograph and extracted parameters of a standalone 2-port inductor.

III. Measured Results

The fabricated LNA was measured on-wafer (GSG probes) using a noise-figure setup under 50 Ω based on a UXA-X-N9042B signal analyzer from Keysight and a 60 GHz noise-source. For S-parameter measurements, a Keysight N5291A VNA was employed with frequency extenders up to 110 GHz.

A. Nominal Performance on Standard Substrate

The measured S-parameter and noise-figure results are plotted in Fig. 3 under the nominal bias condition of V_g of 0.37 V, V_{bg} of 2.0 V, and V_{dd} of 1.1 V. At this bias the 3-stage LNA draws a DC power of 13.7 mW and achieves a peak gain of 21.0 dB, with its 3 dB-bandwidth spanning approximately 25 GHz, from 42 to 67 GHz.

The amplifier is well matched in that band, with the measured S_{11} being below -10 dB from 47 to 69 GHz. S_{22} is below -10 dB from 46 to 69 GHz.

The measured noise figure of the amplifier achieves a minimum value of 3.8 dB in the 50 to 60 GHz range.

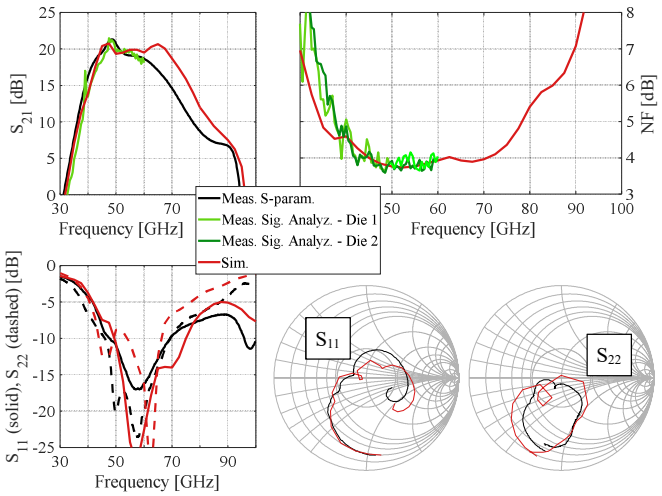

Fig. 3. Measured and simulated performance of the LNA at nominal bias.

B. Model-Hardware Correlation

Fig. 3 also plots simulation results for the LNA at nominal bias. The correlation is excellent in terms of the S-parameter data, with in particular the two in-band resonant behaviours of S_{11} and S_{22} close to the centre of the smith chart being well captured. The gain S_{21} is also well modelled, in terms of in-band peak value, general shape, and out-of-band roll-off, though a slight decrease in its upper-bandwidth is observed.

The simulated NF data is also in excellent agreement with the measurements (limited to 60 GHz by the noise-source), with the in-band values over frequency being well predicted.

C. Variable-Gain Operation

The LNA's V_{bg2} can be tuned to trade-off performance (gain and NF) for DC power consumption. Measurement results pertaining to those states are plotted in Fig. 4, demonstrating that 10 dB of variable-gain control is achieved through the proposed tuning of the back-gates in stage 2.

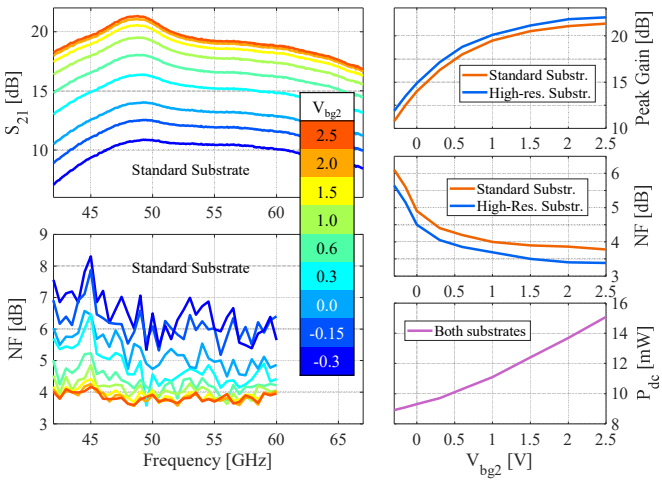

Fig. 4. Gain, NF and P_{dc} variations as a function of applied V_{bg2}.

The overall NF is affected, particularly in the low-gain settings, and increases up to a value of 6.1 dB of average value (in the 50-60 GHz range) for the lowest-gain mode, which remains acceptable for 60 GHz applications, particularly when considering that low-gain settings are to be employed when the input signal is large, i.e. when the input SNR is high.

Fig. 4 also plots the gain and NF variations as a function of the applied V_{bg2} control voltage, and also highlights the effect on the decreased power-consumption at lower gain settings, with the LNA drawing a reduced 8.9 mW for V_{bg2} at -0.3 V

D. Substrate Impact

Fig. 5 plots and compares the RF performance results of the LNA fabricated on both the high- and the standard-resistivity substrates. Several dies were measured at equivalent nominal bias on both wafers (results of 2 dies shown), and Fig. 5 demonstrates clearly that the LNA's performances are improved by approximately 0.9 dB in gain and 0.4 dB in NF using the less lossy silicon substrate. These improvements are supported in magnitude by the associated simulation results, with the silicon resistivity being adapted in the electro-magnetic environment associated to the full layout simulation.

The 0.4 dB improvement in NF is mainly attributed to an increased quality factor of the input inductor L_{in} situated prior to the first amplification stage, that sees its peak Q-factor value increase from 22 to 31 in our EM simulation results (not shown). Those simulations are backed-up by the measurement of a standalone inductor similar to L_{in} on the same chips, whose results were presented in Section II.E. The 0.9 dB increase in gain is impacted by decreased losses in all passives of the design. Fig. 4 shows that these improvements are more or less constant over the entire measured tuning-range (V_{bg2}).

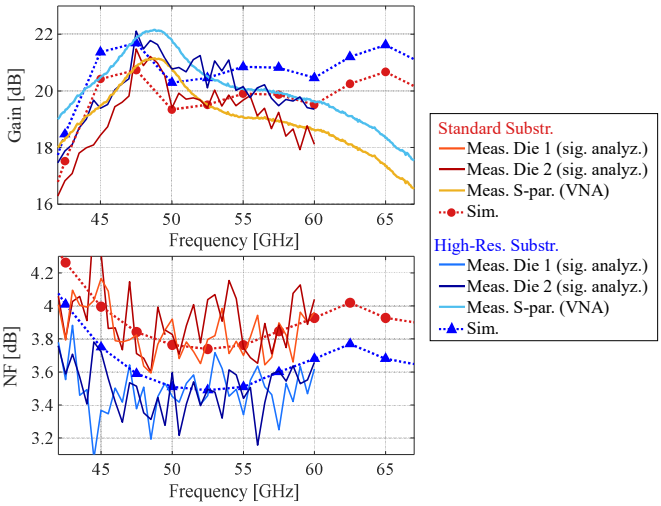

Fig. 5. Gain and NF measurements (in-band) of the LNA (at its nominal bias point) implemented on standard- and high-resistivity substrates.

E. Benchmarking

The performances of the presented LNA are recapped in Table 1 and compared to state-of-the art CMOS LNAs at 60 GHz from the published scientific literature [4-15], with [13-15] being variable-gain designs. The following FoM is utilized for the benchmarking [4, 7], and overall, the proposed LNA offers amongst the highest score, with high values being maintained even in the low-power/low-gain modes.

$$\mathrm{FoM} = 20\log_{10}\left(\frac{\mathrm{Gain[lin.]}\times\mathrm{BW[GHz]}}{\mathrm{P_{dc}[mW]}\times(\mathrm{NF[lin.]}-1)}\right) \quad (1)$$

Table 1. Performance Benchmarking Against State-of-the-Art CMOS LNAs Operating Close to 60 GHz.

Reference		Technology	Topology	Peak Gain [dB]	Bandwidth (span) [GHz]	NF (min.) [dB]	P_{DC} [mW]	Area [10^{-3} mm²]	FoM
[5]	RFIC15	32 nm SOI	4-stage CS differential, transformers	21	51.2-61.8 (10.6)	3.3	18	800[$,*]	14.7
[6]	RFIC16	40 nm CMOS	2-stage cascode	15	48-61 (13)	3.6	20.4	200[$]	8.9
[7]	RFIC18	22 nm FinFET	2-stage CS differential, transformers	20	68.6-79 (10.4)	4	10.8	65[$]	16.1
[4]	TMTT20	22 nm FD-SOI	3-stage cascode, transmission lines	20	70-82 (12)	4.6	9	150[$]	17.0
[8]	MWCL21	22 nm FD-SOI	2-stage cascode	18.1	49.8-68.1 (18.3)	4.4	3.6	392, 255[$,*]	27.3
[9]	RFIC22	28 nm FD-SOI	3-stage cascode	17.1	76-81 (5)	5.5	29.4	18[$,*]	-6.4
[10]	EuMIC22	16 nm FinFET	2-stage differential	17	75.5-83.5 (8)	4.5	31	54[$,^]	0.0
[11]	IMS23	45 nm RF-SOI	3-stage CS differential, transformers	23.4	56.2-69.8 (13.6)	4.85	13.3	138[$]	17.3
[12]	IMS23	55 nm CMOS	4-stage differential, transformers	17.1	74.8-88.8 (14)	6.4	24.3	107[$]	1.8
[13]	ISSCC16[&]	28 nm CMOS	4-stage differential, transformers	18-29.6[&]	68-97 (30.7-28.3[&])	7.8-6.4[&]	11.7-31.3[&]	225[$,*]	12.4 - 18.2
[14]	RFIC20[&]	65 nm CMOS	3-stage differential, transformers	8-25[&]	53.5-61 (7.5)	n/a-4.8[&]	25-47[&]	260, 95[$,*]	n/a - 2.9[&]
[15]	EuMIC22[&]	22 nm FD-SOI	2-stage differential	14-20.4[&]	76-86[*] (10)	6.6-5.9	32-60[&]	100[$,*]	-7.1 - -4.4[&]
This work	EuMIC24[&]	22 nm FD-SOI	3-stage cascode	10.8-21.0[&,µ]	42-67 (25)	6.1-3.8[&]	8.9-13.7[&,µ]	170[$]	10.0 - 23.3[&,µ]
		22 nm FD-SOI with HR substrate[x]		11.9-21.8[&,µ]		5.6-3.4[&]			12.5 - 25.5[&,µ]

[$] without pads (core). [&] variable gain (VG). [*] Estimation. [^] Excluding balun. [x] With interface passivation. [µ] Considering V_{bg2} up to 2 V.

IV. Conclusion

This paper described the design and implementation of a wideband and low-power LNA at 60 GHz using GlobalFoundries' 22 nm FD-SOI technology. On standard-resistivity substrate, the proposed design achieves 3.8 dB of minimal noise-figure in-band for a peak gain of 21 dB at its nominal bias for a 13.7 mW power-consumption using a low supply voltage of 1.1 V, and can achieve an NF down to 3.4 dB and gain up to 21.8 dB when implemented on a high-resistivity substrate, explored for the first time in a mm-wave LNA design in FD-SOI in this paper.

On top of that, the LNA can be configured as a variable-gain device by making use of the unique back-gate bias node of the 22FDX® technology. In that case, a 10 dB gain control is achieved over a 2.3 V bias range at the back-gates, while maintaining a good NF value.

Overall, the proposed design achieves excellent results with respect to the state of the art (see Table 1), reporting low NF and low power and achieving a high FoM score, while consuming a modest amount of chip area (0.17 mm²).

Acknowledgment

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