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Impact of Device Layout on Self-Heating Extraction in MOSFETs☆

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ABSTRACT

This work analyses the impact of device layout on self-heating (SH) extraction and treats it in terms of parasitic series resistance and heat evacuation paths. Specifically, the impact of having four-terminal (4T) gate access structures used in gate resistance technique for SH characterization is investigated. To evaluate the SH parameters, the RF characterization technique is utilized, which includes measuring S-parameters over a wide frequency range. Two devices are compared in this study based on the same core MOSFET: one with the 4T gate access structure and one without these additional accesses. It is experimentally demonstrated that a lower thermal resistance is observed for the 4T device. Apart from cooling through the 4T gate accesses which could explain this observation, it is seen that parasitic series resistances could also affect the extraction of thermal resistance through the RF technique. Through PDK simulations, the impact of the series resistances on SH extraction using the RF technique is explored further. The fact that even for the same core device the layout can affect the extracted thermal parameters is evidenced.

1. Introduction

The downscaling of CMOS technology has raised concerns of the self-heating (SH) effect in advanced nodes. With reduced dimensions, state-of-the-art devices face higher current and power densities that raise device temperatures [1]. Additionally, the buried oxide (BOX) in fully depleted silicon-on-insulator (FDSOI) technology which provides electrical isolation of the channel has much lower thermal conductivity compared to that of bulk Silicon [2]. Both the aforementioned factors could aggravate SH issues in state-of-the-art devices. With the undesirable effects resulting from elevated device temperatures because of SH (such as reduced mobility, threshold voltage shift, reduced reliability, etc.) widely reported in literature [3], it becomes important to have an accurate evaluation and modelling of SH in advanced devices.

With various characterization approaches used to estimate SH features in practice, the advantages and disadvantages of the most prominent techniques have been discussed in different studies [34]. For advanced MOSFETs with smaller thermal time constants, SH characterization methods like pulsed IV technique and AC conductance technique are deemed inaccurate due to technological limitations from a measurement perspective [3]. Two main techniques that are thereby left suitable for SH assessment in state-of-the-art devices are the gate resistance technique [5] and the RF technique [6]. The gate resistance technique (also referred to as gate resistance thermometry in literature) evaluates SH from the temperature variation of the gate resistance using a simple DC measurement process, however, requiring special test structures with additional gate accesses. Generally, a four terminal (4T) gate access structure is used in this technique with two terminals for forcing a current and two others sensing voltage which aids in calculating the gate resistance more accurately. The RF technique, on the other hand, evaluates SH from the frequency variation of output conductance g_d and the temperature variation of drain current I_d. SH parameters (thermal resistance R_{th} and channel temperature rise ΔT) extracted by means of these techniques are often compared and the difference is attributed to the inner device features itself. However, one needs to pay attention to the fact that device configuration has an important impact on the extracted features not only due to difference in the "inner" device configuration (and thus heating and heat evacuation) but also due to different parasitic elements and heat evacuation paths. In this work we demonstrate this based on experimental data for specially designed 4 T gate access RF FET (used for SH estimation with the gate resistance and RF techniques), complemented by product design kit (PDK) simulations of series resistance effect.

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1.1. Experimental details and approach

The device used in this study originates from the 22FDX® from GlobalFoundries [7]. The core FET is an nMOSFET in the common-source configuration of total width of 30 μm.

Fig. 1 shows the layout of the 4T RF test structure (with additional DC pads/accesses to the gate) which allows the application of both the gate resistance and the RF technique to the same device. This device is compared with a standard version of the RF device without the additional DC contacts to the gate (namely Gate2, Gate3 and Gate4 in Fig. 1). While Gate1 and Drain terminals are connected to the central RF signal pad, the source is connected to the ground pads. Thus, in this work, two devices based on the same core FET are studied; one with 4T gate contacts and one without them labelled "4T" and "no 4T", respectively. The assessment of the devices is done solely using the RF technique here; a detailed discussion of the gate-resistance technique is beyond the scope of this work. It is to be noted that in the measurements in this study, the additional DC contacts on the gate (Gate2, Gate3 and Gate4) are left floating.

RF measurements are realized using the MPI TS3000-SE probe station; S-parameters are measured with a VNA in a frequency range from 100 kHz to 1 GHz, de-embedded with dedicated open de-embedding structures and converted to Y parameters. Two Ground-Signal-Ground RF |Z| probes with a pitch of 100 μm are utilized for these measurements. These probes are designed to withstand high temperatures, up to the required value of 125 °C.

To comparatively assess self-heating characteristics, the RF characterization technique, a frequency domain method, is employed. Recent findings have highlighted this technique as particularly adept for self-heating characterization in highly advanced, deeply miniaturized state-of-the-art devices [3]. This is because achieving dynamic self-heating-free conditions in these devices requires reaching frequencies up to the gigahertz range. The output conductance (g_d) is computed as the real part of Y_{dd}, transconductance (g_m) is the real part of Y_{dg}. The g_d versus frequency curve and the drain capacitance C_{dd} versus frequency curve exhibit transitions attributed to self-heating (SH), enabling the assessment of SH-related characteristics such as thermal resistance (R_{th}) and thermal capacitance (C_{th}). It is worth noting that the transition in g_d with frequency arises not solely from self-heating effects, but also from the substrate and back-gate network [89]. In this context, the significance of the zero-temperature coefficient (ZTC) point, where dynamic self-heating is absent, has been demonstrated in [8]. The transition due to the substrate network is removed by considering the transition in g_d at this zero-temperature coefficient (ZTC) point for both the devices studied. R_{th} can then be extracted using (1) given below [10]:

$$R_{th} = \frac{\Delta g_d}{\left(I_d + V_d g_{d,LF}\right)\partial I_d/\partial T} \quad (1)$$

where Δg_d is the difference between g_d at low and high frequencies of 100 kHz and 1 GHz, I_d is the DC drain current, $g_{d,LF}$ is the output conductance g_d at low frequency (100 kHz) and $\partial I_d/\partial T$ is the slope of the I_d versus temperature plot extracted from I_d-V_g curves measured in a temperature range from 25 up to 125 °C (with a step of 25 °C). To maintain a consistent temperature during measurements, the entire system is allowed to stabilize for a minimum of half an hour to ensure temperature equilibrium at each temperature point. The measurements are conducted under saturation conditions with a drain voltage (V_d) of 0.8 V, while the back gate is kept grounded ($V_{bg} = 0$ V).

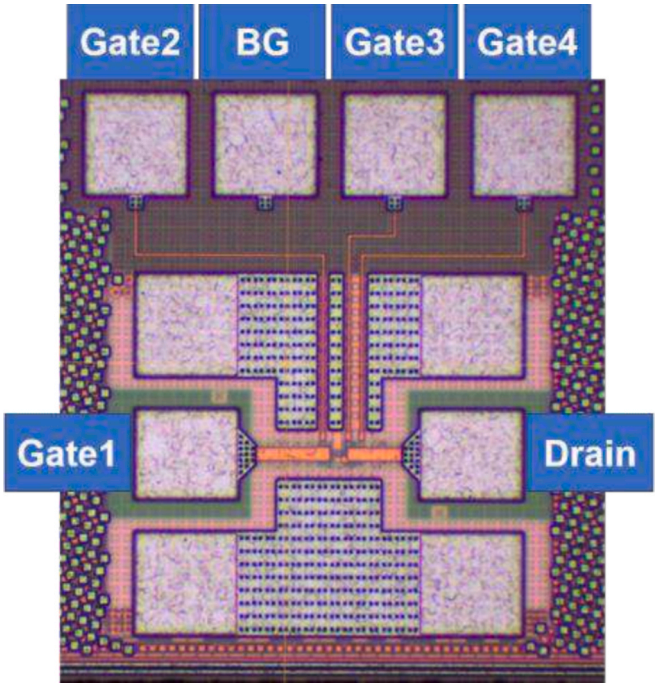

Fig. 1. 4T device layout with the two RF and four DC pads.

2. Results and discussion

The DC characteristics of the devices with 4T additional gate terminals and without them (labelled "4T" and "no 4T", respectively) are similar in terms of threshold voltage, allowing for a direct comparison of their SH features. This can be seen from the I_d-V_g and g_m-V_g characteristics in linear and saturation regimes shown in Fig. 2 and Fig. 3, respectively. However, the difference in magnitude of I_d and g_m in strong inversion in linear regime clearly appears (Fig. 2). This difference can be related to different series resistances in the devices, which in turn can be either due to process variability or layout related effects. Lower I_d attributed to the higher source-drain resistance R_{sd} is seen in 4T FET in linear regime (Fig. 2). It is worth noting that as power dissipation is very low in this bias condition, SH related effects are neglected. However, the difference in IV curves for the two configurations becomes smaller in saturation with heating coming into play (Fig. 3).

Fig. 4 shows the variation of output conductance g_d with frequency for the 4T and no 4T device at $V_d = 0.8$ V and two different V_g biases of 0.8 and 0.9 V. The higher value of g_d obtained for the 4T FET for the two different biases demonstrates the fact that it is less affected by SH compared to the standard no 4T FET.

In Fig. 5, the variation of drain current I_d normalized with respect to the value at 25 °C with temperature is shown. The higher I_d versus

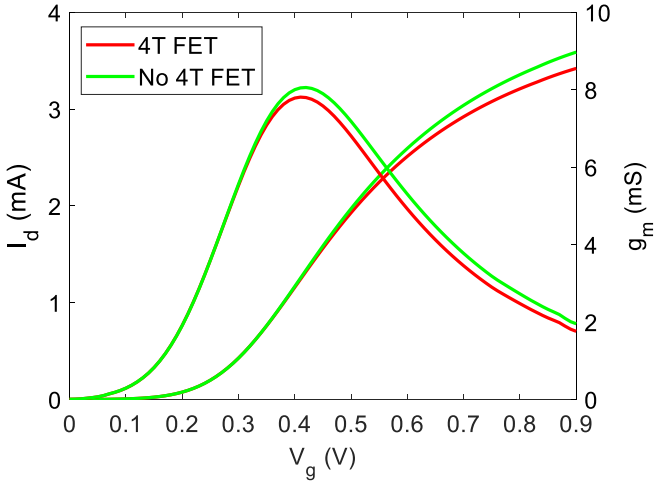

Fig. 2. Drain current I_d and output conductance g_d versus gate voltage V_g for 4T and no 4T device in linear at $V_d = 50$ mV.

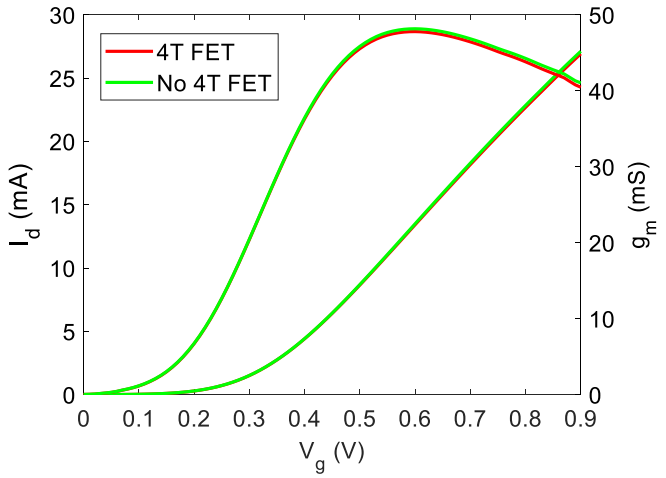

Fig. 3. Drain current I_d and output conductance g_d versus gate voltage V_g for 4T and no 4T device in saturation at $V_d = 0.8$ V.

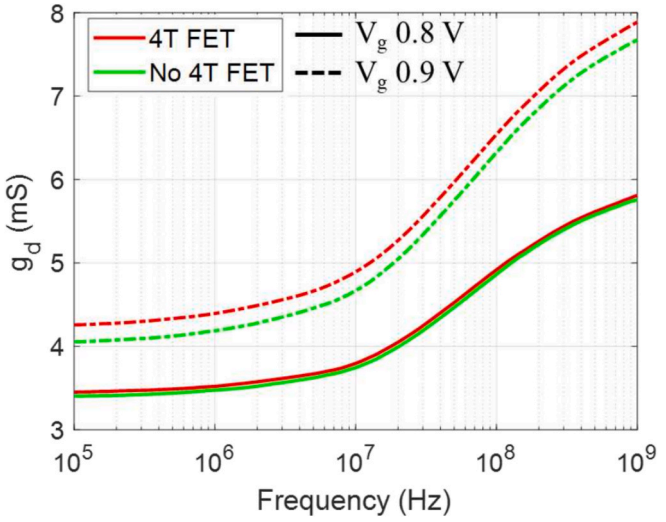

Fig. 4. Output conductance g_d versus frequency for 4T and no 4T device at $V_d = 0.8$ V and V_g 0.8 and 0.9 V.

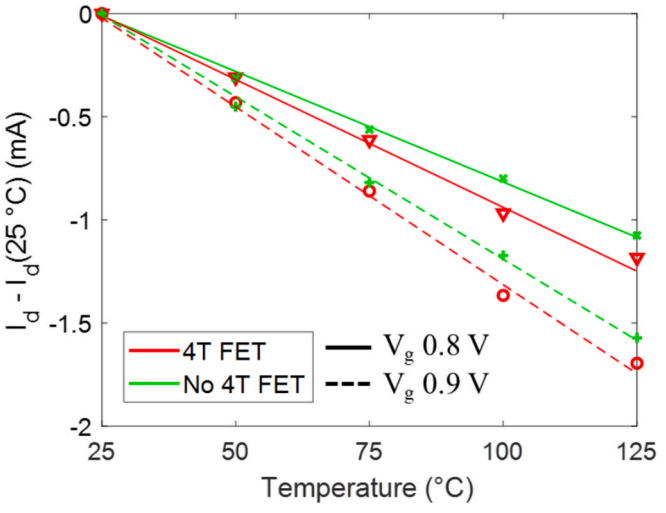

Fig. 5. Drain current I_d vs temperature for 4T and no 4T device at $V_d = 0.8$ V and V_g 0.8 and 0.9 V.

temperature slope (i.e. a steeper slope) for 4T FET demonstrates lower SH. The reason for the above can be seen in [10] as dI_d/dT is higher at higher temperatures is representative of higher SH computed from I_d versus temperature. For a V_d of 0.8 V, two different bias conditions in V_g of 0.8 V and 0.9 V are considered and the aforementioned trends are verified for both cases. At V_g 0.9 V, a higher dI_d/dT is seen as this bias point is further away from the ZTC and device heats stronger than the V_g 0.8 V case.

In Table 1, the SH features such as R_{th} and ΔT extracted from experimental results of the RF technique are shown. One can see 18 % lower R_{th} obtained for the 4T FET case compared to its no 4T counterpart, which is in line with the above observations (Figs. 3–5). Keeping in mind that the core FET ("inner" device) is the same in both configurations, we suggest that the difference in the extracted SH features arises from the different layout/accesses. This difference in extracted thermal parameters can arise from (i) thermal evacuation paths and (ii) parasitic series resistance. Indeed, one can expect more efficient cooling from the accesses in 4T device with larger or more developed heat evacuation path. This hypothesis is in line with our previous works having demonstrated that a heat sink connected to the gate of a device can reduce R_{th} by 8–20 % depending on the sink configuration and area [1011]. From a technique point of view, the actual device R_{th} is therefore underestimated due to the gate accesses themselves acting like heat sinks. This points out one of the possible limitations of the gate-resistance technique.

Apart from this, another reason for the difference in the extracted thermal features could be different series resistances in those devices, which can be either due to variability or layout related effects. In order to study the impact of series resistances further, simulations using the PDK model with various series resistances added to the MOSFET are made to observe their effect on SH parameters extracted using the RF technique. By adding external resistances on the source, drain and gate terminals (R_s, R_d and R_g respectively), this impact is estimated. It is observed that R_g impacts only the gate related transition in g_d versus frequency which comes into play at frequencies around 8–10 GHz; therefore the impact of R_g on SH extraction in our devices is very limited. This observation is in agreement with experiments reported in [12] where the transition due to gate resistance is reported to come into play at around 10 GHz. Although R_g does not have much impact on the extraction of SH parameters, it is noticed that R_s and R_d have a pronounced impact on both the g_d versus frequency and $\partial I_d/\partial T$ (increasing $g_{d,LF}$ and magnitude of $\partial I_d/\partial T$) for SH extraction. This is due to the difference between external applied bias and the one seen by the inner device arising due to a drop in voltage across these resistances. If the biases on the drain, gate and source seen by the inner device are V_d*, V_g* and V_s* respectively, it must be kept in mind that these values are different from the corresponding external biases V_d, V_g and V_s ($V_s = 0$ V). This arises from voltage drops from the series resistances; while V_g* is very close to V_g due to the low gate current I_g, the voltage drop due to I_d across R_d and R_s causes V_d* and V_s* to differ respectively. While R_d affects the V_d seen by the inner device, the relation with R_s is more complicated as it changes V_s which in turn affects both V_{gs} and V_{ds} in the common-source configuration used here. In this work, we shall only focus on just the impact of R_d. The impact of R_d on the g_d transition is illustrated in Fig. 6 and the corresponding change in thermal parameters is seen in Table 2. It is seen that varying R_d affects $g_{d,LF}$ quite strongly and Δg_d slightly. From PDK simulations, the percentage variation in R_{th}

Table 1
Measured self-heating parameters on 4T and no 4T device. $V_G = V_D = 0.8$ V.

Device	$g_{d,LF}$ (mS)	Δg_d (mS)	I_d (mA)	$\partial I_d/\partial T$ (μA/K)	R_{th} (Kμm/mW)	ΔT (°C)
4T FET	3.46	1.69	22.7	12.11	164	99
No 4T FET	3.4	1.81	22.85	10.54	201	123

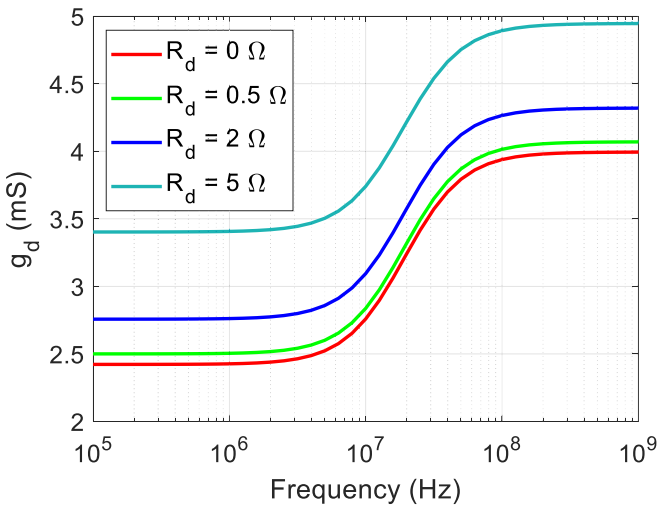

Fig. 6. Output conductance g_d vs frequency from PDK model at $V_d = V_g = 0.8$ V for varying series drain resistance R_d.

Table 2
Pdk model: impact of Rd on self-heating parameters. $V_G = V_D = 0.8$ V.

R_d (Ω)	$g_{d.LF}$ (mS)	Δg_d (mS)	I_d (mA)	$\partial I_d/\partial T$ (μA/K)	ΔT (°C)	R_{th} (Kμm/mW)
0	2.42	1.57	22.74	12.8	90.43	149.12
0.5	2.5	1.57	22.72	12.83	89.98	148.51
2	2.76	1.56	22.64	12.92	88.01	145.78
5	3.4	1.54	22.46	13.12	83.76	139.85

is ~2 % in the case of low added drain resistance of 2 Ω but can go up to 6 % and higher if this resistance is increased to 5 Ω which results in a 1.2 % drop in the dissipated power. It is therefore established that the estimated R_{th} is dependent on the series resistances that need to be taken into account for the SH extraction process. This implies that for the DC I_d versus temperature measurements, correcting for R_d would be necessary otherwise resulting in an underestimated value of R_{th}. Detailed analysis of the impact of all the series resistances provides scope for further work.

3. Conclusion

Our work demonstrates that special care needs to be taken when comparing different techniques and device configurations or layouts from a self-heating perspective. Additional gate accesses used for the gate resistance technique for SH characterization may cause cooling through them resulting in an underestimation of the actual thermal resistance. For the RF characterization technique, it is demonstrated from PDK simulations that the series resistances affect the extraction of the thermal parameters by affecting two major parameters, namely the output conductance variation with frequency and the slope of drain current with temperature. Observed differences should not only be attributed to the inner device but also to non-negligible layout/configuration effects.

CRediT authorship contribution statement

Arka Halder: Writing – original draft, Methodology, Investigation, Formal analysis, Conceptualization. **Martin Vanbrabant:** Writing – review & editing, Formal analysis. **Dimitri Lederer:** Writing – review & editing, Supervision. **Jean-Pierre Raskin:** Writing – review & editing, Supervision, Formal analysis. **Valeriya Kilchytska:** Writing – review & editing, Supervision, Formal analysis.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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Data availability

No data was used for the research described in the article.

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