



UNIVERSITÉ CATHOLIQUE DE LOUVAIN
ICTEAM INSTITUTE
Louvain-la-Neuve

Silicon-on-Insulator Optoelectronic Components for Micropower Solar Energy Harvesting and Bio-Environmental Instrumentation

Jury

Olivier Bulteel

Prof. D. Flandre (Advisor)
Prof. J.-P. Raskin
Prof. F. C. Dualibe
Prof. M. A. Pavanello
Dr. A. Afzalian
Prof. M. Verleysen (President)

Thesis presented for
the degree of Ph.D.
in Engineering Sciences

SEPTEMBER 2011

Acknowledgments

First of all, I would like to sincerely thank Prof. Denis Flandre, my advisor, for his support during these five years. His encouragements and his technical advices were more than helpful during this work. I particularly express my gratitude for the attentive and very long hours of discussion, second readings, corrections and for the trust he placed in me.

I also would like to thank Prof. Jean-Pierre Raskin, for his help during my thesis, his scientific comments and his kindness and humor. I express a special thank to Dr. Aryan Afzalian for his interest in optoelectronics, his attentive reading and constructive comments on this dissertation.

I am very grateful to Profs. Marcelo Pavanello and Carlos Dualibe for their careful reading of my thesis, their remarks and reflexions on my work. And finally, I express my gratitude to Prof. Michel Verleysen for his time concerning administrative/academic matters during these five years, to Dr. Sorin Melinte for his comments on solar and UV applications and to Prof. Laurent Francis for his help and his reflexions on this work.

I sincerely thank the members of the laboratory who contributed to the realization of this work. Especially, thanks to Miloud Zitout for all the circuit encapsulations, thanks to Pascal Simon for his help concerning setup experiments, thanks to Pierre Gerard for his precious help in signal acquisition and his time during the debugging sessions. Thanks to David Spôte and Emmanuel De Pauw for their time during various experiments and to Pascal Dupuis for the first DNA experiments and his useful tips when dealing with statistics. Also, thanks to the research teams of Profs. Jean-Luc Gala and Benoît Macq for their availability during the first DNA measurement campaigns. Thanks to Valeria Kilchytska, Nicolas André, David

Bol, Romain Delamare and Bertrand Rue for various help tips. Thanks to Brigitte Dupont for her availability for computer issues. Many thanks to Michelly De Souza for her collaboration on low-temperature characterization and to Geoffroy Gosset for the solar energy harvesting circuits characterization. A special thank to Nancy Van Overstraeten for the long hours concerning biological experiments. Her analyses and suggestions, particularly in the fourth chapter, constitute a very useful contribution to this work. Last but not least, a very special thank to André Crahay and Christian Renaux for their advices about SOI process, their friendship and listening time during these five years.

And finally, I would like to thank my parents and the rest of my family for their support. Thanks to all my friends for their encouragements and especially to my housemates during the thesis period and to Laureline for her encouraging quotes.

Abstract

This work presents an analysis of optoelectronic components fabricated in silicon-on-insulator (SOI) technology. On one hand the thesis focuses on UV sensors ($\lambda < 400nm$) for bio-environmental applications, and on the other hand it studies integrated solar cells for solar micropower harvesting.

The SOI technology features a thin Si film (with a thickness of $80nm$) in which lateral PIN photodiodes are optimized. The responsivity is modeled to optimize the spectral response in UV by adequate choices of anti-reflection coatings. The best simulated SOI photodiode can reach efficiency up to $0.18A/W$ at $\lambda = 400nm$ with a dual layer anti-reflection coating of SiO_2/Si_3N_4 and metal lines of minimal dimensions. Other structures based on silicon-on-nothing and membrane technologies are also investigated and reach efficiencies of $0.28A/W$ around $\lambda = 400nm$.

A current-to-frequency integrated circuit is designed to interface the UV photodiodes for biomedical or environmental instrumentation. The circuit, consisting of a Miller operational amplifier and a Schmitt trigger, consumes a total power of $27\mu W$ and is linear with respect to the responsivity of the photodiode on a range of 3 decades. The design of the amplifier and a comparison of three Schmitt triggers are presented. A deep analysis of the noise is described with its influence on the thresholds of the trigger. Improvements are presented to increase the optical dynamic up to 6 decades by reducing the minimal detectable signal when increasing the power consumption of the amplifier.

The SOI sensors are used to quantify the concentration of biological material (DNA, bacteria, proteins, ...) by UV transmittance. The UV source is implemented by low wavelength LEDs which directly illuminate the sample contained either in PCR tubes, or in well microplates or in PDMS channel. The optoelectronic transducer (i.e. the photodiode or the complete photosensor) is used to measure the

transmitted light through the samples. The best quantification is achieved with the complete UV photosensor for which DNA is quantified on a range from $400ng/\mu L$ to $40fg/\mu L$, within PCR microtubes. BSA is quantified in a range from $10\mu g/\mu L$ to $1pg/\mu L$ in well microplates. In the PDMS channel, BSA is also quantified from $10\mu g/\mu L$ to $1pg/\mu L$ while DNA is quantified from $10\mu g/\mu L$ to $10pg/\mu L$.

The SOI substrate is also used to integrate novel lateral solar cells, embedded under the buried oxide. Under no active region of the SOI wafer, ungated solar cells reach efficiencies from 10.5% up to 15% for outdoor and indoor irradiances respectively. However, gated solar cells can be fabricated under active region of the SOI wafer and the efficiencies increase from 12% to 22% for outdoor and indoor irradiances respectively by applying a +50V frontgate voltage. A combined Atlas-Matlab approach ensures a good modeling for the behavior of these devices. A lumped-element modeling is also presented for circuit simulator integration. It fits perfectly with the measured curves of the solar cells for each illumination.

Finally, it is proved that miniaturized SOI solar cells can be designed for supplying various specific integrated circuits. For the case of our $27\mu W$ complete photosensor, the die areas needed are $0.21mm^2$ and $1.14mm^2$ for outdoor and indoor irradiances respectively for gated solar cells with maximal +50V frontgate voltage.

Scientific Publications

Conference proceedings

"Conception d'un photocapteur à basses longueurs d'onde pour des mesures environnementales ou biomédicales", **O. Bulteel**, A. Afzalian and D. Flandre, Proceedings of TAISA 2007, 8e Colloque sur le Traitement Analogique de l'Information, du Signal et ses Applications, Lyon/France, October 18-19, 2007.

"Development of New Micro- and Nano- Bio- and Environmental SOI-Sensors at UCL", L. Moreno Hagelsieb, R. Pampin, **O. Bulteel**, B. Olbrechts, N. André, B. Rue and J.-P. Raskin, Proceedings of the BioForum 2007 - 11th Edition, Liège/Belgium, October 11, 2007.

"Development of New Micro- and Nano- Bio- and Environmental SOI-Sensors in UCL", L. Moreno Hagelsieb, R. Pampin, **O. Bulteel**, B. Olbrechts, N. André, B. Rue, J.-P. Raskin and D. Flandre, Proceedings of the Scientific workshop: Microsystems as a Platform for Integrating Micro/Nano/Biotechnologies, Bucharest/Romania, May 23-25, 2007.

"Development of Micro- and Nano- Bio- and Environmental SOI-Sensors", L. Moreno Hagelsieb, R. Pampin, **O. Bulteel**, B. Olbrechts, N. André, B. Rue, J.-P. Raskin and D. Flandre, Proceedings of the Workshop on MEMS and Nanotechnology through Science and Applications, Louvain-la-Neuve/Belgium, March 18, 2008

"Low-cost miniaturized UV photosensor for direct measurement of DNA concentration within a closed tube container", **O. Bulteel**, P. Dupuis, S. Jeumont, L.M. Irengue, J. Ambroise, B. Macq, J.-L. Gala and D. Flandre, Proceedings of the fourth

European Congress for Medical and Biomedical Engineering 2008, Antwerpen/Belgium, November 24-27, 2008.

"Direct Measurement of DNA Concentration within a closed tube container by UV light transmission and lateral p-i-n photodiode read-out in SOI technology", **O. Bulteel**, P. Dupuis, S. Jeumont, L.M. Irenge, J.-L. Gala and D. Flandre, Proceedings of the fourth focused workshop on electronic recognition of bio-molecules, Liège/Belgium, September 10-12, 2008.

"SOI Sensors Advantages for Consumer and Health Monitoring Applications", L. Moreno Hagelsieb, N. André, T. Kezai, **O. Bulteel**, S. Druart, R. Pampin, B. Rue, B. Olbrechts, J.-P. Raskin and D. Flandre, Proceedings of the Commercialization of Micro and Nano Systems Conference - COMS 2008, Puerto Vallarta/Mexico, August 31 - September 4, 2008.

"High-efficiency solar cell embedded in SOI substrate for ULP autonomous circuits", **O. Bulteel**, R. Delamare and D. Flandre, Proceedings of the 2009 IEEE International SOI Conference, Foster City/CA/USA, October 5-8, 2009.

"Aluminium Oxide Based Sensors Integration for Medical and Health Monitoring Applications", L. Moreno Hagelsieb, N. André, G. Scheen, P. Gerard, Y. Nizet, X. Tang, **O. Bulteel**, P. Dupuis, L. Francis, J.-P. Raskin and D. Flandre, Proceedings of COMS'09, 14th Annual Conference on Commercializing Micro- and Nanotechnology, Copenhagen/Denmark, August 30-September 4, 2009.

"Aluminium Oxide Based Sensors for Medical Applications", L. Moreno Hagelsieb, N. André, P. Gerard, T. Kezai, Y. Nizet, X. Tang, **O. Bulteel**, L. Francis, J.-P. Raskin and D. Flandre, Proceedings of the 14th Biodetection Technologies Conference, Baltimore/MD/USA, June 25-26, 2009.

"SOI Lateral PIN Diodes for Temperature and UV Sensing in Very Harsh Environments", B. Rue, **O. Bulteel**, D. Flandre, M. de Souza and M.A. Pavanello, Proceedings of HiTEN'09, IMAPS International Conference on High Temperature Electronics Network, Oxford/UK, September 13-16, 2009.

"Optimization of blue/UV sensors using p-i-n photodiodes in thin-film SOI technology", **O. Bulteel** and D. Flandre, Proceedings of the International Symposium on Silicon on Insulator Technology and Devices, San Francisco/CA/USA, May, 2009.

"Temperature Influence on the Behaviour of Lateral Thin-Film SOI PIN Photodiode in the Blue and UV Range", M. de Souza, **O. Bulteel**, D. Flandre, and M.A. Pavanello, Proceedings of the EuroSOI Conference 2010, Grenoble/France, January 25-27, 2010.

"Electrical Characterization of SOI Solar Cells in a Wide Temperature Range", M. de Souza, **O. Bulteel**, D. Flandre and M.A. Pavanello, Proceedings of the SOI Conference 2010, San Diego/CA/USA, October 11-14, 2010.

"Complete Microsystem Using SOI Photodiode for DNA Concentration Measurement", **O. Bulteel**, N. Van Overstraeten-Schlögel, P. Dupuis and D. Flandre, Proceedings of BIOCAS 2010, IEEE Biomedical Circuits and Systems Conference 2010, Paphos/Cyprus, November 3-5, 2010.

"Complete Microsystem Using SOI Photosensor for DNA Concentration Measurement", **O. Bulteel**, N. Van Overstraeten-Schlögel and D. Flandre, Proceedings of BLOWIN congress 2010, Louvain-la-Neuve/Belgium, December 8 , 2010.

"Disruptive ultra-low-leakage design techniques for ultra-low-power mixed-signal microsystems", D. Flandre, **O. Bulteel**, G. Gosset, B. Rue and D. Bol, Proceedings of FTFC 2011, Marrakech/Morocco, May 31-June 1st, 2011.

"Ultra-High-Efficiency Co-Integrated Photovoltaic Energy Scavenger", G. Gosset, **O. Bulteel**, P. Baijot and D. Flandre, Proceedings of SOI Conference 2011, Tempe/AZ/USA, October 3-6, 2011. *Accepted*

Articles in periodicals

"Optimization of blue/UV sensors using p-i-n photodiodes in thin-film SOI technology", **O. Bulteel** and D. Flandre, ECS Transactions on Device Technology II, Vol. 19, No. 4, pp. 175-180, 2009.

"Fully integrated blue/UV SOI CMOS photosensor for biomedical and environmental applications", **O. Bulteel**, A. Afzalian and D. Flandre, Analog Integrated Circuits and Signal Processing, Vol. 65, No. 3, pp. 399-405, Springer, 2010.

"Analysis of Lateral SOI PIN Diodes for the Detection of Blue and UV Wavelengths in a Wide Temperature Range", M. de Souza, **O. Bulteel**, D. Flandre and M. Pavanello, ECS Transactions on Optoelectronics, Vol. 31, No. 1, pp. 199-206, 2010.

Participation in books

"Low-wavelengths SOI CMOS photosensors for biological applications", **O. Bulteel**, N. Van Overstraeten-Schlögel, A. Afzalian, P. Dupuis, S. Jeumont, L. Irengé, J. Ambroise, B. Macq, J.-L. Gala and D. Flandre, Biomedical Engineering, Trends in Electronics, Communications and Software, pp. 257-276, Editor: Anthony N. Laskovski, Intech 2011

GLOSSARY

List of symbols

α	Absorption coefficient [m^{-1}]
ϵ	Permittivity [F/m]
η	Efficiency [%]
λ	Wavelength [m]
μ	Carrier mobility [$m^2/(V \cdot s)$]
σ_{Blank}	Standard deviation of a blank measurement [%]
σ_{eq}	Equivalent capture cross section [m^2]
τ_{eff}	Effective lifetime of the carriers [s]
Φ	Photon flux [$m^{-2}s^{-1}$]
ω_0	Dominant pole [rad/s]
ω_T	Gain-bandwidth product [rad/s]
$A_{v,0}$	Open loop gain voltage [V/V]
c	Vacuum speed of light [m/s]
C_{OX}	Oxide capacitance [F/m^2]
D_n, D_p	Diffusion coefficients of the carriers [m^2/s]
E_G	Bandgap energy [eV]
f_T	Transition frequency [Hz]
$\frac{g_m}{I_D}$	g_m over drain current ratio of the MOS transistors [V^{-1}]
G	Generation term [$m^{-3}s^{-1}$]
h	Planck's constant [$m^2kg \cdot s$]
$\bar{i}_n^2$	Power spectral density of current noise [A^2/Hz]
I_D	Diode current [A]
I_{Dark}	Diode dark current [A]
I_{Ph}	Diode photocurrent [A]
I_{RG}	Recombination-generation diode current [A]
I_S	Saturation current of a diode [A]
I_{SC}	Short-circuit current of a solar cell [A]
k_B	Boltzmann's constant [$m^2kg \cdot s^{-2}K^{-1}$]
L	MOSFET gate length [m]
L_{abs}	Absorption length [m]
L_F	Finger length [m]
L_i	Intrinsic length of a PIN diode [m]
L_n, L_p	Diffusion lengths of the carriers [m]
L_N, L_P	Cathode and anode lengths of a diode [m]

L_{ZD}	Depletion zone length of a PIN diode [m]
m	Number of fingers of an interdigitated photodiode
N	Refractive index
q	Unit electrical charge [C]
QE	External quantum efficiency [%]
QI	Internal quantum efficiency [%]
R	Responsivity [A/W]
R_C	Characteristic resistance of a solar cell [Ω]
R_S	Series resistance of a solar cell [Ω]
R_P	Parallel resistance of a solar cell [Ω]
S	Surface recombination velocity [m/s]
S_{Ph}	Photosensitive area [m^2]
t	Time [s]
t_{ARC}	ARC thickness [m]
t_{BOX}	Buried oxide thickness [m]
t_{OX}	Front oxide thickness [m]
t_{Si}	Thin Si film thickness [m]
t_{SUB}	Substrate thickness [m]
T	Temperature [$^{\circ}$] or [K]
$\bar{v}_n^2$	Power spectral density of voltage noise [V^2/Hz]
v_{th}	Thermal velocity of electrons [m/s]
V_D	Diode voltage [V]
V_{DD}, V_{SS}	High and low supply voltages [V]
V_{EA}	Early voltage [V]
V_{FB}	Flatband voltage [V]
V_{FG}	Frontgate voltage [V]
v_{GS}	Gate source voltage [V]
V_{HT}, V_{LT}	High and low threshold voltages of a trigger [V]
V_{OC}	Open-circuit voltage of a solar cell [V]
V_T	Thermal voltage [V]
V_{Tn}, V_{Tp}	MOSFET threshold voltage [V]
V_{TH}	MOS capacitance threshold voltage [V]
W	MOSFET gate width [m]
$\bar{X}_{Blank}$	Mean of a blank measurement

List of acronyms

<i>AM</i>	Air mass
<i>ARC</i>	Anti-reflection coating
<i>BHF</i>	Buffered hydrofluoric etching
<i>BOX</i>	Buried oxide
<i>BSA</i>	Bovine serum albumin
<i>CMOS</i>	Complementary metal-oxide-semiconductor
<i>DIT</i>	Defect interface trap
<i>DNA</i>	Deoxyribonucleic acid
<i>dNTP</i>	Deoxyribonucleotide triphosphate
<i>FD</i>	Fully-depleted
<i>FF</i>	Fill factor
<i>FRET</i>	Fluorescence resonance energy transfer
<i>GBW</i>	Gain-bandwidth product
<i>IC</i>	Integrated circuit
<i>ITO</i>	Indium tin oxide
<i>LED</i>	Light-emitting diode
<i>LOCOS</i>	Local oxidation of the silicon
<i>LOD</i>	Limit of detection
<i>LOQ</i>	Limit of quantification
<i>MCU</i>	Microcontroller
<i>MDL</i>	Minimum detectable limit
<i>MOSFET</i>	Metal-oxide-semiconductor field effect transistor
<i>PDMS</i>	Polydimethylsiloxane
<i>OD</i>	Optical dynamic
<i>PECVD</i>	Plasma-enhanced chemical vapor deposition
<i>PET</i>	Polyethylene terephthalate
<i>PL</i>	Precision limit
<i>RIE</i>	Reactive ion etching
<i>SNR</i>	Signal-to-noise ratio
<i>SOI</i>	Silicon-on-insulator
<i>SON</i>	Silicon-on-nothing
<i>SR</i>	Slew rate
<i>SRH</i>	Shockley-Read-Hall
<i>ST</i>	Switching time

<i>TIA</i>	Transimpedance amplifier
<i>TCO</i>	Transparent conductive oxide
<i>ULP</i>	Ultra low-power
<i>UTSOI</i>	Ultra-thin silicon-on-insulator
<i>UV</i>	Ultraviolet
<i>ZTC</i>	Zero temperature compensation

TABLE OF CONTENTS

INTRODUCTION	1
1 PRINCIPLES OF OPTOELECTRONICS IN SOI TECHNOLOGY	7
1.1 Introduction	7
1.2 Optical Principles in Semiconductors	7
1.3 Electrical Behavior of Photodiodes	12
1.4 Silicon-on-Insulator Technology	15
1.5 Light Sources	16
1.5.1 Type of sources	16
1.5.2 Spectrum	17
1.6 Figures of Merit of Photodiodes	17
1.7 Passive Optoelectronic Devices	19
1.7.1 In SOI : the thin film	19
1.7.2 Sensors in other technologies	20
1.8 Active Optoelectronic Devices	21
1.8.1 In SOI : the substrate	21
1.8.2 Solar cells in other technologies	22
1.9 Anti-Reflection Coatings	23
1.10 Conclusion	24
2 OPTIMIZATION OF PIN PHOTODIODES IN SOI TECHNOLOGY	29
2.1 Introduction	29
2.2 Context	29
2.3 DC Performance of a Lateral PIN Diode : Overview	31
2.4 Optical Properties	34
2.4.1 The responsivity	34
2.4.2 Mathematical implementation of the reflections	35
2.4.3 Standard structure	36

2.5	Responsivity Improvement	38
2.5.1	Device optimization	39
2.5.2	ARC optimization	41
2.5.3	Improved SOI structures	44
2.6	SOI-Based Specific Structures	48
2.6.1	Silicon-on-nothing structure	48
2.6.2	Membrane structure	50
2.6.3	Best expected responsivities	51
2.7	Comparison with Other Technologies	51
2.8	Responsivity Adaptation for Different Applications	52
2.9	Conclusion	55
3	INTEGRATED PHOTODETECTORS IN SOI TECHNOLOGY	61
3.1	Introduction	61
3.2	Context	61
3.2.1	Analog output	62
3.2.2	Digital output	63
3.2.3	Figure of merit	64
3.3	The System	65
3.3.1	Top design of the system	66
3.4	The Operational Amplifier	69
3.4.1	Analysis	70
3.4.2	Design	71
3.5	The Schmitt Trigger	74
3.5.1	Design	76
3.5.2	Comparison	80
3.5.3	Temperature variation	81
3.6	Noise Considerations	81
3.6.1	Noise modeling	82
3.6.2	Effect on the trigger thresholds	84

3.7	Measurements and Performance Analysis	86
3.7.1	Linearity of the system	87
3.7.2	Analysis of results and proposals for improvement	88
3.8	Methodology of Design	91
3.9	Conclusion	93
4	BIOLOGICAL APPLICATIONS OF THE UV PHOTSENSORS	99
4.1	Introduction	99
4.2	Context	100
4.3	Current DNA Quantification Optical Methods	101
4.3.1	PCR related methods	101
4.3.2	Spectrometry	102
4.3.3	Fluorometry	102
4.4	The UV Light Sources	103
4.5	Biological Application of the SOI Photodiodes	104
4.5.1	The setup	105
4.5.2	Measurement of DNA samples in quartz containers	105
4.6	Modeling	107
4.7	Results of In-Tube Measurements with Photodiode	109
4.7.1	Detection limit and other statistical considerations	110
4.7.2	Placement	111
4.7.3	Description of the varying parameters	112
4.7.3.1	The light source	112
4.7.3.2	The distance	112
4.7.3.3	The photodiode bias	112
4.7.4	Results and discussion	113
4.7.4.1	Measurement precision	113
4.7.4.2	The DNA	114
4.7.4.3	The bacteria	116
4.8	Measurements with the Integrated System	116

4.8.1	In tubes	118
4.8.2	In well microplates	119
4.8.3	Within a microfluidic PDMS channel	121
4.9	Comparison and Improvements	121
4.9.1	Comparison	121
4.9.2	Improvements	122
4.10	Conclusion	124

5 DESIGN AND MODELING OF SOLAR CELLS IN SOI SUB-STRATE 129

5.1	Introduction	129
5.2	Context and Solar Cells Characteristics	130
5.2.1	Interest of SOI solar cells	130
5.2.2	Solar spectra	130
5.2.3	Figures of merit of solar cells	131
5.2.4	Thermodynamic considerations	133
5.3	Solar Cells in UCL SOI Technology	134
5.3.1	Fabrication	134
5.3.2	Devices	135
5.4	BOX/Substrate Interface Characterization	136
5.5	Ungated Lateral PIN Diode as Solar Cell	140
5.5.1	Design and fabrication	140
5.5.2	Modeling	141
5.5.2.1	Dark characteristic	142
5.5.2.2	Illuminated characteristic	144
5.5.3	Characterization	146
5.5.4	Parameters extraction	149
5.6	Gated Lateral PIN Diode	152
5.6.1	Design and fabrication	152
5.6.2	Modeling	153

5.6.3	Characterization	156
5.7	Equivalent Circuit Model	157
5.8	Comparison with Other Technologies and Improvements	162
5.8.1	Comparison	162
5.8.2	Improvements	163
5.9	Conclusion	164
CONCLUSION		171
APPENDIXES		181
1	- Light Modeling in SOI Multi-Layer Structure	181
2	- Energy Harvesting Circuits for SOI Solar Cells	185
3	- Low Temperature Measurements	191

INTRODUCTION

Light is probably, with the oxygen, the most important source of life on earth. Being either biological or physical, the interactions with light are numerous and have become subject of studies for many years. These interactions include the light emission, propagation, reception and all the modulations that are described by *photonics*, a science focused on the part of the electromagnetic spectrum corresponding to light. More particularly, light can be *emitted* in various ways comprising inter alia the sun, lasers or light-emitting diodes (LED). The modulation of light will not be discussed in this work but its *propagation* may be more important, being very different either in the air or through specific materials (e.g. optical fibers). Finally, the *reception* of light constitutes the major part of this thesis. Light transducers can be for example photosensors, or energy harvesters like solar cells.

The first light interactions in modern physics started in 1839 when the photovoltaic effect was discovered by Alexandre-Edmond Becquerel. This started a new era of energy harvesting and the future development of the first solar cells later in 1954 at the Bell Laboratories. On the other hand, photonics has become an inevitable choice for communicating and transferring data with the discover of lasers and optical fibers. Electronics and modern optics have really started their synergy with the appearance of lasers in 1960.

Concerning the context of this thesis, it has to be noticed that years ago, high wavelengths in the infrared (i.e. $\lambda = 1500nm$) were usually preferred for optical communication protocols. But low wavelengths close to blue and ultraviolet have lately proved their interest for special systems such as optical storage (e.g. Blu-Ray). This way, low-wavelengths light sources have been recently developed and miniaturized, for example with deep UV LEDs. On the other hand, the biological materials reacting to low wavelengths comprised from 200 to 450nm are numerous. Indeed, bacteria, DNA, RNA and proteins can be quantified by low-wavelength absorbance, but blue and UV light can also enable reaction in the solution, such as

light re-emission at upper wavelength. Owing to this opportunity of technological progression and light source miniaturization, the development of complete portable system-on-chip for biological field has raised up.

Furthermore, the light is also an energy supplier. The most obvious example being the sun which delivers an amount up to $1000W/m^2$ on earth. When combined with semiconductor absorption properties, a generation current can be processed and power can be managed. For the past 30 years, different materials, process enhancements and device improvements have permitted a considerable increase of the efficiencies up to more than 40%. However, small solar cells for integrated circuits are still in development and request different challenges than those for industrial solutions.

For every type of light sensor, it is almost always fabricated in a semiconductor material ; the most common being silicon. Silicon-on-insulator (SOI) technology is a particular silicon-based technology offering substantial benefits. From the point of view of its structure, a SOI wafer is composed of two silicon layers separated by a silicon dioxide called the buried oxide (BOX). After reviewing the physics of optics in semiconductors, we will show that devices of two types can be designed in silicon. The sensors are usually fabricated in thin layers and the generators in thicker ones. A SOI wafer is precisely composed of these two types of layers. The thicker silicon region is the substrate and is currently used as a rigid holder for the integrated circuit embedded in the thin silicon film. The thin Si layer contains integrated circuits with high performances, among others thanks to the reduction of parasitic junction capacitances and body effect for MOSFETs.

The goal of this thesis is thus twofold. Firstly, we know from previous works in the same SOI technology that PIN lateral diodes can behave as excellent UV sensors. In this dissertation, their optical optimization in terms of the device characteristics, of advanced anti-reflection coating combinations and innovative specific structures will be studied. An interface integrated circuit will be detailed for photocurrent processing and provide an information easy to handle by the user. The purpose of

this first part is also to demonstrate the feasibility of an original complete system-on-a-chip including the photosensor and its signal processing circuit on the same chip for biological application aiming at higher performances than state-of-the-art equipments.

Secondly, we study the design and optimization of new PIN lateral diodes as solar cells embedded in the substrate of the SOI wafer. The device being currently not much described in the literature, it implies thus a deep analysis from the fabrication to the physic equations through the IV curves of the diodes and the circuit modeling. The main objective is to provide enough power to supply integrated circuits embedded on the same chip, being for example ultra low-power circuits or even circuits for signal processing associated with the UV sensors.

As a matter of published results, the optical optimization of the PIN lateral diodes fabricated in the thin Si film as UV sensors has been presented at the *ECS Conference 2009* and published in the *ECS Transactions*, while the complete photosensor was described in a paper of the *AICSP 2010*. The biological applications of the UV microsystem has been demonstrated and the results were presented in *MBEC 2008* and *IEEE BIOCAS 2010* conferences. A complete description of the experiments has been detailed in a book chapter from *INTECH* in 2011. Concerning the SOI solar cells, the preliminary results were presented at the *IEEE SOI Conference 2009*. A total of 22 international publications were communicated during the five years of the thesis, including one book chapter, three journal papers and seven conference communications as first author.

The thesis is organized as follows : as we deal with optical considerations and photosensitive devices, a first chapter will introduce the basic optical concepts commonly used in the study of optoelectronic devices. The photovoltaic effect and its implication for silicon-based structures will be presented. The photodevices being mainly photodiodes, a review of the photodiodes behavior will be presented as well in dark conditions than under illumination. Then, the UCL SOI technology will be detailed since most of the devices and circuits analyzed in this work were fabricated

in this silicon-based technology. To continue with the photonics fundamentals, a short review of the different light sources used in the thesis will be presented and will be followed by an introduction to the most commonly used figures of merit. The photodiodes can be used as sensors or power generators according to the region of the SOI wafer where they are fabricated. Thus, a short explanation of the devices characteristics and differences will be discussed. Finally, a brief preview of the anti-reflection coatings (ARC) will be presented.

The second chapter is dedicated to the study of the optimization of the PIN lateral diode embedded in the thin Si film as an ultraviolet sensor. The context of utilization and their interest for biomedical, biological and environmental applications will be detailed. An overview of the DC performances of the lateral PIN diodes will be described before a study more dedicated to their optical properties. Different techniques will then be presented to improve the optical efficiency of the photodiodes, including the device optimization and ARC discussion where simulations and measurements will be compared. Some more complex SOI-based structures will then be presented (i.e. silicon-on-nothing (SON) and membrane) and pre-studied as UV sensors. As a final point, we will detail a comparison of the best results achieved in this work with state-of-the-art UV sensors and we will present some perspectives for ultra-thin SOI technologies.

The third chapter is mainly based on the design of signal processing circuits for the UV photodiodes. The motivation of designing an integrated circuit for bio and environmental measurements will be presented and the type of signal processing described : a current-to-frequency converter. We will explain a first approach of design which allows for choosing the external components of the system and for evaluating the specifications of the different blocks of the system, i.e. the integrator (and its operational amplifier), the comparator, a Schmitt trigger in this case and the switch. Then, each component will be designed from a top-down methodology. The operational amplifier will be designed according to the UCL $\frac{g_m}{I_D}$ method while three types of Schmitt triggers will be compared. A finer noise analysis will be presented including noise sources from the photodiode, the switch and the amplifier.

The measurements and the simulations of the behavior of the circuit will be compared to observe and analyze the performances of the system in terms of linearity, optical and transient responses with other realizations mentioned in the literature. To finish, a methodology of design for a complete photosensor is proposed according to application specifications.

As a matter of concrete applications, the fourth chapter presents the results of experiments based on the quantification of biological material concentration. We will first present the context by which biological material can be optically quantified by UV transmission. Then, we will review the most commonly used quantification methods and laboratory equipments and will quickly present the current UV light sources used for biological material measurements. The application setup will then be detailed and the principle of measurement will be demonstrated. We will propose a modeling for the whole microsystem enabling a description of the light intensities as a function of the biological concentration. The first measurements obtained with in-tube solutions of DNA and bacteria measured with a SOI photodiode will be presented and analyzed with the variation of the different parameters of the microsystem. The statistical considerations related to biological experiments will also be reviewed for finer analyses. Moreover, we will present the measurement results achieved with a complete microsystem combining an UV photodiode and a signal processing integrated circuit (as described in the third chapter). In this case, the measurement results will be detailed for in-tubes, in well-microplates and within a PDMS channel containers for various biological material. Finally, we will compare our microsystem with the other methods previously described and will propose some improvements.

The fifth chapter demonstrates the interest of SOI CMOS technology for embedded solar cell fabrication. We will present the purpose of integrated solar cells in SOI technology for self-powered integrated circuits. The main figures of merit for photovoltaic analysis will be presented and we will describe the solar spectra and the thermodynamic efficiency limits for SOI solar cells. Then, we will describe the structure of lateral PIN diodes embedded in the SOI substrate as solar cells, which

results on two possible devices : the ungated or gated solar cells. We will first characterize the SOI wafer with capacitance analysis to extract defects of the technology. Afterwards, we will study the ungated solar cells : their design and fabrication are described, an analytical model for the dark electrical characteristics is presented and a intuitive geometrical model is introduced to calculate the photocurrent. We will then present the measurement curves and compare them with Atlas simulations for the solar cell parameters extraction. After that, we will describe the gated solar cell devices : their design and fabrication methods will be presented before we investigate their photovoltaic behavior modeling. The characterization of the gated solar cell will be extensively presented at that time. As we will explain, Atlas simulations and analytic modeling are not sufficient to fully describe the solar cells. Thus, we will model their I-V curves with an equivalent circuit model built from diodes, resistances and current sources. Finally, we will compare the SOI solar cells with other solar cells in various technologies and will propose some improvements for our process before ending the chapter.

Finally, we will conclude the work with a summary of the achievements and possible improvements for all the optoelectronic components realized in this work. A perspective will be presented concerning the size required for a solar cell embedded in the SOI substrate to supply enough power for the complete UV photosensor described in the third chapter of the thesis, and this, for various illumination conditions. This perspective will also be discussed for other integrated circuits with various power consumptions.

Three appendixes are added : the first one summarizes the light modeling inside a SOI multi-layer structure. The second introduces the design of power management circuits for solar cells. The first step, i.e. the charge pump, has been investigated and described with experimental characterization under illumination. The third appendix concerns low-temperature measurements which have been realized in collaboration with the FEI in Sao-Paulo, Brazil. We study the behavior of UV photodiodes and solar cells in the SOI UCL CMOS technology in a range of temperature from 100 to 400K.

CHAPTER 1

PRINCIPLES OF OPTOELECTRONICS IN SOI TECHNOLOGY

1.1 Introduction

The purpose of this chapter is to briefly present the optoelectronic possibilities of the SOI technology. Since the main part of this work is about optoelectronic, a brief review of the optic principles inside a semiconductor structure is presented. As most of the optical sensors are realized with diodes, a summary of the electrical behavior of these devices under illumination is introduced. Then, the silicon-on-insulator technology is presented by describing a standard SOI wafer, its dimensions and its advantages compared to standard silicon technologies. This work also compares the realized devices with existing works, thus the figures of merit of the photodiodes are defined. As working with optical quantities, a presentation of the different light sources types and their spectra properties is presented in this chapter. Because the SOI technology includes two semiconductor regions, a study of the optoelectronic devices is described for both of them, i.e. the silicon thin-film and the silicon substrate. As it will be extensively explained in this work, the thin film is employed for photosensors while the substrate is mainly used to incorporate power generators, i.e. solar cells. Finally, a description of the anti-reflection coatings is presented.

1.2 Optical Principles in Semiconductors

In this section we review the basic principles of optics. Firstly from an energy point of view, with the energy band theory of semiconductors, and secondly from a more

optical point of view with the indexes of refraction and the generation rate.

Direct and indirect bandgap

To understand how semiconductors handle light, it is first important to analyze their energy bands. Indeed, holes and electrons can move between the valence and the conduction bands, by diverse mechanisms that differ if the semiconductor features a direct or an indirect bandgap. Figure 1.1 shows the energy bands, as a function of the wavenumber k , and the photon absorption mechanism for both types.

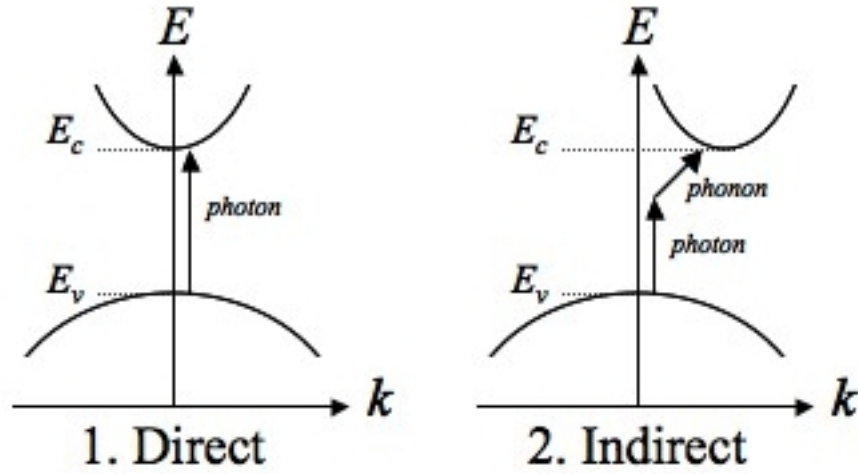


Figure 1.1: E - k diagrams for direct (1) and indirect (2) bandgaps.

We denote E_G as the difference between the conduction band E_C and the valence band E_V . In figure 1.1(1), it is showed that in a direct bandgap, a photon can be absorbed if its energy is higher than the bandgap, independently of the momentum. Contrarily, one can clearly see the vertical misalignment of the energy bands in the second case. It implies that, if the semiconductor crystal features an indirect bandgap, a single photon will not be able to provide the correct couple energy-momentum to a valence electron to reach an empty state in the conduction band. Then, light absorption will only be possible with the contribution of a phonon, which have less energy than a photon, but features a higher momentum in order to reach the bottom of E_C as showed in figure 1.1(2). In this same figure, one can observe that the energy for which a photon can be absorbed is slightly inferior to the bandgap

when aided by a phonon absorption.

Now assuming that a photon with sufficient energy will be associated with a lattice vibration phonon, then the energy of a photon is defined by the Planck's formula :

$$E_{ph} = \frac{h \cdot c}{\lambda}, \quad (1.1)$$

where h is the constant of Planck, c is the vacuum speed of light and λ is the wavelength of the photon. This implies a maximal wavelength λ_{max} that will be absorbed by the material according to the minimal energy of the photon which has to be at least equal to the bandgap :

$$\lambda \leq \frac{h \cdot c}{E_G} = \lambda_{max}. \quad (1.2)$$

This is resumed in table 1.1 for various technologies.

Technology	Bandgap [eV]	λ_{max} [nm]
Si	1.12	1110
Ge	0.66	1880
GaAs	1.424	870

Table 1.1: Comparison of the maximum absorption wavelength of light in various technologies according to their bandgap.

While silicon features an indirect bandgap, the maximum wavelength to be absorbed is about $1100nm$, in the near infrared. Contrarily, germanium and gallium-arsenide are direct bandgap semiconductors. Due to its small bandgap, germanium is preferred for large spectrum absorption while GaAs is used for lower wavelengths pass-filters.

Since the other differences of the direct and indirect bandgap have been extensively explained in previous works (for example : [1]), only the case of the silicon indirect bandgap will be studied in this work but both types will be compared in the following chapters.

Generation and photovoltaic effect

For an optical formalism including the notions of absorption, reflexion and transmission of light, the materials are defined by their refractive index . This index of refraction N is defined by [1]:

$$N = n - j \cdot \kappa = \sqrt{\epsilon_r}. \quad (1.3)$$

Equation 1.3 also defines the relation between the refractive index and the relative permittivity of the material ϵ_r . If N is a complex number, so is the permittivity of the material, which implies a loss of power in the material.

But when the light is absorbed into a material, its power is reduced with its depth penetration following a decreasing exponential law. The power is related to the photon flux density $\Phi(\lambda, x)$ and its evolution with the distance is expressed by the Beer-Lambert law :

$$\Phi(\lambda, x) = \Phi_0(\lambda) \cdot e^{-\alpha(\lambda) \cdot x}, \quad (1.4)$$

where $\Phi_0(\lambda)$ is the incident flux density of photons, i.e. the light power at the beginning of the material. In equation 1.4, the term α is called the absorption coefficient. The parameter depends on the material structure and is defined by :

$$\alpha = \frac{4\pi \cdot \kappa}{\lambda}. \quad (1.5)$$

It then only exists if the material is lossy. We can also define the absorption length L_{abs} of the material as $\frac{1}{\alpha}$. The absorption length of silicon can be plotted as a function of the wavelength as showed in figure 1.2. This figure shows that high energy photons below $370nm$ have a small absorption length, and thus are directly absorbed by silicon while the influence of the phonon particle can be seen from $400nm$ where the absorption length increases as well as the absorption of the photon with less energy decreases. We can observe in figure 1.3 the optical power decrease ($\frac{\Phi(x)}{\Phi_0}$) in silicon for wavelengths of 300, 400 and $500nm$ (a) and 600, 700 and $800nm$ (b). It is remarkable that most of the low wavelengths are quickly absorbed in the first

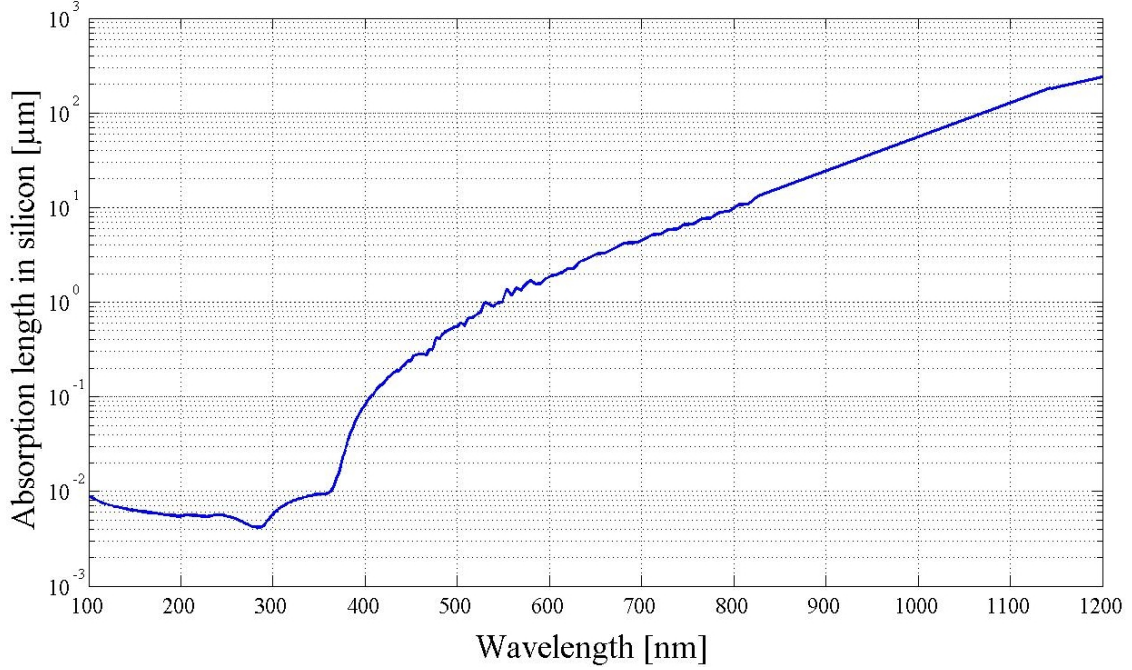


Figure 1.2: Absorption length in silicon as a function of the wavelength.

hundreds of nanometers. Contrarily, higher wavelengths are attenuated after a few tens of micrometers.

When dealing with light inside a semiconductor, the notion of carrier generation is used in the transport equations. It is defined as a function of the light wavelength at a depth x inside a semiconductor by :

$$G(\lambda, x) = -\frac{d\Phi(\lambda, x)}{dx}, \quad (1.6)$$

which becomes

$$G(\lambda, x) = \alpha(\lambda) \cdot \Phi_0(\lambda) \cdot e^{-\alpha(\lambda) \cdot x} = \frac{1}{L_{abs}(\lambda)} \cdot \Phi_0(\lambda) \cdot e^{\frac{-x}{L_{abs}(\lambda)}}. \quad (1.7)$$

Finally, the term G corresponds to the rate of electron-hole pairs generated in volume in the silicon device by the photon whose energy is sufficient. This is called the photovoltaic effect. The most common devices used to collect light by photovoltaic effect are diodes.

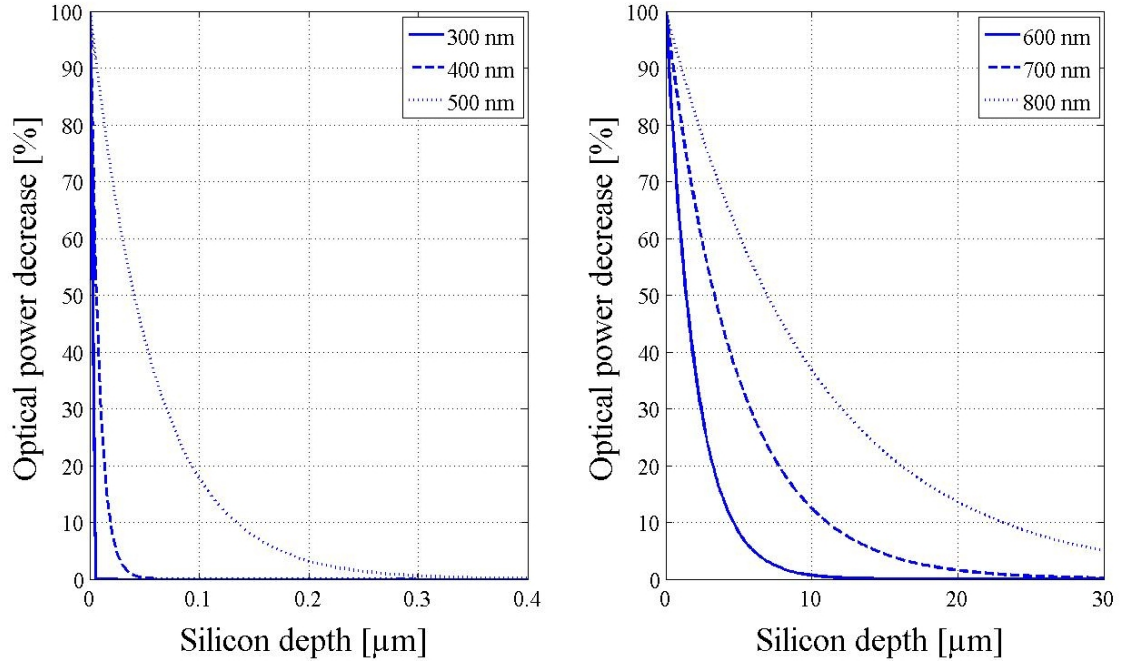


Figure 1.3: Optical power decrease in silicon as a function of the depth penetration.

The figure 1.4 illustrates the generation of electron-hole pairs phenomenon in a diode. These electrons and holes are then pulled forwards the regions when they are majority carriers by the electric field applied in the depletion zone. The current is then formed by the carriers that have not recombined and are collected at the contacts. On this figure the photon flux is represented as vertical to the PN junction, but the phenomenon is the same for a lateral illumination since the carriers will move towards the contacts under the influence of the electric field.

1.3 Electrical Behavior of Photodiodes

The diode behavior, in the dark, is described by its $I_D = f(V_D)$ equation :

$$I_{D,Dark}(V_D) = I_S \cdot (e^{\frac{V_D}{V_T}} - 1) + I_{RG}, \quad (1.8)$$

where V_T is the thermal voltage and $I_{R,G}$ is the generation-recombination current :

$$I_{RG}(V_D) = I_{Srg} \cdot (e^{\frac{V_D}{2 \cdot V_T}} - 1). \quad (1.9)$$

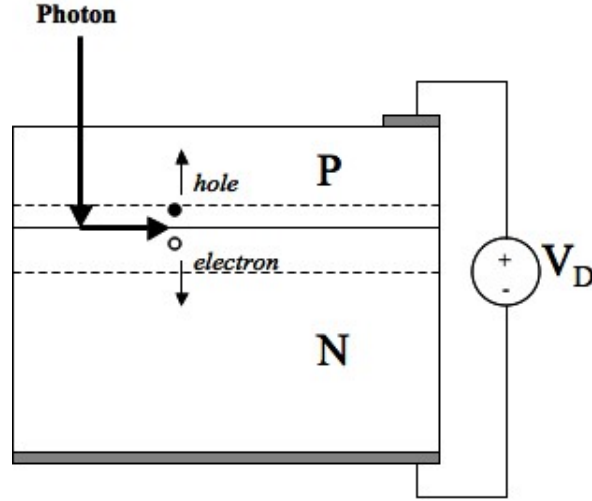


Figure 1.4: Electron-hole generation by photon absorption in a diode.

In silicon, I_{Srg} is usually greater than I_S , which is why the generation-recombination current dominates when V_D is well above V_T in reverse bias but also when the positive voltage of the diode is small (i.e. from 0 to 300mV typically). This specific current will be discussed in more details in this work because of its importance for the devices. However, when illuminated, the diode receives generation, and its current-voltage curve is shifted down vertically assuming a constant generated current I_{ph} called the *photocurrent* :

$$I_{D,tot}(V_D) = I_{D,Dark} - I_{ph}. \quad (1.10)$$

It has already been explained and proved in many previous works [1, 2](and so will not be demonstrated again here) that I_{ph} is directly proportional to the depletion and diffusion lengths in case of a volume generation :

$$I_{ph} \propto q \cdot G \cdot (L_{ZD} + L_n + L_p), \quad (1.11)$$

where L_{ZD} is the depletion zone length and L_n and L_p are the diffusion lengths of electrons and holes respectively. That is why PN diodes are improved by the adjunction of an intermediate quasi intrinsic zone that increases the depletion zone and so the photocurrent. The new device is called a PIN diode. The optimal choices

of the structure dimensions will be discussed in the next chapter.

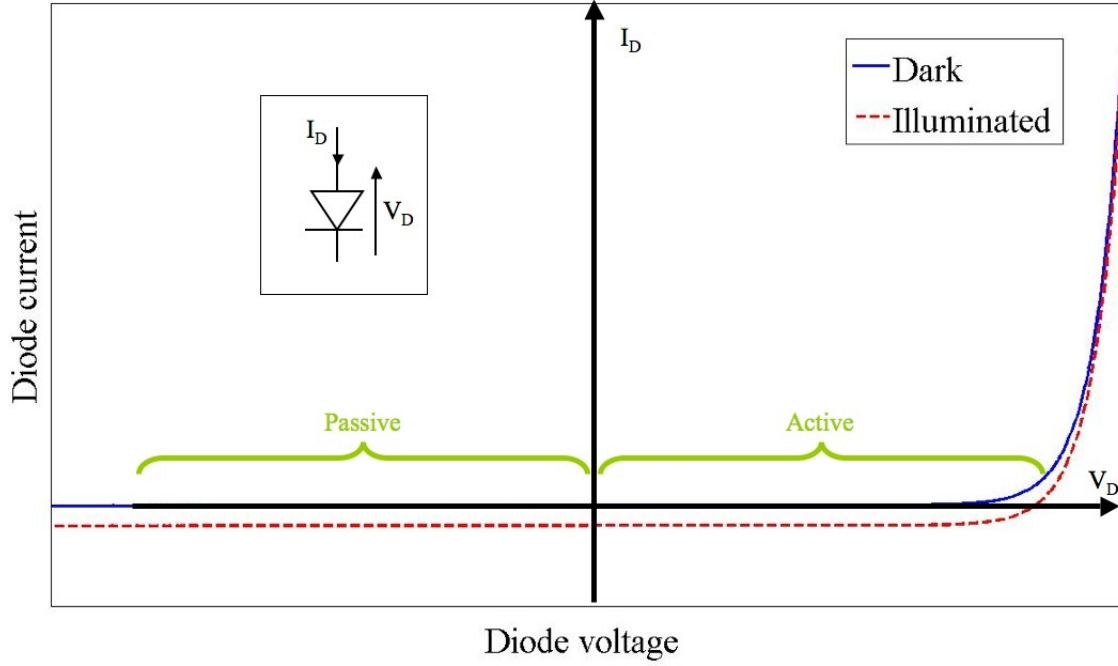


Figure 1.5: Theoretical IV characteristic of a diode in the dark (continuous line) and under illumination (dashed line).

The curve shift of equation 1.10 is illustrated in figure 1.5. On this figure, two operation modes of the diode are distinguishable. Firstly, the diode can be used in passive mode with a negative current for a negative voltage. Indeed, by increasing the reverse voltage, the depletion area is increased which leads to a larger collection of the photons. Such diodes may be embedded in thin layers for UV or blue detection (see figure 1.3(a)) and act as light sensors (i.e. often, they are focused on a specific spectral range). Secondly, the diode can also be used in active mode with a negative current for a positive voltage. Compared to the reference directions of current and voltage of a classical diode, the power loss in the device is then negative, which in fact corresponds to a power generator. The diode serving in active mode is usually utilized when collecting a larger part of a light spectrum, needing a higher thickness of silicon according to figure 1.3(b), typically like a solar cell.

1.4 *Silicon-on-Insulator Technology*

SOI combines the advantages of silicon technology fabrication with high performance in multiple fields. SOI yields a better behavior at high and low temperatures, a higher resistance to radiations and a consistent reduction of power consumption.

UCL $2\mu m$ technology

The particular technology in which the circuits and devices have been fabricated in this thesis is a $2\mu m$ SOI FD (for fully-depleted) CMOS technology [3, 4]. The wafers result from smart-cut process consisting in a wafer bonding process and thin Si layer exfoliation after hydrogen ions implantation at small depth [5]. Figure 1.6 presents the sketch of a MOSFET fabricated in the UCL SOI thin film technology. The technical node is $2\mu m$ and the gate oxide thickness is of $30nm$ for a thin film thickness of $80nm$ for a fully-depleted channel. The supply voltage and thus the power consumption can then be reduced and the body factor is around $n = 1.1$ while it is of about 1.5 for classical bulk MOSFETs. Then, SOI technology seems a

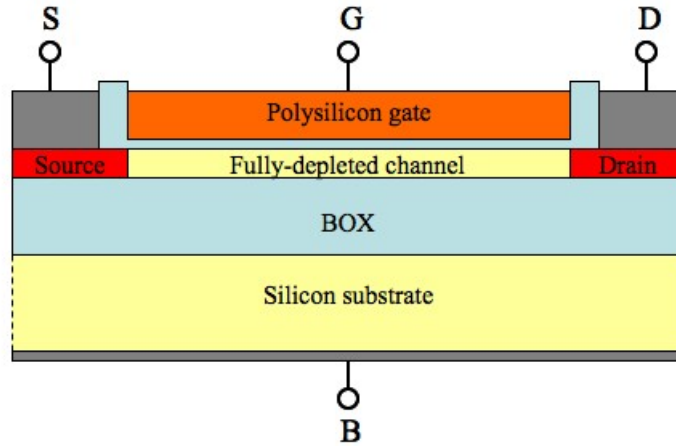


Figure 1.6: Sketch of a MOSFET embedded in SOI technology.

perfect candidate to include an optical device and the processing signal circuit (in case of a sensor) or the power regulator circuit (in case of a generator). It combines high circuit performances, power reduction and portability for a complete low-cost system-on-a-chip [3].

1.5 *Light Sources*

1.5.1 *Type of sources*

Depending on the type of the device, the light quantity to measure can be very different. The light power, the emitting spectrum may vary according to many physical phenomena. The main light sources that are used in this thesis are :

- the large spectrum lamp. That kind of lamp is mostly used for research. For example, halogen-deuterium lamps provide a spectrum from $200nm$ to $1200nm$ with large emitting power. Associated with a monochromator (or with very narrow bandpass optical filters), they allow for selecting with precision any wavelength and measurement of the spectral response of a photosensitive device. They can also be used to simulate any monochromatic light source. But often, the whole system (including the lamp and the monochromator/filters) is too voluminous to be integrated in a portable device.
- the light emitting diode (LED). To combine the advantages of a high emitting light power, a controlled and narrow emitting spectrum, and a low fabrication cost, the LEDs are an opportunistic choice. To ensure a low wavelength emission spectrum, the materials used to fabricate a UV diode are diamond (C), and Al-based materials (i.e. AlN and AlGaN) thanks to their large bandgap, allowing a high energy photons generation when the electron-hole pairs are recombining. The UV LEDs have to be biased with relatively high forward voltage (e.g. $V_D = 6V$) which yields a current of about $I_d \simeq 20mA$. This implies a consistent power needed to bias the diodes (compared to the power needed to supply a microelectronic integrated circuit), which also has to be very stable in time to minimize the fluctuations of the emitted light and reduce the measurement errors. However LEDs are miniaturized, portable and low-cost UV light source, making them good candidates for a complete optoelectronic microsystem aiming at biomedical applications.
- the sun. It is the most powerful natural light source on earth. Assimilated to

a black body with temperature of $6000K$, the sun irradiates from $200nm$ to about $3\mu m$. Its light irradiance on earth is reduced by gases and particles of the earth atmosphere. Thanks to its high energy properties, the sun is used as a power source for the devices.

1.5.2 Spectrum

Each of the light source presented above features a specific emitting spectrum. The LEDs or the light following the output of a monochromator is almost monochromatic. More precisely the spectrum is very narrow around one wavelength, typically $\Delta\lambda = \pm 5nm$ around the peak wavelength λ_0 . The photon flux Φ_0 referred in equation 1.4 is then integrated over these limits.

Contrarily, the halogen-deuterium lamps or the sun feature large spectrum emission. The photon flux is here integrated over a very large range of wavelengths, typically from $200nm$ to $1.1\mu m$ in silicon.

1.6 Figures of Merit of Photodiodes

As optical-to-electrical transducers, photodiodes can be characterized by two kinds of figures of merit. First, their spectral efficiencies which are a measurement of the ability of the device to collect the electron-hole pairs generated by a photon at a given wavelength. They are expressed as a function of the wavelength like spectral filters characteristics. Secondly, their power efficiencies, more often used for the active mode of the diode.

Spectral efficiency

To simulate and measure the spectral efficiency of a photodevice, three major figures of merit are stated in the literature.

- The internal quantum efficiency, which is the ratio of the collected photocurrent to the total generated current in the photosensitive region. It allows a

measurement of the recombination losses in the device and can be expressed by :

$$QI = \frac{J_{ph}}{q \cdot G \cdot L_{ph}}, \quad (1.12)$$

where J_{ph} is the total photocurrent density (measured or simulated), G is the generation term and L_{ph} is the photosensitive distance on which the generation term is defined (assuming a one dimension analysis). Then, if recombination is unconsidered, $QI = 100\%$ for each wavelength.

- The external quantum efficiency is a variant of QI including the reflectances of the structure and the ratio of its photosensitive area compared to the total area of the device :

$$QE = QI \cdot \frac{P_{abs}}{P_{in}}, \quad (1.13)$$

where P_{abs} is the real optical power absorbed in the semiconductor while P_{in} is the incident optical power to the total surface of the device. Due to internal and external reflections, and to front metallic contacts reducing the photosensitive area, the external quantum efficiency is consequently reduced compared to the internal efficiency.

- The spectral responsivity is similar to the previous quantum efficiencies, but instead of being expressed as a percentage, the responsivity is the ratio of the total photocurrent divided by the the incident optical power :

$$R = \frac{I_{D,tot} - I_{D,Dark}}{P_{in}} = \frac{J_{ph} \cdot A}{P_{in}}, \quad (1.14)$$

where A is the area through which the photocurrent is flowing. The responsivity is a more global parameter that can directly estimate the photocurrent induced by the illumination as a function of the light power at each wavelength. The responsivity is the more commonly used figure of merit in literature and will serve as the comparison factor for the sensing photodevices in this work.

Power efficiency

Essentially when working in active mode, the power efficiency of photodiodes is defined by :

$$\eta = \frac{P_{out}}{P_{in}}, \quad (1.15)$$

where P_{in} is again the incident total optical power to the surface of the device but P_{out} is the maximal output electrical power supplied by the device under illumination. P_{out} is found as the I-V product corresponding to the values at the maximal point of the P-V curve. The context will be explained in more details in chapter 5.

1.7 Passive Optoelectronic Devices

1.7.1 In SOI : the thin film

As previously said, optoelectronic devices may be embedded in the SOI thin film. Due to its weak thickness, most of SOI thin film optoelectronic devices are lateral carrier collectors : the electronic device is laterally fabricated and the light is collected perpendicularly to the electrical flow of the carriers. The first PIN diode in SOI technology were realized by Colinge [6]. Later, the AC and DC performances of the basic structure of PIN photodiodes in the UCL SOI technology were studied by Afzalian [7]. A description of the device with dimensions of the UCL technology is shown in figure 1.7. Thanks to the low thickness of the thin Si film (i.e. $80nm$), and to the high doping of the anode and cathode regions (i.e. $N_A = N_D \simeq 10^{20}cm^{-3}$ for the P and N regions respectively), the intrinsic zone is fully depleted which allows an enhancement of the depleted zone and thus an increase of the generated photocurrent.

The internal quantum efficiency (QI, as referred to equation 1.12) for this structure has been simulated in figure 1.8, where it is plotted as a function of its maximal value. The best QI occurs for $380nm$ which corresponds to the maximal wavelength for a photon to be absorbed in silicon with its own energy (i.e without additional energy from a phonon) as shown in figure 1.2. After this cut-off wavelength, the

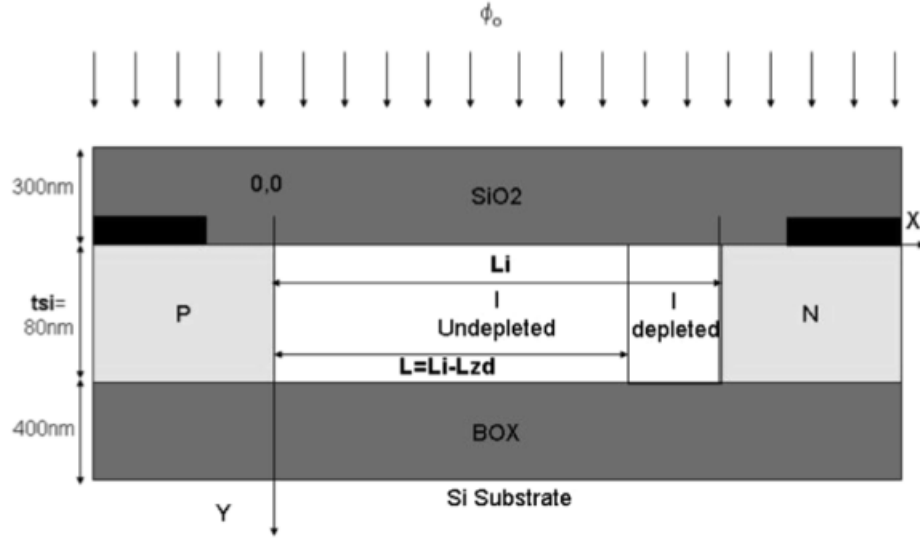


Figure 1.7: Lateral view of a lateral PIN diode designed in UCL SOI technology [8].

probability for a photon to be absorbed is decreased as well as the quantum efficiency. Lower wavelengths reach a weak efficiency due to reflection at the surface of the device which presents a top silicon oxide passivation layer of $300nm$ as shown in figure 1.7.

1.7.2 Sensors in other technologies

Of course optical sensors have been developed in other technologies. Bulk silicon remains the lowest-cost technology to fabricate a photodiode and can absorb photons with a wavelength up to slightly more than $1100nm$ thanks to its $1.1eV$ bandgap. Unfortunately, to realize a spectral filter, in order to only absorb photons with an associate low wavelength, a low thickness of the silicon is needed since most of the photons are absorbed in the first $5\mu m$ of the silicon thickness.

This leads to reducing as much as possible the thickness of the silicon region where the photons are absorbed and to reduce the reflections. Consequently, a high responsivity can be achieved in the appropriate wavelength by other techniques like spatial modulation of light [9] or special devices such as avalanche diodes [10].

Silicon is the most common semiconductor but other materials can be used to

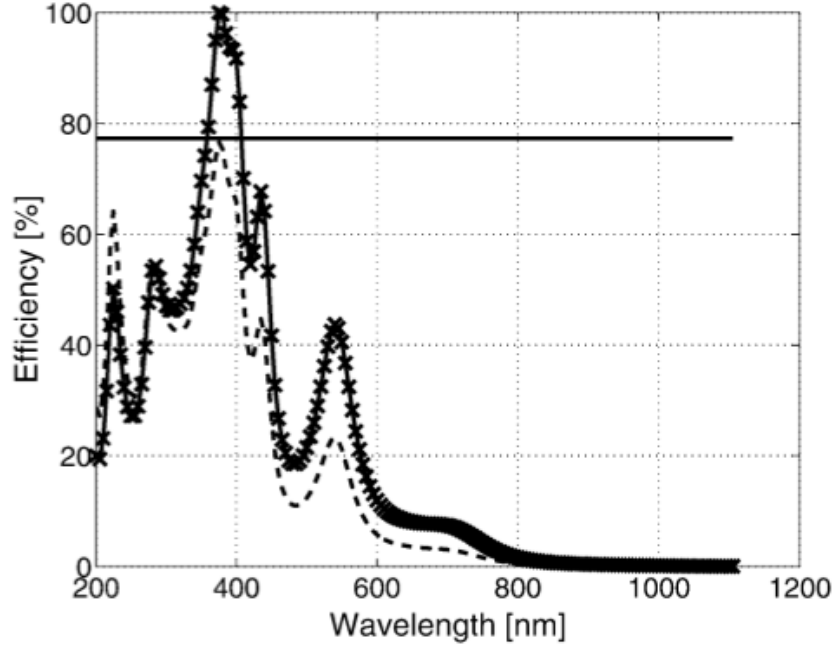


Figure 1.8: One dimensional analysis of a lateral PIN diode in SOI technology [8]. For $L_i = 20\mu m$ and $V_D = -3V$, the figure represents the internal quantum efficiency (QE, solid line), the ratio QE/QI (dashed line) and the total normalized photocurrent (crossed line).

implement a photosensor. Thanks to their larger bandgap, materials based on gallium nitride (GaN) can more easily absorb photons associated to low wavelengths independently of its thickness and then achieve high responsivities below $400nm$ [11, 12, 13, 14]. Another frequently used technology is the silicon carbide (SiC) that has proven its interest by the past, despite its indirect bandgap, due to its use in the first commercial LEDs [15, 16].

1.8 Active Optoelectronic Devices

1.8.1 In SOI : the substrate

Usually, the substrate of a SOI wafer is only used as a rigid holder for the integrated circuits embedded in the thin silicon film. But by etching the buried oxide down to the substrate, it is possible to implant the anode and cathode regions of a diode. A

lateral view of such a device is showed in figure 1.9.

In the figure, the device fabricated is again a lateral PIN diode. Because of

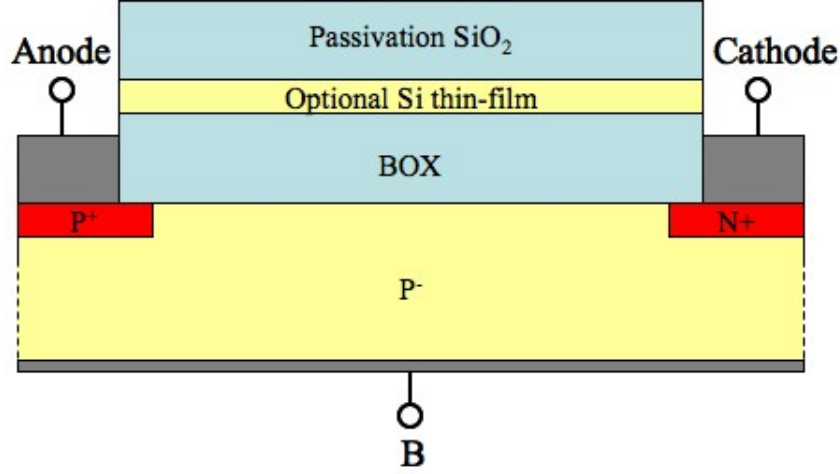


Figure 1.9: Sketch of a solar cell embedded in the substrate of an SOI wafer.

the existence of a back electrical contact under the substrate, the backgate voltage has to be chosen carefully in order to avoid leakage currents through the P^- region. According to whether the solar cell is below an active region for CMOS process or not, the thin silicon film can be present or not. If the solar cell is fabricated outside an active region, the thin Si film is oxidized and a three-layers oxide coating protect the diode.

Otherwise the thin silicon film remains above the BOX on the solar cell and may absorb a part of the light if the illumination is incident to the top of the wafer. The performances of this type of device will be discussed in chapter 5.

1.8.2 Solar cells in other technologies

Solar cells have been studied for more than 35 years for high efficiency achievement. The first ones were engineered in silicon-based technologies. A roadmap of the solar cell efficiencies in research laboratories is presented in figure 1.10. Nowadays, the best efficiencies for silicon solar cell are about 25% for monocrystalline silicon, reaching a top efficiency of 27.6% [17]. As for sensors, diode in III-V materials such as GaAs can reach higher efficiencies and the records are achieved by multijunctions cells

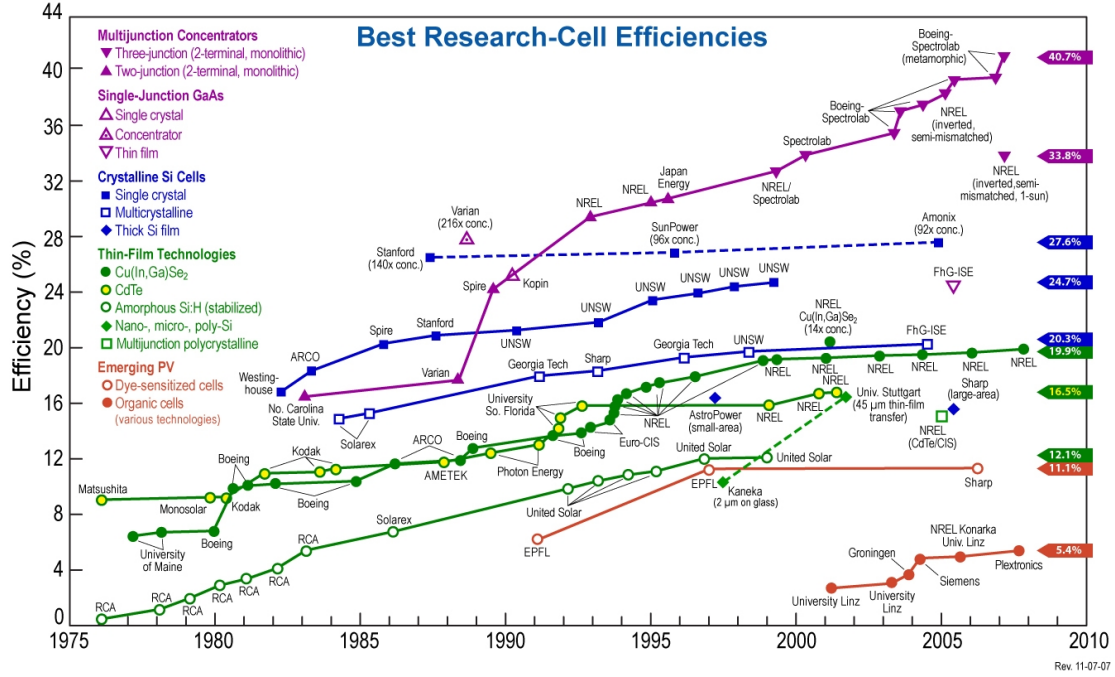


Figure 1.10: Efficiencies of the best solar cell in laboratory research [18].

coupled with sun concentrators. Multijunctions solar cells are designed by a bandgap engineering to absorb the greatest part of the solar spectrum as possible and thus can reach efficiencies of 40% in the best case [17]. However, thin-film semiconductor solar cells achieved efficiencies near 20% while new organic solar cells have recently emerged but are not still offering high efficiencies. Most of efficiencies improvements are based on contacts, anti-reflection coatings, and bandgap engineering in case of multijunctions cells.

1.9 Anti-Reflection Coatings

The anti-reflection coatings (ARC) are layers deposited on the top of a photodevice to prevent from optical reflections. The choice of the material and its thickness are dependent on its refractive index and are chosen correspondingly to the adaptation of the quarter-wavelength. The advantage of depositing a dual-layer anti-reflection coating above a photodiode has been proven in [19]. It can considerably reduce the reflections of light by an accurate choice of thickness according to the index of

refraction of the material and the wavelength at which the efficiency has to be improved. The most common ARC's are silicon dioxide (SiO_2), silicon nitride (Si_3N_4) and alumina (Al_2O_3). Great advances have been made in the solar cell laboratory research concerning ARC. Recently, the researches are more focused on the development of texturized surfaces which are also often used to ensure a greater absorption of the light in the device with multiple reflections at the incident interface. The patterned protective layers allow an augmentation of their transmittance, leading to an increase of the quantum efficiencies of the cells [20, 21, 22].

For low wavelengths applications, transparent conduction oxide (TCO) are in polyethylene terephthalate (PET) or indium-tin-oxide (ITO) [23]. But the optical reflectivity under $\lambda = 400nm$ is poor, meaning accurate for UV sensors.

For the solar cells particularly, the reflections must be minimized for the largest wavelength range as possible. Black silicon is thus often used, as well as nano pillar structuration of the silicon [24].

1.10 Conclusion

In this chapter, we reviewed the basis of optoelectronic principles in semiconductors more especially for the silicon regions inside a SOI wafer. Since diodes, are the most common electrical devices to collect photons, we reviewed the electrical principles of diodes and demonstrated that a PIN diode is an accurate solution for optical sensors and generators thanks to an enlargement of the photosensitive area. Inside a SOI wafer, photodiodes can behave as sensors in the thin Si film or as generators in the substrate. But in both cases, they benefit from the advantages of the SOI technology : low-power, temperature and radiation resistance. Finally, to improve the responsivity of a device, a dual-layer anti-reflection coating of SiO_2 , Si_3N_4 or Al_2O_3 for example are suggested. The structuration of the ARC can also greatly improve the transmission of light into the photodevice.

References

- [1] H. Zimmermann, "Integrated Silicon Optoelectronics", *Springer Series in Optical Science*, Springer, Berlin, 2000.
- [2] M. Green, "Solar Cells - Operating Principles, Technology, and System Applications", *Prentice-Hall Series in Solid State Physical Electronics*, 1982.
- [3] D. Flandre et al. "Fully-Depleted SOI CMOS Technology for Low-Voltage Low-Power Mixed Digital/Analog/Microwave Circuits", *Analog Integrated Circuits and Signal Processing*, Vol. 21, No. 3, pp. 213-228, December 1999.
- [4] D. Flandre et al., "Fully depleted SOI CMOS technology for heterogeneous micropower, high-temperature or RF microsystems", *Solid-State Electronics*, Vol. 45, No. 4, pp. 541-549, April 2001.
- [5] M. Bruel, B. Aspar and A.-J. Auberton-Herve, "Smart-cut : A new silicon on insulator material technology based on hydrogen implantation and wafer bonding", *Japanese journal of applied physics*, Vol. 36, No. 3B, pp. 1636-1641, 1997.
- [6] J.-P. Colinge, "p-i-n photodiodes made in laser-recrystallized silicon-on-insulator", *IEEE Transactions on Electron Devices*, Vol. 33, No. 2, pp. 203-205, 1986.
- [7] A. Afzalian, "Optical Detectors in SOI CMOS Technologies for Blue DVD and Short Distance Optical Communication", *PhD Thesis*, Université catholique de Louvain, Belgium, 2006.
- [8] A. Afzalian and D. Flandre, "Physical Modeling and Design of Thin-Film SOI Lateral PIN Photodiodes", *IEEE Transactions on Electron Devices*, Vol. 52, No. 6, pp. 1116-1122, June 2005.
- [9] Y. Chen and M. du Plessis, "An integrated 0.35 μm CMOS optical receiver with clock and data recovery circuit", *Microelectronics Journal*, Vol. 37, No. 9, pp. 985-992, September 2006.

- [10] A. Pauchard, A. Rochas, Z. Randjelovic, P.A. Besse and R.S. Popovic, "Ultraviolet Avalanche Photodiode in CMOS Technology", *International Electron Devices Meeting Technical Digest*, pp. 709-712, San Francisco, December 2000.
- [11] S.-H. Chang, Y.-K. Fang, K.-C. Hsu and T.-C. Wei, "GaN UV MSM photodetector on porous β -SiC/(111)Si substrates", *Sensors and actuators. A - Physical*, Vol. 147, No. 1, pp. 1-5, September 2008.
- [12] S.J. Chang, W.S. Chen, C.F. Shen, T.K. Ko, Y.K. Su, Y.Z. Chiou, C.S. Chang, S.C. Shei, J.K. Sheu, W.C. Lai and Y.C. Lin, "GaN-Based p-i-n Sensors With ITO Contacts", *IEEE Sensors Journal*, Vol. 6, No. 2, pp. 406-411, April 2006.
- [13] N. Biyikli, I. Kimukin, T. Tut, O. Aytur and E. Ozbay, "Fabrication and characterization of solar-blind $\text{Al}_{0.6}\text{Ga}_{0.4}\text{N}$ MSM photodetectors", *Electronics Letters*, Vol. 41, No. 5, pp. 274-275, March 2005.
- [14] E. Monroy, F. Calle, J.L. Pau, E. Munoz, F. Omnes, B. Beaumont and P. Gibart, "AlGaN-based UV photodetectors", *Journal of crystal growth*, Vol. 230, No. 3-4, pp. 537-543, 2001.
- [15] D.M. Brown, E. Downey, J. Kretchmer, G. Michon, E. Shu and D. Schneider, "SiC Flame Sensors for Gas Turbine Control Systems", *Solid-state electronics*, Vol. 42, No. 5, pp. 755-760, 1998.
- [16] Y.K. Fang, S.-B. Hwang, K.-H. Chen, C.-R. Liu, M.-J. Tsai and L.-C. Kuo, "An Amorphous SiC/Si Heterojunction p-i-n Diode for Low-Noise and High-Sensitivity UV Detector", *IEEE Transactions on Electron Devices*, Vol. 39, No. 2, pp. 292-296, February 1992.
- [17] A. Luque and A. Marti, "Theoretical Limits of Photovoltaic Conversion", *Handbook of Photovoltaic Science and Engineering*, Chap. 4, Wiley and Sons, Edited by A. Luque and S. Hegedus, 2003.
- [18] NREL - National Renewable Energy Laboratory, <http://www.nrel.gov/>
- [19] B. Kumar, T.B. Pandian, E. Sreekiran and S. Narayanan, "Benefit of dual layer silicon nitride anti-reflection coating", *Record of the Thirty-first IEEE*

Photovoltaic Specialists Conference 2005, pp. 1205-1208, Pangalore, January 2005.

- [20] K.S. Han, H. Lee, D. Kim and H. Lee, "Fabrication of anti-reflection structure on protective layer of solar cells by hot-embossing method", *Solar Energy Materials and Solar Cells*, Vol. 93, No. 8, pp. 1214-1217, August 2009.
- [21] J.B. Chu, S.M. Huang, H.B. Zhu, X.B. Xu, Z. Sun, Y.W. Chen and F.Q. Huang, "Preparation of indium thin films without external heating for application in solar cells", *Journal of Non-Crystalline Solids*, Vol. 354, No. 52-54, pp. 5480-5484, December 2008.
- [22] A. Gombert, W. Glaubitt, K. Rose, J. Dreibholz, B. Blasi, A. Heinzl, D. Sporn, W. Doll, and V. Wittver, "Antireflective transparent covers for solar devices", *Solar Energy*, Vol. 68, No. 4, pp. 357-360, 2000.
- [23] T.-H. Chou, K.-Y. Cheng, T.-L. Chang, C.-J. Ting, H.-C. Hsu, C.-J. Wu, J.-H. Tsai and T.-Y. Huang, "Fabrication of antireflection structures on TCO film for reflective liquid crystal display", *Microelectronics Engineering*, Vol. 86, No. 4-6, pp. 628-631, 2009.
- [24] X. Hongbo, L. Nan, Q.-I. Dianpeng, G. Ligu, H. Juanyuan, W. Yandong and C. Lifeng, "Broadband antireflective Si nanopillar arrays produced by nanosphere lithography", *Microelectronics Engineering*, Vol. 86, No. 4-6, pp. 850-852, 2009.

CHAPTER 2

OPTIMIZATION OF PIN PHOTODIODES IN SOI TECHNOLOGY

2.1 *Introduction*

In this chapter, we present the lateral PIN diode used as a photosensor and its optical optimization. Since the devices are embedded in a thin silicon film, their optical sensitivity is mostly located in the low wavelengths close to blue and ultraviolet as introduced in the previous chapter. The context of utilization of the sensors will first be defined. A mathematical model was implemented to describe the electrical behavior of the diode and has been adapted to a multilayer device to include the anti reflection coatings (ARC) in the optical responsivities. An overview of the DC performances and the optical properties is first presented. Then, the optimization of the standard PIN photodiode in different SOI technologies is presented for deep UV and blue applications including the tuning of the electronic device itself and of different ARCs. Perspectives are described from simulations to adapt the model for more exotic technologies such as silicon-on-nothing (SON) and membrane structures. Finally, a comparison of the best results is made with current optical devices and the evolution of the performances for ultra-thin SOI technologies is presented.

2.2 *Context*

Optical detection at low wavelengths close to blue and ultraviolet (i.e. for $\lambda < 480nm$) is commonly used in biomedical and environmental fields. For example, DNA concentration measurement, bacteria or proteins detection require optical light

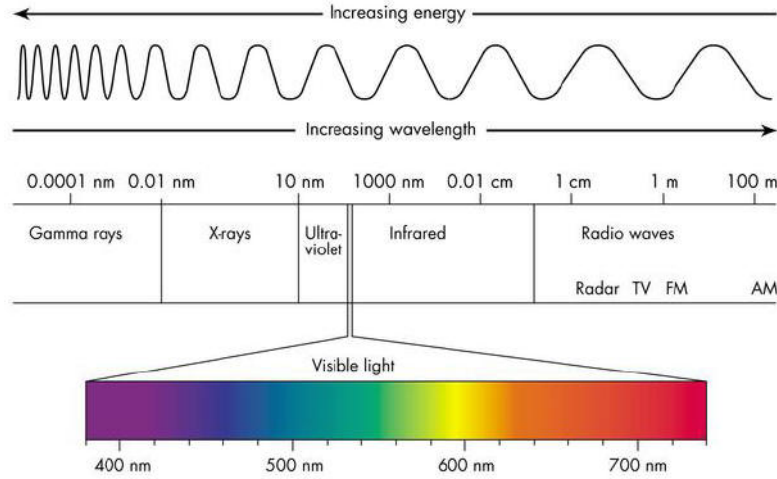


Figure 2.1: Electromagnetic spectrum [4].

whose emission wavelength is below $\lambda = 300nm$ [1, 2, 3]. On the other hand, UV and ozone rates are measured in upper wavelengths close to $\lambda = 400nm$. So, there is a real need for miniaturized sensors able to quantify optical signals in this wavelength range. In addition, such applications require low levels of detection, due to the low power of the emitted optical signals to monitor. It is thus important to minimize photodiode dark currents and to achieve high optical responsivities in order to reach a detection level as small as possible.

Considered wavelengths

The PIN diodes are embedded in the thin silicon film of the SOI wafer, they can only absorb light of low wavelengths as discussed in the first chapter. More precisely, the targeted wavelengths lay in the range from 200 to 480nm. The electromagnetic spectrum, as a function of the wavelength is shown in figure 2.1. The considered wavelengths are located from deep UV to blue-violet in the visible spectrum.

Applications

The applications targeted by optical measurements of blue/UV lights are numerous. More especially blue light, from 400 to 480nm, is directly linked to sleep-wake cycle

in two ways :

- by melatonin production. Melatonin is a molecule, regulating the sleep cycle, that is excited by darkness and suppressed by light, principally blue light at $480nm$. It has been showed that people wearing blue-blocking light glasses were in favorable sleepiness condition [5].
- by blue light exposure during night sleep. However blue light is blocking melatonin production during day-light, Harvard scientist proved that blue light exposure during the biological night directly and immediately improves alertness and performance of the patient during its day work [6].

The combination of these opposed effects has also been observed and studied by a Canadian research team [7]. It proves the need of blue light monitoring for this type of studies.

On the other hand, UV is known for being harmful for health, particularly concerning skin illnesses. Indeed, ultraviolet rays lying in the UV-B range (i.e. from 280 to $315nm$) can induce skin cancers. But UV rays are also present in many applications such as security, communications, fire-detection, curing, water turbidity measurement and many more. In biological field, DNA features an absorption peak at $260nm$ [8], which also requires an UV measurement of light as will be extensively described in chapter 4. However, measuring UV is also challenging due to the small number of low cost sensors able to detect such low wavelengths with precision.

2.3 *DC Performance of a Lateral PIN Diode : Overview*

The DC behavior of a lateral PIN diode has been presented and discussed by Afzalian in [9]. Then, we will not detail all the equations leading the computation of the current in the device. However, some important characteristics will be discussed in this chapter, and will be briefly described in this section. First, we define the carriers characteristics :

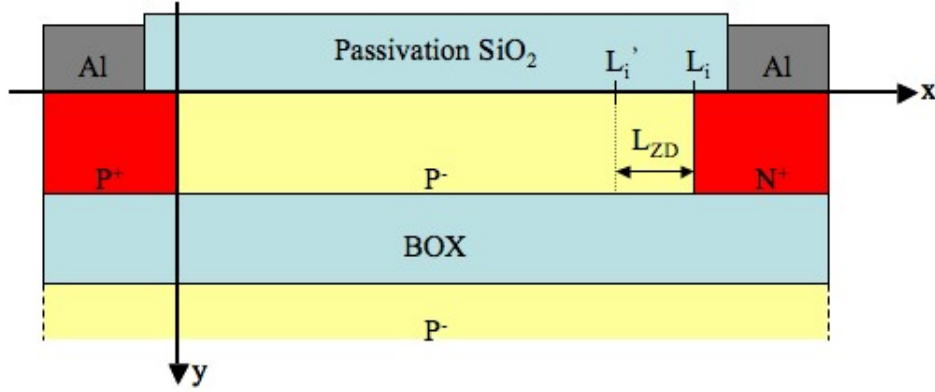


Figure 2.2: Sketch of the lateral PIN diode.

- their diffusion coefficients,

$$D_n = \mu_n \cdot \frac{k_B T}{q} \quad \text{and} \quad D_p = \mu_p \cdot \frac{k_B T}{q}, \quad (2.1)$$

where μ_n and μ_p are the electron and hole mobilities respectively.

- and their diffusion lengths,

$$L_n = \sqrt{D_n \cdot \tau_n} \quad \text{and} \quad L_p = \sqrt{D_p \cdot \tau_p}, \quad (2.2)$$

where τ_n and τ_p are the electron and hole lifetimes respectively.

If we refer to figure 2.2, the lateral depletion length is called L_{ZD} . By integrating the Poisson equation on the particular PIN lateral structure, we find:

$$L_{ZD} = \sqrt{\frac{2 \cdot \epsilon_{Si}}{q} \cdot \frac{(V_0 - V_D) \cdot (N_{A,P^-} + N_{D,N^+})}{N_{A,P^-} \cdot N_{D,N^+}}}, \quad (2.3)$$

where V_0 is the built-in potential and V_D is the external voltage applied to the diode. As we work on a slightly P doped substrate of silicon, the depletion length will almost be concentrated in the intrinsic zone of the P^-/N^+ interface.

As presented in chapter 1, the current in a photodiode under illumination has the form of equation 1.10. The generation can be considered as constant, regarding the small thickness of the silicon layer, and homogenous. So that the analysis can

be made in one dimension along x as demonstrated by Afzalian in [9]. But this total current, as recalling the diode fundamentals can also be written by :

$$J_{D,tot} = J_{n,P^-}(L'_i) + J_{p,N^+}(L_i) + q \cdot \int_{L'_i}^{L_i} G \, dx, \quad (2.4)$$

where $L'_i = L_i - L_{ZD}$. We can decompose the minority carriers current densities under illumination by :

$$J_{n,P^-}(L'_i) = J_{n,P^-} + q \cdot G \cdot L_n \cdot \tanh\left(\frac{L'_i}{L_n}\right) \quad \text{and} \quad (2.5)$$

$$J_{p,N^+}(L_i) = J_{p,N^+} + q \cdot G \cdot L_p \cdot \tanh\left(\frac{L'_i}{L_p}\right), \quad (2.6)$$

where J_{n,P^-} and J_{p,N^+} are the components of the saturation current of the diode in the dark. Since, $N^+ \gg P^-$, J_{p,N^+} becomes neglectable compared to J_{n,P^-} and we find that the total density of current in the lateral PIN photodiode is given by :

$$J_{D,tot} = J_{n,P^-}(L'_i) + q \cdot G \cdot (L_n \cdot \tanh\left(\frac{L'_i}{L_n}\right) + L_p \cdot \tanh\left(\frac{L'_i}{L_p}\right) + L_{ZD}), \quad (2.7)$$

where L_{ZD} reveals its importance and by the resolution of the transport equation of minority carriers in the structure,

$$J_{D,dark} = J_{n,P^-}(L'_i) = \frac{-q \cdot D_n}{L_n} \cdot n_{P^-} \tanh\left(\frac{L'_i}{L_n}\right) \cdot (e^{\frac{V_D}{V_T}} - 1). \quad (2.8)$$

Nevertheless, as used in passive mode, the diode is usually biased with a reverse voltage, typically ranging from $V_D = -0.1V$ to $V_D = -5V$. In this regime the generation current in the device becomes important and has to be added to the dark current. It has been expressed by Afzalian in [9] as :

$$J_{rg} = \frac{-q \cdot n_i}{2 \cdot \tau_{eff}} \cdot \min(L_i, L_{ZD}) \cdot (e^{\frac{V_D}{2 \cdot V_T}} - 1), \quad (2.9)$$

where τ_{eff} is the effective lifetime of electrons in the P^- region. J_{rg} is the dominant term in the particular operation regime in which the photodiode is used.

However, these equations are valid for a single diode while PIN lateral photodiodes are interdigitated diode with finger defined as in figure 1.7. If m indicates the number of finger, the total density of current is

$$J_{D,tot} = J_{D,F} \cdot m. \quad (2.10)$$

2.4 Optical Properties

2.4.1 The responsivity

As introduced in chapter 1, a photodiode can be characterized by different figures of merit. In this section, we will mainly discuss about the responsivity defined in equation 1.14. With the definition of the photocurrent and equations 2.7 and 2.8, the maximal responsivity becomes :

$$R_{max} = \frac{q \cdot A \cdot G \cdot (L_n + L_p + L_{ZD})}{P_{in}}, \quad (2.11)$$

and is achieved when $\tanh\left(\frac{L'_i}{L_n}\right) = 1$. It also appears that the maximal responsivity can thus be increased when increasing the depletion length. This can thus be made when the quasi intrinsic P^- zone is doped as less as possible. Furthermore, a low-doping zone increases the diffusion length of the electron which is also favorable for the responsivity. But to take full advantage of the diffusing electrons, the intrinsic length L_i must be as close as possible to L_n . However a too large intrinsic zone decreases the number of interdigitated diodes for the same area, which is contrarily opposed to a maximal responsivity.

The choice of the intrinsic length is thus a tradeoff to which we have to also add the parameter m for a finite area available to design a photodiode. Moreover, the anode and cathode regions, i.e. the N^+ and P^+ doped regions, are covered with aluminum. The available electrons from anode region which have been optically generated are limited due to reflections from aluminum and feature a low diffusion length due to the weak mobility in a high doped area. It is the same phenomenon for

holes generated in the cathode. Contrarily, the electrons generated in the intrinsic zone are more numerous and feature a higher diffusion length for the exact opposites reasons. So the L_n and L_p term in equation 2.11 have to be calculated carefully. To maximize the photocurrent, L_i has to be in the same order of magnitude of L_n due to the hyperbolic tangence dependency. Taking that into account and neglecting the holes generated at the cathode, the responsivity becomes :

$$R = \frac{q \cdot A \cdot G \cdot (L_n \cdot \tanh(\frac{L_i}{L_n}) + L_{ZD})}{P_{in}} = \frac{q \cdot A \cdot G \cdot L_{ph}}{P_{in}}, \quad (2.12)$$

where L_{ph} is the photosensitive length of one PIN diode finger.

2.4.2 Mathematical implementation of the reflections

To simulate the responsivity, the generation term on equation 2.12 has to be computed. Afzalian proposed an implementation of a mathematical model of reflections, transmission and absorption of electromagnetic waves inside a classical SOI structure as in figure 1.7 in [9]. The generation term is the absorbed wave in the thin Si film and is defined as the difference between the incident and the transmitted waves in the thin silicon layer. More details are described in the first appendix concerning the calculations of the responsivity.

For the measurement of the responsivity, a setup consisting of a halogen-deuterium light source, emitting from 200 to 1200nm followed by a monochromator allowed for selecting a single wavelength being incident to the surface of the diode thanks to an optical fiber. For each selected wavelength, the incident light power density is measured by a power meter and the total current is measured to which the dark current is subtracted. Due to the very low currents, a four-wires sensing method is preferred to monitor the current through the diode.

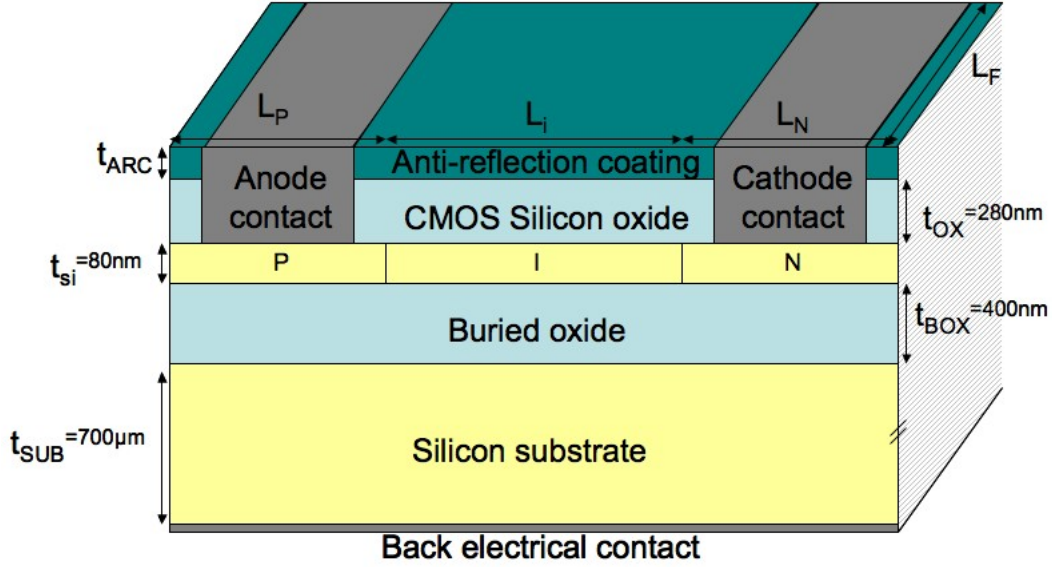


Figure 2.3: Transversal view of one finger of an interdigitated PIN lateral photodiode with typical dimensions of our UCL SOI technology.

2.4.3 Standard structure

A transversal view of one finger of a standard interdigitated photodiode is shown in figure 2.3 for the classical PIN photodiode in SOI UCL technology. The UCL SOI technology features an $80nm$ thick silicon layer which allows absorption of light below $\lambda = 400nm$. The thin Si film is separated from the silicon substrate by a $400nm$ buried silicon oxide. A CMOS process silicon oxide of $280nm$, which consists in a gate oxide of $30nm$ and an interdielectric oxide of $250nm$, covers the photodiode. In addition to this standard process, anti-reflection coatings of silicon oxide (SiO_2), silicon nitride (Si_3N_4) or alumina (Al_2O_3) can be deposited to reduce the reflections.

In most of the standard CMOS process on which the PIN photodiode can be implemented, the ARC consists of a passivation silicon oxide whose thickness is $500nm$ which implies a total SiO_2 of $780nm$ above the diode. The cathode and anode lengths are chosen as the minimal dimension of the source and drain contacts, to be of $L_N = L_P = 10\mu m$ in UCL SOI technology. With the mathematical model implemented in Matlab, we simulated and measured the spectral responsivity of a classical lateral PIN diode with intrinsic length of $L_i = 20\mu m$ and total area of $0.25mm^2$ according to the methods explained above. The comparison of simulation

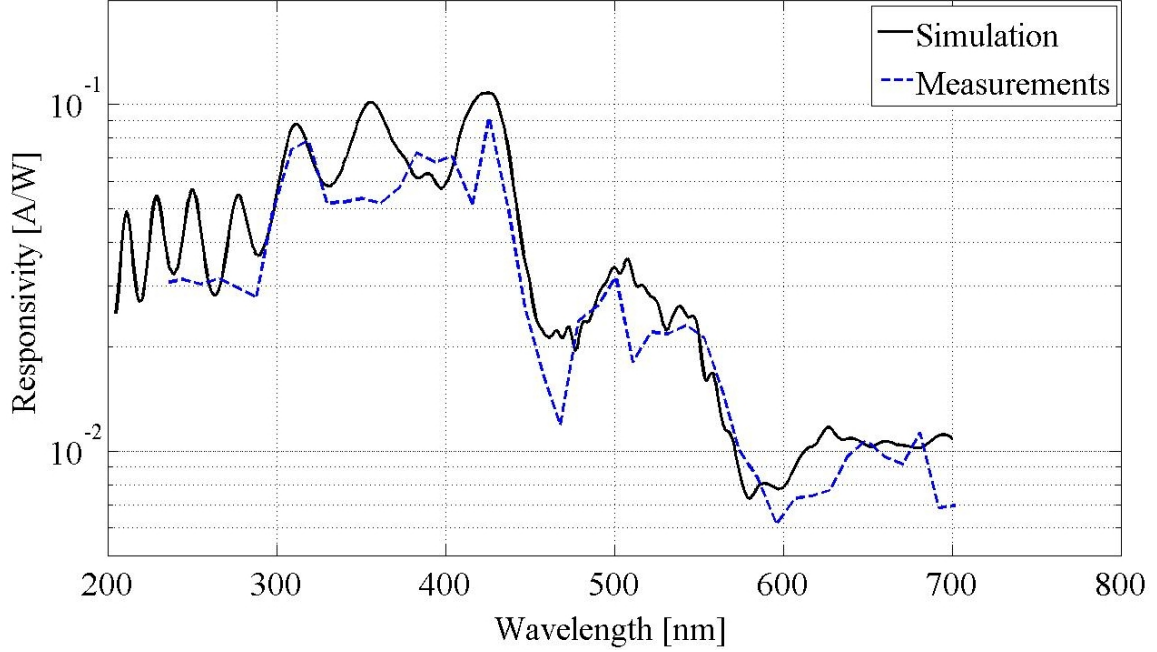


Figure 2.4: Simulation (continuous line) and measurements (dashed line) of the photodiode responsivity with SiO_2 ARC : $L_F = 1000\mu m$, $L_i = 20\mu m$, $L_N = L_P = 10\mu m$ and $\tau_{eff} = 0.1\mu s$ for $V_D = -0.5V$ and $t_{ARC} = 500nm$.

and measurements of its responsivity is shown in figure 2.4. The doping concentrations are $N_{A,P+} = 4 \times 10^{20}cm^{-3}$, $N_{D,N+} = 10^{20}cm^{-3}$ and $N_{A,P-} = 10^{15}cm^{-3}$ for the intrinsic region. Dark measurements of the diode in the range of $V_D = [0 ; 0.3V]$ allows us for measuring the effective lifetime in the diode (see equation 2.9) whose value was comprised between $0.07\mu s$ and $0.2\mu s$. For the simulations, τ_{eff} was then fixed at the value of $0.1\mu s$ which corresponds to a diffusion length of $L_n = 18\mu m$. The good fit of the measurement curve with the simulated one validates the model and the experimental setup. The global tendency of the responsivity is the same for both curves, however small oscillations occur below 400nm in the simulation and are not reported in the measurements. One reason may be related to small thickness variations of the silicon oxide layer along the total area of the device.

Figure 2.5 presents the responsivity variation at $\lambda = 250, 300, 350$ and $400nm$ for a $50nm$ variation of the total SiO_2 thickness around its $780nm$ expected thickness. The $50nm$ variation was chosen as 10% of the thickness of the last deposited layer. Indeed, the passivation silicon oxide suffers for more variability (and quality) than

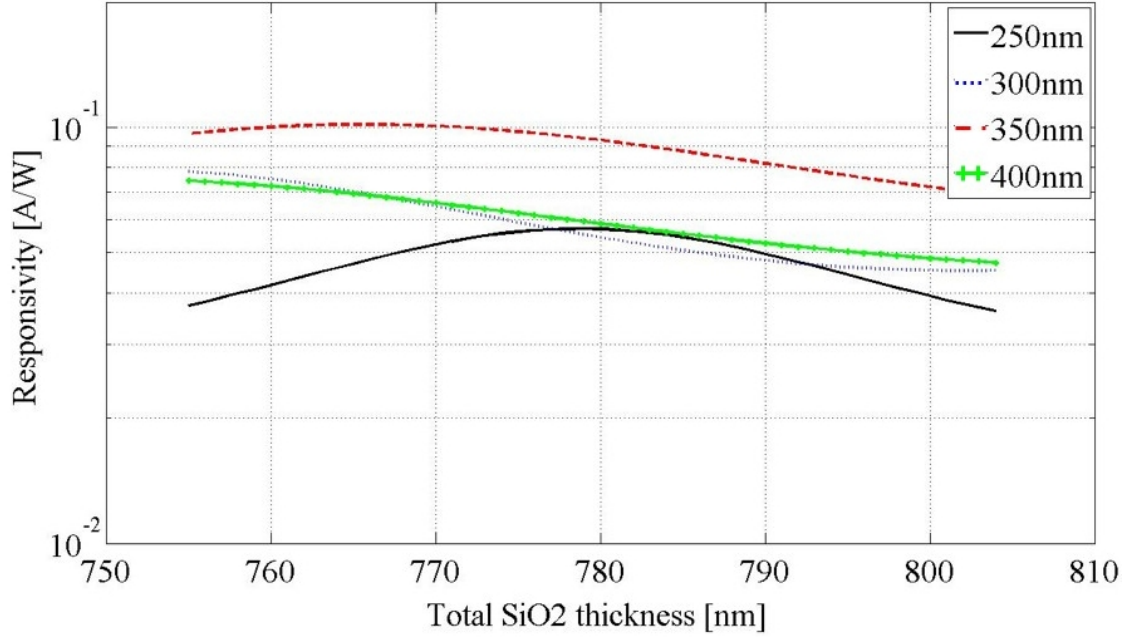


Figure 2.5: Responsivity variation of the photodiode at $\lambda = 250, 300, 350$ and $400nm$ with SiO_2 thickness varying from 755 to $805nm$ for $L_F = 1000\mu m$, $L_i = 20\mu m$, $L_N = L_P = 10\mu m$ and $\tau_{eff} = 0.1\mu s$ for $V_D = -0.5V$.

the gate and the inter-dielectric oxide. The slope deviance of responsivity varies at each wavelength according to the index of refraction of silicon and silicon oxide, and thus the global responsivity presents oscillations of variable amplitudes and locations below $400nm$ as can also be shown in figure 2.6. This reinforces the hypothesis proposed in figure 2.5, and also shows that process uniformities are not significant at upper wavelengths, since photons are not absorbed by the layer. By integrating the variations of the curves in figure 2.6, the measurement curve in figure 2.4 could be deduced and corroborate our hypothesis.

2.5 Responsivity Improvement

The curves of figure 2.4 show the potential of lateral PIN diodes to be excellent candidates for UV-blue photodetectors. But, even if they offer a suitable solar-blind filter shape, the responsivity magnitude in the targeted wavelength range can be improved to surpass state-of-the-art devices and the shape of the curve can also be

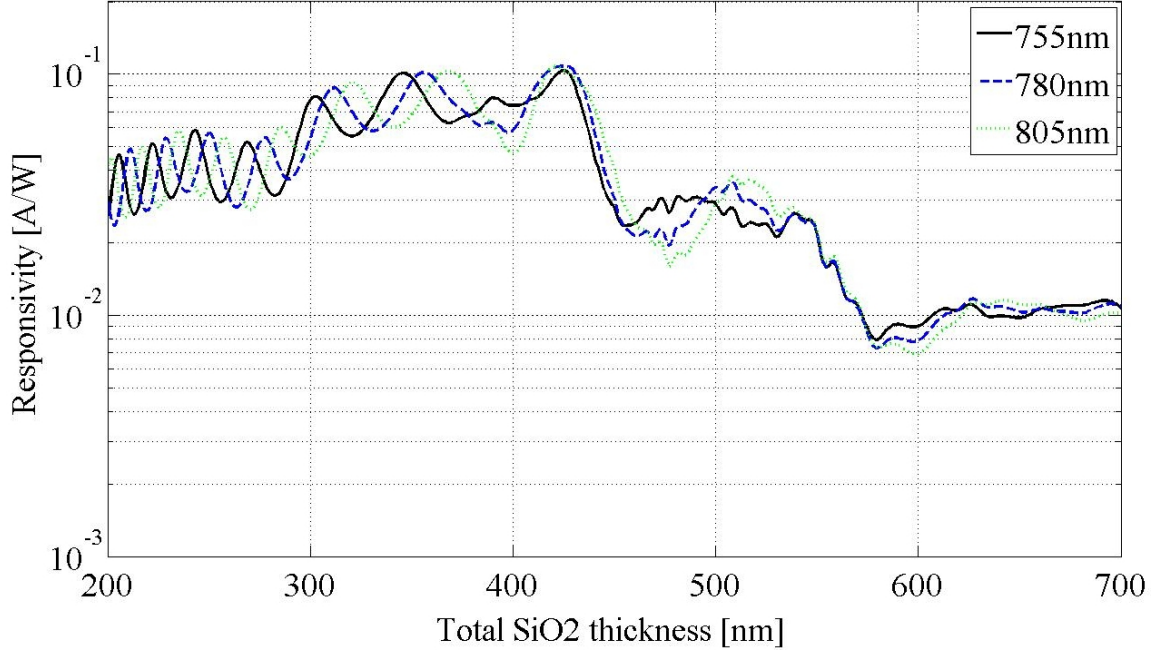


Figure 2.6: Responsivity variation of the photodiode with SiO_2 thickness of from 780 ± 25 nm for $L_F = 1000\mu m$, $L_i = 20\mu m$, $L_N = L_P = 10\mu m$ and $\tau_{eff} = 0.1\mu s$ for $V_D = -0.5V$.

adapted to be more wavelength sensitive, i.e. by having a higher cut-off slope after $400nm$.

2.5.1 Device optimization

As previously introduced, the design of the PIN diode is always a trade-off concerning the size of the intrinsic length. On one hand, a large intrinsic length will reduce the number of fingers and thus reduce the dark current. On the other hand, a large intrinsic length could increase the generated electrons-holes recombination. Consequently, L_i has to be reduced to increase the collection of generated carriers. Finally, the intrinsic length has to be adequately sized to maximize the photosensitive length of the diode.

As referred to equation 2.12, it would be possible to increase the responsivity by increasing the photosensitive length. Figure 2.7 shows the evolution of the photosensitive length L_{ph} of a single photodiode, i.e. one finger of the interdigitated diode. It proves that the photocurrent will increase with the intrinsic length augmentation

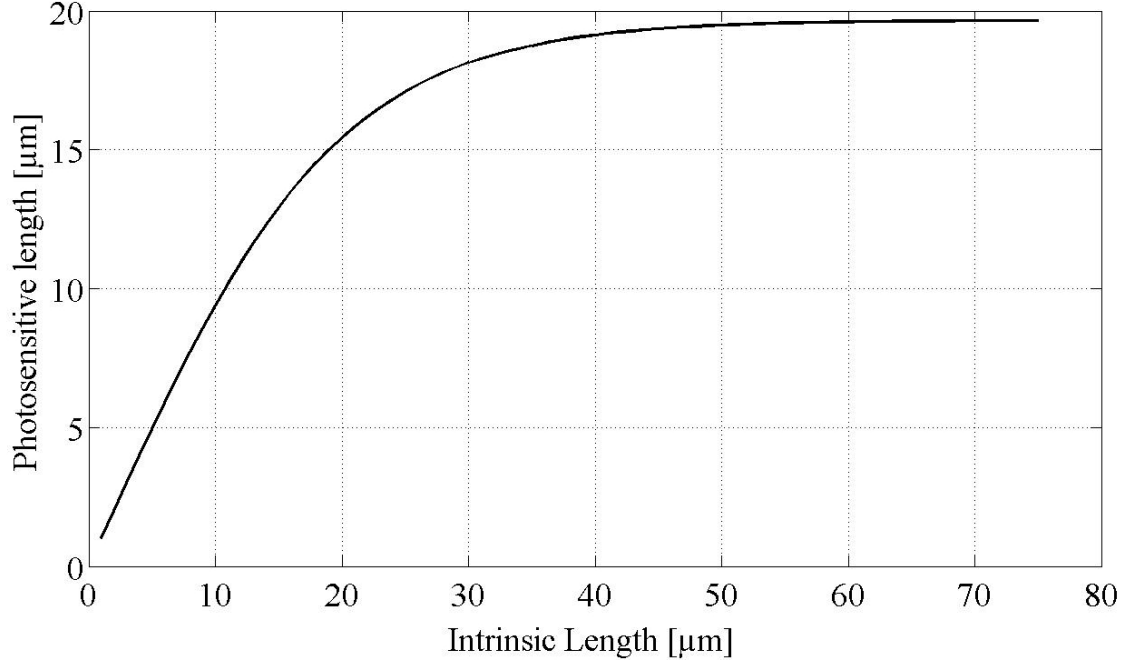


Figure 2.7: Evolution of the photosensitive length L_{ph} with the intrinsic length L_i at $\tau_{eff} = 0.1\mu s$.

and will logically saturate when the intrinsic length will become greater than the electron diffusion length where $L_{ph} \simeq L_i = 18\mu m$.

This is also illustrated in figure 2.8, where the ideal photosensitive area ratio is given by :

$$S_{ph,ideal} = \frac{m \cdot L_i}{m \cdot (L_N + L_P + L_i) + L_N}, \quad (2.13)$$

while the real photosensitive area ratio is defined by :

$$S_{ph,real} = \frac{m \cdot L_{ph}}{m \cdot (L_N + L_P + L_i) + L_N} \quad (2.14)$$

for photodiodes with m fingers.

The saturation of the photosensitive area maximum arises around the diffusion length of the electrons in the intrinsic zone as expected.

Moreover, a limiting factor is the surface of the light blocking regions, i.e. the anode and cathode covered with aluminum. In UCL SOI technology, the standard

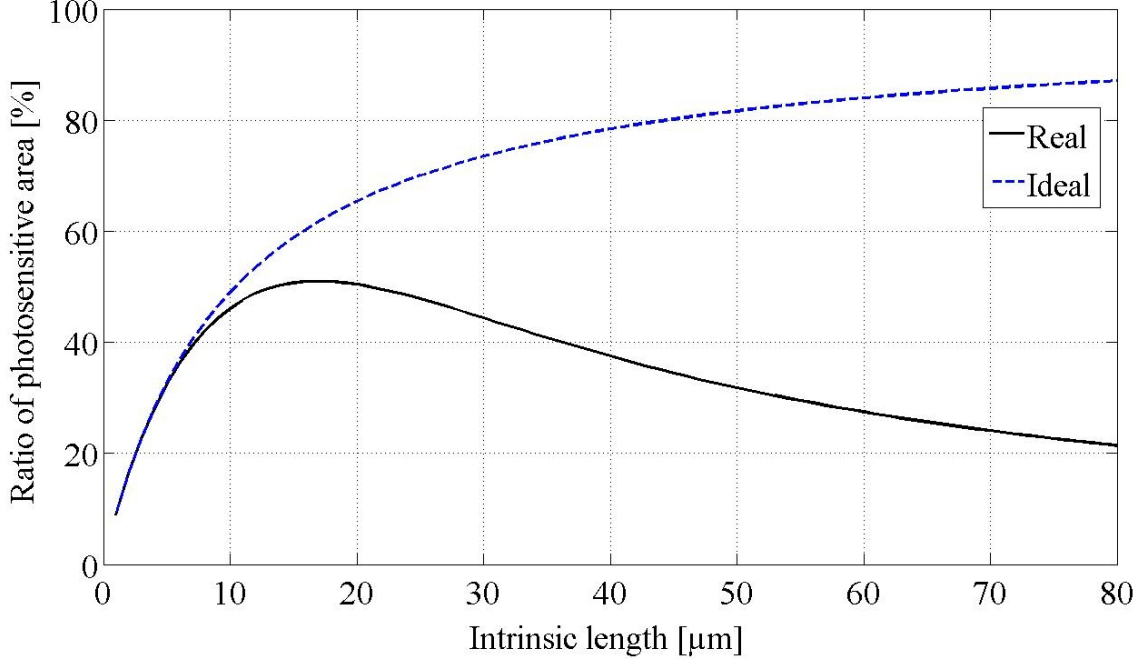


Figure 2.8: Evolution of the photosensitive area ratios S_{ph} with the intrinsic length L_i in the real (continuous line) and ideal (dashed line) cases at $\tau_{eff} = 0.1\mu s$.

L_N and L_P lengths are of $10\mu m$. It could be reduced to less than one micron in advanced industrial technologies. Figure 2.9 illustrates the benefit of this reduction on the photosensitive area ratio. By reducing the anode and cathode lengths to less than one micron, it is possible to almost double the photosensitive area and thus the responsivity.

2.5.2 ARC optimization

Another way to optimize the responsivity is to maximize the generation term G . As the standard basis of SOI wafer (consisting in the substrate and the buried oxide) is imposed by the fabrication process, and the thin Si film and the CMOS process oxide thicknesses are also constant on the wafer, the only parametrical layer is the additional ARC, which replaces a standard SiO_2 passivation layer. The reflected power can be minimized as described by the quarter-wave adaptation. The targeted wavelength in this section is $\lambda = 400nm$ being at the corner of the UV and the blue ranges. Silicon nitride (Si_3N_4) and alumina (Al_2O_3) are materials widely used

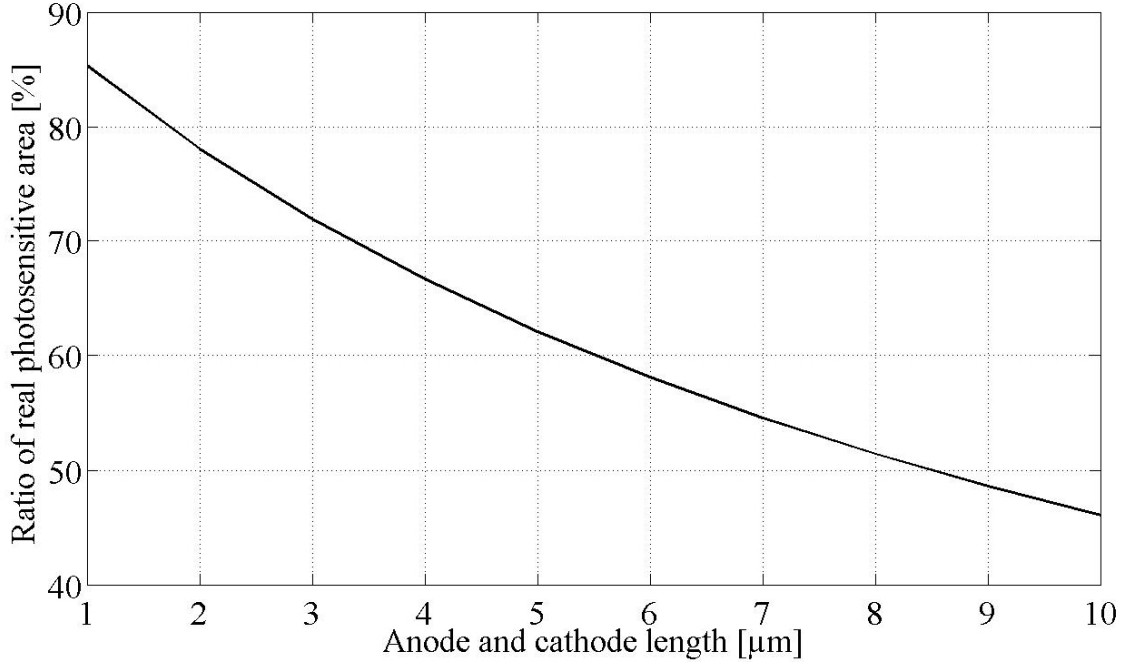


Figure 2.9: Evolution of the real photosensitive area ratio $S_{ph,real}$ with the anode and cathode length $L_{N,P}$ at $L_i = 18\mu\text{m}$ and $\tau_{eff} = 0.1\mu\text{s}$.

in CMOS process as anti-reflecting coatings. Their index of refraction allows for reducing reflections when combined to silicon oxide creating a dual-layer ARC [10].

Simulations

Figure 2.10 shows the responsivity evolution at $\lambda = 400\text{nm}$, for a PIN diode with top ARC in silicon nitride or aluminum oxide. The responsivity features a periodical response with the second ARC thickness for which the first 100nm are presented in figure 2.10. Both materials can improve the responsivity at 400nm by a factor of about two even if nitride seems a little bit more performant for a lower thickness.

The spectral responsivities for the photodiodes with $L_F = 500\mu\text{m}$, $L_i = 18\mu\text{m}$, $L_N = L_P = 10\mu\text{m}$ and $\tau_{eff} = 0.1\mu\text{s}$ are simulated in figure 2.11 for a reverse bias of $V_D = -0.5\text{V}$. The responsivity improvement compared to the standard structure with the natural SiO_2 passivation layer is well confirmed at 400nm as expected. The benefit of adding a nitride or alumina layer can also be observed at upper wavelengths, for example around 500nm. However, the response in the UV

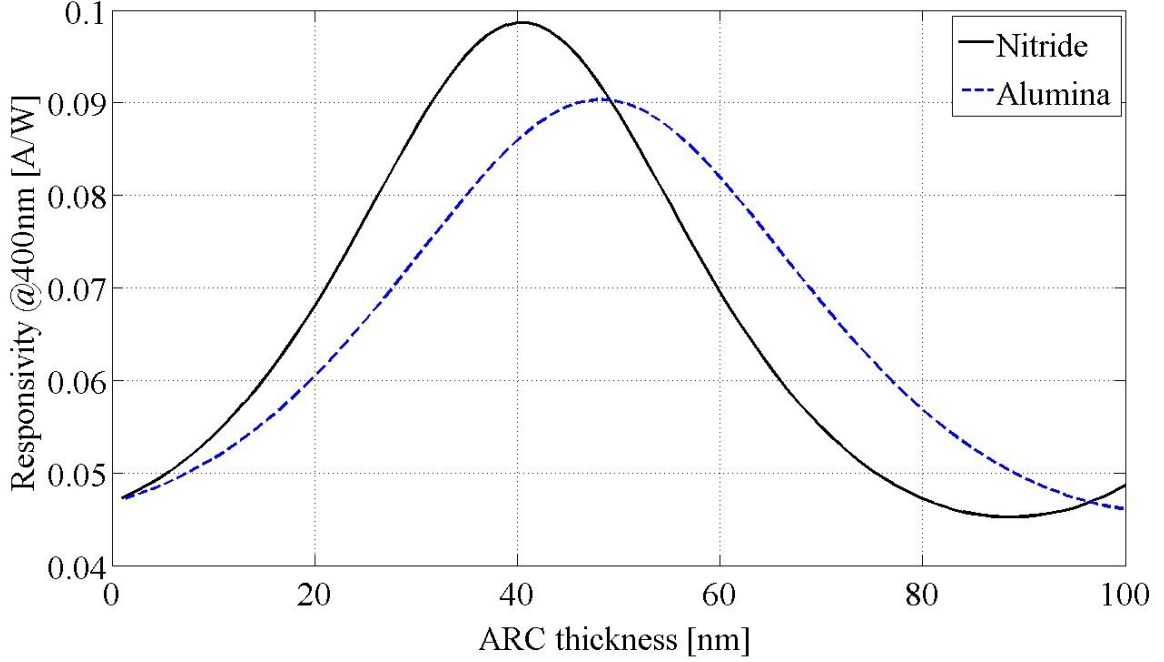


Figure 2.10: Evolution of the responsivity of PIN lateral photodiode as a function ARC thickness in Si_3N_4 and Al_2O_3 with $L_{N,P}$ at $L_i = 18\mu m$ and $\tau_{eff} = 0.1\mu s$ for silicon nitride (continuous line) and aluminum oxide (dashed line) over $280nm$ of SiO_2 .

bandwidth seems lower. It is indeed difficult to minimize reflections at a precise wavelength without handicap other ones when designing a photosensor for a specific application. Nevertheless, previous measurements proved that regions where the simulated responsivity features oscillations should not be worrying due to process non-uniformities.

Measurements

The responsivity of photodiodes passivated with silicon nitride and aluminum oxide has been measured and is showed in figures 2.12 and 2.13 for squared photodiodes with $L_F = 1000\mu m$, $L_i = 8\mu m$, $L_N = L_P = 9\mu m$ and $\tau_{eff} = 0.1\mu s$ at $V_D = -0.5V$. The ARC thicknesses were chosen to minimize the reflections as in figure 2.10. Measurements are fitting the simulated curves from $\lambda = 400nm$ to upper wavelength. As for the silicon dioxide, the oscillations in the UV range leave place to a smoother curve in the responsivity measurement. In the previous figures (2.11, 2.12 and

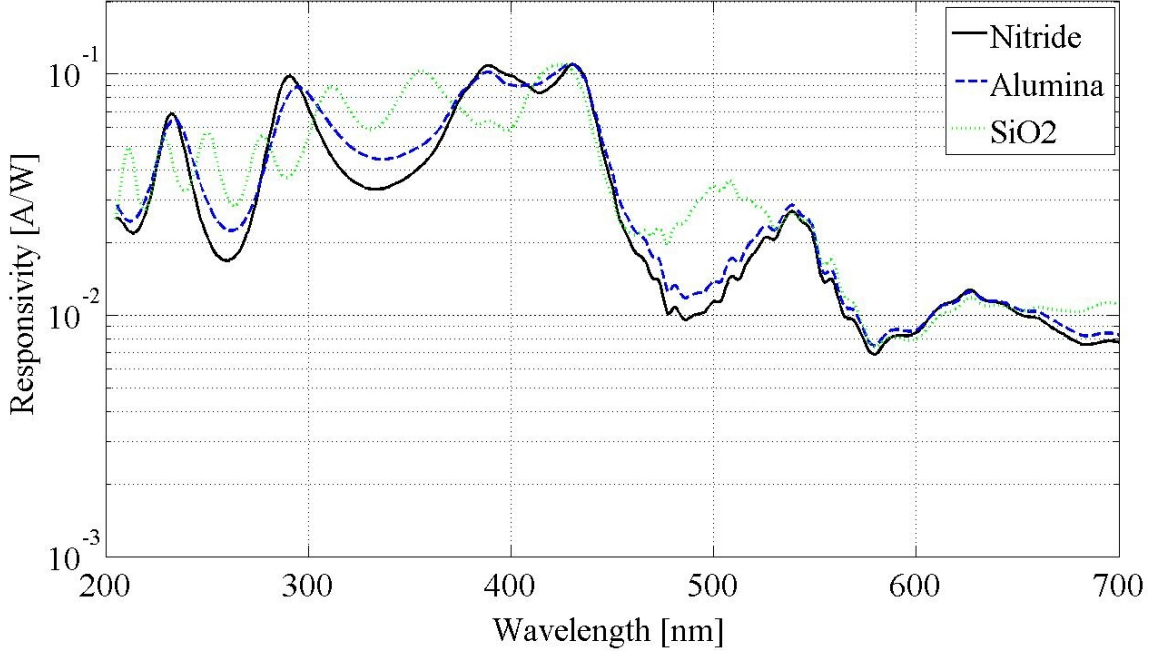


Figure 2.11: Comparison of simulated photodiode responsivities : $L_F = 500\mu m$, $L_i = 18\mu m$ and $L_N = L_P = 10\mu m$, $\tau_{eff} = 0.1\mu s$ for $V_D = -0.5V$ with different ARCs : silicon nitride (continuous line) of $40nm$ over $280nm$ of SiO_2 , aluminum oxide (dashed line) of $48nm$ over $280nm$ of SiO_2 and silicon dioxide (dotted line) of $780nm$.

2.13) the cut-off wavelength of the responsivity was of about $\lambda_c = 435nm$, and an attenuation of 90% was reached after $50nm$.

2.5.3 Improved SOI structures

Another important improvement would be the adaptation, i.e. the reduction, of the front silicon oxide thickness while keeping an appropriate Si_3N_4 thickness to increase the absorption at $400nm$. It could also reduce the oscillations in the bandwidth and considerably increase the responsivity values at different wavelengths.

The figure 2.14 presents the responsivity at $400nm$ with the thicknesses of SiO_2 and Si_3N_4 deposited as anti-reflection coatings on the top of the lateral PIN photodiode. An optimal $t_{ARC} = 48nm$ of Si_3N_4 over a minimal silicon oxide layer allows a maximal responsivity of $0.1A/W$ at $400nm$. The total responsivity of the photodiode with $t_{ARC} = 48nm$ and $t_{OX} = 1nm + k \cdot 134$ is shown in figure 2.15 (continuous line)

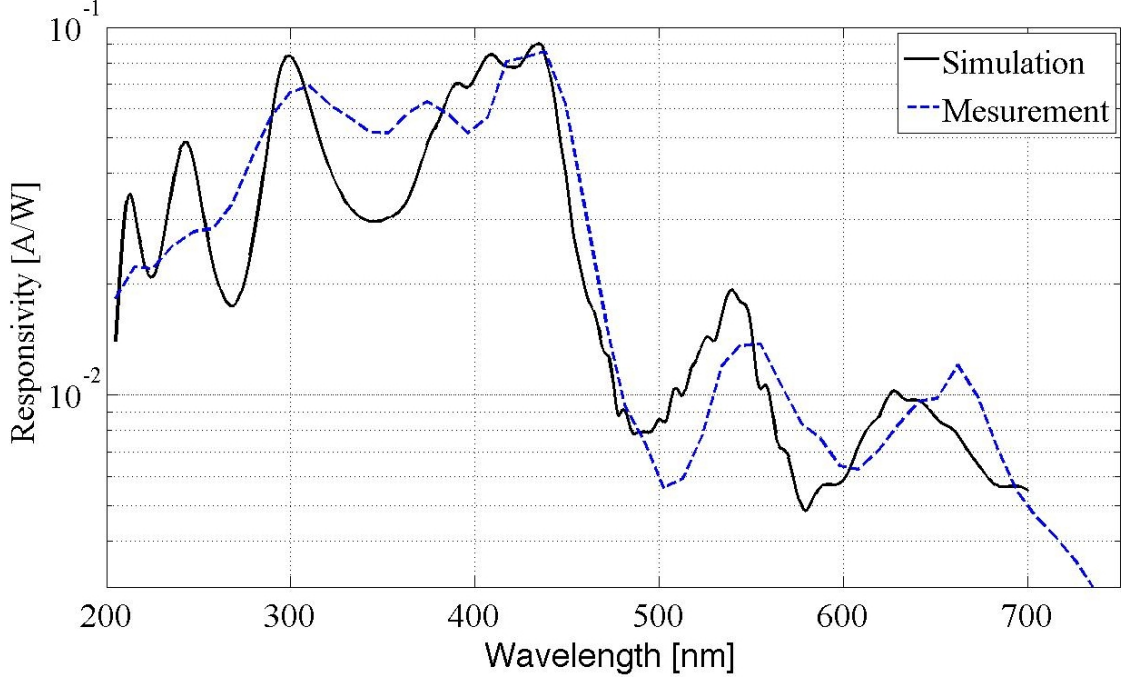


Figure 2.12: Simulation (continuous line) and measurements (dashed line) of the photodiode responsivity with Si_3N_4 ARC : $L_F = 1000\mu m$, $L_i = 8\mu m$ and $L_N = L_P = 9\mu m$ $\tau_{eff} = 0.1\mu s$ for $V_D = -0.5V$ and $t_{ARC} = 40nm$ with $t_{OX} = 280nm$.

where it is compared to other responsivities in various SOI technologies. However the $1nm$ silicon dioxide is very difficult to fabricate, and the next periodical oxide thickness of $135nm$ implies a more oscillating shape of the responsivity below $400nm$. That is why the simulation features a silicon dioxide thickness of $t_{OX} = 6nm$ as it has previously been realized in our SOI technology [11].

Based on the same structure (i.e. using similar material layers superposed in the same order) but with lower thicknesses of the layers as well as lower lateral dimensions of the PIN diode, a similar device has been investigated in a $150nm$ fully-depleted SOI CMOS process by *OKI Semiconductor* [12]. Featuring a Si film thickness of $t_{Si} = 50nm$, the dark measurements of the diode showed an effective lifetime in the diode whose value was comprised between $0.05\mu s$ and $0.15\mu s$. The associate value for the simulation was thus again $\tau_{eff} = 0.1\mu s$. Our simulations in figure 2.15 (dashed line) indicate higher responsivity values thanks to an increase of the sensitive area (the anode and cathode lengths are reduced to less than $1\mu m$) but

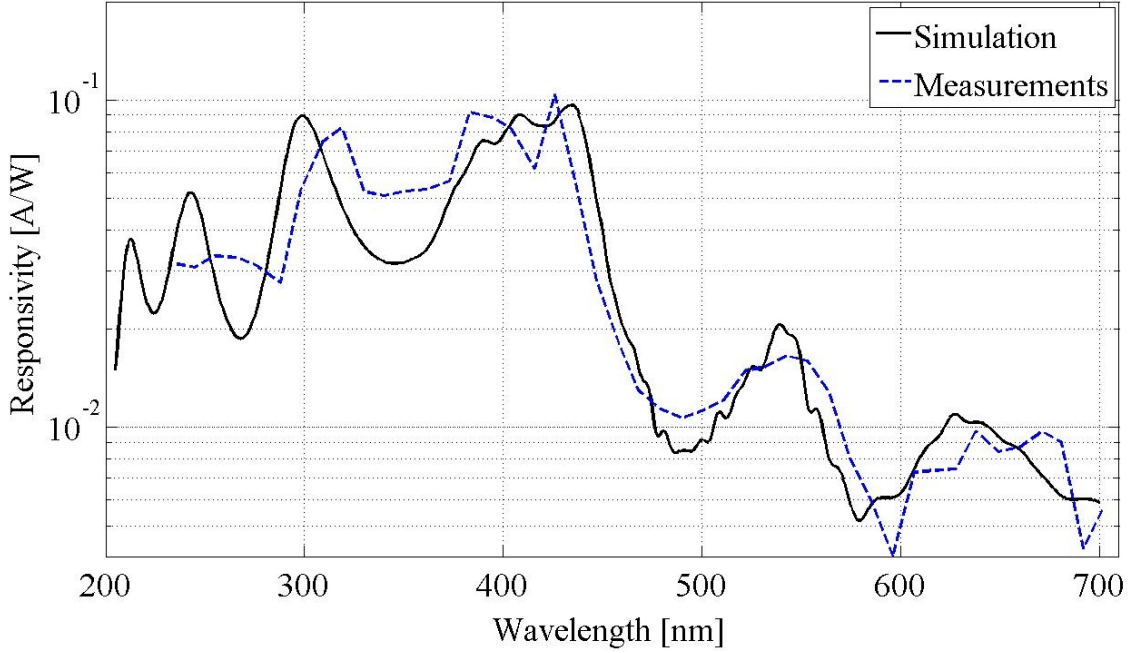


Figure 2.13: Simulation (continuous line) and measurements (dashed line) of the photodiode responsivity with Al_2O_3 ARC : $L_F = 1000\mu m$, $L_i = 8\mu m$ and $L_N = L_P = 9\mu m$ $\tau_{eff} = 0.1\mu s$ for $V_D = -0.5V$ and $t_{ARC} = 50nm$ with $t_{OX} = 280nm$.

the cut-off wavelength is lowered to $\lambda_c = 380nm$ due to our reduction of the silicon film thickness and the attenuation of 90% is now achieved over $200nm$ because of the thicker top oxide ($t_{OX} = 8260nm$) in that industrial process with a large number of metal layers.

As observed with the $150nm$ CMOS process simulations and predicted by our simulation in figure 2.9, an easy way to increase responsivity is to reduce the anode and cathode areas. Nevertheless, the carriers lifetime which depends on the quality of the material may be improved in industrial processes. The effective lifetime is mainly determined by the surface recombination velocities at the interfaces between the thin silicon film with front gate and buried oxides. These interfaces can be improved which can reduce the recombination velocities leading to an augmentation of the effective lifetime. In smart-cut process, the quality of the thin Si film interface with BOX is determined by the wafer fabrication and can be improved by the fabricant through technology advances [13]. Moreover, the quality of thin Si film interface with gate oxide can be improved by using a vertical oven for example, ensuring no

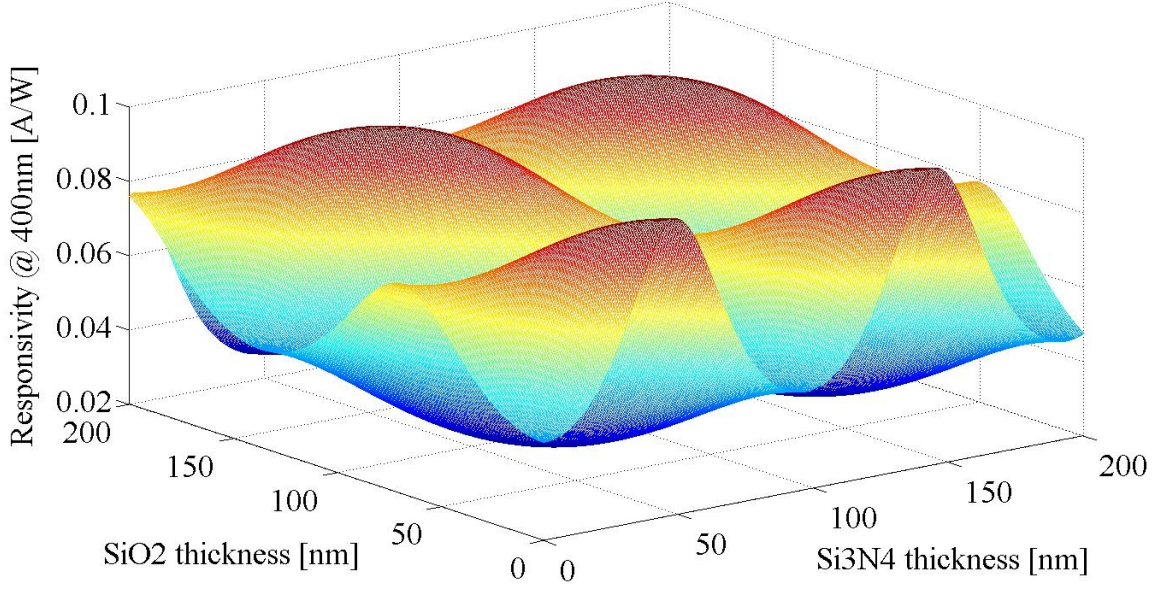


Figure 2.14: Photodiode responsivity at 400nm with SiO_2 and a Si_3N_4 ARC thickness variation : $L_F = 500\mu m$, $L_i = 18\mu m$ and $L_N = L_P = 10\mu m$ $\tau_{eff} = 0.1\mu s$ for $V_D = -0.5V$.

Techno	t_{Si} (nm)	$L_{N,P}$ (μm)	τ_{eff} (μs)	t_{OX} (nm)	t_{ARC} (nm)	$R(A/W)$
$2\mu m$ UCL	80	9	0.1	6	48	0.1
150nm OKI	50	1	0.1	8260	NA	0.1
Improved	80	1	1	6	48	0.18

Table 2.1: SOI photodiodes characteristics.

air contamination during the growth of the 30nm SiO_2 . Recent experiments in the UCL fabrication cleanrooms proved that the carrier lifetimes can be increased by a factor near to 5 when the front gate oxide is grown in a *Koyo* vertical oven.

The dotted curve in figure 2.15 presents the responsivity of an improved SOI technology with minimal anode and cathode length, an ideal ARC thickness and an effective lifetime of $\tau_{eff} = 1\mu s$. We obtain high responsivity values in UV, close to $R = 0.2A/W$ with a spectral cut-off wavelength of $\lambda_c = 400$ nm. The table 2.1 summarizes the characteristics of the three SOI simulations of figure 2.15 and gives the responsivities at $\lambda = 400nm$. A first observation is that the reduction of L_N and L_P is very useful to improve the responsivity values. The thinner silicon dioxide is as well appreciable to obtain a smoother curve in the UV bandwidth. However, the decreasing slope of the curve is lower than with the standard thicknesses of the $2\mu m$

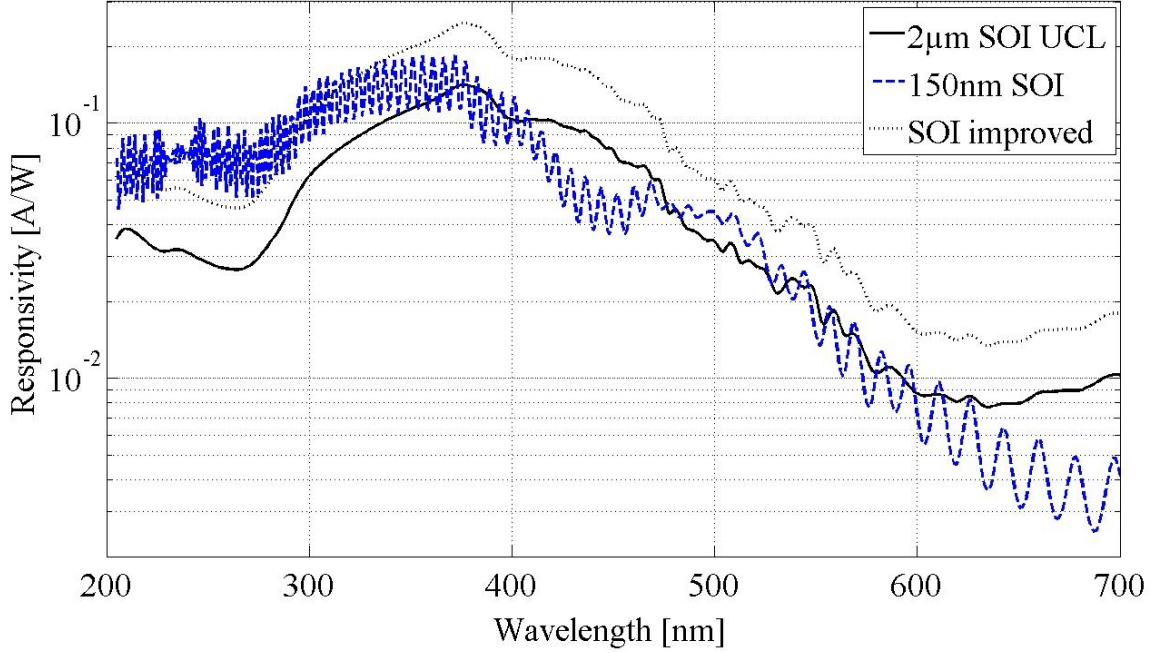


Figure 2.15: Simulations of SOI improved structures with $L_i = 18\mu\text{m}$: UCL $2\mu\text{m}$ SOI with $t_{ARC} = 48\text{nm}$ and $t_{OX} = 6\text{nm}$ (continuous line), 150nm SOI (dashed line) and improved SOI structure (doted line).

CMOS SOI process as presented in figures 2.12 and 2.13 where the silicon dioxide was thicker (i.e. $t_{OX} = 250\text{nm}$). Finally, the material quality linked to the effective lifetime is essential as seen with a double responsivity when τ_{eff} is increased ten times.

2.6 SOI-Based Specific Structures

The SOI substrate can also be the starting point of advanced technologies used in complex electronic transducers and MEMS, for example, the silicon-on-nothing (SON) and membrane SOI structures.

2.6.1 Silicon-on-nothing structure

The silicon-on-nothing technology consists in etching a part of the buried oxide under the thin silicon film and fill it either with an appropriate dielectric or with air [14]. The air cavity can be realized either by vapor-HF etching (for full etching below the

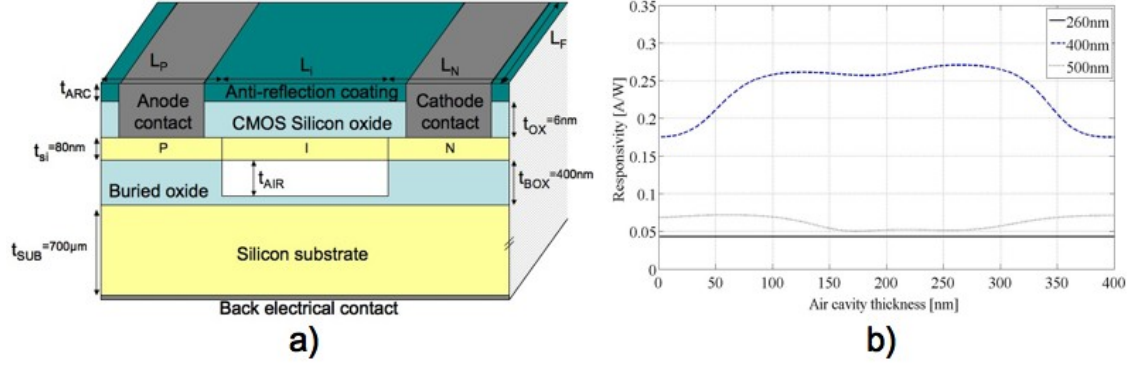


Figure 2.16: Structure of a silicon-on-nothing photodiode (a) and its simulated responsivity at $\lambda = 260nm$ (continuous line), $\lambda = 400nm$ (dashed line) and $\lambda = 500nm$ (dotted line), as a function of the air cavity thickness(b). At figure a, $t_{OX} = 6nm$, $t_{ARC} = 48nm$, $L_i = 18\mu m$, $L_N = L_P = 1\mu m$ and $\tau_{eff} = 1\mu s$.

Si channel) or pre-etching (for a more controlled air thickness). In the last case, the thin Si film is then deposited over the cavity. The SON structure has been realized in SOI technology by pre-etched cavity method [15] and has proven good behavior. Figure 2.16-a presents the structure of the SON photodiode embedded in the thin film over the air gap with thickness t_{air} . The responsivity of the SON structure at 260, 400 and 500nm is showed in figure 2.16-b as a function of the air cavity thickness. The other characteristics are similar to the improved SOI technology as referred in table 2.1. The behavior of the responsivity is very different for each wavelength. Indeed, for $\lambda = 260nm$, the light is already entirely absorbed in the thin Si film and the responsivity is thus constant for any layer below the thin film. We can observe a maximal value of R at 400nm when $t_{air} = 270nm$ for $t_{air} + t_{BOX} = 400nm$. The responsivity at this wavelength is minimal for 0 and 400nm air thicknesses (i.e. for 400 and 0nm BOX thicknesses respectively) for which destructive interferences appear at this wavelength. Due to the interface with the BOX, light begins to be reflected if an air cavity is created and the responsivity becomes flat from 100 to 300nm since all the reflected light will be absorbed in the thin film. Concerning the responsivity at 500nm, it is also periodical but the destructive interferences are shifted since the combined air/BOX thickness is not a multiple of its wavelength. Indeed, in simulations, the evolution of the responsivity at 500nm is similar to figure

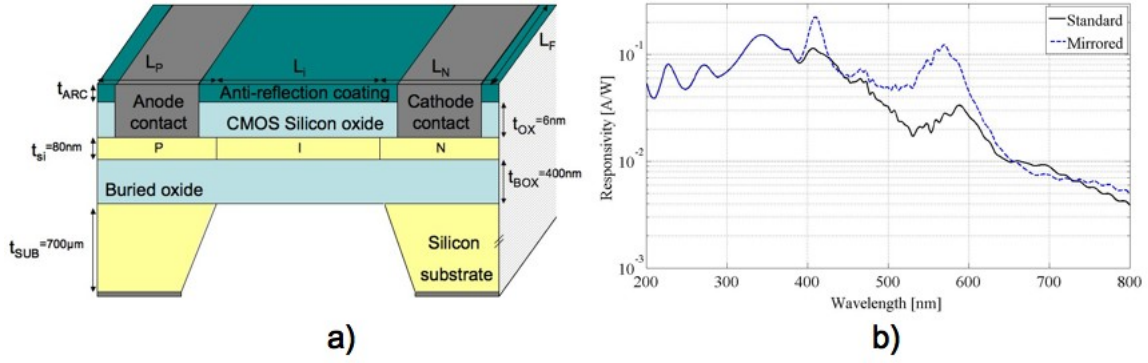


Figure 2.17: Structure of a membrane (a) and its responsivity at $\lambda = 400nm$ as a function of the air cavity thickness. At figure a, $t_{OX} = 6nm$, $L_N = L_P = 1\mu m$ and $\tau_{eff} = 1\mu s$. $t_{ARC} = 48nm$ for un-mirrored membrane (standard), $t_{Al} = 900nm$ for the mirrored membrane.

2.16-b) if $t_{air} + t_{BOX} = 500nm$. The simulation of the complete responsivity in figure 2.18 (continuous line) shows that this structure could allow for reducing the spectral sensitive bandwidth, in order to be more selective around $\lambda = 375nm$ while keeping high responsivity values.

2.6.2 Membrane structure

As for the SON technology, the SOI wafer can be adapted by flipping the wafer and etching isotropically the silicon bulk [16]. By following the crystalline planes of the silicon down to the buried oxide, a trapezoidal cavity can be obtained under the photodiode resulting to a membrane as showed in figure 2.17-a. The membrane structure could also be back illuminated and the responsivity of the photodiode with characteristics similar to the improved SOI technology as referred in table 2.1 is showed in figure 2.17-b (continuous line) in the case of backside illumination.

The membrane can be improved by adding an aluminum layer, as for the anode and cathode contacts over the top of the intrinsic region. The aluminum has to be separated from the silicon by the thin $6nm$ silicon oxide in order to avoid Schottky contacts and to prevent recombination issues at the interface. Of course if the recombination speed is $S = \infty$ along the intrinsic zone, the responsivity will drastically go down and the photodiode will loose its interest. The responsivity of

the mirrored membrane photodiode is also showed in figure 2.17-b (dashed line). A first observation is that the responsivity around $400nm$ is greatly improved with the presence of a narrow peak of $0.28A/W$ around $410nm$. However, the metal layer also reflects light with higher wavelengths from 530 to $580nm$. Nevertheless this can also be an advantage if there is a need for increasing the spectral bandwidth without increasing the thin silicon film thickness.

2.6.3 Best expected responsivities

A comparison and summary of the best responsivities achieved by the different SOI technologies is presented in figure 2.18 : the improved SOI technology, the SON and the mirrored membrane structures. For the device dimensions, each photodiode features the following parameters : $t_{OX} = 6nm$, $L_i = 18\mu m$, $L_N = L_P = 1\mu m$ and $\tau_{eff} = 1\mu s$. The SON and improved SOI feature a Si_3N_4 ARC with $t_{ARC} = 48nm$ and the aluminum thickness in the mirrored membrane photodiode has a thickness of $t_{Al} = 900nm$.

At $\lambda = 400nm$, the SON structure features the highest responsivity of $0.27A/W$. Both SON and the improved SOI photodiodes present a smooth response with a bell shape from 300 to $450nm$. However from $420nm$ to the upper wavelengths, the slope of the SON structure is more favorable to a blue/UV sensor with a lower responsivity. Both membrane and optimized SOI devices reach a responsivity of about $0.18A/W$ at $400nm$ but the membrane behaves more oscillatingly under $500nm$ and presents the disadvantage of a responsivity peak in upper wavelengths.

2.7 Comparison with Other Technologies

Table 2.2 summarizes most representative results for the previously cited technologies. For classical Si photodiodes (i.e. except for avalanche diodes or else), SOI technology remains much more efficient than classical bulk silicon as can be seen on the table above. Comparatively, larger bandgap materials can achieve a higher responsivity, but their fabrication cost is much higher and even if SOI technology

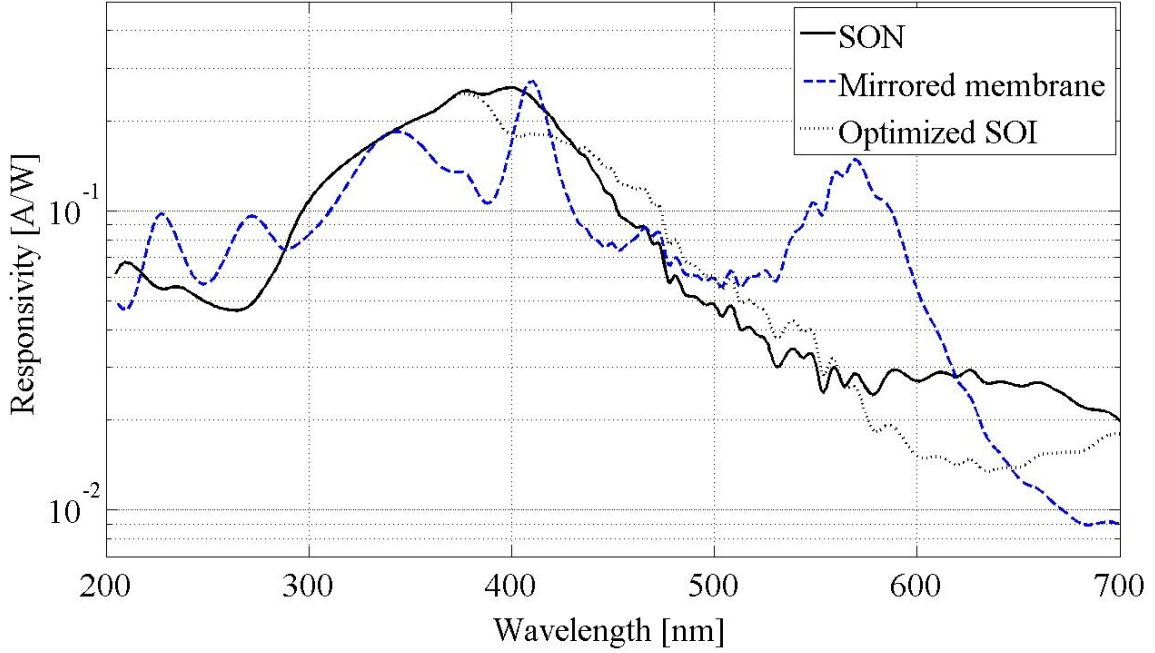


Figure 2.18: Simulations of lateral PIN photodiodes optimized in different technologies and their comparison to the improved SOI structure.

reaches a lesser responsivity, its value remains on the same order of magnitude than the other semiconductor materials.

2.8 Responsivity Adaptation for Different Applications

As presented in the beginning of this chapter, the thin-film photodiodes are used to measure light ranging from 200 to 480nm. This chapter was focused to improve the responsivity of photodiodes around the precise wavelength $\lambda = 400nm$. But in biological process, UV lights have to be monitored and measured with high precision. For example in DNA quantification ($\lambda = 260nm$) or purity and proteins quantification ($\lambda = 280nm$). The blue light around $\lambda = 480nm$ has also to be measured for sleepiness studies.

Table 2.3 summarizes, for the optimized SOI and SON structures, the ARC thickness and air cavity thickness (with the same ARC respectively as the optimized

Source	Techno	Performance
This work	Improved SOI	$R = 0.18@400nm$
This work	SON	$R = 0.27@400nm$
[17]	Bulk Si	$R = 0.025@400nm$
[18]	Bulk Si	$R = 0.05@400nm$
[19]	Bulk Si (lateral)	$QE = 67@400nm$
[20]	Bulk Si (Avalanche)	$R = 0.17@400nm$
This work [21]	SOI	$R = 0.1@400nm$
[22]	SOI	NA
[23]	GaN	$R = 0.15@[300 - 400]nm$
[24]	GaN	$R = 0.18@350nm$
[25]	AlGaN	$R = 0.1@250nm$
[26]	AlGaN	$R = 0.2@350nm$
[27]	SiC	$R = 0.15@280nm$
[28]	SiC	$R = 0.26@380nm$
[29]	Si and Patterned ARC	$QE = 60@400nm$

Table 2.2: Comparison of the photodiode characteristics among the different technologies.

λ (nm)	t_{ARC} (nm)	R(A/W)	t_{air} (nm)	R(A/W)
260	16	0.14	NI	0.14
280	20	0.15	NI	0.15
400	48	0.18	270	0.27
480	55	0.1	75	0.11

Table 2.3: Parameters of the optimized SOI and SON structures for $\lambda = 260, 280, 400$ and $480nm$.

SOI diode associated with the same wavelength) at $\lambda = 260, 280, 400$ and $480nm$ with the responsivity obtained with the parameters at the targeted wavelength.

As showed in this table, the air thickness cavity has no influence (NI) at 260 and $280nm$ where the photons have completely been absorbed in the thin silicon film. But the Si_3N_4 thickness combined to a thin oxide film ($t_{OX} = 6nm$) increases with the absorption length. In terms of applications of the structures, the air cavity can also be used for special application (e.g. by introducing particles or gases in the cavity for a detection based on the refraction index variation) while the membrane can be a receptacle for particles or biological components to be optically characterized.

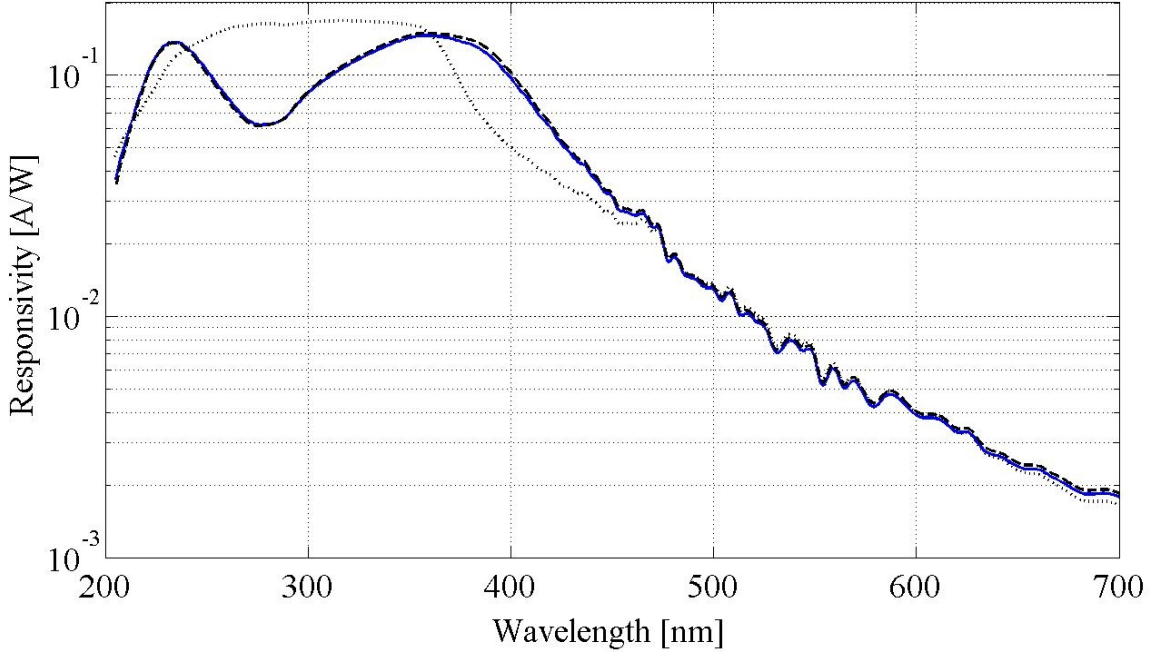


Figure 2.19: Simulations of UTISOI photodiodes responsivities with Si_3N_4 ARC, $L_i = 18\mu m$, $L_N = L_P = 1\mu m$ and $\tau_{eff} = 1\mu s$. $t_{ARC} = 20nm$ for 260nm target (dotted line), and $t_{ARC} = 60nm$ for 400nm target in SOI (continuous line) and SON (dashed line) with full air cavity ($t_{air} = 20nm$).

Perspective in ultra-thin SOI technologies

For current state-of-the-art research technologies, the thin Si film is reduced to a few nanometers leading to ultra-thin silicon-on-insulator (UTSOI) technology. For example in IBM technology, the thin silicon film features a thickness of $10nm$, while the buried oxide is $20nm$, and the top silicon oxide has an equivalent thickness of $3nm$ [30]. It has already been showed in figure 2.15 that a short reduction of the thin film decreases the absorption of light for visible wavelengths. This is explained by the dependency of the absorption length on the wavelength (cfr figure 1.2 in chapter 1). It is thus supposed that a $10nm$ thin Si film will only absorb deep-UV wavelengths. A simulation of lateral photodiodes in UTISOI technologies is presented in figure 2.19. The photodiodes parameters for the simulation are $L_i = 18\mu m$, $L_N = L_P = 1\mu m$, $\tau_{eff} = 1\mu s$ and a silicon nitride ARC of either $20nm$ targeted for deep-UV ($\lambda = 260 - 280nm$) or $60nm$ to minimize the reflections at $\lambda = 400nm$. The figure clearly shows higher responsivity at deep-UV wavelengths than for $\lambda = 400nm$, even with

the $60nm$ Si_3N_4 ARC due to the thinner Si film. Nevertheless, the ARC can greatly improve the $400nm$ responsivity but the benefit of an air cavity is not significant with a so small buried oxide. Indeed, to reflect light with higher wavelengths close to $400nm$, a thicker buried oxide (for thicker air cavity) would be needed as previously observed in figure 2.16-b). Moreover, the dark current is directly dependent on the thickness of the film. Then, a thin film thickness reduction by eight (compared to the UCL SOI technology) will also reduce the dark current by the same factor.

2.9 Conclusion

In conclusion, we demonstrated the potential of the SOI technology to implement high efficiency blue and UV photodetectors fully compatible with a standard CMOS process. Most of the work is based on the addition of anti-reflection coatings compatible with a CMOS process such as silicon nitride and aluminum oxide that show a real benefit in terms of responsivity. For $\lambda = 400nm$, the best responsivity achieved is $R = 0.1A/W$ in the current UCL SOI $2\mu m$ with a minimal SiO_2 thickness and a $48nm$ second ARC. We simulated the evolution of the responsivity with the intrinsic length and technological parameters of the process, such as effective lifetime and metal zone widths that can improve the responsivity up to $0.18A/W$ with anode and cathode length less than $1\mu m$ and $\tau_{eff} = 1\mu s$. Specific structures derived from a classical SOI photodiodes like silicon-on-nothing and membrane proved their ability to be excellent candidates for UV sensors in particular applications with a maximal responsivity of $0.27A/W$ for the SON one. The membrane structure is also interesting with high efficiency of $0.28A/W$ at $410nm$ for backside illumination.

A comparison to state-of-the-art photodiodes placed our photodiodes in excellent position : the high responsivities added to their low-cost of fabrication proved that the PIN SOI-based photodiodes are excellent blue-UV photodetectors. Moreover, the different parameters of the structure are easily adaptable to the various applications lying in the UV-blue range. A perspective of evolution for UTSOI technologies showed a very interesting behavior for deep-UV wavelengths, although thicker film

CHAPTER 2. OPTIMIZATION OF PIN PHOTODIODES IN SOI TECHNOLOGY

will still be interesting for blue applications.

References

- [1] J.A. Huberman, "Importance of measuring nucleic acid absorbance at 240 nm as well as at 260 and 280 nm", *BioTechniques*, Vol. 18, No. 1, pp. 62-63, January 1995.
- [2] J.A. Glasel, "Validity of nucleic acid purities monitored by 260nm/280nm absorbance ratios", *BioTechniques*, Vol. 18, No. 4, pp. 636, April 1995.
- [3] A.V. Tataurov, Y.You and R. Owczarzy, "Predicting ultraviolet spectrum of single stranded and double stranded deoxyribonucleic acids", *Biophysical Chemistry*, Vol. 133, No. 1-3, pp. 66-70, 2008.
- [4] <http://www.antonine-education.co.uk>, Available online.
- [5] G.C. Brainard et al., "Action spectrum for melatonin regulation in humans: evidence for a novel circadian photoreceptor", *Journal of Neuroscience*, Vol. 21, No. 16, pp. 6405-6412, 2001.
- [6] <http://sleep.med.harvard.edu/news/28>, Available online.
- [7] A. Sasseville and M. Hebert, "Using blue-green light at night and blue-blockers during the day to improves adaptation to night work: A pilot study", *Progress in neuro-psychopharmacology & biological psychiatry*, Vol. 34, No. 7, pp. 1236-1242, 2010.
- [8] A. Karczemska and A. Sokolowska, "Materials for DNA sequencing chip", *3rd International Conference on Novel Applications of Wide Bandgap Layers*, pp. 176, Zakopane, June 2001.
- [9] A. Afzalian, "Optical Detectors in SOI CMOS Technologies for Blue DVD and Short Distance Optical Communication", *PhD Thesis*, Université catholique de Louvain, pp. 29-62, 2006.
- [10] B. Kumar, T. Baskara Pandian, E. Sreekiran and S. Narayanan, "Benefit of dual layer silicon nitride anti-reflection coating", *Record of the Thirty-first IEEE Photovoltaic Specialists Conference/2005*, pp. 1205-1208, Bangalore, 2005.

- [11] M. Bawedin, "Transient Floating-Body Effects for Memory Applications in Fully-Depleted SOI MOSFETs", *PhD Thesis*, Université catholique de Louvain, 2007.
- [12] OKI semiconductor website : <http://www.okisemi.com/en/>
- [13] M. Bruel, B. Aspar and A.-J. Auberton-Herve, "Smart-cut : A new silicon on insulator material technology based on hydrogen implantation and wafer bonding", *Japanese journal of applied physics*, Vol. 36, No. 3B, pp. 1636-1641, 1997.
- [14] M. Jurczak, T. Skotnicki, M. Paoli, B. Tormen, J. Martins, J. Regolini, D. Dutartre, P. Ribot, D. Lenoble, R. Pantel, and S. Monfray, "Silicon-on-Nothing (SON) - an Innovative Process for Advanced CMOS", *IEEE Transactions on Electron Devices*, Vol. 47, No. 11, pp. 2179-2187, November 2000.
- [15] V. Kilchytska, M.T. Chung, B. Olbrechts, Ya. Vovk, J.-P. Raskin and D. Flandre, "Electrical characterization of true Silicon-On-Nothing MOSFETs fabricated by Si layer transfer over a pre-etched cavity", *Solid State Electronics*, Vol. 51, No. 9, pp. 1238-1244, 2007.
- [16] J. Laconte, "Micromachined Thin-Film Sensors for SOI-CMOS Co-integration", *PhD Thesis*, Université catholique de Louvain, 2004.
- [17] V. Torres-Costa, R. Martín-Palma, and J. Martínez-Druart, "All-silicon color-sensitive photodetectors in the visible", *Materials Science and Engineering : C*, Vol. 27, No. 5-8, pp. 954-956, September 2007.
- [18] Y. Chen and M. du Plessis, "An integrated 0.35 μm CMOS optical receiver with clock and data recovery circuit", *Microelectronics Journal*, Vol. 37, No. 9, pp. 985-992, September 2006.
- [19] H. Zimmermann and B. Muller, "Ultralow-capacitance lateral p-i-n photodiode in a thin c-Si film", *IEEE Transactions on Nuclear Science*, Vol. 49, No. 4, pp. 2032, August 2002.

- [20] A. Pauchard, A. Rochas, Z. Randjelovic, P.A. Besse and R.S. Popovic, "Ultraviolet Avalanche Photodiode in CMOS Technology", *International Electron Devices Meeting Technical Digest*, pp. 709-712, San Francisco, December 2000.
- [21] O. Bulteel, A. Afzalian and D. Flandre, "Fully integrated blue/UV SOI CMOS photosensor for biomedical and environmental applications", *Analog Integrated Circuits and Signal Processing*, Vol. 65, No. 3, pp. 399-405, Springer, 2010.
- [22] N. Miura, T. Chiba, H. Yamada and S. Baba, "Development of Silicon-on-Insulator (SOI) UV Sensor IC", *OKI Technical Review*, Vol. 74, Vol. 3, No. 221, pp. 38-39, October 2007.
- [23] S. Chang, Y. Fang, K. Hsu and T. Wei, "GaN UV MSM photodetector on porous β -SiC/(111)Si substrates", *Sensors and actuators. A, Physical*, Vol. 147, No. 1, pp. 1-5, September 2008.
- [24] S. Chang, T. Ko, Y. Su, Y. Chiou, C. Chang, S. Shei, J. Sheu, W. Lai, Y. Lin, W. Chen and C. Shen, "GaN-Based p-i-n Sensors With ITO Contacts", *IEEE Sensors Journal*, Vol. 6, No. 2, pp. 406-411, April 2006.
- [25] N. Biyikli, I. Kimukin, T. Tut, O. Aytur and E. Ozbay, "Fabrication and characterization of solar-blind $\text{Al}_{0.6}\text{Ga}_{0.4}\text{N}$ MSM photodetectors", *Electronics Letters*, Vol. 41, No. 5, pp. 274-275, March 2005.
- [26] E. Monroy, F. Calle, J. Pau, E. Muñoz, F. Omès, B. Beaumont, and P. Gibart, "AlGaN-based UV photodetectors", *Journal of crystal growth*, Vol. 230, No. 3-4, pp. 537-543, 2001.
- [27] D. Brown, E. Downey, J. Kretchmer, G. Michon, E. Shu, and D. Schneider, "SiC Flame Sensors for Gas Turbine Control Systems", *Solid-state electronics*, Vol. 42, No. 5, pp. 755-760, 1998.
- [28] Y. Fang, S. Hwang, K. Chen, C. Liu, M. Tsai, and L. Kuo, "An Amorphous SiC/Si Heterojunction p-i-n Diode for Low-Noise and High-Sensitivity UV Detector", *IEEE Transactions on Electron Devices*, Vol. 39, No. 2, pp. 292-296, February 1992.

- [29] K.-S. Han, H. Lee, D. Kim, and H. Lee, "Fabrication of anti-reflection structure on protective layer of solar cells by hot-embossing method", *Solar Energy Materials and Solar Cells*, Vol. 93, No. 8, pp. 1214-1217, August 2009.
- [30] A. Kumar and R.H. Dennard, "Carrier confinement in UTSOI Devices: Impact of metal gate work function", *IBM research report*, August 2005.

CHAPTER 3

INTEGRATED PHOTSENSORS

IN SOI TECHNOLOGY

3.1 *Introduction*

This chapter is about the design of an integrated circuit to process the photocurrent of UV-blue photosensors. As for the devices, the circuits are designed in SOI CMOS technology with the aim of co-integration. We firstly describe the context of utilization of such a system to establish the adequate type of the processing signal circuit. The circuit is then described and its major components, i.e. an operational amplifier and a Schmitt trigger are studied in more details. A design of the Miller amplifier is described for this photosensor and three Schmitt triggers are investigated and compared. Due to the small quantities to measure, a finer noise analysis is presented to ensure a minimal noise floor of the system. A realization of the photosensor is analyzed and its performances are discussed and compared to the state-of-the-art. Finally a global methodology is presented to design photosensors for biomedical and environmental applications.

3.2 *Context*

Optical power measurement in the low wavelengths close to blue and ultraviolet light finds many applications in the environmental and biomedical fields. In the environmental sector, one will mention the measurement of the ultraviolet rate of the sun light, the UV absorption of ozone or the turbidity of a liquid which is characterized by a factor of reflection of the ultraviolet rays onto the liquid [1]. This type of measurement system can also be used as a flame detector [2] e.g. in a car motor or to prevent a forest fire. In the biomedical field, applications concern for

example the absorption by bacteria in the low wavelengths or the quantification of the concentration of a solution of DNA. Such applications may require a precise, miniaturized and portable system. Basically, it consists of a photodiode and a read-out integrated circuit.

In the previous chapter, we saw that the responsivity reached by the bulk Si photodiode used in similar works was not accurate enough for those applications. The system we propose contains a photosensor which is better suited to the target applications implying the measurement of UV and blue light in the range of wavelengths from 200 to 480nm. It was shown that low thickness of silicon film around 100nm implies an optical responsivity increased around 400nm, which corresponds to our applications. Moreover, the same SOI technology allows for including a low-power/low-noise processing circuit on the same chip than this photodiode in order to obtain a complete integrated photosensor [3]. Depending on the signal to measure and the application, the photocurrent can be transduced into an analog or a digital signal.

3.2.1 Analog output

A common way to monitor the light intensity is to transform the photocurrent into a voltage. It allows real-time measurement and high speed applications, such as blu-ray data storage. In order to read the voltage signal, the current has to pass through an impedance. A transimpedance amplifier (TIA) may be a possibility as presented in figure 3.1.

This configuration enables high speed applications such as studied in [4]. The complete design of a photodetector using a multistage TIA in various CMOS technologies has been investigated by Afzalain in [5]. The performances reached in a 0.13 μm PD-SOI technology were a transimpedance gain of 623 Ω in dynamic range from 22.5 to 465 μA with a power consumption of 1.5mW for a 10GHz operating frequency. These characteristics proved that the SOI technology is an excellent candidate for analog high speed photoreceivers.

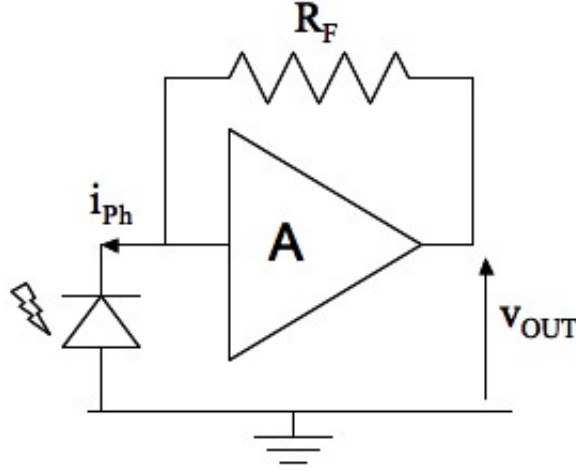


Figure 3.1: Transimpedance amplifier for high speed analog measurement.

3.2.2 Digital output

However, depending on the application, it is sometimes more convenient to manipulate a digital output, for example to be easily interfaceable with a microcontroller. One way to do it is to make follow the TIA by an analog-to-digital converter. However, this kind of solution is complex and should require a high power consumption. Nevertheless, for very high-speed applications, a TIA followed by a flash ADC can be an appropriate choice. Other analog-to-digital circuits were studied for biomedical applications in a conventional CMOS technology in [6] and [7]. The schematic of the architecture is showed in figure 3.2. If we assume that the optical illumination acts as a slow phenomenon, the photocurrent will be regarded as constant during one measurement time period of the circuit. This constant current will then be integrated by the capacitor C_F and the slope of the integrated voltage will be as large as the absolute value of the photocurrent. Then, the output voltage of the integrator is compared to a reference value V_{REF} , and the output of the comparator is connected to a monostable vibrator, the *One shot* block, which generates a rising edge that starts a phase of resetting of the integrator. By short circuiting the capacitor, the integrated voltage goes down abruptly until going below the reference voltage for which the output of the vibrator becomes null and the integrator can restart its integrating mode. It thus acts as a current to frequency converter. Indeed, for the

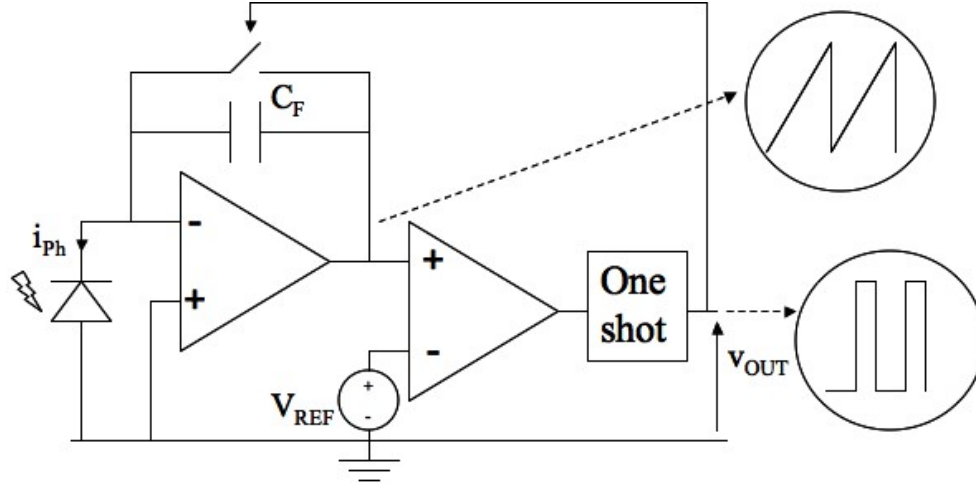


Figure 3.2: The current-to-frequency circuit and voltage waveforms at the various nodes.

same period of observation, the larger the photocurrent, the larger the number of the pulses generated at the output of the circuit. Other systems featuring a digital output based on the same principle for different application are related in the literature. For example : ion current measurement [8], distance measurement [9] or bioluminescence detection [10].

3.2.3 Figure of merit

In addition, knowing that the luminous signals to be measured could feature either weak levels (e.g. from luminescent labels) or higher levels (such as UV from the sun lightning), we propose a new figure of merit for comparison purposes : the optical dynamic (OD) of the measurable signal defined as :

$$OD = \frac{I_{Max}}{I_{Min}}, \quad (3.1)$$

where I_{Max} and I_{Min} are respectively the maximum and minimum photocurrents which the system is able to process. This definition is acceptable for a linear relationship between the light source power and the photocurrent: i.e a given phenomenon associated to a precise spectral emission or a single wavelength, as it is often the case in biomedical or environmental applications.

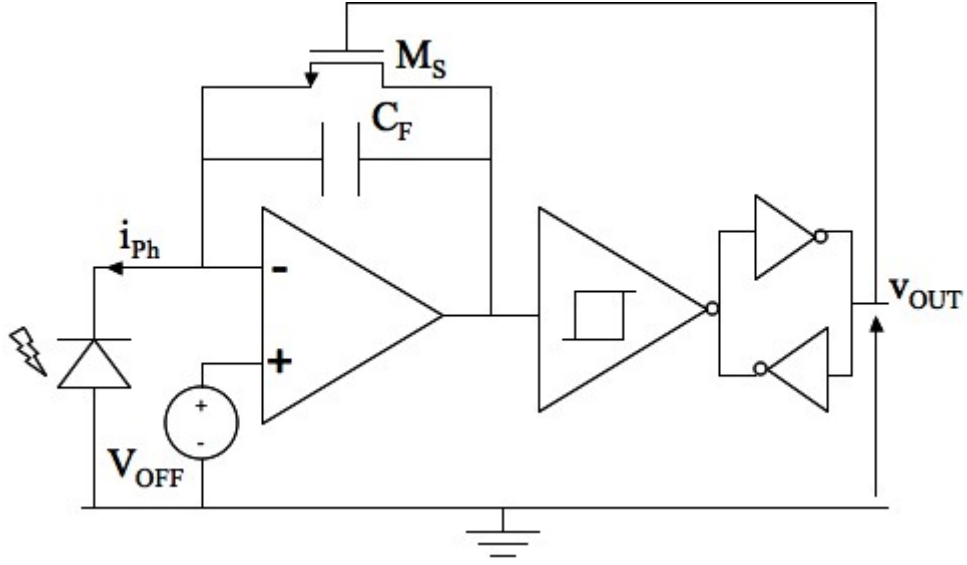


Figure 3.3: The photosensor implemented in this work.

Nevertheless, the minimal and maximal currents will be defined by several factors of the system such as the minimal detectable signal, noise considerations in the circuit, temperature drift of the sensor and the dark current that will be discussed in this chapter.

3.3 The System

The system we designed to interface the UV photodiodes presented in the previous chapter is mainly based on a current-to-frequency converter. The block diagram of the photosensor system we conceived is shown in figure 3.3. However, contrarily to the circuit in figure 3.2, we choose a two-thresholds comparator : the Schmitt trigger. As an inverting block, the trigger is followed by two cross-coupled inverters in order to start the reset phase of the integration when the digital value of the output is held at *One*. The latch also ensures a memorization of the output by preventing the switch from small oscillations of the trigger. This implies a stable state of the output and a faster swing of the trigger output since the second inverter also switches during each phase. The behavior is thus slightly different. When the output of the integrator reaches the high threshold level of the trigger, its output

becomes null and the output of the system is then high due to the cross-coupled inverters starting a reset phase of the integrator by closing the NMOS M_S . Then, the integrated signal abruptly goes down reaching the low threshold level of the trigger whose output becomes high. At this moment, the output of the system becomes null again and the integrator can restart to integrate the photocurrent until the next resetting signal.

3.3.1 Top design of the system

In this section, we design each part of the microsystem as a *black box* before a more specific transistor level design. The purpose of this global design is to determine the specifications for each part of the system. We mentioned the importance of miniaturizing the system for portability purpose. This would imply a battery cell as power supply for example. In this case, the total power consumption would be inferior to $1mW$.

The photodiode

The properties of the photodiode were simulated with the MATLAB software according to a formalism of reflection, transmission and absorption of electromagnetic waves between various layers with different indexes of refraction and thicknesses presented in the previous chapter (and described in details in the first appendix). The current to measure will depend on the optical phenomenon to measure, i.e. UV in sunlight will induce a far higher photocurrent than measuring fluorescence in biomedical process. The design of the photodiode implies also a tradeoff concerning its area.

A large sized photodiode will induce a higher photocurrent but also a greater noise since the noise generated by this photodiode is of shot type as described hereafter. Moreover, a large photodiode implies less place left for the processing signal circuit and a bigger internal capacitance to add to the input capacitance of the integrator. For example, the dark currents of the photodiode biased with a reverse

voltage of $V_D = -0.5V$ and an effective lifetime of $\tau_{eff} = 0.1\mu s$ are ranging from $15pA$ ($Li = 18\mu m$) to $65pA$ ($Li = 8\mu m$) for a photodiode with 0.25 and $1mm^2$ total area respectively. As for the photocurrent, measured values under deep-UV LED illumination (for which the irradiance has been measured to be about $2.5W/m^2$ in the emission range from 260 to $280nm$) reach maximal values around $100nA$. We then fixed the upper limit to $1\mu A$ in case of unexpected higher irradiances.

The integrator

Based on the typical measurements of photodiodes, we considered a maximum photocurrent of $1\mu A$ and a minimal dark current of $100pA$ which is the worst case for our SOI photodiodes of the size mentioned in the previous section. Considering an output swing of $1V$ under a supply voltage of $\pm 1V$, we then made the choice of a feedback capacity for the integrator having a value of $C_F = 10pF$. In this case, after one second of observation, we may count 10^5 pulses for a photocurrent of $1\mu A$ and only 10 pulses for a dark current of $100pA$.

Taking a first order approximation for the transfer function of the operational amplifier in the Laplace domain:

$$G(s) = \frac{A_{v,0}}{1 + \frac{s}{s_0}} \quad , \quad (3.2)$$

where $A_{v,0}$ is the open-loop gain and s_0 the cut-off frequency of the amplifier, the transfer function of the integrator becomes :

$$H(s) = \frac{V(s)}{I_{Ph}} = \frac{1}{s \cdot C_F} \cdot \left(\frac{A_{v,0}}{1 + A_{v,0} + \frac{s}{s_0}} \right). \quad (3.3)$$

It can be seen that to ensure a sufficiently-good integrating function, the operational amplifier has to feature a minimal open-loop gain voltage of $60dB$ for an error of 0.1% at the edge of its bandwidth. We also propose a minimum bandwidth of $f_0 \geq 3 \cdot \frac{f_m}{A_0}$ where f_m is the maximal output frequency of the signal. In this example, in order to measure a maximum number of 10^5 pulses per second, i.e. $f_m = 100kHz$,

the bandwidth of the amplifier is fixed to a minimal value of $300Hz$ (for a minimal transition frequency of $f_T = 300kHz$).

The trigger

The thresholds of the trigger are designed according to the dynamic range V_{DR} at the output of the amplifier. Supposing a common supply voltage $V_{DD} - V_{SS}$ for the system, the threshold values are :

$$V_{TH,trigg} = \pm \frac{V_{DD} - V_{SS} - V_{DR}}{2}, \quad (3.4)$$

when their value is defined relatively to the supply voltage and if we assume that the output swing is symmetrically positioned between the supply voltages. In the current example, to have a dynamic range at the output of the operational amplifier of $1V$ knowing that the circuit is powered at $\pm 1V$, the thresholds have an absolute value of $0.5V$. However, the way to fix those levels depends on the implementation of the trigger as it will be seen further.

The switch

The switch transistor, M_S , has to be designed carefully to some criteria:

- it has to feature the lowest *on* impedance when discharging the capacitor, or at least the appropriate one according to the fall time requirements at the output of the circuit.
- contrarily, it has to feature the highest *off* impedance during the integrating period which is linked to a minimal leakage current in *off* mode in order to reduce the error on the integrated current.

In SOI technology, a single NMOS transistor is sufficient to fill up the previous conditions [11]. For example, a NMOS can thus be chosen and sized with a ratio $\frac{W}{L} = 1$ and a minimal length of the technology to assume a minimal leakage current

less than $10fA$ when off in a $2\mu m$ node. In this case, its equivalent ON resistance is

$$R_{SW,ON} = \frac{2.5}{\mu_n C_{OX} \frac{W}{L} \cdot (v_{GS} - V_{Tn})} \quad (3.5)$$

for a transistor passing from saturated region to triode during the discharge of the capacitance [12].

3.4 The Operational Amplifier

It has been previously showed that an operational amplifier featuring a high open-loop gain with a relatively small bandwidth, less than $1kHz$, was suitable for biomedical and environmental applications, where small intensities (i.e. small photocurrents) with long time constants of variations have to be quantified. These requirements, when adding a micropower consumption for the portability of the system, fit very well with the Miller operational amplifier characteristics for example whose architecture implemented in CMOS technology is presented in figure 3.4.

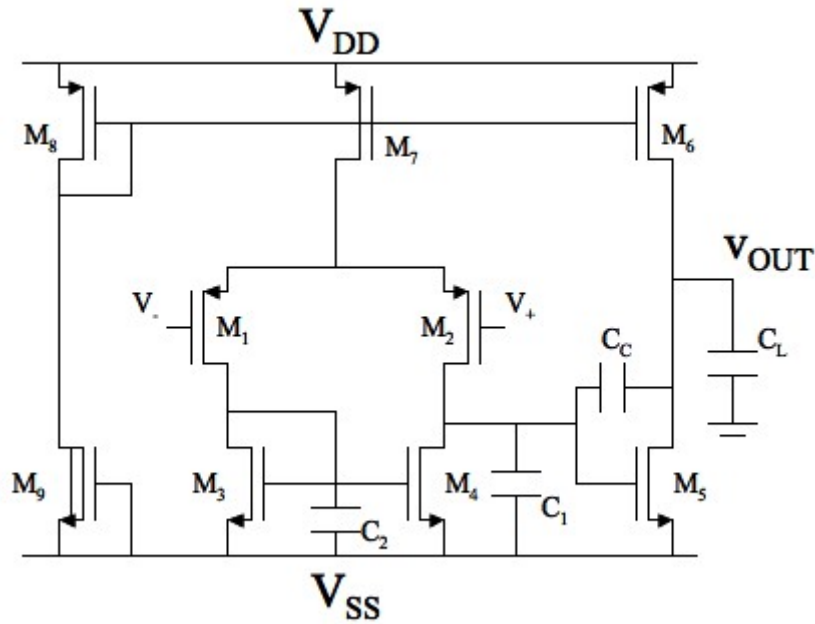


Figure 3.4: Architecture of the Miller operational amplifier in CMOS technology.

3.4.1 Analysis

Inspecting in more details figure 3.4, the Miller compensation is ensured by the external Miller capacitance C_C . C_L is the total output capacitance, consisting in the feedback capacitance of the integrator, the drain-bulk capacitances of $M_5 - M_6$ and the input capacitance of the Schmitt trigger. C_1 and C_2 are the internal parasitic capacitances due to transistors at the concerned nodes. The differential pair input in a PMOS type ensuring a lower noise as demonstrated later. Finally the bias currents in each branch are imposed by a robust implementation of a current source : an intrinsic NIN SOI transistor (M_9). Featuring a low channel doping, it acts like a depletion transistor providing a constant current at zero temperature compensation (ZTC) when short-circuiting the gate and source accesses. For harsh environment measurements, i.e. high temperature, a more complex implementation has been studied in the same technology [13].

The amplifier can be designed according to the $\frac{g_m}{I_D}$ method [14]. The open-loop gain in the bandwidth $A_{v,0}$ and the dominant pole ω_0 (or the gain-bandwidth product, ω_T) can then be expressed by :

$$A_{v,0} = \left(\frac{g_m}{I_D} \right)_2 \cdot \left(\frac{g_m}{I_D} \right)_5 \cdot V_{EA2,4} \cdot V_{EA5,6} \quad (3.6)$$

and

$$\omega_0 = -\frac{I_{D2}}{C_c \cdot \left(\frac{g_m}{I_D} \right)_5 \cdot V_{EA2,4} \cdot V_{EA5,6}} \Leftrightarrow \omega_T = \frac{g_{m2}}{C_c}, \quad (3.7)$$

where $V_{EA2,4}$ and $V_{EA5,6}$ are the equivalent Early voltages of parallel output impedances of the transistors M_2 and M_4 and equivalently for the transistors M_5 and M_6 [15].

The Miller capacitance C_c also implies a right-half plane zero :

$$\omega_{Z,RHP} = \frac{g_{m5}}{C_c}, \quad (3.8)$$

and a non-dominant pole :

$$\omega_{PND} = -\frac{g_{m5} \cdot C_c}{C_c(C_1 + C_L) + C_1 C_L} . \quad (3.9)$$

Moreover a pole-zero doublet is created due to the mirror $M_3 - M_4$ in the differential pair :

$$\omega_{P,PZD} = -\frac{g_{m3}}{C_2} \text{ and } \omega_{Z,PZD} = -\frac{2 \cdot g_{m3}}{C_2} . \quad (3.10)$$

3.4.2 Design

The operational amplifier was sized with the $\frac{g_m}{I_D}$ methodology assuming that A_{v0} , ω_0 (or the GBW) and the slew-rate (SR) are the requirements that satisfy a sufficient phase margin of 60° for insuring unconditional stability in the loop. Indeed in the present case, the maximal number of pulse to be measured, i.e. the maximal photocurrent fixes thereby the bandwidth of the amplifier, while the precision needed to get the most ideal integration function fixes the open-loop gain.

For the values that are mentioned at the system design level, we need a minimal $60dB$ open-loop gain at $300Hz$ which implies a $300kHz$ gain-bandwidth product. The parameters $\frac{g_m}{I_D}$ of the transistors $M_{1,2}$ were fixed at $20V^{-1}$ to keep these transistors in moderate inversion, reduce their noise, and achieve high gain with low power consumption. The slew rate fixes a $10\mu A$ current in the output branch in order to ensure a reset time ten times smaller than the integration time in the worst case (i.e. a photocurrent of $1\mu A$). For stability issues, we imposed a non-dominant pole ω_{PND} five times higher than ω_T and the right-half plane zero $\omega_{Z,RHP}$ ten times higher than ω_T . We imposed by the same occasion identical $\frac{g_m}{I_D}$ values for the transistors of the mirror $M_{3,4}$ and for the transistor M_5 to cancel the systematic offset. Then, if we increase the $\frac{g_m}{I_D}$ values of these transistors, their sizes will increase for the same specifications and the Miller capacitor C_c must be increased to guarantee a sufficient phase margin, which leads to an increase of the power consumption. The other sizes were chosen to ensure the lowest power consumption but guaranteeing a sufficient phase margin. Concerning the bias transistors : M_6 has to be sized to obtain a

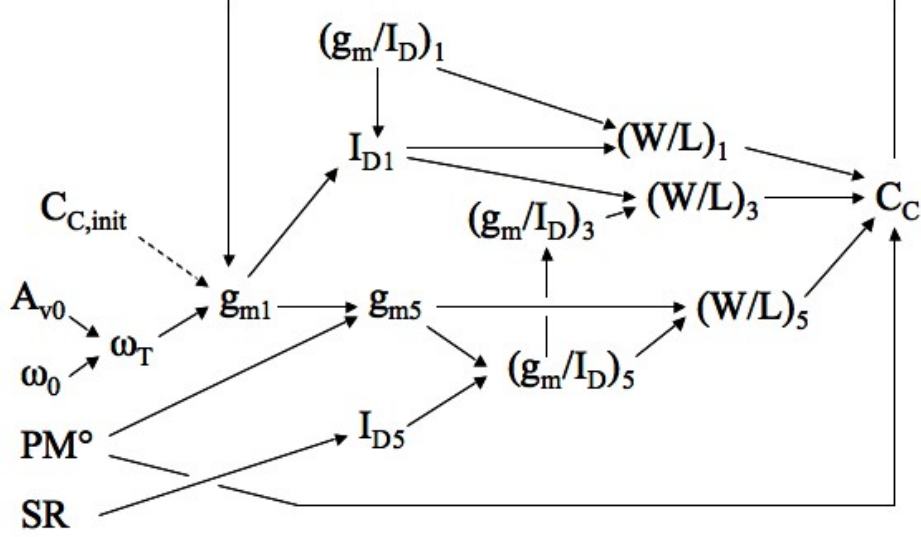


Figure 3.5: $\frac{g_m}{I_D}$ design flow for the Miller operational amplifier.

minimal 1V output swing and M_7/M_8 are sized to ensure an adequate ratio current $\frac{2 \cdot I_{D,1}}{I_{D,5}}$ with M_6 . The design flow schematic according to the $\frac{g_m}{I_D}$ methodology for the present specifications is shown in figure 3.5.

A Matlab methodology of design enabled us to calculate the sizes and biases of each transistor and the amplifier was simulated at SPICE level using the Eldo simulator and a C_∞ -continuous model for FD SOI MOSFETs [16, 17]. The comparison of Bode diagrams of the amplifier is showed in figure 3.6 for SPICE and Matlab models for both magnitude and phase. According to both simulations, the operational amplifier reaches a 86.8dB DC gain and gain-bandwidth product of 298kHz in the SPICE simulation with a load capacitance of 10pF, dominated by the feedback capacitance of the integrator. The reason of the slight differences between the curves can be explained because Matlab does not take into account the additional parasitic capacitances of the transistors. The amplifier consumes a total current of 12.5μA which, with the voltage supply of 2V, implies a static power consumption of 25μW. It also features a 64° phase margin for a Miller capacitor of $C_C = 4pF$. The sizes of the transistors are listed in table 3.1 and the performances of the amplifier are detailed in table 3.2. In addition to the tables, the lengths of transistors $M_3 - M_4$ were fixed to 40μm which implies for the pole-zero doublet $\omega_{P,PZD} = 928kHz$ and

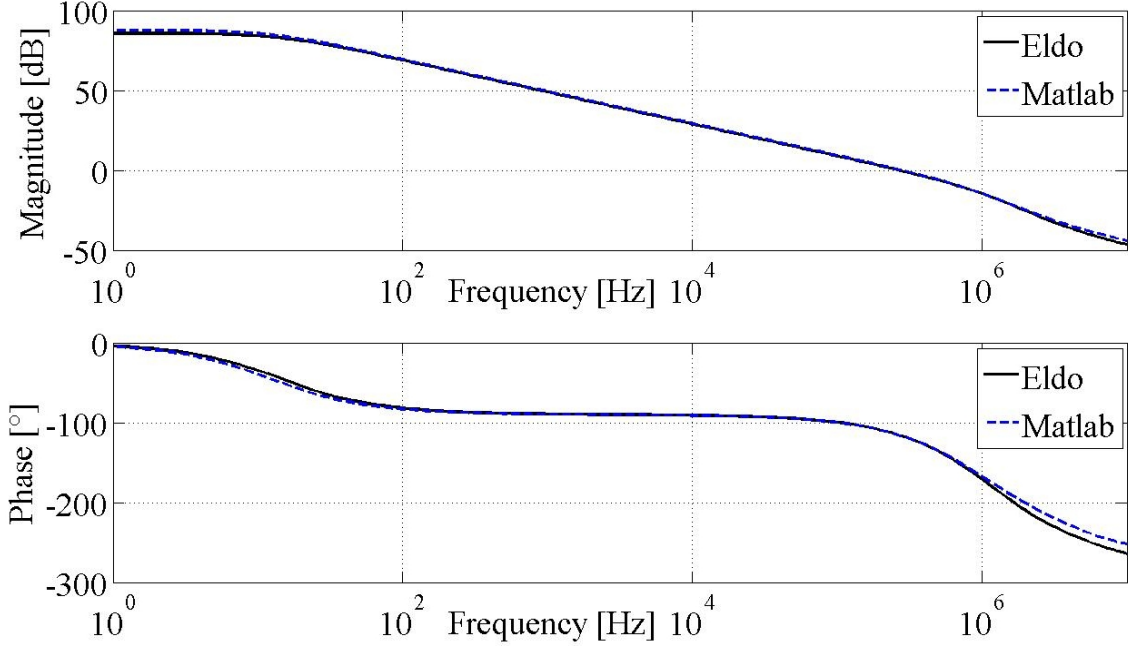


Figure 3.6: SPICE (continuous line) and Matlab (dashed line) simulations of the bode diagram of the Miller operational amplifier.

$\omega_{Z,PZD} = 1.856 MHz$, avoiding stability issues since far beyond the transition frequency. More discussion on the sizes of the mirror transistors is provided in the noise analysis section.

Transistor	$M_{1,2}$	$M_{3,4}$	M_5	M_6	$M_{7,8}$	$M_9(NIN)$
W [μm]	18	8	10.5	10.5	4	5
L [μm]	4	40	2	2	10	10

Table 3.1: Sizes of the transistors for the low-power Miller operational amplifier.

Performances	P_{OW}	$A_{v,0}$	f_T	PM
Values	$25\mu W$	$86.8dB$	$298kHz$	64°
Performances	SR	$CMRR$	$PSRR_{DD}$	$PSRR_{SS}$
Values	$10^6 V/s$	$-106.3dB$	$-96.3dB$	$-91.8dB$

Table 3.2: Performances of the low-power Miller operational amplifier.

Our choice of a PMOS differential input with large sized NMOS transistors of the current mirror is justified to guarantee a low noise amplifier at low operating frequencies as it will be discussed in the noise analysis hereafter. Simulations showed a higher phase margin if a RC-Miller compensation would have been used instead

of the classical architecture of figure 3.4. Indeed, to reach the same $A_{v,0}$, ω_T and slew rate, a $25\mu W$ RC-compensated Miller implementation with phase margin of 71° has been simulated in SPICE. The sizes of the transistors are as given in table 3.1 and the amplifier also features a $C_C = 4.1pF$ capacitance and a $R_C = 45k\Omega$ nulling resistance.

As mentioned earlier, the $\frac{g_m}{I_D}$ parameters of transistors $M_{3,4}$ and M_5 are equal to cancel the systematic offset of the amplifier. However, we can calculate an offset implied by process variations. More precisely, considering a mismatch of the input transistors of the differential pair, we can express a variation of the output DC voltage by:

$$\Delta V_{OUT} = \frac{I_{D5} \cdot V_{DD} + \Delta I_{OUT} \cdot V_{EA5,6}}{2 \cdot I_{D5} + \Delta I_{OUT}} - V_{OUT,0}, \quad (3.11)$$

where $V_{OUT,0}$ is the DC value of the output voltage when no process variation is supposed. ΔI_{OUT} is the parasitic variation of output current implied by the process variations and is given by :

$$\Delta I_{OUT} = \frac{g_{m5}}{g_{m4}} \left(\frac{I_{D1}}{\beta} \cdot \sigma_\beta + g_{m1} \cdot \sigma_{V_T} \right). \quad (3.12)$$

In equation 3.12, we can define the process variation parameters by :

$$\frac{\sigma_\beta^2}{\beta^2} = \frac{A_\beta^2}{W_1 \cdot L_1} \text{ and } \sigma_{V_T}^2 = \frac{A_{V_T}^2}{W_1 \cdot L_1}, \quad (3.13)$$

where the parameters are respectively evaluated at $A_{V_T} = 13 \times 10^{-3} mV \cdot \mu m$ and $A_\beta = 0.05\% \cdot \mu m$ in UCL FD SOI technology [18]. The variation process offset is then of $\Delta V_{OUT} = 35mV$ in this case.

3.5 The Schmitt Trigger

As mentioned above, the block comparator is a Schmitt trigger which we have implemented in a CMOS technology. Its architecture is shown in figure 3.7.

The first stage ($M1$ to $M4$) behaves like a pseudo traditional CMOS inverter

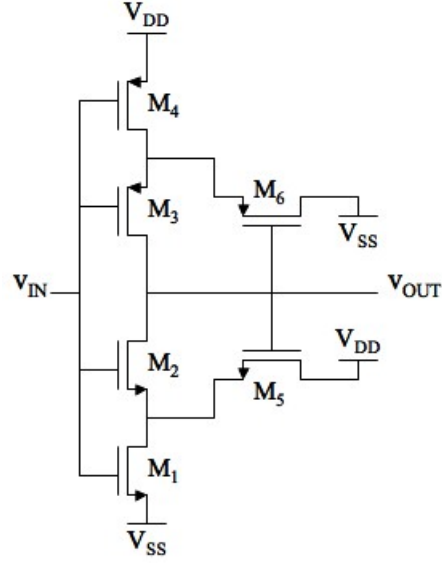


Figure 3.7: Classical CMOS architecture of the Schmitt trigger.

where two additional transistors ($M5$ and $M6$) are used to saturate the transistors $M1$ and $M4$ more quickly for a faster swing due to a positive loop reaction as they act as source followers. It can be useful in case of high photocurrents, when the slope of the integrated signal is high. The latch (constituted with two simple CMOS inverters) is finally placed at the output of the trigger to retain the state and stabilize the first stage of the output as indicated in figure 3.3. In comparison, when a single threshold comparator is used as in [6] and [7], we could note that the integrated signal might oscillate too fast around this comparison threshold without letting time for transistor M_S to reset the integrator. Our simulations further showed that the use of a trigger and two comparison thresholds made it possible for our circuit to obtain an optimal operation. Thanks to the hysteresis, any noisy effect should be larger than the threshold difference to cause an error transition of the output. Moreover, this Schmitt trigger features a high input impedance, a good robustness against noise and allows the threshold levels to be symmetrical with respect to $\frac{V_{DD}-V_{SS}}{2}$.

3.5.1 Design

CMOS Schmitt trigger

According to [19] and assuming the strong inversion and a body factor of $n \simeq 1$ as in our FD SOI CMOS process [3], the transconductance ratio during the transition phase yields the following sizes for the transistors :

$$\left(\frac{W}{L}\right)_1 = \left(\frac{V_{DD} - V_{HT}}{V_{HT} - V_{SS} - V_{Tn}}\right)^2 \quad \text{and} \quad \left(\frac{W}{L}\right)_4 = \left(\frac{V_{LT} - V_{SS}}{V_{DD} - V_{LT} - |V_{Tp}|}\right)^2 \quad (3.14)$$

where V_{HT} and V_{LT} are respectively the high and low threshold levels of the trigger. V_{Tn} and V_{Tp} are the threshold voltages of the NMOS and PMOS transistors. The main disadvantage of this structure is its relative high power consumption. Indeed, during the rising phase of the integrated signal, the output voltage node is high and the power current consumption is mainly due to the transistor M_1 which is first saturated until M_2 turns on for which the output node then falls down. The current is then dominated by M_1 .

However, another important factor is the switching time of the trigger, determined by its slew rate at the switching node. It is thus defined as the ratio of the maximal current during the switching phase by the total capacitance at the switching node. In this case, the capacitance at the switching node is composed of the input capacitance of the latch following the trigger (i.e. two gate-source capacitances and two drain-bulk capacitances of the inverters), of the gate-source capacitances of transistors M_5 and M_6 and of the drain-bulk capacitances of the transistors M_2 and M_3 .

Other implementations

Although the most common Schmitt trigger implementation fills up the requirements of the system, the Schmitt trigger can be implemented by other architectures. First of all, an operational amplifier based-structure is commonly used to realize monostable vibrators, and can be designed as a ratio of resistances according

to the desired thresholds. The disadvantages are the realization of the resistances in a standard CMOS process and the need of another operational amplifier which implies a static consumption while an inverter based solution has not. With matters of power consumption and miniaturization, this choice is not considered as convenient for biomedical or low-power processing signals. Nevertheless, two slight modifications of the standard CMOS inverter-based implementation of the Schmitt trigger presented in figure 3.7 are mentioned in the literature.

First, a low-power modification of the classical CMOS trigger was investigated in [20]. The architecture is presented in figure 3.8. As for the classical trigger, the architecture is complementary as a matter of transistors arrangement. If v_{IN} is low, M_2 is cut off while M_3 is ON and thus inversely for M_5 and M_6 respectively. This situation forces the output to be low and the transistors M_4 and M_1 to be ON and OFF respectively. But as the input voltage rises, the first inverter will switch on for a high voltage value, V_{HT} , since both M_1 and M_2 are cut off. From this moment, the second M_5/M_6 inverter also switches and v_{OUT} goes high which then turns on M_1 and cut off M_4 . A similar behavior is then observed for the low threshold, V_{LT} , of the trigger. The equations allowing the design of the transistors are as follow [20]:

$$V_{HT} = V_{DD} \cdot \frac{R_P \cdot (R + 1)}{R_P \cdot (R + 1) + 1} - |V_{Tp}| \cdot \frac{R_P \cdot (2R - 1) - 1}{R_P \cdot (R + 1) + 1} \quad (3.15)$$

and

$$V_{LT} = V_{DD} \cdot \frac{R_N + 1}{R_N \cdot (R + 1) + 1} + V_{Tn} \cdot \frac{R_N \cdot (2R - 1) - 1}{R_N \cdot (R + 1) + 1}, \quad (3.16)$$

where the size ratios coefficients are given by

$$R = \sqrt{\left(\frac{\mu_n \left(\frac{W}{L}\right)_2}{\mu_p \left(\frac{W}{L}\right)_3}\right)}, \quad R_N = \sqrt{\left(\frac{\left(\frac{W}{L}\right)_1}{\left(\frac{W}{L}\right)_2}\right)} \quad \text{and} \quad R_P = \sqrt{\left(\frac{\left(\frac{W}{L}\right)_4}{\left(\frac{W}{L}\right)_3}\right)}. \quad (3.17)$$

Its main disadvantage is the reduction of the output dynamic due to the transistors M_1 and M_4 . It requires the addition of two series CMOS inverters for keeping the same output voltages values of the pulses as the supply voltage of the circuit. This

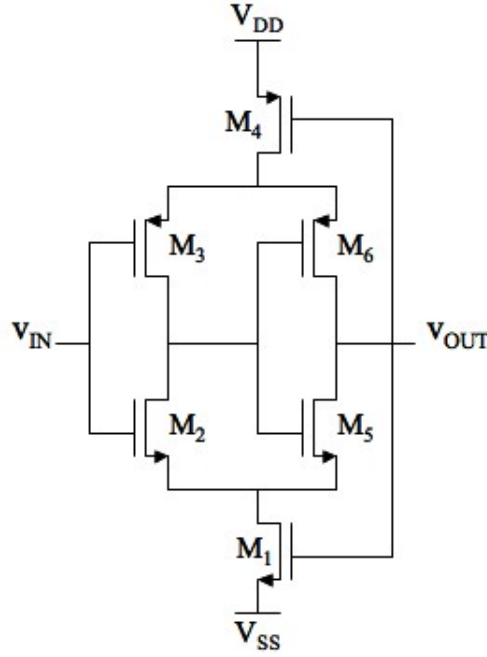


Figure 3.8: Low-power architecture of the Schmitt trigger.

would ensure the expected behavior of the switch and avoid a parasitic delay. Nevertheless, this Schmitt trigger presents the advantage of a lower power consumption compared to the classical CMOS trigger. Indeed, in this case, the current is dominated by the transistor M_2 during the rising phase, and its V_{GS} and V_{DS} voltages are reduced compared to the classical trigger due to the transistor M_1 . The capacitance at the switching node is composed of the gate-source capacitances of the inverter M_1 - M_4 and the drain-bulk capacitances of M_5 and M_6 to which we need to add the input capacitance of the next inverter ($2 \cdot C_{gs}$).

Secondly, a new CMOS Schmitt trigger is showed in figure 3.9 and was studied in [21]. In some applications, it is important to control the voltage range of the hysteresis with high precision. In the present implementation of the Schmitt trigger, it is exactly the role of transistor M_3 which always guarantees the hysteresis. Contrarily to the two previous architectures, this trigger is not fully symmetrical with regards to the supply voltages. As v_{IN} is low, the intermediary node, v_X , is high and the output is low which cuts off M_3 . As the input increases the first inverter will switch with a V_{HT} threshold voltage only defined by transistors M_1 and M_2 .

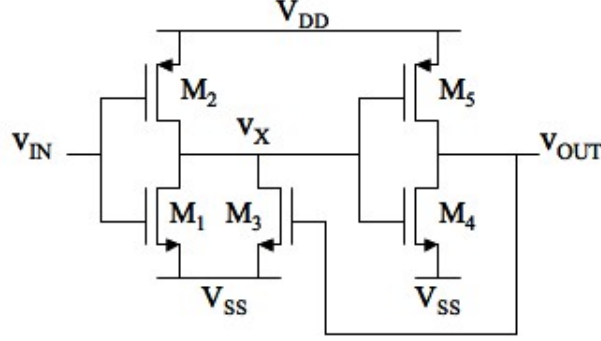


Figure 3.9: Guaranteed hysteresis CMOS architecture of the Schmitt trigger.

But then, the second inverter has also switched and forced M_3 to be ON. It thus decreases still more the output voltage of the first inverter. This positive feedback ensures the stable state of the output node. Contrarily, when v_{IN} is high, v_X is low and M_3 is ON and acts like a current source. So, to switch the first inverter, the second switching voltage has to be inferior to V_{HT} to compensate the extra current created by M_3 . This last case implies a lower threshold voltage, V_{LT} , which is thus dependent on the sizes of M_1 , M_2 and M_3 . Then, the thresholds are defined as [21]:

$$V_{HT} = \frac{V_{Tn} + (V_{DD} - V_{Tp}) \cdot X}{1 + X} \quad \text{and} \quad V_{LT} = V_{HT} - \frac{(V_{DD} - V_{Tn}) \cdot Y}{2(1 + Y)}, \quad (3.18)$$

where the ratios are defined by

$$X = \sqrt{\left(\frac{\mu_p \left(\frac{W}{L} \right)_2}{\mu_n \left(\frac{W}{L} \right)_1} \right)} \quad \text{and} \quad Y = \sqrt{\left(\frac{\mu_n \left(\frac{W}{L} \right)_3}{\mu_p \left(\frac{W}{L} \right)_2} \right)}. \quad (3.19)$$

This trigger ensures a low-power consumption in addition to its high precision, and the inverter composed of transistors M_4 and M_5 prevents from an additional latch. The power is here dominated by transistor M_1 and for this last implementation, the capacitance at the switching node is composed of the input capacitance of the inverter M_4 - M_5 and the gate-bulk capacitances of M_1 , M_2 and M_3 .

3.5.2 Comparison

Each Schmitt trigger was designed in the UCL FD SOI CMOS technology, and their behavior was simulated when connected to the system consisting of the integrator and the switch designed as previously detailed. The transistors dimensions were chosen to ensure a $1V$ dynamic range between the thresholds under a $\pm 1V$ power supply. We set the input swing at $1V$ symmetrical to the middle of the power supply i.e. $0V$. Thus, $V_{HT} = +0.5V$ and $V_{LT} = -0.5V$ for our example.

The triggers were compared according to their power consumption P_{Trigg} , the switching time ST , the precision of the trigger and its transistors surface, S . For a $1nA$ photocurrent, the number of pulses to be measured at the output of the ideal circuit has to be of 100 for a 1 second measurement time. A different amount of pulses compared to the 100 expected indicates the precision of the trigger while the power consumption is calculated as the average power supplied during one period of measurement. Table 3.3 resumes those results as obtained by SPICE simulations.

Trigger	$P_{Trigg}[\mu W]$	$ST[ns]$	Precision	$S [\mu m^2]$
Classical CMOS (fig. 3.7)	30	2	99%	342
Low-power (fig. 3.8)	18	20	92%	980
Low-power and Hysteresis (fig. 3.9)	2	52	99%	352

Table 3.3: Performances of the three Schmitt triggers as described by SPICE simulations.

As indicated in the table, the Schmitt trigger ensuring a low-power and a guaranteed hysteresis is the most convenient for this applications. The classical CMOS trigger reaches the same performances in terms of surface and precision but suffers from higher power consumption while the low-power improvement of the classical CMOS trigger suffers from precision and large area although it is a weak power consumer. Logically, the benefit of a low power consumption imply a higher switching time due to the slew rate, but compared to the period of $0.01s$ per pulse, the highest switching time of $52ns$ remains totally acceptable.

3.5.3 *Temperature variation*

It is known that in fully depleted SOI technology, the variation of the threshold voltage of a transistor MOS is of $1mV/K$. If one considers a rise of temperature of $100K$, the threshold voltage of each transistor decreases by $100mV$ in absolute value. The consequence is an increase of the input swing of the Schmitt trigger which varies according to the three structures : $60mV$ for the first classical trigger (fig. 3.7), $200mV$ for the second one (fig. 3.8) and $120mV$ for the third one (fig. 3.9). As the desired initial integrated signal dynamic was of $1V$, the rise of $100K$ increases the dynamic range by 6%, 20% and 12% respectively. One can then suppose that for one constant period of observation of the output of the circuit, the pulse repetition frequency will be decreased by the same percentage for each implementation because these pulses will be less quickly generated if the dynamic range of the two comparison thresholds has increased. A solution for this problem is to control the trigger in temperature or to introduce a temperature sensor featuring an adaptation of the period of measurement according to the temperature.

As an other solution, the integrated circuit could be periodically recalibrated using a current source constant with temperature in place of the photocurrent. Such SOI current sources with low drift in a large temperature range have been proposed in [13].

3.6 *Noise Considerations*

The noise analysis is a crucial point of consideration during the design of a low-power microsystem designed to measure small electrical signals. Particularly in the considered system, the noise sources in the circuit can induce a stochastic signal at the output of the integrator. This undesired perturbation can induce an error on the input swing of the Schmitt trigger, and thus a global error at the output of the circuit. Each source is presented as a function of the frequency and must hence be integrated along the desired frequency range.

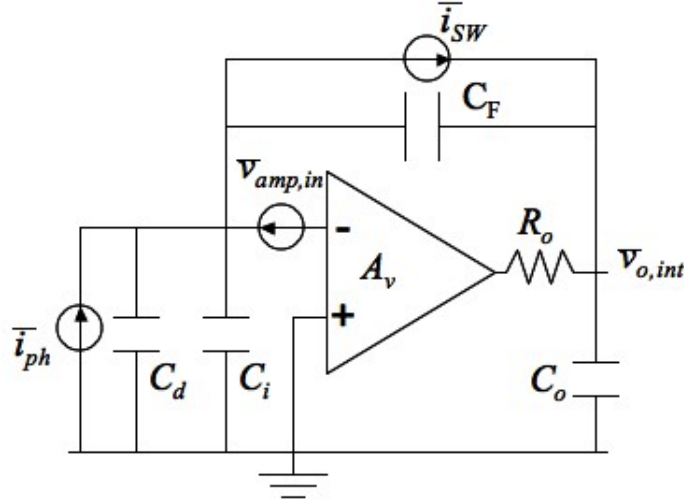


Figure 3.10: Noise sources influencing the trigger swing.

3.6.1 Noise modeling

The noise sources are presented in figure 3.10. They include, the noise current sources of the photodiode and the switch and the voltage source at the input of the operational amplifier.

Noise of the photodiode

As introduced previously, the noise generated by the photodiode is a shot noise type. Its power spectral density of current noise is given by :

$$\bar{i}_{ph,n}^2 = 2 \cdot q \cdot I_D [A^2/Hz]. \quad (3.20)$$

This noise is directly dependent on the photocurrent and must be multiplied by the transfer function of the integrator in order to evaluate its contribution to the voltage at the output of the integrator.

Noise of the amplifier

The noise induced by the behavior of the transistors in the operational amplifier can be modeled by an equivalent voltage noise source at the input of the integrator $v_{amp,in}$. The equivalent power spectral density of voltage noise at the input of the

amplifier is given by :

$$\bar{v}_{amp,in}^2 = \frac{1}{A_v^2} \bar{v}_{amp,out}^2, \quad (3.21)$$

where $\bar{v}_{amp,out}^2$ is the power spectral density of voltage noise at the output of the operational amplifier in open-loop :

$$\begin{aligned} \bar{v}_{amp,out}^2 = & \left(\frac{g_{m2} \cdot g_{m5}}{(g_{d2} + g_{d4})(g_{d5} + g_{d6})} \right)^2 (\bar{v}_{1,n}^2 + \bar{v}_{2,n}^2) \\ & + \left(\frac{g_{m4} \cdot g_{m5}}{(g_{d2} + g_{d4})(g_{d5} + g_{d6})} \right)^2 (\bar{v}_{3,n}^2 + \bar{v}_{4,n}^2) \\ & + \left(\frac{g_{m5}}{g_{d5} + g_{d6}} \right)^2 \bar{v}_{5,n}^2 \\ & + \left(\frac{g_{m6}}{g_{d5} + g_{d6}} \right)^2 (\bar{v}_{6,n}^2 + \bar{v}_{7,n}^2 + \bar{v}_{8,n}^2), \end{aligned} \quad (3.22)$$

and A_v is the open-loop transfer function of the amplifier. This definition is acceptable assuming that the non dominant poles and zeros are beyond the transition frequency, which is the case here. $\bar{v}_{amp,in}^2$ depends thus on the internal small-signal characteristics of the amplifier and of the equivalent power spectral density of voltage noise generated by each transistor, $\bar{v}_{i,n}^2$, defined by :

$$\bar{v}_{MOS,n}^2 = \frac{K}{W \cdot L \cdot C_{OX}^2 \cdot f} + 4kT \frac{\epsilon}{g_m} [V^2/Hz], \quad (3.23)$$

where $\epsilon = 2/3$ and $\epsilon = 1/2$ in strong and weak inversion respectively [22]. Since operating at low frequency, we only consider the thermal and flicker noises in the channel, where the flicker dominates. In UCL SOI technology, the K parameters in equation 3.23 are $K_n = 7.5 \times 10^{-27} V^2 F$ and $K_p = 5 \times 10^{-28} V^2 F$ for N and P type transistors respectively. The choice of a P-type differential pair input is then justified to minimize the flicker noise at the input of the amplifier as it is showed by equations 3.21, 3.22 and 3.23. Indeed, the flicker noise coefficients are much smaller for P-channel MOSFETs but transistors $M_3 - M_4$ have to be sized according to minimize their contribution (see table 3.1) and hence reduce the excess of noise from the mirror.

Noise of the switch

According to its mode, the noise of the switch is modeled by a power spectral density of current noise $\bar{i}_{SW}^2$. When cut off, the switch can be considered as a current source whose value is the leakage current as discussed before [23], and then :

$$\bar{i}_{SW,OFF}^2 = 2 \cdot q \cdot I_{OFF} [A^2/Hz]. \quad (3.24)$$

While when discharging the feedback capacitance, the switch can be modeled by the equivalent resistance defined by equation 3.5 and the associated source noise is the thermal power spectral density of current noise source :

$$\bar{i}_{SW,ON}^2 = \frac{4kT}{R_{SW,ON}} [A^2/Hz]. \quad (3.25)$$

3.6.2 Effect on the trigger thresholds

When the integrated voltage is rising up, the switch is cut off and its resulting noise due to the leakage current can be neglected with regards to the shot noise of the photodiode. Contrarily, during the reset phase, the current flowing through the feedback capacitance is dominated by the drain current of the switch as well as for the noise. The noise voltage density at the input of the trigger is thus :

$$\bar{v}_{trig,in}^2 = \bar{v}_{int,o}^2 = \bar{v}_{amp,in}^2 \cdot \left(\frac{v_{out}}{v_-} \right)_{int}^2 + (\bar{i}_{ph}^2 + \bar{i}_{SW}^2) \cdot \left(\frac{v_{out}}{i_{in}} \right)_{int}^2, \quad (3.26)$$

where

$$\left(\frac{v_{out}}{v_-} \right)_{int} = \left(\frac{A_v C_F + C_i (s C_F R_o - A_v)}{(1 + A_v + s R_o C_o) C_F - (C_d + C_i) (A_v - s C_F R_o)} \right) \quad (3.27)$$

and

$$\left(\frac{v_{out}}{i_{in}} \right)_{int} = \left(\frac{-(A_v + s C_o R_o)}{s [(A_v + s R_o C_o) (C_d + C_i) - (1 + A_v - s C_o R_o) (C_d + C_i + C_F)]} \right). \quad (3.28)$$

In those transfer functions of the integrator, C_i is the equivalent capacitance at the input of the integrator in parallel with the photodiode capacitance C_d . R_o being the output resistance of the amplifier (composed of the output resistances of the transistors M_5 and M_6 as referred in figure 3.4) and C_o its output capacitance, i.e. the input capacitance of the trigger and the internal output capacitance of the amplifier. The switch noise current depends on the *ON* or *OFF* mode as discussed before. The RMS voltage can thus be estimated by taking the square root of $\bar{v}_{trig,in}^2$ integrated along the frequency range (i.e from $\omega = 0$ to $\omega_{Noise} = 10 \cdot \omega_T$):

$$v_{trig,in} = \sqrt{\int_0^{\omega_{Noise}} \bar{v}_{trig,in}^2 d\omega}. \quad (3.29)$$

For the values of the designed Miller amplifier (i.e. associated with the Bode diagram of figure 3.6), the noise contributions of each component of figure 3.10 have been simulated in MATLAB according to the previous detailed models. For a diode current of $1nA$, the values are as follow : $300\mu V_{RMS}$ for the photodiode, $15\mu V_{RMS}$ for the Miller amplifier, $10mV_{RMS}$ for the switch when *ON* and $0.5\mu V_{RMS}$ when *OFF*. The evolution of the total noise superposed to the rising and falling integrated signals is showed in figure 3.11 as a function of the diode current. To understand how this noise can perturb the behavior of the circuit, we consider a photocurrent of $1nA$ for example. It is thus integrated in 0.01 second and the circuit would generate 100 pulses in one second. Each noise contribution during the rise and fall periods of the integrated signal, can make the trigger swing earlier or later than expected. The noise amplitude has to be compared to the slope $\frac{I_{INT}}{C_F}$ of the integrated signal during the phase in which it has to be considered and where I_{INT} is the current through C_F .

Indeed, for $1nA$, the noise during the rising phase is of $315\mu V_{RMS}$ superposed to the integrated signal whose slope is $100V/s$. The associated time error is of $315 \times 10^{-8}s$ for a period of $0.01s$ implying a possible error of 0.03% for each pulse. Contrarily, for the reset period of the integrator, the switch yields an average current of $10\mu A$ and thus the slope of the decreasing signal is of $-1 \times 10^6 V/s$ for a resetting

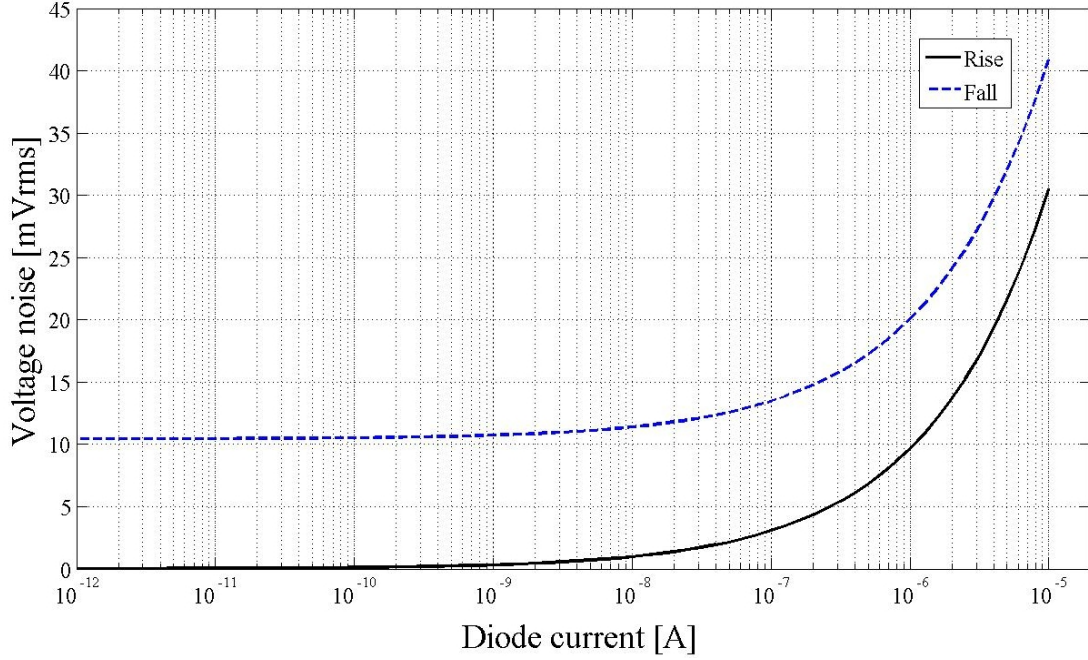


Figure 3.11: Noise voltage evolution at the input of the Schmitt trigger as a function of the diode current. The noise voltage are represented for the rise (continuous line) and fall (dashed line) phases of the integrator.

time of $1\mu s$. A noise of $10mV_{RMS}$ is superposed on quasi vertical decreasing signal implying an error time of $10ns$, thus 1% compared to the time required to reset completely the integrator and of $10^{-4}\%$ compared to the total period of a pulse. Due to the very high slope of the reset signal, the $10mV$ amplitude of the noise is thus negligible and the total error on one pulse is dominated by the noise on the rising signal, i.e. 0.03%.

3.7 Measurements and Performance Analysis

We fabricated a lateral PIN photodiode type in UCL CMOS SOI technology. Its cross-section was introduced in figure 2.3. As said above, the structure of the SOI PIN photodiode features a maximum absorption of the photons whose energy corresponds to a wavelength of $\lambda = 400nm$ in a silicon film for which the thickness is $t_{Si} = 80nm$. A realization of the complete current-to-frequency system featured a $0.25mm^2$ photodiode for which the parameters were $L_i = 8\mu m$, $L_N = L_P = 10\mu m$

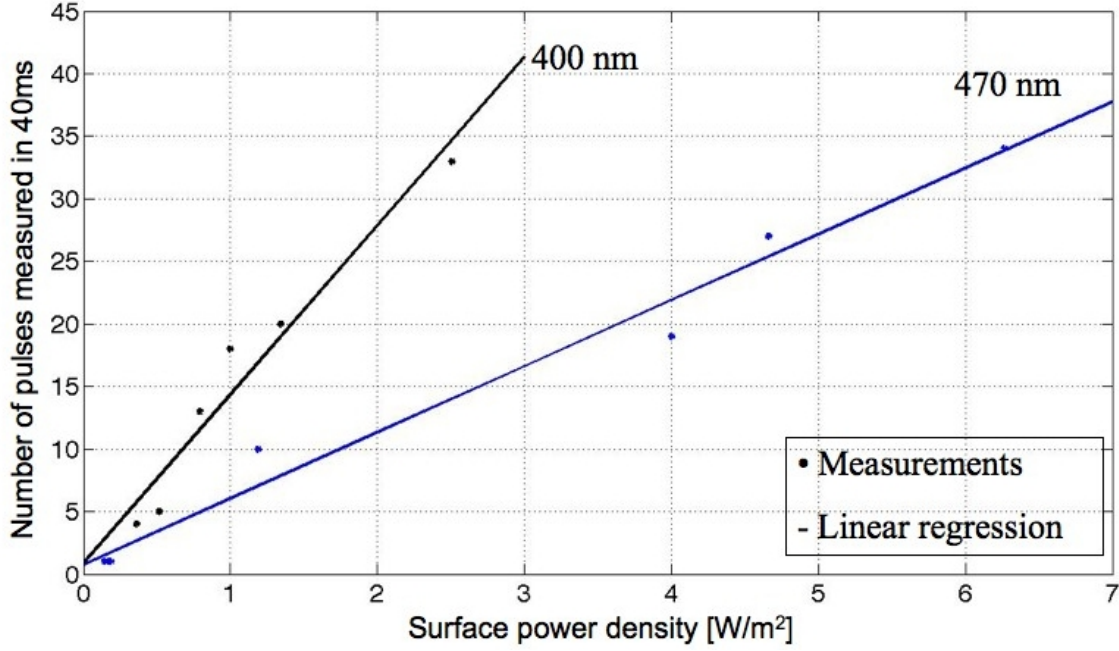


Figure 3.12: Pulse repetition frequency at output of the circuit over one period of 40ms under various surface power densities of illumination for 400 and 470nm emitting LED wavelengths.

and a passivation silicon oxide of 500nm. The classical CMOS Schmitt trigger featuring a 1V dynamic range followed the integrator including a Miller operational amplifier.

3.7.1 Linearity of the system

In order to measure the response of the photosensor to an optical input, we selected four LEDs to be used as light sources with various wavelengths. Two blue LEDs emit at 470nm, while the two other UV LEDs emit at 400nm. By integrating the spectrum of a LED, one obtains, for a given emission wavelength of a LED, the total power density per unit area emitted by the LED [W/m^2]. While varying the bias of LEDs, we swept a range of power densities for each LED. This allowed us to test the circuit at room temperature by illuminating it under two different emitting LED wavelengths and this, with various power densities. The graph given in figure 3.12 illustrates this result. We observe a better responsivity at 400nm than at 470nm, which consolidates the simulation of the responsivity of the photodiode (see figure

2.11). A ratio of responsivity, between $\lambda = 400nm$ and $\lambda = 470nm$, close to 3 is indeed observed in both figures 2.11 and 3.12.

3.7.2 Analysis of results and proposals for improvement

Optical dynamic

By taking again our figure of merit (equation 3.1), the minimal signal detectable depends on the signal-to-noise ratio (SNR) during the integrating period. The noise voltage at the output of the integrator (equivalent to the continuous line in figure 3.11) can be transposed into an equivalent noise current at the input of the integrator. This can be calculated when dividing the noise at the trigger input by the transfer function $\left(\frac{v_{out}}{i_{in}}\right)_{int}$ (see equation 3.28) for which we obtain the continuous line in figure 3.13 as result. The figure 3.13 presents the evolution of the photocurrent and this equivalent noise current during the integrating period as a function of the diode current at the input of the integrator. Their ratio defines the SNR and their intersection gives, the minimum signal detectable (MSD), I_{Min} . On this figure the equivalent noise at the input of the integrator is almost constant because it is dominated by the noise of the amplifier. We can establish that $I_{Min} = 200pA$ due to the noise of the integrator by the intersection of the two curves. It can be seen that from this threshold value, the photocurrent to be processed by the integrator dominates the noise of the system.

As for I_{Max} , simulations showed that a maximum photocurrent of $1\mu A$ was the limit so that the circuit preserves its normal operation and for which the falling time of the integrated signal is ten times higher than its rising time. In other words, the precision of the system, i.e. the trigger, is still of 90%. Beyond this limit, the rise and fall times of the integrated signal are of the same order of magnitude. The output voltage of the integrator is then not able anymore to decrease correctly during the phase of resetting. We can thus write that for this circuit:

$$OD = \frac{1\mu A}{200pA} = 5 \times 10^3.$$

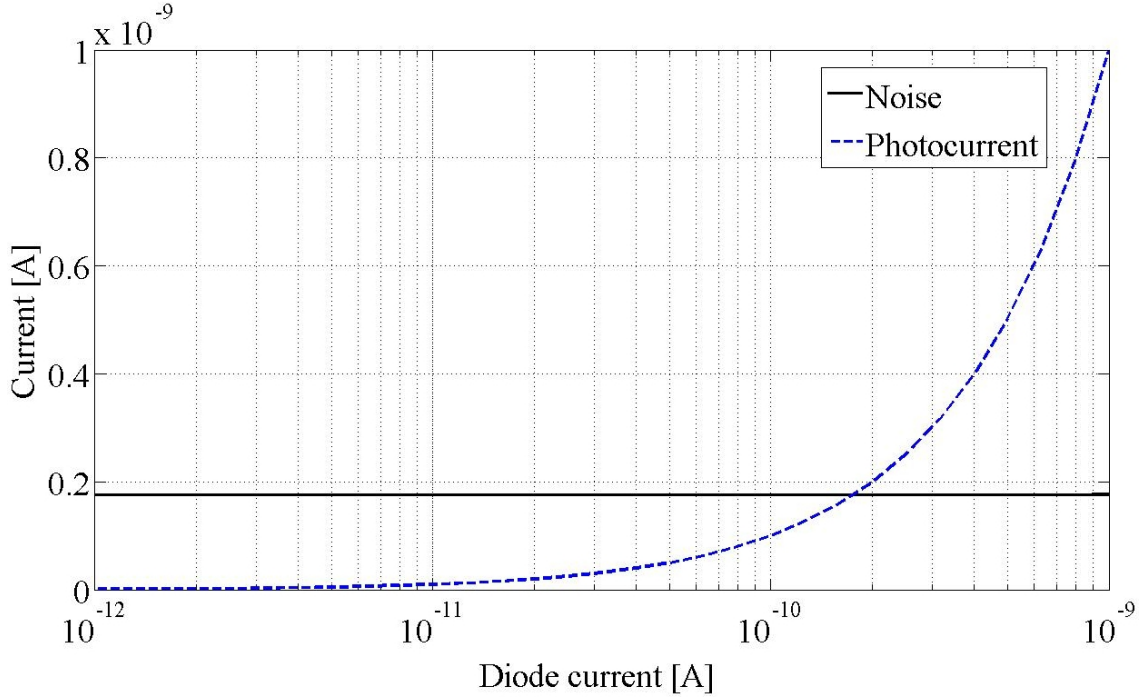


Figure 3.13: Evolution of the noise (continuous line) and the photocurrent (dashed line) as a function of the diode current during the integrating period at the input of the integrator.

Moreover, we can improve our circuit with a design methodology especially studied to minimize the noise. It showed a possible reduction of the equivalent noise at the output of the amplifier allowing the noises of the amplifier and of the photodiode to be of the same order of magnitude for $I_{ph} = 10pA$. This can be achieved by increasing the $\frac{g_m}{I_D}$ parameters of transistors $M_{1,2}$ to increase the voltage gain of the Miller and by increasing the lengths of transistors $M_{3,4}$ to reduce their noise.

Reducing the noise of the switch is possible by increasing its length, however it would increase the reset time of the integrator while it has been previously showed that the noise of the switch during the falling phase was not significant. In the same purpose, the maximal current can also be increased by increasing the slew-rate of the amplifier, and thus, its power consumption. For example, following the same $\frac{g_m}{I_D}$ methodology (see figure 3.5), the table 3.4 presents the features of the amplifier allowing for increasing the optical dynamic. The last line of the table summarizes the performances of the amplifier used for biomedical experiments in chapter 4. It was

however designed with a different methodology, not adapted for low-power purpose at this time.

P_{OW}	$A_{v,0}[dB]$	f_T	$PM[^\circ]$	$I_{Min}[pA]$	$I_{Max}[\mu A]$	OD
$25\mu W$	86.8	$300kHz$	64	200	1	5×10^3
$800\mu W$	79	$1MHz$	61	50	40	8×10^5
$1mW$	96	$4MHz$	60	10	50	5×10^6
$1mW$	68.7	$3.2MHz$	64	50	1	2×10^4

Table 3.4: Evolution of the optical dynamic according to different Miller amplifier performances.

Finally, it is also possible to reduce the dark current of the photodiode by a CMOS-mirror trick [25]. Indeed, by copying the photocurrent of the diode when illuminated, the system is as before. But, when in the dark, if the mirror is *off*, the diode dark current is not recopied and the leakage current of the mirror, whose value is of a few fA as previously demonstrated, is dominating and processed by the integrator. It also could greatly improve the OD and reduce the noise of the photodiode in the dark.

Transient performance

We estimate that one output pulse data is generated for an integrated charge of $10pC$ (i.e. the $1V$ voltage drop on the $10pF$ feedback capacitance) which corresponds to :

- either a maximum current of $1\mu A$ during $10\mu s$. This is compatible with the settling time of the amplifier (given the simulated GBW) and with the slew rate (given its maximum output current of about $10\mu A$). For the improved cases, the slew rate is still adapted to keep a reset time at least ten times small than the lowest integrating time.

- or a minimal $200pA$ photocurrent (for the current case) which corresponds to an integration time of $0.05s$. For the improved cases, the noise-limited $10pA$ current implies a $1s$ period time compatible with the requirements of the typical biomedical applications.

Comparison

Finally, a comparison with other current-to-frequency converters is shown in table 3.5. The comparison is made on the total power consumption of the system (P_{tot}), the minimum signal detectable (MSD) and the optical dynamic (OD). Our work presents

Criteria	Techno	$P_{tot}[W]$	MSD	OD
[6, 7]	$0.5\mu m$ Bulk	NA	$0.15fA$	1.3×10^5
[8]	$0.5\mu m$ Bulk	$130\mu W$	$1pA$	2×10^5
[10]	$0.18\mu m$ Bulk	$26mW$	$1nA/cm^2$	NA
This work	$2\mu m$ SOI	$27\mu W$	$200pA$	5×10^3
This work improved	$2\mu m$ SOI	$1mW$	$10pA$	5×10^6

Table 3.5: Performances of current-to-frequency converters.

the advantage of a low power consumption due to SOI technology. However, due to small intensities to measure, the photodiode is large and its photocurrent fixes the MSD relatively high. We showed that a noise reduction and a higher power consumption could increase the OD to be highly competitive.

3.8 Methodology of Design

The realization of a complete signal processing signal circuit is complex and requires loops of re-design due to noise analysis and optical dynamic performances for example. The choice of the architectures for the components of the system depends on the application and the magnitudes of the optical signal to measure. A block diagram of design is presented in figure 3.14 according to a similar system as in figure 3.2 and especially as our system of figure 3.3.

Firstly, the precision of the system and the frequency to measure give specifications for the first block of the integrated circuit (IC), the integrator and its operational amplifier. In the same time of design, the application fixes the design of the photodiode (i.e. the targeted wavelengths) and a primary idea of the expected range of photocurrents to be processed. The application would also give an idea of the expected time of observation which, combined with the predicted photocurrents, will

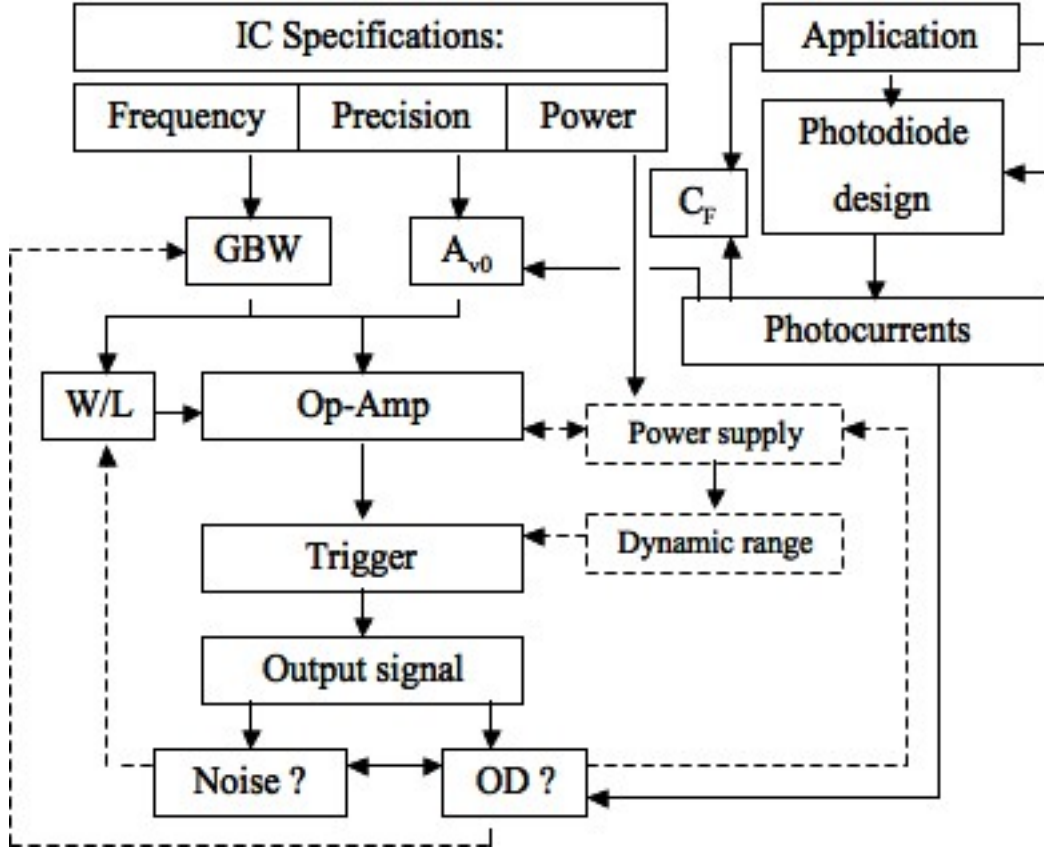


Figure 3.14: Block diagram of design of a photosensor for environmental or biomedical applications.

fix the feedback capacitance value C_F . The choice of the operational amplifier is made based on these specifications, for example a Miller architecture for high gain at relatively low frequencies requirements, or a folded cascode amplifier for higher gain and bandwidth imperatives (but lower output swing). The design of the amplifier is then achieved based on the specifications according to a design algorithmic method such as the $\frac{gm}{I_D}$ one. The power consumption of the system depends on the portability of the system for example and will also be decisive for the design choice of the amplifier. Furthermore, it is related to the dynamic range of the digital signal generation block, i.e. the Schmitt trigger in our case.

The output of the system would then decide whether its accuracy is sufficient as a matter of noise and optical dynamic that are inter-related. A too great noise increases the value of I_{Min} (see figure 3.13) and thus reduces the OD. A re-design of

the operational amplifier is thus needed. On the other hand, to increase the optical dynamic, the maximal current I_{Max} can be increased by increasing the power supply of the amplifier and its GBW in order to be able to process bigger photocurrents and have a sufficient slew-rate.

3.9 Conclusion

In order to process the photocurrent of SOI PIN photodiodes for biomedical and environmental applications, a high-performance current-to-frequency integrated circuit is proposed. After reviewing different kinds of processing signal circuits, a current-to-frequency converter appears to be the most appropriate choice for small current sensing and interface. We presented an architecture composed of an integrator including a Miller operational amplifier followed by a Schmitt trigger. The Miller operational amplifier is designed following the $\frac{gm}{I_D}$ method and consumes $25\mu W$ for a $87dB$ open-loop gain and a $300kHz$ gain-bandwidth product. A single SOI NMOS transistor appears to be sufficient as a switch in terms of leakage currents in this application fields.

Three Schmitt triggers are investigated and we compared their power consumption, slew rate, precision and surface. A low power and guaranteed hysteresis implementation seems to be the most appropriate in terms of dynamic power consumption and precision.

A noise analysis of the system allows to estimate an error on the trigger thresholds due to the noise of the photodiode, the switch and the operational amplifier. The modeling of the noise takes into account the imperfections of the amplifier and the parasitic capacitances of the system in the bandwidth. It is shown that the noise is dominated by the falling edge of the integrated signal due to the large current flowing through the switch. However, the measurement error would be dominated by the noise amplifier during the rising phase. An equivalent modeling of the noise also shows that for the $25\mu W$ amplifier, the minimal detectable signal is of $200pA$ that can be reduced to $10pA$ by increasing the power consumption up to $1mW$.

The system has been fabricated and it proves to be highly sensitive and selective to UVs and adopts the expected behavior of photocurrent to frequency conversion in a broad dynamic range of 3 orders of magnitude (which could be improved to 6 decades with the $1mW$ power consumption). Its function is linear regarding the photodiode responsivity and the comparison with state-of-the-art confirms the realization as competitive.

Finally a global design method has been proposed as a diagram flow taking into account the design of the amplifier with specifications of the applications, the design of the trigger and a re-design loop function of the noise and optical dynamic accuracy.

References

- [1] R.E. Cantwell and R. Hofmann, "Inactivation of indigenous coliform bacteria in unfiltered surface water by ultraviolet light", *Water research*, Vol. 42, No. 10-11, pp. 2729-2735, 2008.
- [2] P.E. Sims, J.D. Lesko, J.A. Cox, E. Chalfin, J.B. McKitterick, "High-temperature optical flame sensor", *High Temperature Electronics Conference - HITEC*, 1998.
- [3] D. Flandre et al., "Fully-depleted SOI CMOS technology for low-voltage low-power mixed digital/analog/microwave circuits", *Analog Integrated Circuits and Signal Processing*, Vol. 21, pp. 213-228, 1999.
- [4] M. Fortsch, H. Zimmermann and H. Pless, "220-MHz monolithically integrated optical sensor with large-area integrated PIN photodiode", *IEEE Sensors Journal*, Vol. 6, No. 2, pp. 385-389, 2006.
- [5] A. Afzalian and D. Flandre, "Monolithically integrated 10Gbit/s photodiode and transimpedance amplifier in thin-film SOI CMOS technology". *IEE Electronics Letters*, Vol. 42, No. 24, pp. 1420-1421, 2006.
- [6] M.L. Simpson, G.S. Sayler, G. Patterson, D.E. Nivens, E.K. Bolton, J.M. Rochelle, J.C. Arnott, B.M. Applegate, S. Ripp and M.A. Guillorn, "An integrated CMOS microluminometer for low-level luminescence sensing in the bioluminescent bioreporter integrated circuit", *Sensors and actuators B*, No. 72, pp. 134-140, 2001.
- [7] E.K. Bolton, G.S. Sayler, D.E. Nivens, J.M. Rochelle, S. Ripp and M.L. Simpson, "Integrated CMOS photodetectors and signal processing for very low-level chemical sensing with the bioluminescent bioreporter integrated circuit", *Sensors and actuators B*, No. 85, pp. 179-185, 2002.
- [8] H.S. Narula and J.G. Harris, "A time-based VLSI potentiostat for ion current measurements", *IEEE Sensors Journal*, Vol. 6, No. 2, pp. 239-247, 2006.

- [9] A. Nemecek, K. Oberhauser and H. Zimmermann, "Distance measurement sensor with PIN-photodiode and bridge circuit ", *IEEE Sensors Journal*, Vol. 6, No. 2, pp. 391-397, 2006.
- [10] H. Eltoukhy, K. Salama and A. El Gamal, "A 0.18- μm CMOS bioluminescence detection lab-on-chip", *IEEE Journal of Solid-State Circuits*, Vol. 41, No. 3, pp. 651-662, 2006.
- [11] A. Luque, D. Vasquez and A. Rueda, "Leakage current and charge injection measurement in thin-film SOI switches", *XVIII conference on Design of Circuits and Integrated Systems*, pp. 706-710, 2003.
- [12] K. Martin, "Digital Integrated Circuit Design", *The Oxford University Series*, 2000.
- [13] J.-P. Eggermont, V. Dessard, A. Vandooren, D. Flandre, J.-P. Colinge, "SOI current and voltage reference sources for applications up to 300°C", *Fourth International High Temperature Conference*, pp. 55-59, Albuquerque, June 1998.
- [14] F. Silveira, D. Flandre, and P.G.A. Jespers, "A gm/ID Based Methodology for the Design of CMOS Analog and Its Application to the Synthesis of a SOI Micropower OTA", *IEEE Journal of Solid-State Circuits*, Vol. 31, pp. 1314-1319, 1996.
- [15] J.-P. Eggermont, D. De Ceuster, D. Flandre, B. Gentinne, P.G.A. Jespers, J.-P. Colinge, "Design of SOI CMOS operational amplifiers for applications up to 300°C", *IEEE Journal of Solid-State Circuits*, Vol. 31, pp. 179-186, 1996.
- [16] B. Iniguez, L.F. Fereira, B. Gentinne and D. Flandre, "A Physically-Based C_{∞} -Continuous Fully-Depleted SOI MOSFET Model for Analog Applications", *IEEE Transactions on Electron Devices*, Vol. 43, No. 4, pp. 568-575, April 1996.
- [17] B. Iniguez, B. Gentinne, V. Dessart and D. Flandre, "A Physically-Based C_{∞} -Continuous Model for Accumulation-Mode SOI pMOSFETs", *IEEE Transactions on Electron Devices*, Vol. 46, No. 12, pp. 2295-2303, December 1999.

- [18] J.-P. Eggermont, "Study and realization of soi operational amplifiers for high-temperature or high-frequency applications", *PhD Thesis*, Université catholique de Louvain, 1998.
- [19] I.M. Filanovsky and H. Baltes, "CMOS Schmitt Trigger Design", *IEEE Transactions on Circuits and Systems*, Vol. 41, No. 1, pp. 44-49, January 1994.
- [20] S.F. Al-Sarawi, "Low power Schmitt trigger circuit", *Electronics Letters*, Vol. 38, No. 18, pp. 1009-1010, August 2002.
- [21] M. Steyaert and W. Sansen, "Novel CMOS Schmitt trigger", *Electronics Letters*, Vol. 22, No. 4, pp. 203-204, February 1986.
- [22] T. Suharli, J. Van Der Spiegel and H.H. Williams, "Analytical and Experimental Studies of Thermal Noise in MOSFET's", *IEEE Transactions on Electron Devices*, Vol. 41, No. 11, pp. 2069-2075, 1994.
- [23] Y.P. Tsividis, "Operation and Modeling of the MOS Transistor", *McGraw-Hill*, New York, 1987.
- [24] O. Bulteel, A. Afzalian and D. Flandre, "Fully integrated blue/UV SOI CMOS photosensor for biomedical and environmental applications", *Analog Integrated Circuits and Signal Processing*, Vol. 65, No. 3, pp. 399-405, Springer, 2010.
- [25] M. Estrada, A. Afzalian, D. Flandre, A. Cerdeira, H. Baez and A. de Lucca, "FD MOS SOI circuit to enhance the ratio of illuminated to dark current of a co-integrated a-Si:H photodiode", *Microelectronics reliability*, Vol. 43, No. 2, pp. 189-193, 2003.

CHAPTER 4

BIOLOGICAL APPLICATIONS OF THE UV PHOTSENSORS

4.1 Introduction

In this chapter we demonstrate the capacity of the SOI photosensors to be exploited in a concrete biological application. UV photodiodes and processing signal circuits, as described in chapters 2 and 3, are used to measure biological material concentration. We first describe the context in which the SOI devices and circuits will be used, and then review the current laboratory methods and apparatus able to perform similar analysis. Since the principle that we exploit is based on the UV absorbance of DNA, the most common UV light sources that will be used in these applications are also reviewed.

The principle of measurement is then explained and the experimental setup is detailed. Afterward, a modeling of the complete system is presented, aimed at being adaptive for any type of optical biological material concentration measurement by light transmission. Preliminary measurements are performed with DNA and bacteria contained in laboratory tubes. The measurements results are first described for a single photodiode. Then, measurements with the complete photosensor including the photodiode and the processing signal circuit are presented. New experiments of a complete system including well microplates or a microfluidic channel for the biological materials are investigated. Finally, we propose some improvements and compare our implementation with the current lab equipments and most used clinic methods.

4.2 *Context*

Biological agents may be characterized (in terms of quantity (or concentration), purity, nature) using optical means like spectrometry, fluorometry and real-time PCR for example. Most of these techniques are based on absorbance or fluorescence. Indeed, many biological molecules can absorb the light when excited at wavelengths close to blue and ultraviolet (UV). For example, DNA, RNA and proteins feature an absorption peak in the deep UV, more precisely around 260 and 280nm [1]. This work is widely focused on those wavelengths. A biological sample concentration measurement method can be based on UV light absorbance or transmittance, as already known and realized with high-cost and large-size biomedical apparatus. But, often, the difficulties come from the limitation for measuring very small concentrations (close to a few ng/ μ L or lower) since the measurement of such small light intensity variations at those low wavelengths requires a precise light source, and very efficient photodetectors. Reducing the dimensions of such a characterization system further requires a small light source, a miniaturized photosensor and a processing system with high precision to reduce the measurement variations. Some light-emitting diodes (LED) performing at those UV wavelengths have recently appeared and may be used to implement the light source. Concerning the optical sensor, while accurate but high-cost photosensors in technologies such as AlGaIn and SiC provide high sensitivities in UV low wavelengths thanks to their semiconductor bandgap [2], the silicon-on-insulator (SOI) layers absorb the photons in that specific range thanks to an appropriate thickness of the silicon. Adding excellent performances of low power consumption, good temperature behavior and high speed [3, 4], the SOI technology allows the designers to integrate a specific signal processing CMOS circuit to transform the photocurrent into a digital signal for example. This opens the possibility to build a low-cost, complete and portable microsystem, including the light source, the photodetector and a recipient for the sample to characterize.

4.3 *Current DNA Quantification Optical Methods*

Nowadays the DNA concentration in liquid samples may be measured by different techniques. For example, it is possible to quantify DNA by its property to absorb light around 260 nm. However, the DNA quantities are usually too small to be detected, so the DNA concentration has to be amplified. A very-well known method to amplify DNA is the polymerase chain reaction (PCR).

4.3.1 *PCR related methods*

The polymerase chain reaction consists in a cyclic repetition of different temperature stages of a solution containing the DNA to amplify, dNTPS, primer and the DNA polymerase enzyme. A heating stage is necessary to separate the two strands of the DNA. At the lower temperature, each strand is used as a template for the synthesis of a new complementary strand by the DNA polymerase. After a consistent number of cycles, the target DNA (determined by the primer) is amplified by a factor 2^x (where x is the cycle number). The DNA concentration can next be measured by two different ways :

- the agarose gel electrophoresis. This consists in a migration of the DNA in an agarose gel under a bias voltage. The size of the double stranded DNA is revealed by a luminescent incorporation agent and estimated by comparison with a DNA ladder used as reference. The detection is visual which is inconvenient because of its dependence on the personal visual accuracy.
- the quantitative real-time PCR. This method allows the measurement of DNA concentrations during the amplification of the DNA by the addition of aspecific fluorophores. Basically, one type of fluorophore is initially added to the solution and engraft to the double stranded DNA along with the increase of the DNA. After each cycle, the DNA solution is illuminated and the fluorophores grafted to the DNA emit a light at a specific wavelength. The emitted fluorescence is thus proportional to the DNA quantity. The main problem of the

real-time PCR is the relatively poor efficiency of the fluorophores and thus the light emission does not always reflect the accurate DNA concentration.

Anyway, the PCR-based methods feature the disadvantages of a long measurement time before obtaining the results, usually between 2 and 3 hours. Moreover, it requires a large-sized laboratory equipment, including a specific software for analyzing the results. They also depend on the PCR amplification efficiency which is not constant with the number of cycles and thus introduce a high variance on statistical analyses.

4.3.2 Spectrometry

Spectrophotometers are used in molecular biology to quantify DNA and also to assess its purity. The spectrometers use a method combining optical fiber and liquid tension to illuminate a droplet of a DNA sample with a UV light. The instrument measures the DNA absorbance at $260nm$ and can also perform a measurement at $280nm$ to detect the presence of contaminating proteins in the sample. The spectrometers allow for quick measurement but with a poor reproducibility when the analysis is made on a stretched droplet.

4.3.3 Fluorometry

Fluorescence spectroscopy is used in biological quantification techniques. It requires fluorescent dyes that can specifically bind to the DNA or RNA molecules. The fluorometry is based on a measurement at 90° of a fluorescent light emitted by a dye excited by the instrument. The fluorometry features a very statistically significant (i.e. inducing a very low variance) result but implies several manipulations, and a long analysis time.

4.4 *The UV Light Sources*

In order to fully take advantage of the UV absorbance property of the DNA, the samples must be illuminated with a light source at appropriate wavelength and power. In laboratories, the equipments described in the previous section feature light sources that are encumbering or expensive. Hereunder is a non-extensive list of such sources :

- the flash lamp. In the spectrometers, Xenon flash lamps are used. They feature an emitting spectrum for which the high emission peak is around $260nm$. This kind of lamp provides a high power but unfortunately generates second order peaks at higher wavelengths so that a precise photosensor is required to detect only the transmitted light at $260nm$ or precise filters must be integrated to cut off the parasitic wavelengths. This could lead to a sensible loss of light power.
- the laser. In the PCR apparatus for example, the light source used to excite the fluorophores has to be very powerful and narrow around the exciting wavelength. The best choice is thus a laser. But apart from these excellent optical characteristics, a laser is very expensive and not suitable for a portable application, since it requires a stabilized supply power and is not miniaturizable.
- the fluorophores. These chemical components allow the detection of a molecule. They are used in the PCR to visually follow the amplification of a target DNA during the exponential stages of the PCR. The nature of the fluorophores may be various. For example, SYBR Green fluorescent dyes bind to the double stranded DNA molecules and emit after excitation a light at a specific wavelength when the DNA is re-assembled. So the emission depends on the hybridization rate of the DNA. Another example is the Taqman probe which, contrarily to the SYBR Green, is based on the FRET principle : a probe is covalently bonded with a fluorophore and a quencher inhibits its fluorescence. Once the exonuclease activity of the polymerase degrades the probe, fluorescence is generated by the fluorochrome. But even if the nature of the

fluorophore may be quite different, their common characteristic is their dependence on their affinity with their target and a relatively poor emission requiring so a long observation time (in order to integrate a sufficient photocurrent) and a very low-noise photosensor.

- the light emitting diode (LED). The LEDs were introduced in the first chapter, and we saw that due to their narrow emitting spectra and their reduced size, they act as excellent portable light source for embedded biological measurement microsystem. The LEDs have also been characterized with a spectrophotometer showing the inverse correlation between their illuminating power and the distance. Therefore a modulation of the optical power of the LED is possible when displacing it from its target.

4.5 Biological Application of the SOI Photodiodes

The current optical measurement methods (presented above in this chapter) require a lot of manipulations (e.g. pipetting, purification, etc.) and are not convenient for portable and low-cost applications. We present here an innovating system to measure DNA concentrations by optical transmittance. As previously introduced, the DNA features an absorption peak around $260nm$, so that its concentration in a liquid sample can be assessed by measuring a ray of light passing through the DNA solution. According to the Beer-Lambert law, the DNA concentration can be directly deduced from the light transmitted through the sample. Previous results demonstrate the feasibility of such a system [6] with a monochromator and our SOI photodiode based on measurements. These early results of the experiments were compared to spectrometry, fluorometry and quantitative real-time PCR. It was shown that the PCR featured the highest detection range but a poor precision and reproducibility. The spectrometry-based method has the lowest detection range and a poor precision. Fluorometry-based quantification presented the highest precision and a relatively good detection range, reaching the one obtained with the SOI photodiode.

4.5.1 The setup

Figure 4.1 shows a setup of the experiment. Starting with a light source, implemented with a LED with appropriate wavelength, we can place the DNA in its container to be directly illuminated by the almost monochromatic light. Finally the sensor is positioned to receive the light that has passed through the DNA in order to measure the transmitted light.

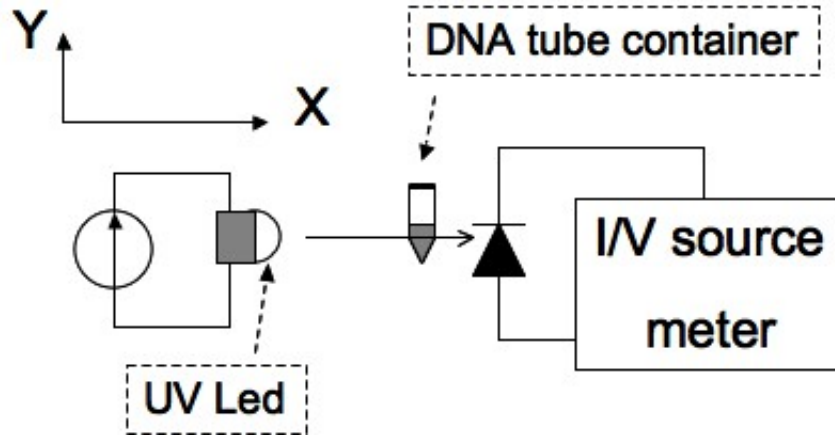


Figure 4.1: Schematic of the system : an UV LED illuminates the DNA sample and the transmitted light is measured by a SOI photodiode coupled to a IV meter.

4.5.2 Measurement of DNA samples in quartz containers

First of all, we wanted to confirm the literature reported results and compare them with those obtained with our system. Thus, we measured DNA samples from *Escherichia coli* in a reference absorption cell from Hellma. These cuvettes are $50\mu L$ quartz containers whose good UV transmittance is a well-known property. The light is focused on a $2.5mm$ diameter circular transparent window confining the DNA in a small cylinder illuminated by the light source. For the first step, the emitting wavelength of the LED was $260nm$. The LED was biased and monitored by a Keithley 236 IV source associated with a four-wire connection ensuring a minimal noise floor needed for the small currents to measure (i.e. a few nA).

Genomic DNA was pipetted and deposited in the quartz cuvettes with concentrations ranging from $400ng/\mu L$ to $400pg/\mu L$. Three currents were measured for

calibrating the system : the dark current of the photodiode, the photocurrent generated directly by the light source (denoted *Light*), and the photocurrent resulting of a blank measurement consisting of $50\mu L$ of water in the quartz cuvettes (denoted H_2O) as referred in figure 4.2 showing the photocurrents of the experiment. Under a $V_D = -0.5V$ reverse bias, an average dark current of $45pA$ was measured. A

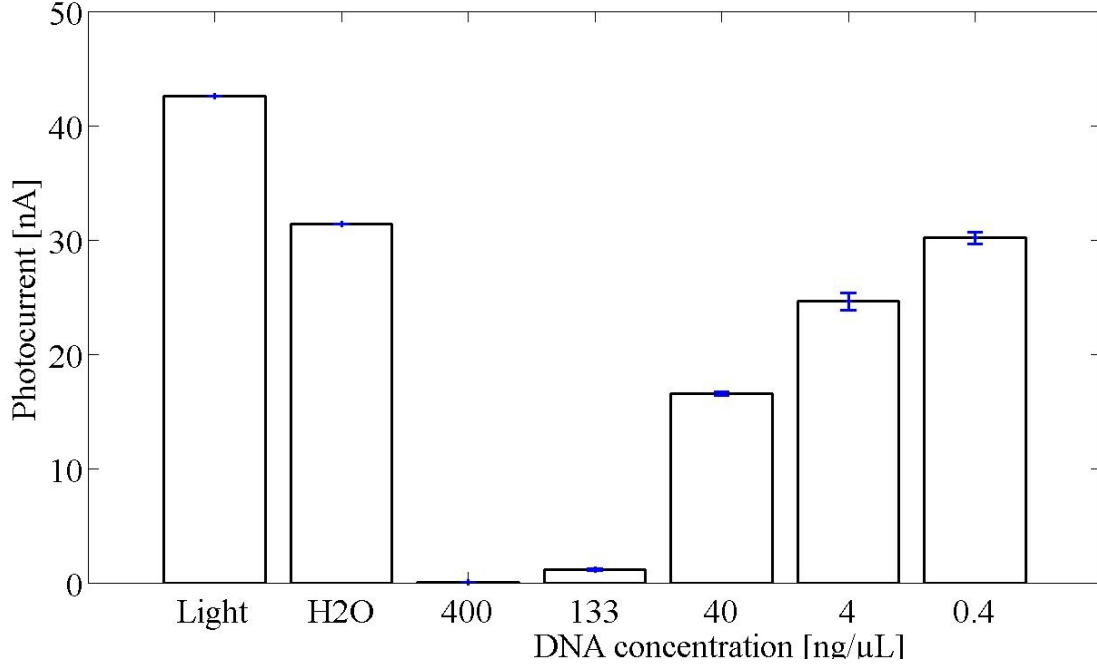


Figure 4.2: Detection of different DNA concentrations (*Escherichia coli*) in the quartz cuvettes: Light and H_2O concentrations were used as references.

monotonic relation between the photocurrent and the DNA concentration was observed. As previously demonstrated in [6], the higher the DNA concentration, the more UV light is absorbed, and the lesser the induced photocurrent is generated in the diode. Evenly the lowest DNA concentration implied the highest photocurrent. This photocurrent was not significantly different from the blank sample. The error bars also shown in the figure correspond to the standard variations at each DNA concentration and pose another limit to the precision as discussed below.

4.6 Modeling

All the experiments feature a certain amount of common characteristics : a miniaturized UV light source, a biological material to quantify, the container and finally, the optical sensor. The UV light source, would be preferably a LED as is has been shown that it offers the best compromise between portability and monochromaticity at low-price. All these components induce a loss of power at each step of the path followed by the light from the LED to the photodiode. The photocurrent can then be modeled as a function of the initial LED power density and the losses at each interface as in figure 4.3 where the evolution of the optical density $I(x)[W/m^2/\lambda]$ is schematized as a function of the distance x .

The LED emitting spectrum has been discussed before as well as its evolution

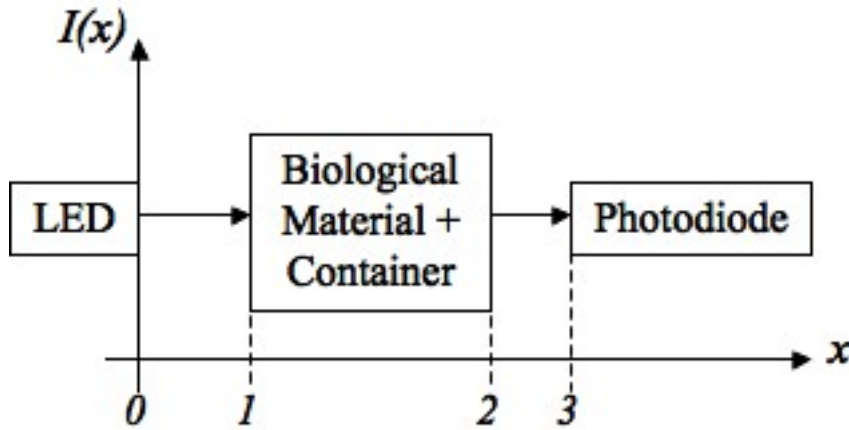


Figure 4.3: Model of the light intensity in the system as a progression through the interfaces.

as a function of the distance. Then, we can write :

$$\frac{I_1}{I_0} = a + \frac{b}{x} \quad \text{and} \quad \frac{I_3}{I_2} = c + \frac{d}{x} \quad (4.1)$$

where a , b , c and d are the fitting parameters deduced during the characterization of the LEDs.

The container, whatever its type (assay tube, well or PDMS channel), it can also be modeled as in chapter 2 by a mathematical implementation of electromagnetic

waves. Moreover, since most of the measurements are monochromatically defined, a global transmittance expressed in percentage can simply model the container behavior with the light.

The most difficult part to model is the biological material which responds to the light absorption phenomenon defined by the Beer-Lambert law as already mentioned in chapter 1 for the light flux. Of course, the transmitted light can be deduced as the light intensity at a length equal to the total path through the sample. To measure the DNA concentration, we can rewrite this law by decomposing the absorption coefficient for biological substance. The Beer-Lambert law then becomes :

$$I(x) = I_i \cdot e^{-\sigma \cdot N \cdot x}, \quad (4.2)$$

where σ is the surface of light absorption per particle of the biological material and N is the volume density of particles. I_i and $I(x)$ being defined as the incident light intensity and the light intensity at a x depth of the material.

As the volume of solution is constant, the length of light path (x) is constant for each measurement, as well as σ since the section of the beam is also the same. Then the extinction of the light will relate only to N which is logically an image of the sensitive particles density [5], i.e. the biological material concentration. We saw in chapter 3 that the circuit was linear with regards to the responsivity of the photodiode. Then, when plotting the results, as a function of a base-10 logarithm progression of the decreasing concentration, it is logical to observe a curve shape as the one of figure 4.2. This confirms the hypothesis of the observed phenomenon. To model the combined behavior of the biological material and its container, the Beer-Lambert law is thus sufficient. This is valid as unless the material concentration, all the other parameters are constant and only depend on the materials composition. Then, as referred to figure 4.3, we can write :

$$\frac{I_2}{I_1} = \alpha \cdot e^{-\beta N}. \quad (4.3)$$

In this equation, α is a constant term for each wavelength and represents the reflection (and eventual (constant) absorption of the container if it is not exactly insulating). β represents the extinction due to the nature of the sample and its depth. Depending on the material, it is also dependent of the wavelength. Those parameters are difficult to exactly define with a single equation but can be deduced from measurement curves and thereby can be useful for a global system calibration.

Finally, the photocurrent (or the number of pulses as they are linearly related), can be expressed by :

$$I_D = \int_{\lambda} \frac{I_3}{I_2} \cdot \frac{I_2}{I_1} \cdot \frac{I_1}{I_0} \cdot I_0(\lambda) \cdot R \cdot S_D d\lambda, \quad (4.4)$$

$$I_D = \int_{\lambda} \left(a + \frac{b}{x_{0 \rightarrow 1}}\right) \cdot \left(c + \frac{d}{x_{2 \rightarrow 3}}\right) \cdot \alpha(\lambda) e^{-\beta(\lambda)N} \cdot I_0(\lambda) \cdot R(\lambda) \cdot S_D d\lambda, \quad (4.5)$$

where R is the responsivity and S_D the surface of the photodiode. As can be seen in these equations, an integral bounded on the emitting spectrum of the LED is needed to obtain the total photocurrent. Finally, the parameters a , b , c and d can be deduced by measurements as well for α and β as explained before.

4.7 Results of In-Tube Measurements with Photodiode

The first step of our methodology demonstrated the principle of DNA measurements in a quartz container with a LED as light source and SOI diode as photosensor. But one condition to be fulfilled by the DNA container is to be as transparent as possible so that the light can interact with the DNA sample with as much optical power as possible. Therefore, we next practiced our experimentations on 200 μ L PCR tubes, as they have already proven their usability [6]. Another advantage is that while the quartz absorption cells require pipetting, drying and cleaning steps, the tube containers allow wasteless measurements with minimal manipulation steps and are much cheaper. A photograph of the setup is shown in figure 4.4. On the left of the

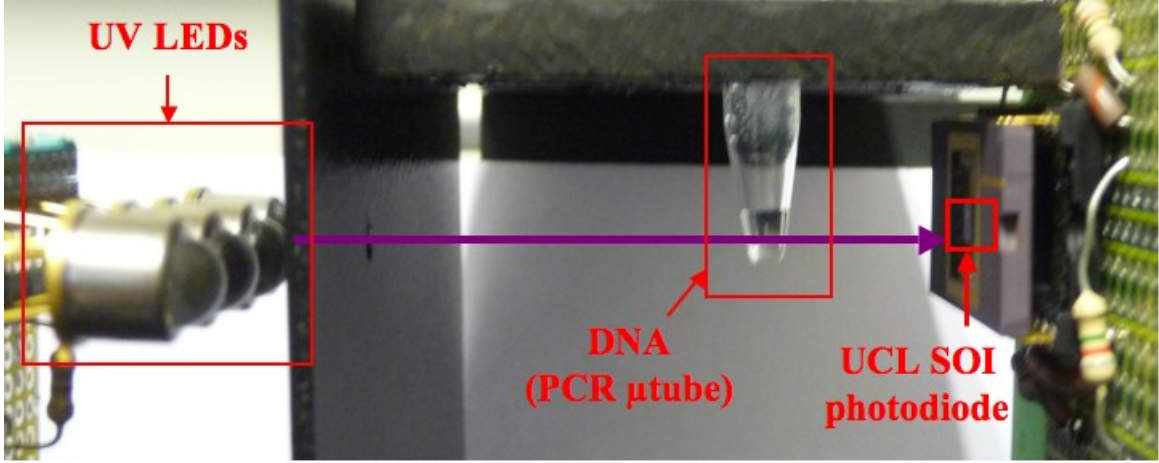


Figure 4.4: Photograph of the tested system for in-tube measurements.

photograph, one can see a rack line of four LEDs emitting respectively at $260nm$, $280nm$, $295nm$ and $360nm$. They are mounted on a XYZ displacer allowing for a selection of the most suitable wavelength according to the molecular nature of the biological target. The photodiode stands on the right of the picture and is encapsulated in a DIL-24 package (also mounted on a XYZ displacer for alignment) while the PCR tube is centered in the photograph on a two dimensional YZ displacer.

4.7.1 Detection limit and other statistical considerations

When dealing with biological samples in order to establish faithfully their concentration, it is crucial to compare the results to commonly used statistical definitions [7]. The most used functions are the precision limit (PL), the minimum detection limit (MDL) also called the limit of detection (LOD) for the laboratory measurements, and the limit of quantification (LOQ). Those are first linked to the blank sample measurements. So, for 20 measurements of a blank tube containing a solution without DNA (i.e. H_2O), the precision limit can be defined as :

$$PL = 3 \cdot \frac{\sigma_{Blank}}{\bar{X}_{Blank}}, \quad (4.6)$$

where σ is the standard deviation and $\bar{X}$ is the mean. Since the number of our measurements is less than 30 per sample, the results are distributed along a Student

distribution, associated with its t-value (i.e. the result of a t-test). Secondly the MDL for a DNA concentration is defined with its t-value compared to the blank measurements as :

$$MDL = (t - value)_n \cdot \sigma_{Blank} = LOD. \quad (4.7)$$

And finally, the LOQ is calculated as follow :

$$LOQ = 10 \cdot \sigma_{Blank}. \quad (4.8)$$

The precision limit will be mainly discussed furtherly on this chapter.

Error bars are displayed for each figure of experimental results in the chapter. The error bars were calculated as the standard deviation for each DNA concentration and are centered around the mean of each DNA concentration. They represent the samples variation, the unhomogeneity of the solutions, and the random behavior of tube placements. Indeed, each tube was regularly vortexed and replaced in the system. Thus, this takes into account the manipulations errors, the placement and samples variations.

4.7.2 Placement

The system is firstly calibrated with no assay tube. For a fixed position of the LED and the blocking mask, the photodiode is placed for obtaining a maximal value of the generated photocurrent under illumination. Then, a PCR tube containing an *europium*-diluted solution is hold on the YZ tube displacer and positioned to induce a minimal value of the photocurrent while fluorescence of the *europium* can confirm the correct alignment of the LED, the sample and the photodiode.

4.7.3 *Description of the varying parameters*

4.7.3.1 *The light source*

Since the LEDs are packaged with a hemispherical lens providing a straight illumination diagram, an aperture mask composed of a dark mask with a 2.5mm diameter circular window is used to focus the light on the tube. The blocking mask is shown in figure 4.4 between the LEDs and the assay tube. The aperture mask also prevents from the diffraction of the light on the rounded boundaries of the PCR tube, which could perturb the measurements.

Among the four available LEDs in the system previously presented, the two with emitting peak wavelengths of 260nm and 280nm were used, respectively for the DNA and proteins measurements. It is established that DNA absorbs the light at 260nm while proteins are more sensitive to a 280nm illumination, but both wavelengths were tested on each target, the ratios of the measurements enabling purity assessments.

4.7.3.2 *The distance*

As discussed in the modeling section above, the LED power illuminating the sample tube can be modulated by the distance between the LED and the tube. While the tubes are at 1 cm from the photodiode, and the blocking mask is also fixed (at a distance of 1.5cm of the tube, i.e. 2.5cm from the photodiode), the LEDs were disposed at three distances from the photodiode : 4.5cm , 6.5cm and 8cm , which corresponds to a reduction of the power by respectively two and three whereas the closest distance displaying the highest power was 4.5cm .

4.7.3.3 *The photodiode bias*

As discussed before, the choice of the photodiode bias is a trade-off between the dark and the photogenerated currents. Moreover, the measurement noise is highly related to the shot noise of the diode, as discussed and estimated in chapter 3. This implies a limit for the current to fill with the MDL of the system. In the experiments, a

reverse voltage sweep range from 0 to $-5V$ was applied to the diode and has lead to choose a reverse bias of $V_D = -0.5V$ to maximize the photocurrent under a constant $\lambda = 280nm$ illumination. The photodiode features a Si_3N_4 anti-reflection coating with thickness of $t_{ARC} = 40nm$ and its other characteristics are $L_i = 8\mu m$, $L_N = L_P = 9\mu m$ and $L_F = 1000\mu m$ for a total area of $1mm^2$. It implies a dark current I_{Dark} of about $60pA/mm^2$ for the following experiment results. The optical dynamic (OD) is the value of the current of a blank sample reported to the dark current [8]. When PCR tubes were used, the current measured with a blank sample was of $3nA$. We then calculated that the OD was of 50, while it was of 700 with the quartz cuvettes.

4.7.4 Results and discussion

To validate the system, two types of samples were tested and the results are reported in this section. Firstly, pure genomic DNA (*Escherichia coli*), and secondly, spores from bacteria (*Bacillus subtilis*). Each substance was diluted into the microtubes to a volume of $50\mu L$ (corresponding to the same volume as in the quartz cuvettes) and each tube was measured four times with the LEDs emitting at $\lambda = 260nm$ and $\lambda = 280nm$. The repeated measurements are essential to take into account the tube displacements, the heterogeneity of the solution (each tube is periodically vortexed to re-homogenize the solution) and other measurement fluctuations. As discussed for the quartz calibration experiment, since the lowest concentration provides the highest photocurrent, all results are displayed as a percentage of the maximal measured current. This enables a normalization of the different tests over the optical dynamic.

4.7.4.1 Measurement precision

The precision of our system, as introduced above in the statistical considerations section, was calculated to be 2.16% over 20 blank measurements and multiplied by 3 to compute the precision limit (PL) from the maximum measured current, as can

been seen in the curves of figures 4.5 to 4.7. The intersection of the precision limit and the sample curve yields an estimate of the lowest limit of detection range.

4.7.4.2 The DNA

The genomic DNA was extracted from *Escherichia coli*, a Gram negative bacterium, and diluted in concentrations ranging from $400\text{ng}/\mu\text{L}$ to $4\text{pg}/\mu\text{L}$. Figures 4.5 and 4.6 report the data for the DNA concentrations that have been measured for the two wavelengths (260 and 280nm), at the three LED-to-photodiode distances.

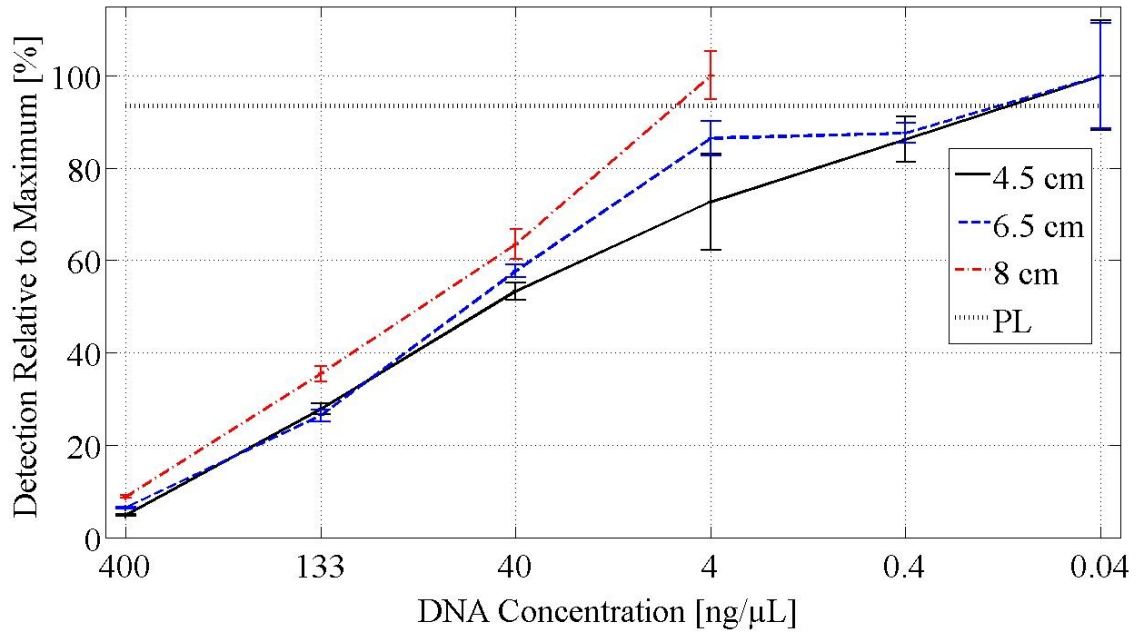


Figure 4.5: DNA concentration measurements from $400\text{ng}/\mu\text{L}$ to $40\text{pg}/\mu\text{L}$ for different distances between the 260nm LED and the photodiode : 4.5cm (solid line), 6.5cm (dashed line), 8cm (dashed and dotted line). Precision limit is indicated as PL (dotted horizontal line) and the standard deviation at each concentration by error bars.

As expected, one can observe a monotonic relation between the photocurrent and the DNA concentration in both figures and shown by the calibration data of figure 4.2. Nevertheless, a closer analysis of the curves can point out the influence of the parameters.

- A first observation is that the LED emitting at $\lambda = 280\text{nm}$ allows a detection range down to $4\text{pg}/\mu\text{L}$, which is better than the detection threshold of $40\text{pg}/\mu\text{L}$

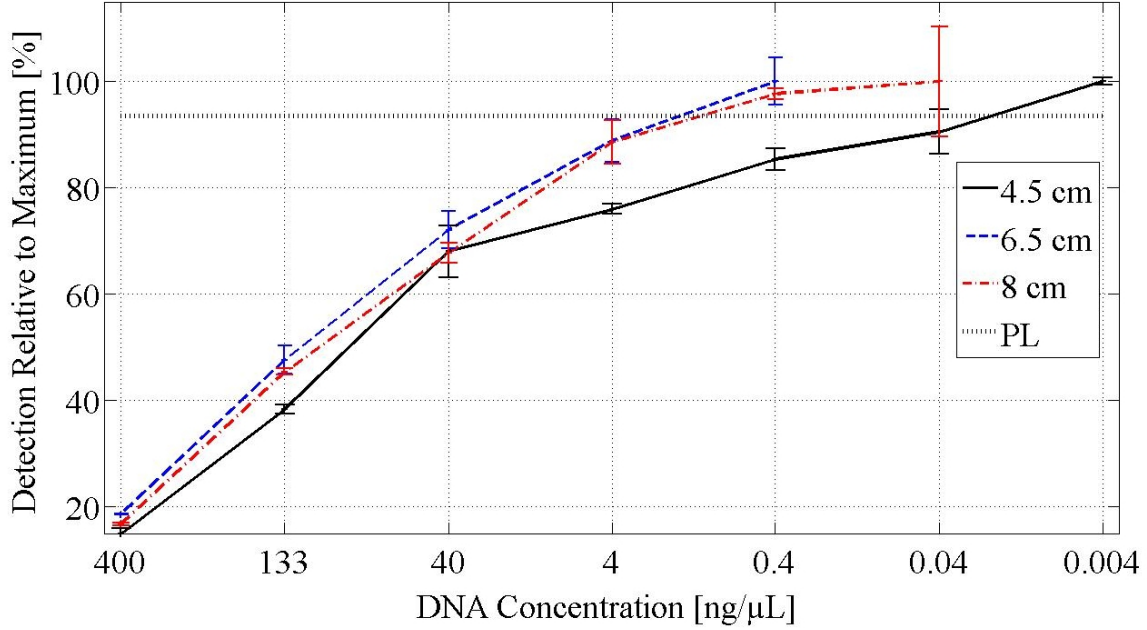


Figure 4.6: DNA concentration measurements from $400\text{ng}/\mu\text{L}$ to $4\text{pg}/\mu\text{L}$ for different distances between the 280nm LED and the photodiode : 4.5cm (solid line), 6.5cm (dotted line), 8cm (dashed and dotted line). Precision limit is indicated as PL (dotted horizontal line) and the standard deviation at each concentration by error bars.

when the LED of $\lambda = 260\text{nm}$ is at a distance of 4.5cm . Concerning the other distances, the low detection range limits appear for $4\text{ng}/\mu\text{L}$ and $40\text{pg}/\mu\text{L}$ at 260nm and 280nm respectively. This observation has already been made [6], and the phenomenon may be explained by the fact that the peak absorption is too high at 260nm , implying a lower threshold for the detection. On the opposite, the slope of the absorption spectrum is lower at $\lambda = 280\text{nm}$ [1] and that would so enable more accurate measurements.

- About the LED emitting at $\lambda = 260\text{nm}$, when decreasing the power, the upper detectable concentration decreases. The upper limit of the detection seems to increase linearly with the distance. This makes sense since the measurement is made at the absorption peak wavelength. In opposition, the distance relation is less clear for $\lambda = 280\text{nm}$.
- It appears that the measurements realized at $\lambda = 280\text{nm}$ are more precise with

regards to standard deviation and are more reproducible than at $\lambda = 260nm$. The excessive absorption at $260nm$ might disturb the level of detection, and this phenomenon may increase if the power fits with the maximum absorption. Contrarily, the measurements carried out at $280nm$ imply less variations on the results because of the lower but more reproducible absorption of DNA around this wavelength.

- The standard deviation generally increases at both wavelengths, except for the shortest distance at $280nm$, with the diminution of the concentration under characterization. A usual trade-off between sensitivity and noise must hence be determined. In figure 4.6, the best threshold of detection then appears to be $0.02ng/\mu L$ when the PL line crosses the measurement curve.

4.7.4.3 The bacteria

Lyophilized spores of a Gram positive bacterium (*Bacillus subtilis*), were resuspended in water in concentrations ranging from $6 \times 10^{11} spores/mL$ to $6 \times 10^4 spores/mL$. Figure 4.7 presents the in-tube measurements for both wavelengths. The measurements at $\lambda = 260nm$ can cover a range down to $6 \times 10^7 spores/mL$, and a decade lower for the LED at $280nm$. Nevertheless, the measurements at $280nm$ are more precise in the measured range compared to those at $260nm$. Indeed the standard deviation at $260nm$ for the concentration of $6 \times 10^8 spores/mL$ is larger.

4.8 Measurements with the Integrated System

As previous experiments have demonstrated, DNA concentration can be measured with a UV SOI photodiode and a UV light source. Therefore, it should also be possible to repeat the results with the complete integrated system presented in the chapter 3. The experiment has been performed by replacing the photodiode chip with a current-to-frequency converter and its associated photodiode in a single chip. The photodiode is $0.25mm^2$ squared and covered with a $500nm$ SiO_2 ARC. The

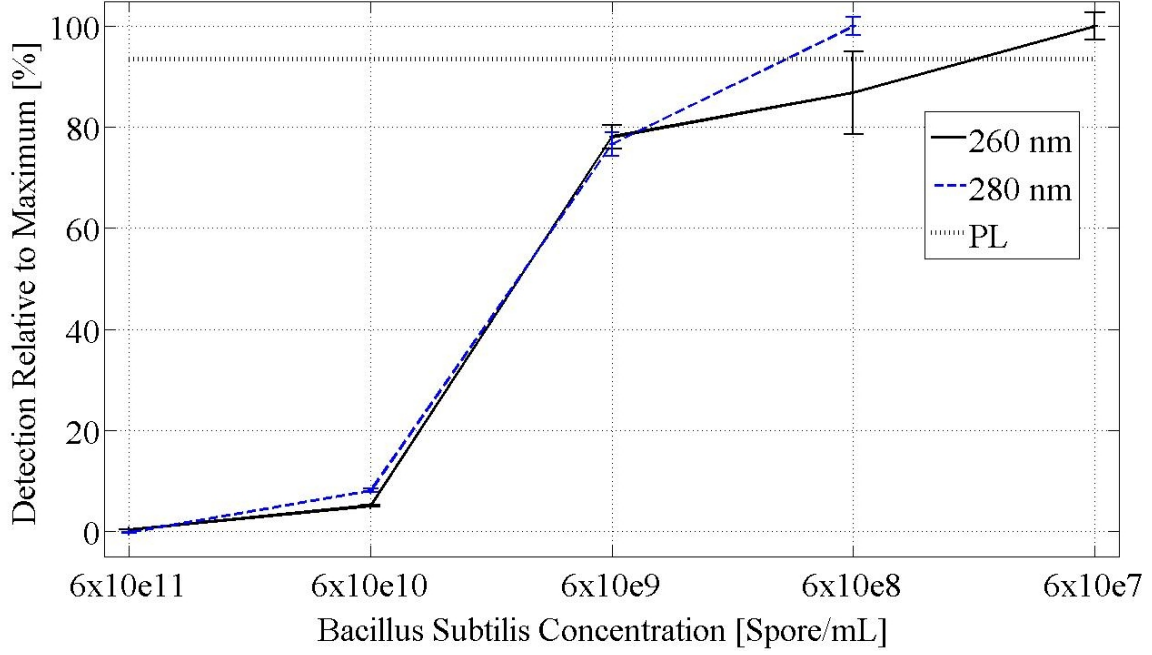


Figure 4.7: *Bacillus subtilis* concentration measurements from 6×10^{11} spores/mL to 6×10^4 spores/mL at $\lambda = 260\text{nm}$ (solid line) and $\lambda = 280\text{nm}$ (dashed line) at a LED-to-photodiode distance of 6.5cm . Precision limit is indicated as PL (dotted horizontal line) and the standard deviation at each concentration by error bars.

device dimension are $L_i = 10\mu\text{m}$ and $L_N = L_P = 10\mu\text{m}$. The operational amplifier features a 68.7dB open-loop gain, a GBW of 3.2MHz and a phase margin of 64° . The Schmitt trigger was implemented with the CMOS classical architecture (see chapter 3 for details) and the total power consumption of the chip is of 1.2mW . The optical dynamic is comprised between $I_{Min} = 50\text{pA}$ and $I_{Max} = 1\mu\text{A}$ ($OD = 2 \times 10^4$).

Following the integrated circuit, a digital system interface (i.e. a digital counter) was externally included to automatically take measurements on a definite time period. The interface send the data to a monitored interface by ZigBee modulation as already made with other biological sensors [9]. For the very low DNA concentrations, a high number of pulses is expected. It was thus required to set the measurement time to 20s to observe a significant response below concentrations of $1\text{pg}/\mu\text{L}$ and hence observe a difference between small concentrations.

4.8.1 In tubes

The 260nm LED has been used to light the DNA tubes at a distance of 4.5cm to the tubes. It was biased with a Keithley 2400 I-V source as well as the integrated circuit. A dark measurement gave a result of 3 pulses only for a 50 seconds observation period. The precision limit has been measured over 20 blank tubes as for the photodiode experiments and computed to be of 11.6%. Figure 4.8 shows the results for this first experiment as a percentage of the maximum number of pulses obtained for the lowest detectable DNA concentration.

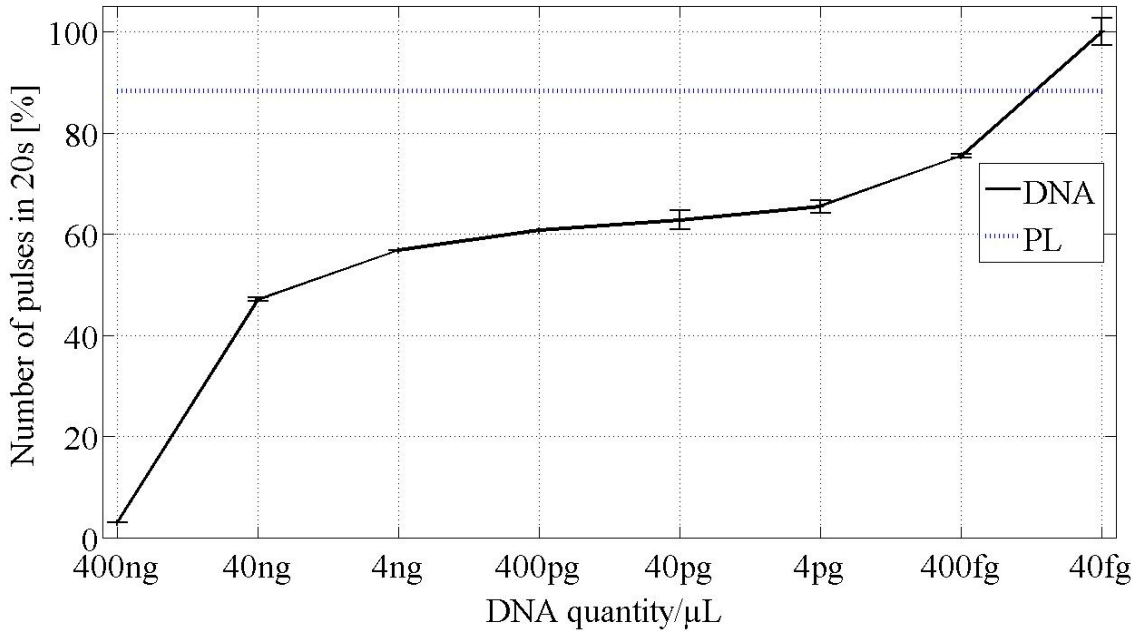


Figure 4.8: DNA concentration measurement from 400ng/ μL to 40fg/ μL for $\lambda = 260nm$ with the I-f circuit during a 20 seconds measurement period (solid line). Precision limit is indicated as PL (dotted horizontal line) and the standard deviation at each concentration by error bars.

One can observe that the circuit is able to measure DNA concentrations over the whole tested range. However, the 11.6% precision limit fixes the detection limit at 200fg/ μL . Nevertheless, using a current-to-frequency converter may imply a better noise stability as can be seen with the small standard deviations at each DNA concentration. A non-ambiguous detection appears maintained down to the lowest tested DNA concentration and allows to yield a detection range of 8 orders of

magnitude.

4.8.2 In well microplates

Since in-tube measurements of DNA associated with the integrated system are concluding, commercial well polystyrene microplates by *Greiner Bio-One* have been used to contain Bovine Serum Albumin (BSA). They offer the advantage of a single cell polymer wall and thus less power loss. Indeed, a spectrophotometry measurement of the bottom well indicated a 90% transmittance from 260nm to upper wavelengths.

For the microplate experiment, the LED and the photosensor are vertically rotated in order to illuminate the well along its depth. The range of tested BSA concentration was from $10\mu\text{g}/\mu\text{L}$ to $1\text{pg}/\mu\text{L}$. The figure 4.9 presents the results of the experiment for BSA.

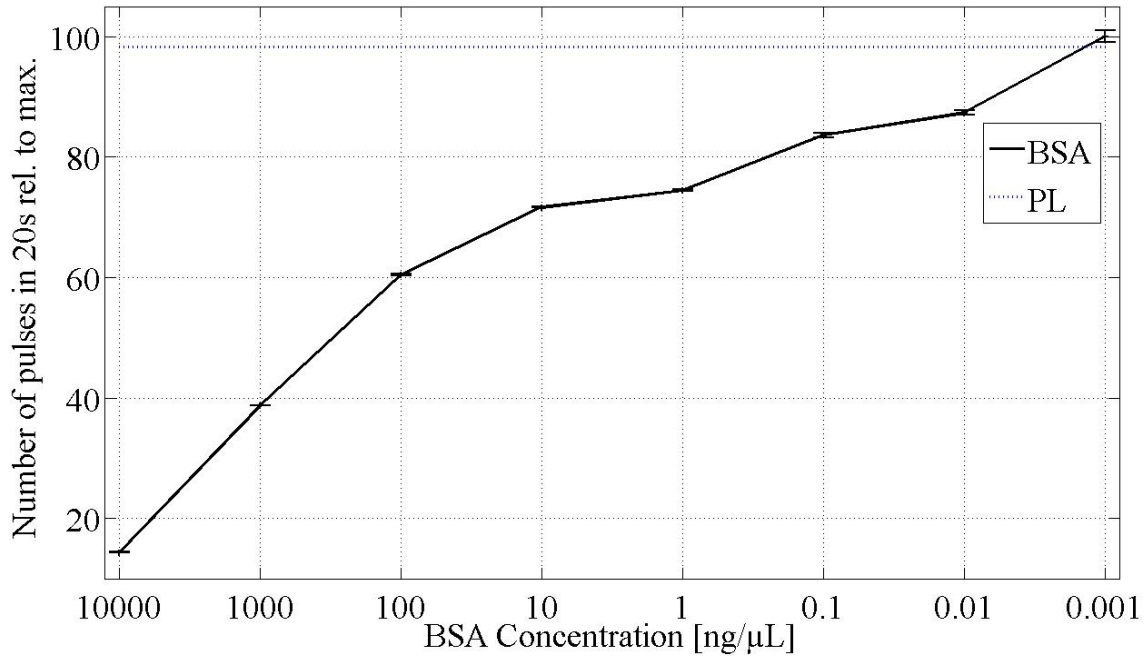


Figure 4.9: BSA concentration measurement from $10\mu\text{g}/\mu\text{L}$ to $1\text{pg}/\mu\text{L}$ for $\lambda = 260\text{nm}$ with the I-f circuit during a 20 seconds measurement period (solid line). Precision limit is indicated as PL (dotted horizontal line) and the standard deviation at each concentration by error bars.

A detection over the whole BSA concentration tested range is achieved for this ex-

periment with the I-f circuit. It confirms the interest of transparent microplates. Here again, the standard deviation is very narrow around each concentration. The limit of detection is almost maximal with $3pg/\mu L$ due to the precision limit of 1.72%.

Influenza measurements

As a perspective of future measurements, *Influenza* virus strains have been measured in the well microplates. The strains were diluted from their initial concentration into dilutions of 1/100, 1/1000 and 1/10000. The measurements resulting from the experiment are presented in figure 4.10. We can observe the previous monotonic

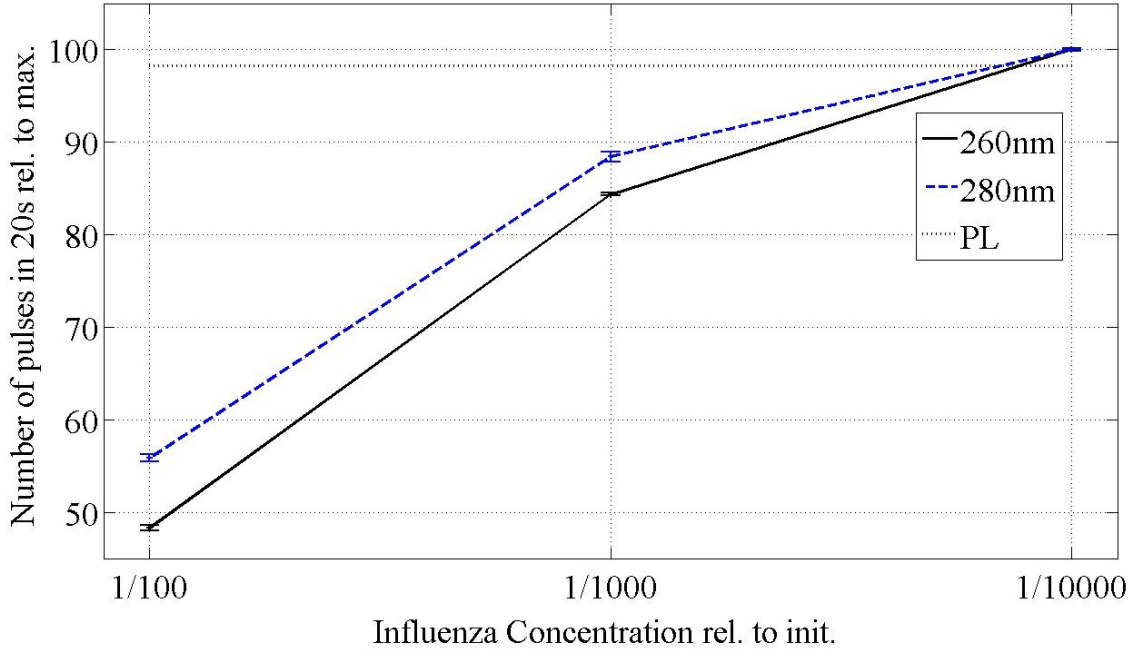


Figure 4.10: Influenza concentration measurement in dilutions from 1/100 to 1/10000 for $\lambda = 260nm$ (continuous line) and $\lambda = 280nm$ (dashed line) with the I-f circuit during a 20 seconds measurement period. Precision limit is indicated as PL (dotted horizontal line) and the standard deviation at each concentration by error bars.

relation between the different dilutions and the induced number of pulses generated by the system during 20s even if the detection range is limited to three orders of magnitude. A preliminary estimation of the limit of detection is set to a dilution of 4/10000 with a precision limit of 1.72% again for the well microplates.

4.8.3 *Within a microfluidic PDMS channel*

The DNA container may also be optimized, as well in size for more portability, as in optical transmittance. Recently, PDMS (for poly(dimethylsiloxane)) microfluidic channels have been fabricated for biological applications [10]. The big advantages of PDMS are UV transparency, electrical insulation, chemical stability, biocompatibility and a fabrication cost fifty times lower than silicon. Hybrid microsystems for biomedical applications have been realized and demonstrate the benefit of using PDMS as a component of bio-SoC [11, 12, 13].

The setup of our experiment was also slightly different from the in-tube measurement, because the measurement was vertical again. The PDMS channel dimensions were a width of $1mm$, a height of $400\mu m$ and a length of $4cm$. The channel was suspended just between the photosensor chip and the LEDs which were on top, illuminating the whole system. A photograph details the experiment in figure 4.11.

For the PDMS measurements, both BSA et DNA were measured in concentrations from $10\mu g/\mu L$ to $1pg/\mu L$. The results of the experiments are detailed in figure 4.12.

The photosensor coupled with the PDSM channel is able to measure DNA over the 7 orders of magnitude of the concentrations. BSA was detected over the first 8 decades. However, for the DNA, the results are very narrow in terms of the number of pulses, as they are ranging in the last 7% of the dynamic. Due to the precision limit of 1.57%, it implies a limit of detection of $200pg/\mu L$. For the BSA, the limit of detection is of $10pg/\mu L$.

4.9 *Comparison and Improvements*

4.9.1 *Comparison*

Our system was compared to most commonly used methods and laboratory equipments used for DNA quantification : the spectrometry, the fluorometry and the PCR, described previously. Table 4.1 summarizes the results of the experiment where, for each DNA concentrations, the sign $\checkmark$ indicated a detection and X an

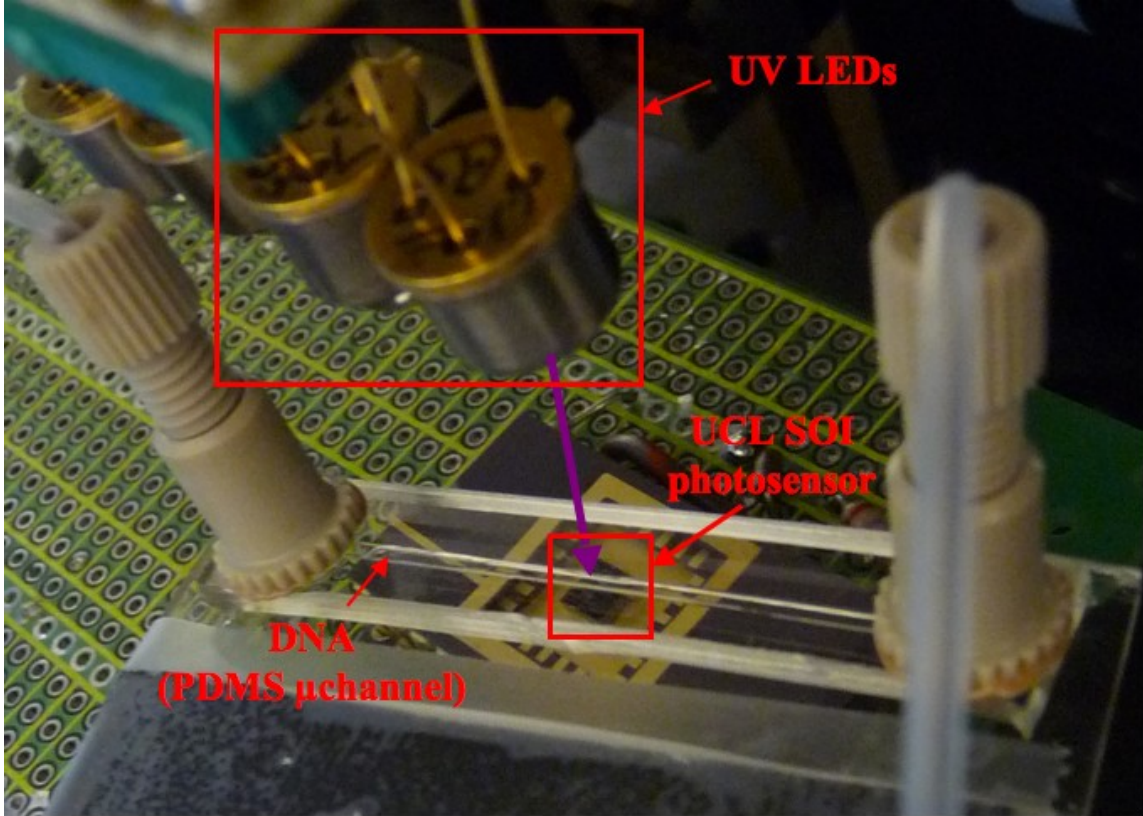


Figure 4.11: Photograph of the setup with PDMS channel.

absence of detection (or an irrelevant measurement result).

It can be seen that the SOI microsystem associated with in-tube measurements yields the largest detection range with the smallest concentration detectable of $40 fg/\mu L$. Even if spectrophotometry was proven as the most accurate according to standard deviation [6], its detection range is quite limited, added to its manipulation inconvenience. The fluorometry features the worse detection range and precision while PCR is also limited in precision due to a combination of different factors : the PCR efficiency, the precision of the optical measurement and the emission efficiency of the fluorophores.

4.9.2 Improvements

One of the major limits of the system is the increase of the standard deviation of light measurements for low DNA concentrations for in-tube measurements with the pho-

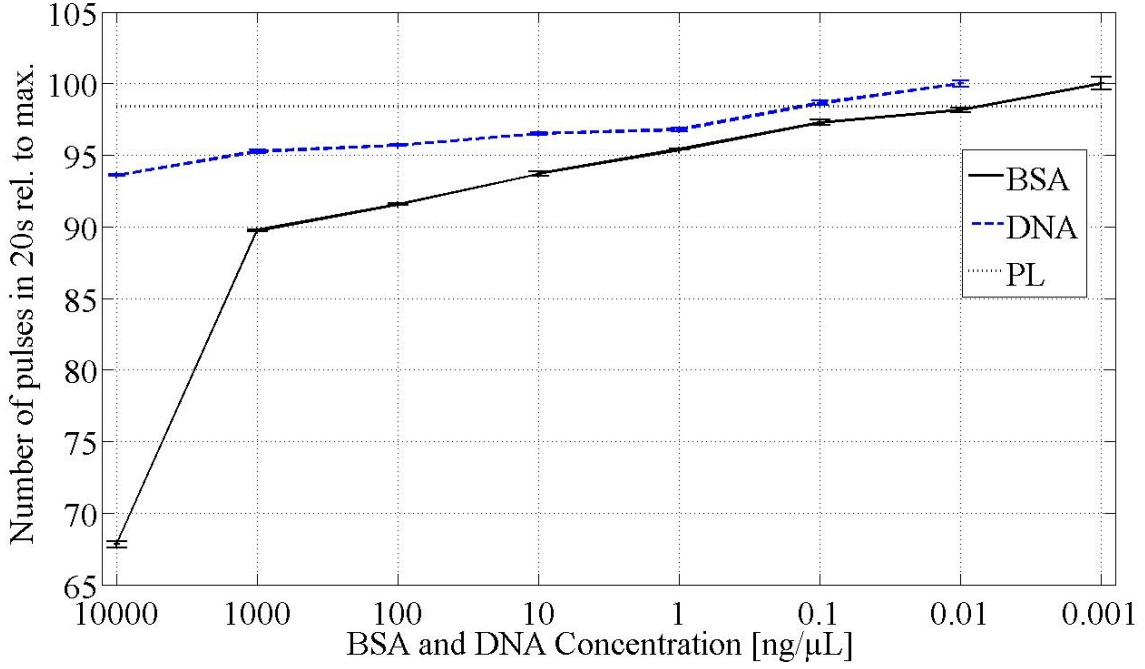


Figure 4.12: BSA (continuous line) and DNA (dashed line) concentration measurement from $10\mu\text{g}/\mu\text{L}$ to $1\text{pg}/\mu\text{L}$ within a PDMS container at $\lambda = 260\text{nm}$. Precision limit is indicated as PL (dotted horizontal line) and the standard deviation at each concentration by error bars.

todiode. To reduce these variations, a first step could be to measure replicates and multiply the number of measurements therefore reducing the standard deviation. On the other hand, the mechanical setup may be improved. With the miniaturization of a future completely portable system, more combined measurements (e.g. concentrations, wavelengths and distances) or increasing the optical dynamic of the system (e.g. by modulating the LED power or improving the photodiode responsivity as demonstrated in [14]) can increase the detection range or reduce the variations at very low concentrations.

Concerning the integrated circuit measurements, it has been showed in chapter 3 that noise reduction and an increase of the optical dynamic could greatly increase the performances of the system. A longer measurement period allows for finer analysis in the small concentrations.

The PDMS channel proved its high interest but complete microsystem including a PDMS channel deposited over the photodiode should be investigated and lead to

[DNA] \ Technology	SOI	Spectrometry	Fluorometry	PCR
$400ng/\mu L$	✓	✓	✓	X
$40ng/\mu L$	✓	✓	✓	✓
$40ng/\mu L$	✓	✓	✓	✓
$400pg/\mu L$	✓	✓	✓	✓
$40pg/\mu L$	✓	X	X	✓
$4pg/\mu L$	✓	X	X	✓
$400fg/\mu L$	✓	X	X	X
$40fg/\mu L$	✓	X	X	X

Table 4.1: Performances of laboratory equipments and current biomedical methods with our systems.

complete microsystems such as real-time PCR on-chip [15].

Currently, a high-stability Keithley DC source biases the LEDs. A temperature and current stable source would be miniaturized to deliver the current biasing the LED. Commercial devices already exist and feature high precision programmable current sources for optoelectronic applications and are indicated for this purpose [16].

4.10 Conclusion

Our experimentations have proven the ability of new photosensors implemented in SOI technology and combined with UV LEDs to establish a monotonic relation between a DNA concentration and the resulting photocurrent after UV transmittance through assay microtubes containing the samples under test. The photodiode alone achieves a current measurement precision of 2% and a detection range over 5 decades of concentrations, down to $4pg/\mu L$ in optimal conditions. The threshold of quantification was estimated at $20pg/\mu L$. With the same PCR tubes, the photodiode is also able to establish a relation between the diode photocurrent and bacteria samples.

The integrated circuit including a SOI photodiode and a CMOS current-to-frequency converter is able to measure DNA concentration down to $40fg/\mu L$ with a precision of about 10%. However, the current-to-frequency converter was also used to measure BSA concentration in well microplates in a range of concentration from

$10\mu\text{g}/\mu\text{L}$ to $1\text{pg}/\mu\text{L}$ with a limit of detection of $3\text{pg}/\mu\text{L}$ due to the precision limit of 1.72% in this configuration. Influenza strains were also correlated to the measurement curve when using the microsystem and the microplates on a range of three decades.

Finally, as opening a new field of experiments, a PDMS channel was used to contain DNA and BSA in the microsystem. The results showed a monotonic relation between the number of pulses generated by the circuit and the concentrations in the ranges from $10\mu\text{g}/\mu\text{L}$ to $1\text{pg}/\mu\text{L}$ for BSA and from $10\mu\text{g}/\mu\text{L}$ to $10\text{pg}/\mu\text{L}$ for DNA. In this experiments, the LODs are of $10\text{pg}/\mu\text{L}$ and $200\text{pg}/\mu\text{L}$ for BSA and DNA respectively with a precision limit of 1.57%.

Compared to optical apparatus and laboratory equipments commonly used to quantify the concentration of biological samples, the detection limits are improved with a very high accuracy. The SOI technology next offers the possibility to integrate the measurement setup into a complete lab-on-a-chip, while the miniaturized components of the system will drive a cost reduction.

Acknowledgments

The authors thank Coris BioConcept for supplying the genomic DNA and the Center of Applied Molecular Technologies (CTMA) of the Université catholique de Louvain and the Defense Laboratory Department (DLD-Bio) for supplying the *Bacillus subtilis* spores.

References

- [1] A. Karczemska and A. Sokolowska, "Materials for DNA sequencing chip", *3rd International Conference on Novel Applications of Wide Bandgap Layers*, pp. 176, Zakopane, June 2001.
- [2] R. Yotter and D. Wilson, "A Review of Photodetectors for Sensing Light-Emitting Reporters in Biological Systems", *IEEE Sensors Journal*, Vol. 3, No. 3, pp. 288-303, June 2003.
- [3] D. Flandre et al., "Fully-Depleted SOI CMOS Technology for Low-Voltage Low-Power Mixed Digital/Analog/Microwave Circuits", *Analog Integrated Circuits and Signal Processing*, Vol. 21, No. 3, pp. 213-228, Decembre 1999.
- [4] D. Flandre et al., "Fully depleted SOI CMOS technology for heterogeneous micropower, high-temperature or RF microsystems", *Solid-State Electronics*, Vol. 45, No. 4, pp. 541-549, April 2001.
- [5] J.D.J. Ingle and S.R. Crouch, "Spectrochemical Analysis", *Prentice Hall*, New Jersey, 1988.
- [6] O. Bulteel, P. Dupuis, S. Jeumont, L. Irengue, J. Ambroise, B. Macq, J.-L. Gala and D. Flandre, "Low-cost miniaturized UV photosensor for direct measurement of DNA concentration within a closed tube container", *Proceedings of the fourth European congress for medical and biomedical engineering 2008*, pp. 1057-1061, Springer, Berlin, 2008.
- [7] J. Ripp, "Analytical detection limit guidance & Laboratory Guide for Determining Method Detection Limits", *Wisconsin Department of Natural Resources Laboratory Certification Program*, April 2006.
- [8] O. Bulteel, A. Afzalian and D. Flandre, "Fully integrated blue/UV SOI CMOS photosensor for biomedical and environmental applications", *Analog Integrated Circuits and Signal Processing*, Vol. 65, No. 3, pp. 399-405, Springer, 2010.
- [9] N. Andre, S. Druart, P. Gerard, R. Pampin, L. Moreno-Hagelsieb, T. Kezai, L. Francis, D. Flandre, and J.-P. Raskin, "Miniaturized Wireless Sensing System

- for Real-Time Breath Activity Recording", *IEEE Sensors Journal*, Vol.10, No. 1, pp. 178 - 184, January 2010.
- [10] J.C. McDonald, D.C. Duffy, J.R. Anderson, D.T. Chiu, H. Wu, O.J.A. Schueller and G.M. Whitesides, "Fabrication of microfluidic systems in poly(dimethylsiloxane)", *Electrophoresis*, Vol. 21, No. 1, pp. 27-40, 2000.
- [11] L. Griscom, Y. Chateau, J.-P. Pennec, L. Misery and B. Le Pioufle, "Co-culture of cells in PDMS microsystem for sensitized artificial skin", *Proceedings of 3rd IEEE/EMBS Conference of Microtechnology in Medicine and Biology*, pp. 184-187, May 12-15, 2005.
- [12] J. Blain Christen and A.G. Andreou, "Design, fabrication and testing of a hybrid CMOS/PDMS microsystem for cell culture and incubation", *IEEE Transactions on Biomedical Circuits and Systems*, Vol. 1, No. 1, pp. 2-14, April 2007.
- [13] N.H. Moreira, A.L. de Jesus de Almeida, M.H. de Oliveira Piazzeta, D.P. de Jesus, A. Deblire, A.L. Gobbi and J.A. Fracassi da Silva, "Fabrication of a multichannel PDMS/glass analytical microsystem with integrated electrodes for amperometric detection", *Lab on a Chip - Miniaturisation for Chemistry and Biology*, Vol. 9, No. 1, pp. 115-121, 2009.
- [14] O. Bulteel and D. Flandre, "Optimization of Blue/UV Sensors Using PIN Photodiodes in Thin-Film SOI Technology", *ECS Transactions of 215th ECS Meeting*, Vol. 19, No. 4, pp. 175-180, San Francisco, May 2009.
- [15] Q. Xiang, B. Xu, R. Fu and D. Li, "Real Time PCR on Disposable PDMS Chip with a Miniaturized Thermal Cycler", *Biomedical Microdevices*, Vol. 7, No. 4, pp. 273-279, 2005.
- [16] Datasheet available online : <http://www.analog.com/en/fiberoptic/laser-drivers/adn8810/products/product.html>

CHAPTER 5

DESIGN AND MODELING OF SOLAR CELLS IN SOI SUBSTRATE

5.1 *Introduction*

In this chapter, we present an analytical numerical analyze of solar cells embedded in the substrate of an SOI wafer. The context of photovoltaic science for silicon solar cell is described as well as the main figures of merit and thermodynamic considerations.

As a premise, the wafer is analyzed with C-V characterization in order to extract the interface charges in the buried oxide and the surface recombination velocities. This also allows for discussing the different conditions (i.e. accumulation, depletion, inversion) of the space charge layer under the BOX. Two devices based on a PIN lateral diode are investigated.

Firstly, an ungated diode acting like a solar cell under the buried oxide of the SOI wafer is investigated. Its modeling and design are studied and discussed, and the measurements curves are presented for different illumination conditions. The comparison between simulated and measurements curves are then discussed. The operating temperature will be extracted from measurements while the values of the surface recombination velocities are extracted from fitted *Silvaco Atlas* simulations.

Secondly a gated solar cell with transparent electrode is studied in more details. Its electrical and photovoltaic behavior according to the gate modulation voltage will be discussed. Measurements of the device are presented and analyzed and also compared with the simulations curves.

Typically, solar cells are connected to circuitry implying a circuit modeling for

simulation softwares like SPICE. The gated and ungated solar cells are modeled with circuit elements like diodes, current sources and resistances to implement an equivalent circuit which models the physics of the photovoltaic cell. The values of the components and the solar cells characteristics are discussed according to the illumination conditions.

Finally, the SOI solar cells are compared to photovoltaic devices in other technologies, and we will propose future improvements to increase their efficiency.

5.2 Context and Solar Cells Characteristics

5.2.1 Interest of SOI solar cells

Sparing silicon and decreasing fabrication costs have become challenging nowadays, in particular for embedding energy autonomy in microsystems such as wireless sensor networks [1]. When using SOI technology, the silicon substrate is usually just considered as a passive rigid holder. But by the use of only one more fabrication mask, with regards to our UCL SOI CMOS process, we can integrate a diode, in the same wafer as CMOS circuitry, just under the buried oxide of a SOI wafer. This can be used as a solar or photovoltaic (PV) cell, whether or not an integrated circuit is realized in the active Si layer of the SOI wafer.

The solar cell can be illuminated by the upper side of the wafer (containing the circuitry), but in future applications, the wafer would be flipped. As for new thin-film solar cells, the substrate can be thinned to a few tens of micrometers and then be back illuminated. This way, the sun would only illuminate the solar cell, and the generated power would supply the active circuitry contained in the active regions of the thin silicon film as schematized in figure 5.1.

5.2.2 Solar spectra

The sun irradiates electromagnetic waves and behaves like a black body whose temperature is about 6000K. However, the emitted total power of the sun is far different

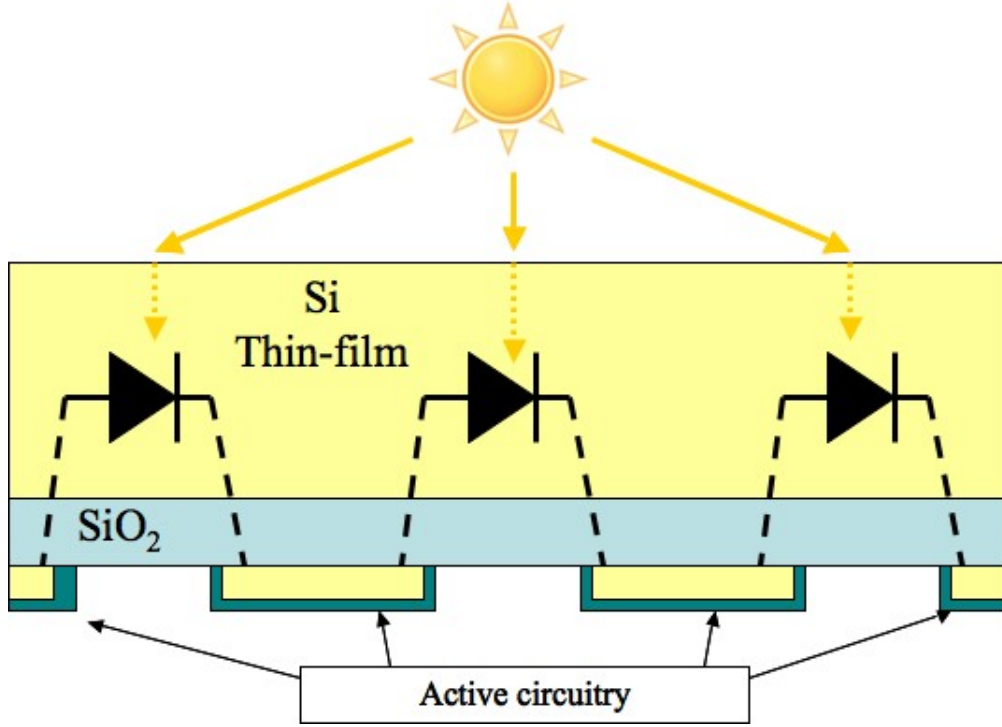


Figure 5.1: Future perspective of embedded solar cell in the substrate of an SOI wafer in the case of a backside illumination.

from the power density of light reaching the solar cell, due to space distance attenuation mainly. The power density of sunlight reaching the outer atmosphere is characterized by the terrestrial spectrum AM0. Nevertheless, the light power density lighting the solar panels is reduced from the AM0 spectrum due mostly to gas attenuation and cloud reflection. For classical solar cells, the irradiation is characterized by the AM1.5G solar spectrum whose total power density is of about $1000\text{W}/\text{m}^2$. Solar cells featuring a concentrator can only concentrate the direct spectrum (called AM1.5D) which irradiates $775\text{W}/\text{m}^2$, the remaining part being dispersed by clouds is the diffuse spectrum. The AM1.5 solar spectra are represented in figure 5.2.

5.2.3 Figures of merit of solar cells

To characterize the solar cells, the current versus voltage (I-V) and power versus voltage (P-V) curves are often plotted based on measurements. The I-V curve has already been showed in the first chapter but both curves for a typical solar cell are

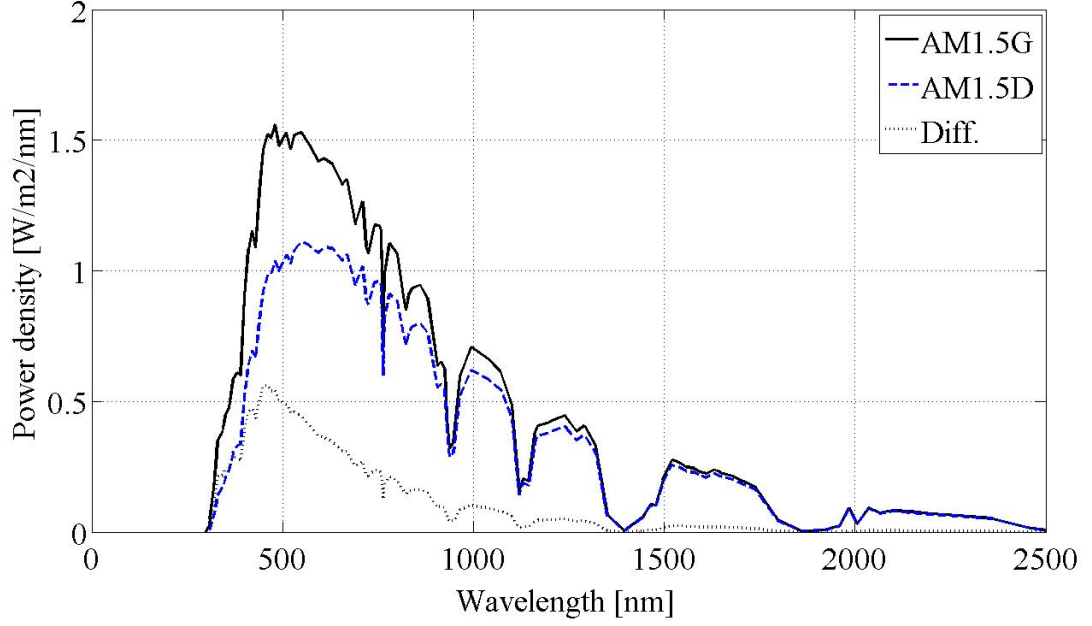


Figure 5.2: Solar spectra densities AM1.5 as a function of the wavelength: the global spectrum (continuous line), the direct (dashed line) and the diffuse spectrum (dotted line).

presented in figure 5.3. On the P-V characteristic, we can observe the maximum of the curve, P_{MAX} which corresponds to the current and voltage I_{MAX} and V_{MAX} respectively. On the I-V curve, we can define the maximal values for the current and voltage obtained at the intersection of the axes, i.e. the short-circuit current I_{SC} and the open-circuit voltage V_{OC} . Of course, as the I-V characteristic follows a curve, the product of $I_{SC} \times V_{OC}$ is always greater than the product $I_{MAX} \times V_{MAX}$. The fill factor FF is defined as the ratio of the maximal area of the rectangle found under the real I-V curve of the solar cell by the area of the rectangle of length V_{OC} and width I_{SC} . The fill factor is given by the equation :

$$FF = \frac{V_{max} \cdot I_{max}}{V_{oc} \cdot I_{sc}}. \quad (5.1)$$

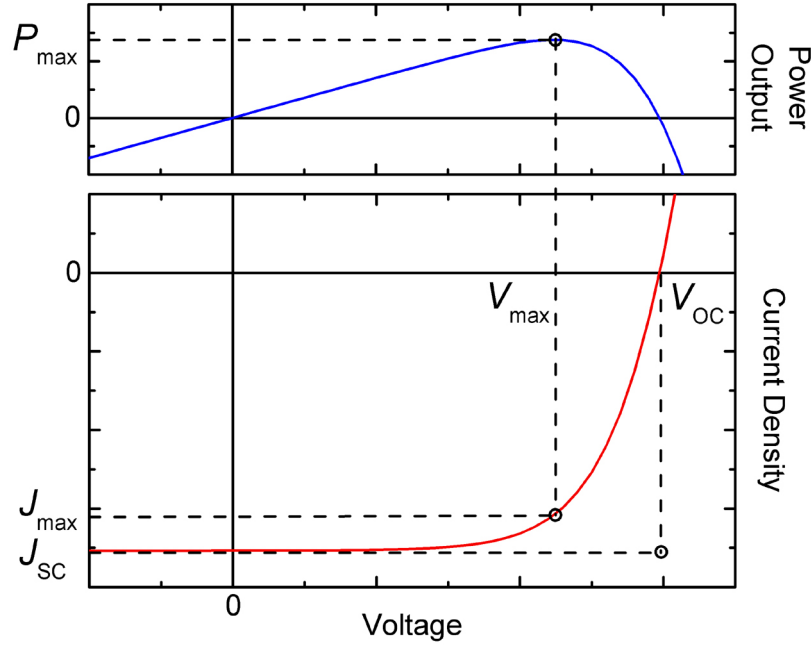


Figure 5.3: Power and current versus voltage of a solar cell [2]. The P-V curve is above in blue and the I-V curve is below in red.

Similarly, the efficiency of the solar cell, η is defined as the ratio of P_{MAX} by the total light power to the surface of the photodiode, P_{in} :

$$\eta = \frac{V_{max} \cdot I_{max}}{P_{in}}. \quad (5.2)$$

5.2.4 Thermodynamic considerations

The upper efficiency limit of a single PN diode in silicon has been estimated at 40.7% while the efficiency of a solar converter can reach higher values up to 86.8% when using array of different solar cells with appropriate bandgaps [3]. However, the maximal photocurrent density equivalent to the maximal number of electron-hole pairs generated can be computed as the integration of the generation term on the thickness of the silicon as indicated by equation 5.3 :

$$J_{Ph,Max} = q \cdot \int_0^\infty G dy. \quad (5.3)$$

For a solar spectrum AM1.5G with incident energy of $1000W/m^2$, the maximal current density in silicon is $J_{Ph,Max} = 420A/m^2$. However, the photocurrents will generally be smaller because all electron-hole pairs cannot participate to the effective current due to various recombination phenomena. It will be discussed later in more details.

However, it has been shown that impact ionization phenomenon can improve efficiency. Indeed, under the influence of an intense electric field, an avalanche breakdown is created and additional electron-hole pairs are generated. Then internal quantum efficiencies can reach values higher than 100% [3].

5.3 Solar Cells in UCL SOI Technology

5.3.1 Fabrication

As previously explained in chapter 1, in order to capture the largest part of the sun irradiation, the thickness of the silicon must be large enough for light absorption. That is why we fabricated the solar cells in the silicon substrate of a SOI wafer. The substrate is naturally low doped with an acceptor concentration of $N_{A-} = 10^{15}cm^{-3}$ like for the thin silicon film and is covered at the back of the wafer with aluminum. To implant the anode and cathode regions, it is necessary to etch the buried oxide whose thickness is of $400nm$. This is done by reactive ion etching (RIE) for the first $370nm$ and finished with buffered hydrofluoric etching (BHF) for the last $30nm$. This is the only additional step compared to our basic fully-depleted SOI CMOS process. However, substrate contacts through oxide exist in more complex SOI technologies. Then, the MOS oxide is grown on top of both thin Si overlayer and Si substrate in the contact regions with thickness of about $30nm$ and the anode and cathode regions are implanted through this last oxide. The implantation parameters are a dose of $4.5 \times 10^{15}cm^{-2}$ at $40keV$ of Arsenic for the N region and a dose of $5 \times 10^{15}cm^{-2}$ at $20keV$ of Bore for the P region. The junction would then be at a depth of about $200nm$ as simulated with the *Silvaco Athena* process simulator. Concerning

the dopings , they reach values of $N^+ = 10^{20}cm^{-3}$ and $P^+ = 4 \times 10^{20}cm^{-3}$ for the contacts within a slightly P^- doped substrate in which the concentration is $P^- = 10^{15}cm^{-3}$ for the intrinsic region.

Process defects

Two major problems occur during the fabrication of a SOI solar cell in the substrate causing parasitic recombination. The first one comes from the fabrication of the wafer by a smart-cut process. Indeed, during the wafer bonding which creates the buried oxide, the BOX may feature defects near the interface with the substrate [4]. A density of fixed charges and defect interface traps (DIT) with the associated surface recombination velocities can be expected and extracted from various measurement techniques. For example, pseudo-MOSFET characterization technique can be used to measure the surface recombination velocities and defects in SOI wafers [5, 6]. Otherwise, gated diode techniques allow for determining the lifetime in SOI from separate sources (at top interface, bottom interface and in the volume) [7, 8].

Secondly, the interface can be further contaminated with the deposition of ARC layer in the process. If the additional layers are deposited by plasmas method, ions can increase the trap density. For example, during the UCL fabrication process of the solar cells, PECVD Si_3N_4 was deposited during the final passivation of the wafer, like for the UV sensors (cfr. chapter 2). From those phenomena, a net charge density can be used to model the different mobile and fixed charges in the oxide and at its interface with the substrate, as described in [9]. This will be discussed and studied in more details hereafter.

5.3.2 *Devices*

On a CMOS die, some places in the SOI layer do not contain active circuitry. In this case, the thin silicon film is fully oxidized in a step called *local oxidation of the silicon* (or the LOCOS [10]). Two types of devices can thus be fabricated : if the thin silicon film is oxidized, the solar cell is just protected with silicon dioxide on its

top and is called an *ungated solar cell*. Otherwise, the thin silicon film remains over the BOX and can be biased to modulate the charges in the solar cell under it. The second device is called a *gated solar cell* and the biased active circuitry in the thin film is called the *frontgate* by opposition with the classical *backgate* of the substrate. The frontgate consisting of the thin Si film is thus transparent to electromagnetic waves for which the wavelength correspond to the visible spectrum. Both devices will be extensively studied in this chapter.

5.4 BOX/Substrate Interface Characterization

As discussed here above, the interface between the buried oxide and the silicon substrate is the main source of recombination for the two types of solar cells that we designed. The study of the interface and the oxide charge density is thus primordial. To characterize it, we study the MOS capacitor of a gated structure. The tested structure is showed in figure 5.4. To evaluate the modes of operation of the space

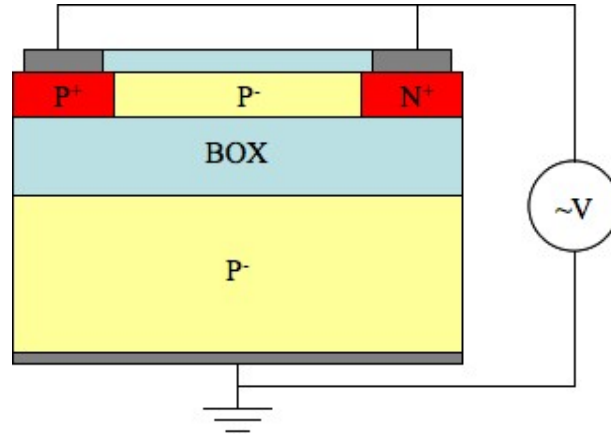


Figure 5.4: Test structure for the CV characterization of the BOX/substrate interface.

charge region under the BOX, a MOS capacitor analysis is needed to calculate the flatband and the threshold voltages. The frontgate must be mostly semiconductor in order to be conductive but not metallic to avoid reflections in case of a front illumination. The gate can then be for example a silicon resistor or a PIN diode. The silicon frontgate featuring a global Fermi level E_{FG} , and the substrate itself for

which $E_{SUB} = \frac{kT}{q} \ln \left(\frac{N_{A,P-}}{n_i} \right)$, the flatband voltage is calculated as:

$$V_{FB} = \Phi_{MS} + V_{Q,BOX} = \frac{-(E_{FG} - E_{SUB})}{q} - \frac{Q_{BOX}}{C_{OX}}, \quad (5.4)$$

where Q_{BOX} is the total equivalent density of charges at the oxide/substrate interface and C_{OX} is the surface capacitance of the BOX. Q_{BOX} consists in the fixed oxide charge $Q_{OX,f}$, the mobile oxide charge $Q_{OX,m}$, the oxide trapped charge Q_{OT} and the interface trapped charge Q_{IT} at the flatband voltage as referred in [9]. For our technology, the BOX capacitance is of $8.62nF/cm^2$ for a total oxide thickness of $400nm$. The threshold voltage of the capacitor is given by the classical formula :

$$V_{TH,C_{OX}} = V_{FB} + 2|\Phi_{SUB}| - \frac{Q_D}{C_{OX}}, \quad (5.5)$$

where Q_D are the depletion charges expressed by $Q_D = -\sqrt{4q\epsilon_{Si}N_{A,P-}\Phi_{SUB}}$. In this case, the BOX depletion charges is $Q_D = -1.4 \times 10^{-8}C$. Those considerations allows for evaluating the charge type under the BOX as a function of the frontgate voltage V_{FG} . If $V_{FG} < V_{FB}$, the solar cell is in accumulation and if $V_{FG} > V_{TH,C_{OX}}$, the solar cell is in inversion. Otherwise, the solar cell stays in depletion, and so it is when no voltage is applied on the frontgate.

Even if the resistor is the most accurate choice of frontgate, the PIN diode was investigated creating a structure consisting of a UV sensor superposed on a solar cell. As a three different doping device, the PIN diode implies a spatial distribution of the flatband and threshold voltages like for a graded channel transistor [11].

The C-V characteristic of the BOX capacitance has been measured by AC sweeps. The figure 5.5 shows the curves for frequency ranging from $100Hz$ to $1MHz$ for frontgate to backgate voltages from -10 to $+10V$. From this figure, estimations for the global flatband and threshold voltages are $0V$ and $2V$ respectively. A representation of the depletion voltage ranges of the three regions of the PIN diodes is shown in figure 5.6.

An average flatband voltage of $V_{FB,Av} = 0V$ calculated as the mean of the three

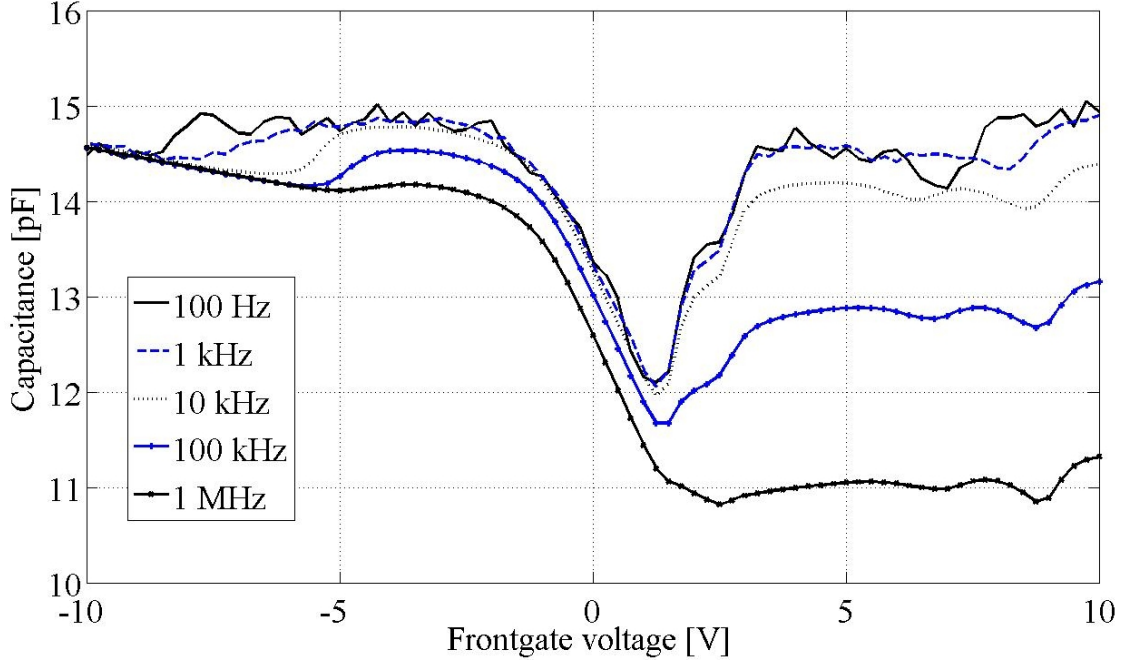


Figure 5.5: C-V measurement of the BOX capacitance for frontgate voltage from -10 to $+10V$ at frequencies of $100Hz$ (continuous line), $1kHz$ (dashed line), $10kHz$ (dotted line), $100kHz$ (-+-) and $1MHz$ (-x).

flatband voltages of each region implies a total equivalent Q_{BOX} charge density of $-10^{10}cm^{-2}$ while the average threshold voltage is of $V_{TH,Av} = 2.2V$. These values coincide with the measurement curve of figure 5.5 if we consider the same doping levels as for the CMOS process. For a doping of $N^+ = 10^{20}cm^{-3}$, the flatband voltage is of $-0.86V$ while the threshold voltage is of $+1.5V$. The associated flatband and threshold voltages of the P^- and P^+ are shifted by $0.9V$ and $1.2V$ respectively to the positive voltages due to their lower Fermi level as represented in the figure 5.6. This value is quite high for photovoltaic applications but is however good for CMOS processes [12]. The Q_{BOX} value can be explained by the particular bonding interface of the SOI technology and by the use of plasma etching (i.e. RIE for the BOX and the inter-dielectric SiO_2) and deposition (PECVD SiO_2 for the inter-dielectric and PECVD Si_3N_4 for anti-reflecting coatings). In smart-cut SOI process, the interface charges are usually positive but the three-doping frontgate implies shifted and multi levels flatband and threshold voltages. The associated equivalent interface charge is thus negative in this case, due to this particular structure and the average value

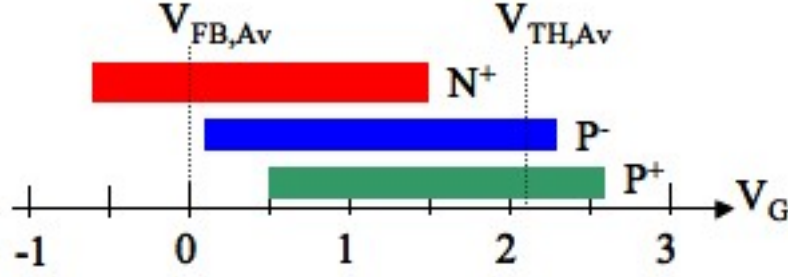


Figure 5.6: Representation of the depletion voltage ranges for the three semiconductor doping levels of the PIN diode in the thin-film. $N^+ = 10^{20} \text{cm}^{-3}$, $P^+ = 4 \times 10^{20} \text{cm}^{-3}$, $P^- = 10^{15} \text{cm}^{-3}$ and $Q_{BOX} = -10^{10} \text{cm}^{-2}$.

extraction.

The interface trapped charges capacitance C_{IT} can be calculated from the values of the low-frequency (C_{LF}) and the high-frequency (C_{HF}) capacitance for the voltage corresponding to the minima of the low-frequency capacitance. According to [9], the D_{IT} is then expressed as :

$$D_{IT} = \frac{C_{OX}}{q^2} \cdot \left(\frac{C_{LF}}{C_{OX} - C_{LF}} - \frac{C_{HF}}{C_{OX} - C_{HF}} \right). \quad (5.6)$$

From curves of figure 5.5, $D_{IT} = 2.2 \times 10^{10} \text{cm}^{-2} \text{C/eV}$.

The value of the D_{IT} allows for calculating the equivalent surface recombination velocities at the interface S . Both are related by the expression [8] :

$$S = \frac{\pi}{2} \cdot \sigma_{eq} \cdot v_{th} \cdot \frac{kT}{q} \cdot D_{IT}, \quad (5.7)$$

in which $\sigma_{eq} = \sqrt{\sigma_n \cdot \sigma_p}$ is the equivalent capture cross section related to the capture cross sections σ_n and σ_p for electron and hole respectively. v_{th} is the thermal velocity of the carrier whose value is about $2.5 \times 10^7 \text{cm/s}$. For solar cells, S is ranging from 0 to 10^3cm/s for passivated interfaces and from 10^5 to $3 \times 10^6 \text{cm/s}$ for metal contacts [13]. The interface fabrication is the result of wafer bonding as explained above and is thus of a poor quality. The surface recombination velocities must probably range between both values, from 10^3 to 10^5cm/s . The value of S will be discussed hereafter when comparing the P-V curves of simulated and measured solar cells

under illumination. Another phenomenon to observe is the bell shape of the C-V curve from in the $[-5V, -2V]$ range. This may be explained by the particular constitution of the gate, i.e. a gate with three Fermi levels short-circuited.

5.5 Ungated Lateral PIN Diode as Solar Cell

5.5.1 Design and fabrication

As introduced at the beginning of this chapter, a lateral PIN diode can be fabricated in the substrate of a SOI wafer. Compared to a standard CMOS process, a single additional step is required : etching the BOX before anode and cathode implantations which are separated by an intrinsic region naturally P^- doped. The cell N^+ and P^+ type zones are implanted with same impurities as source and drain concentrations of transistors in the thin film, i.e. $N^+ = 10^{20}cm^{-3}$ and $P^+ = 4 \times 10^{20}cm^{-3}$ and their width is of $L_N = L_P = 10\mu m$. The interconnect vias and layers are also shared with the CMOS process. The fabricated diodes were designed as interdigitated devices of intrinsic length $L_i = 34\mu m$ in a square of $500\mu m$ side. As a result, three semiconductor devices appear in the substrate as this can be seen in figure 5.7: a lateral PIN diode just below the buried oxide, a vertical PN diode between the PIN anode and the substrate back contact, and finally, a resistance between the cathode of the PIN and the substrate back contact. To only take into account the behavior of the PIN lateral diode during the measurements, the resistor has to be short-circuited or the backgate left floating.

On top of the BOX and hence over the intrinsic zones of the PIN diodes, a thin silicon film of $80nm$ (or less) is usually used to integrate the FD SOI CMOS circuits. For ungated diodes, this thin Si film can otherwise be oxidized for the same thickness (by recessed LOCOS), if no active zone is needed over the diode area. In both cases, in a CMOS process, interdielectric and passivation oxides (with a total thickness of $750nm$ here) are deposited on the top of the structure and added to the gate oxide of $30nm$ and the buried oxide of $400nm$ where it is left.

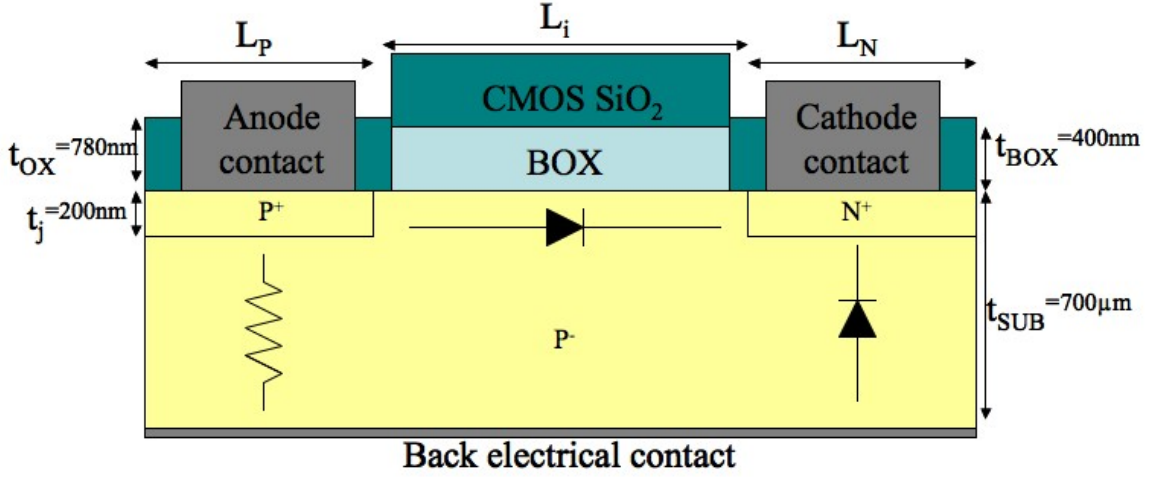


Figure 5.7: Schematic of the ungated solar cell in the SOI UCL substrate and the three electronic devices resulting of the fabrication.

5.5.2 Modeling

To model the PIN diode, a sketch of the device is presented in figure 5.8. As discussed previously, the depth of junction is of $t_j = 200nm$ but the depletion length whose formula was given in chapter 2 is of about $L_{ZD} = 1\mu m$. The depletion area surrounds thus the cathode of the solar cell and $L'_i = L_i - L_{ZD}$. Then, the electric field is concentrated in the depletion region around the N^+ region. The diode current equation is calculated using the minority carrier concentrations in the quasi-neutral regions as usual.

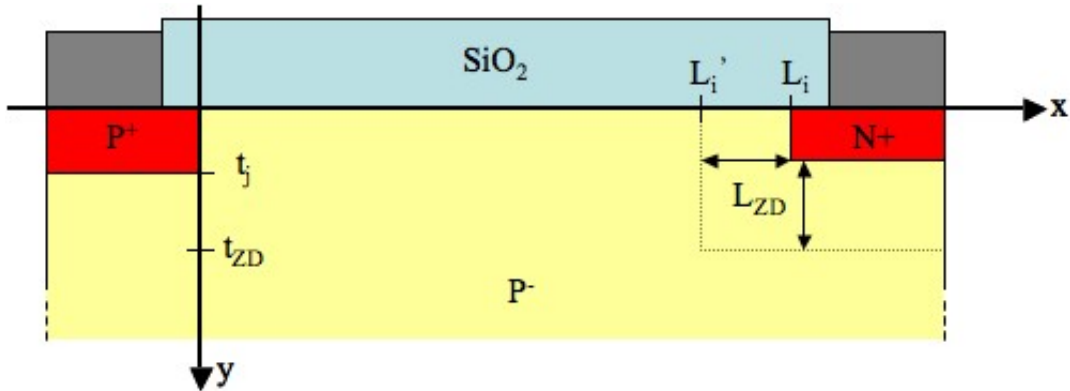


Figure 5.8: Lateral view of the ungated solar cell in the SOI substrate.

5.5.2.1 Dark characteristic

The dark characteristic of the diode is derived from classical transport equations but in two dimensions. However, when no generation is assumed, the carrier concentration is assumed constant in the y direction over a thickness of $t_{ZD} = t_j + L_{ZD}$. In a first point, the recombination is neglected in the depletion region and the hole current in the N^+ region is also neglected due to the weak number of carriers $p_{n,0}$. The total current due to diffusion is given by :

$$J_{D,diff} = J_{n,P-}(L'_i) + J_{p,N+}(L_i) \simeq J_{n,P-}(L'_i) + J_{p,N+}(L'_i) \simeq J_{n,P-}(L'_i), \quad (5.8)$$

where $J_{n,P-}(L'_i)$ is the minority carriers (electrons) density of current in the substrate at $x = L'_i$ and $J_{p,N+}(L'_i)$ is the minority carriers (holes) density of current in the cathode at $x = L'_i$.

The resolution of the transport equations is obtained with the boundary conditions $\Delta n(L'_i) = (e^{\frac{V_D}{V_T}} - 1)$ and $S = 0$ at $x = 0$ which implies $J_n(0) = 0$ [14]. We demonstrated the presence of a net charge of $Q_{BOX} = -10^{10} cm^{-2}$ in the oxide in the case of a gated structure. This can create a small depletion layer under the BOX and thus increase the real depletion length, i.e. decrease the value of L'_i in the above formula. Moreover, the solar cells are mostly biased with a middle forward voltage for which the recombination current in the depletion zone is not negligible and the high and low injection levels have to be taken into account. Then, the total dark current, as already explained in chapter 2, has a form given by :

$$J_{D,dark} = J_{S,1} \cdot (e^{\frac{V_D}{V_T}} - 1) + J_{S,2} \cdot (e^{\frac{V_D}{2 \cdot V_T}} - 1), \quad (5.9)$$

and $I_{D,dark} = J_{D,dark} \cdot A$ where $A = L_F \cdot t_j \cdot \zeta$, L_F being the length of one finger of the interdigitated diode and ζ is the volume amplification factor taking into account the three-dimensional volume current distribution.

Influence of DIT on the dark characteristic

We mentioned previously that the Si/SiO_2 interface below the buried oxide was contaminated during the smart-cut process. The resulting flatband voltage creates a depletion layer below the BOX at $V_{FG} = 0V$. The DIT will imply a surface recombination velocity for the carriers under the BOX. The total recombination current will then include the SRH recombination term and the surface charge recombination, at both high and low injection levels. The saturation currents of the diode can be estimated in equation 5.9 by :

$$J_{S,1} = q \cdot \left(\frac{D_n \cdot n_{0,P^-}}{L_n} + S \cdot n_{0,P^-} + \frac{L_{ZD} \cdot n_{0,P^-}}{2 \cdot \tau_{eff}} \right), \quad (5.10)$$

$$J_{S,2} = q \cdot \left(S \cdot n_i + \frac{L_{ZD} \cdot n_i}{2 \cdot \tau_{eff}} \right), \quad (5.11)$$

where the first term in equation 5.10 is the solution of equation 5.8. As for the lateral PIN diodes in the thin Si film, the effective lifetime can be extracted from dark current measurements [15]. The dark current being mostly dominated by surface generation/recombination and thermal volume SRH recombination, described by equation 5.11, it is easy to relate τ_{eff} to $I_{D,dark}$. Figure 5.9 illustrates the comparison between the measured and simulated dark current of the solar cell if $J_{S,1} \simeq 6 \times 10^{-10} A/cm^{-2}$ and $J_{S,2} \simeq 5 \times 10^{-6} A/cm^{-2}$. The second term, $J_{S,2}$, dominates the dark current but the slope of the first exponential term (below $V_D = 300mV$) is poorly put in evidence in the model for which the shift is at worse of 10 below $V_D = 100mV$. The effective lifetime is extracted to be $\tau_{eff} = 0.1\mu s$ from figure 5.9 and equation 5.11.

Other lifetime extraction techniques for solar cells are based on a pulse of light applied to the solar cell. The purpose is then to measure the extinction of photocurrent, i.e. the decay of the carriers, related to the lifetime. Those methods include the photo-conductivity decay and the open-circuit voltage decay [13]. However the decay-based techniques are really efficient when the diffusion length of the carriers is longer than the anode-to-cathode distance, i.e. for a short base solar cell, which is not our case.

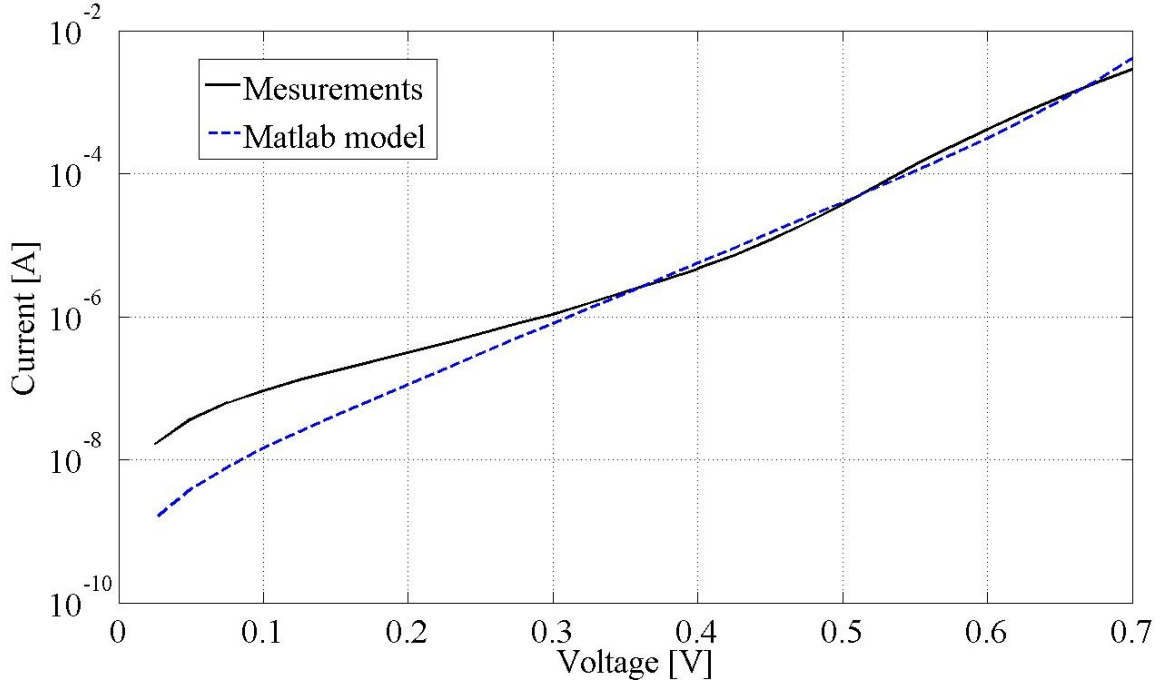


Figure 5.9: Comparison of the measured (continuous line) and simulated dark currents (dashed line) of the ungated solar cell.

5.5.2.2 Illuminated characteristic

The illuminated characteristic of a lateral photodiode have been investigated within a two-dimensional model in [16]. It has been showed in chapter 1 that the generation rate follows a Beer-Lambert law decreasing along y :

$$G(y, \lambda) = \alpha \cdot \Phi_0 \cdot e^{-\alpha y}, \quad (5.12)$$

where α is the absorption coefficient of the material (Si) and Φ_0 is the incident photon flux at the beginning of the silicon.

Then, when considering the minority carriers in the quasi-intrinsic region, we can assume that it also follows a decrease along y :

$$\Delta n(x, y) = n(x, y) - n_0 = f(x)e^{-\alpha y}. \quad (5.13)$$

The diffusion equation becomes

$$\frac{\partial^2 f(x)}{\partial x^2} + \left(\alpha^2 - \frac{1}{L_n^2} \right) f(x) + \frac{\alpha \Phi_0}{D_n} = 0, \quad (5.14)$$

for which $f(x)$ is a solution depending if the product $(\alpha \times L_n)$ is superior, inferior or equal to 1. The value $\alpha = \frac{1}{L_n}$ also corresponds to a precise wavelength in silicon. For example if the lifetime of carriers is assumed to be $\tau = 0.1\mu s$ in P^- , then the value corresponds to $\lambda = 840nm$.

The photocurrent term is then obtained by derivation of $\Delta n(x, y)$ along x . However, as demonstrated in the paper, three currents are obtained according to the wavelength. In our case, all currents resulting from a wavelength $\lambda \leq 840nm$ are described by an oscillating equation implying an abnormal behavior for this situation. The problem may come from invalid geometrical limits for the resolution of the equation : indeed, the limit conditions are taken at the edge of the junction depth while the light is penetrating far beyond this depth in the semiconductor.

New interpretation of the photocurrent

However, the usual expressions for analytical photocurrent expression are often difficult to obtain in more complex structure and present the disadvantage to be only valid down to a thickness of t_{ZD} . It may be thus more convenient to derive the photocurrent from geometrical analysis. Indeed, the photocurrent consists in the electron-hole pairs generated in the depletion zone and those within a distance less or equal to the diffusion length so that they would be able to reach this depletion area and be accelerated by the electric field of the diode. We can then use the equation 5.3 which has to be integrated down to a depth of $t_{ZD} + L_n$ so that the generation takes into account the electron-hole pairs generated in the depletion layer and those able to reach the depletion region (i.e. with diffusion length less or equal to L_n).

For example, in our photodiodes with an effective lifetime of $\tau_{eff} = 0.1\mu s$ (i.e. $L_n = 18\mu m$), an intrinsic length of $L_i = 34\mu m$ and a width of $500\mu m$, the generated

calculated photocurrent is of $95\mu A$ for a standardized $AM1.5$ solar spectrum with irradiance of $1000W/m^2$. This value takes also into account the carriers generated outside the diode area within a distance less or equal to L_n and the photosensitive area does not include all the metal interconnections. Another hypothesis is that with a supposed equilibrium $0V$ potential on the top of the oxide, the intrinsic region under the BOX/substrate interface is in depletion. The measurements gave a short-circuit current of $98\mu A$. This close result demonstrates the method and the slight difference probably comes from the calculation of the diffusion length.

5.5.3 Characterization

Photoelectric characterization of the solar cells shows a poor responsivity as light sensors, contrarily to the thin film UV FD SOI diodes of the same wafer [17]. Indeed, the responsivity exhibits a flat response along the visible wavelength range with values around $R = 10^{-3}A/W$. The main explanation is that the difference between the total and the dark currents is not significant in reverse mode. This implies poor values of the responsivity as recalled by equation 1.14 and can be explained by two reasons. First, during reverse operation, the dark current is dominated by generation and yields values around $I_{D,Dark} = -0.5\mu A$ for $V_D = -0.5V$. This is much higher than lateral PIN diodes in the thin Si film, which can be mostly explained due to the higher thickness of the silicon substrate. Secondly, the contribution of each monochromatic light used during the responsivity characterization only implies currents comprised between $0.8\mu A$ and $4\mu A$ according to the different wavelengths. The dark and total current ranging in the same order of magnitude, for the small light power densities, the responsivity is thus weak.

Photovoltaic analysis has been carried out, yielding excellent results. The diodes were illuminated, perpendicularly, by an Oriel solar simulator featuring the reference $AM1.5$ spectrum for terrestrial PV cells for three different light power densities of $1000W/m^2$, $500W/m^2$ and $100W/m^2$ while the electrical characterization has been made with a HP4145 analyzer. The current versus voltage and power versus voltage

curves summarizing those measurements are plotted in figures 5.10 and 5.11 respectively.

During this characterization, the backgate was left floating. Similar results were

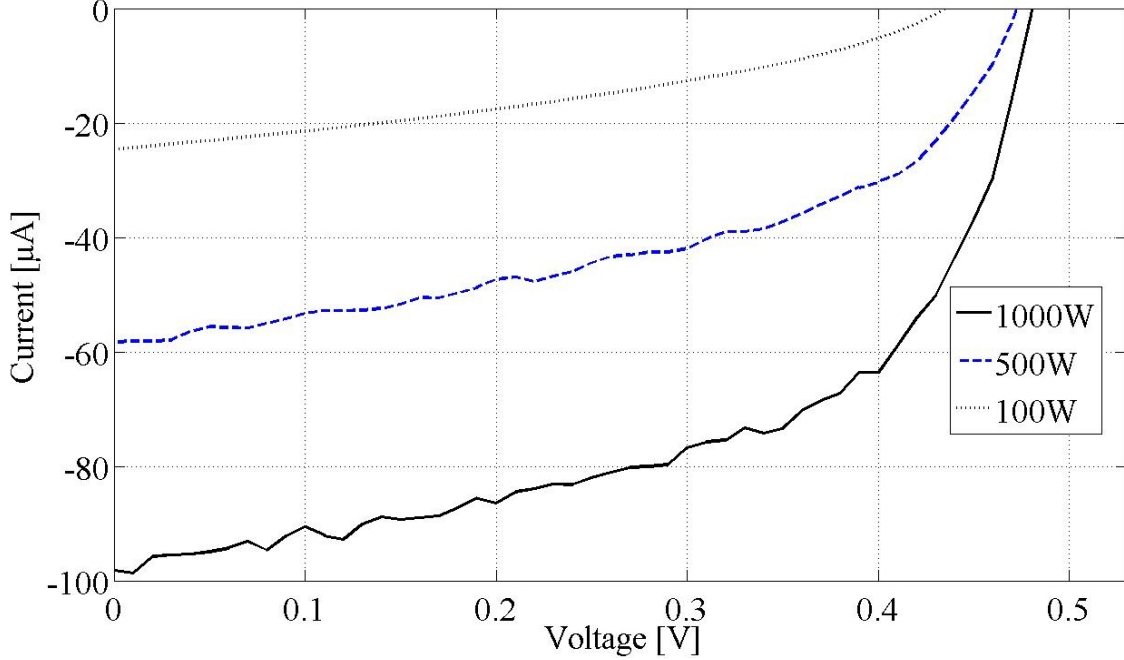


Figure 5.10: Measured I-V curves of lateral PIN diodes implanted in the substrate with $L_i = 34\mu m$, $L_N = L_P = 10\mu m$, and $L_F = 500\mu m$. The light power densities were of $1000W/m^2$ (solid line), $500W/m^2$ (dashed line) and $100W/m^2$ (dotted line) for AM1.5 solar spectrum.

however obtained when short-circuiting the P^+/P^- resistor. As mentioned before, the short-circuit current for a $1000W/m^2$ illumination was measured to be $98\mu A$. However, values corresponding to the lower illuminations were of $59\mu A$ and $24.5\mu A$ for the irradiances of $500W/m^2$ and $100W/m^2$ respectively. The ratio of power is thus not respected at lower light power densities. For example, between 1000 and $500W/m^2$, the I_{SC} ratio should be 2 and it should be of 10 with the $100W/m^2$ condition according to equation 5.3. Instead of these ideal values, the measured ratios are of 1.69 and 4 respectively, i.e. the photocurrents are too large with regards to the theoretical thermodynamic limits. This imply another phenomenon not taken into account in the previous predictions, and discussed in the analysis hereafter. Another remark is the varying behavior of the current at irradiances of $500W/m^2$ and

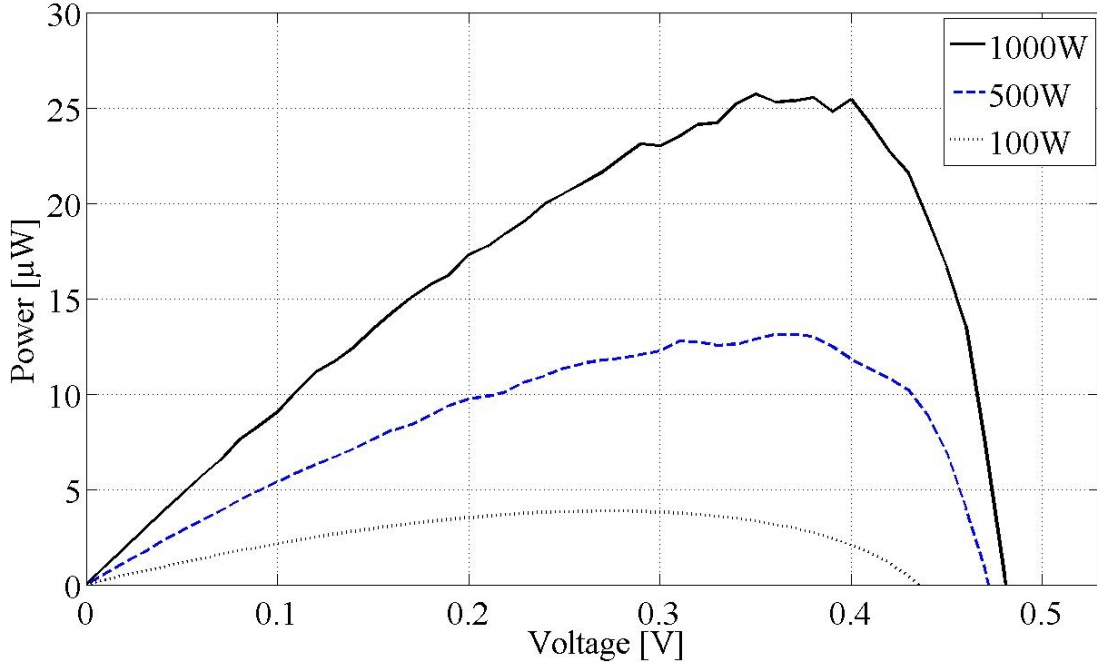


Figure 5.11: Measured P-V curves of lateral PIN diodes implanted in the substrate with $L_i = 34\mu m$, $L_N = L_P = 10\mu m$, and $L_F = 500\mu m$. The light power densities were of $1000W/m^2$ (solid line), $500W/m^2$ (dashed line) and $100W/m^2$ (dotted line) for AM1.5 solar spectrum.

$1000W/m^2$ contrarily to the smoother curve at $100W/m^2$ which can be explained by the larger variation of the irradiance of the Xenon lamp at high driving currents (i.e. 40A) of the Solar simulator.

The parameters of the solar cell as defined at the beginning of the chapter were extracted from measurements and are listed in the table 5.1. Several observations

Irradiance [W/m^2]	$I_{SC}[\mu A]$	$V_{OC}[mV]$	$FF[\%]$	$\eta[\%]$
1000	98	482	54.3	10.3
500	58	472	47.6	10.5
100	25	436	36	15.5

Table 5.1: Performance of the measured ungated solar cells.

can be made with the values of the table concerning the values related to the light power.

First of all, the decrease of current is normal even if the corresponding values do not correspond with the literature as discussed above. An attempt of explanation is given at the end of the section. The open-circuit voltage decrease is as predicted

by the literature and can also be explained by a light power decrease. The decrease of the fill factor is logically due to the drastic reduction of I_{SC} current compared to a slow decrease of V_{OC} . Finally, the increase of the efficiency is due to the slowest decrease of I_{SC} with regards to the decrease of power.

5.5.4 Parameters extraction

Temperature

As an irradiance of $1000W/m^2$ illuminates the diodes, it is logically supposed that heat losses will occur in solar cells, as already predicted and verified in the literature [18, 19, 20]. To measure the temperature reached in the wafer under illumination, the solar cells have been previously characterized in the dark. It is known that the voltage under a constant current yields a shift of about $-2mV/K$. Then, by applying a constant forward current at different temperatures, it is possible to calibrate the diode deviance and hence obtain a temperature sensor. Concerning our measurements, different temperatures ranging from 293 to $348K$ were applied to the backside with the thermal controlled chuck of the probe station while a constant $5\mu A$ forward current was flowing through the solar cell. The measured forward voltage allows us for plotting the temperature versus voltage graph of the solar cell showed in figure 5.12. Under the illumination of $1000W/m^2$, a voltage of $338mV$ was measured for the same $5\mu A$ forward current : this corresponds to a temperature of $320K$.

Atlas comparison and surface recombination extraction

Simulations were carried out with Atlas and the module Luminous. The models used to simulate the solar cells were : a concentration and temperature dependent mobility (*ANALYTIC*), a parallel field dependent mobility (*FLDMOB*), a Shockley-Read-Hall (SRH) concentration-dependent lifetime model (*CONSRH*), the Auger recombination (*AUGER*), the band-to-band tunneling (*BBT.STD*), the Klaassen model for bandgap narrowing (*BGN.KLAASSEN*), self-heating simulation (*HEAT.FULL*)

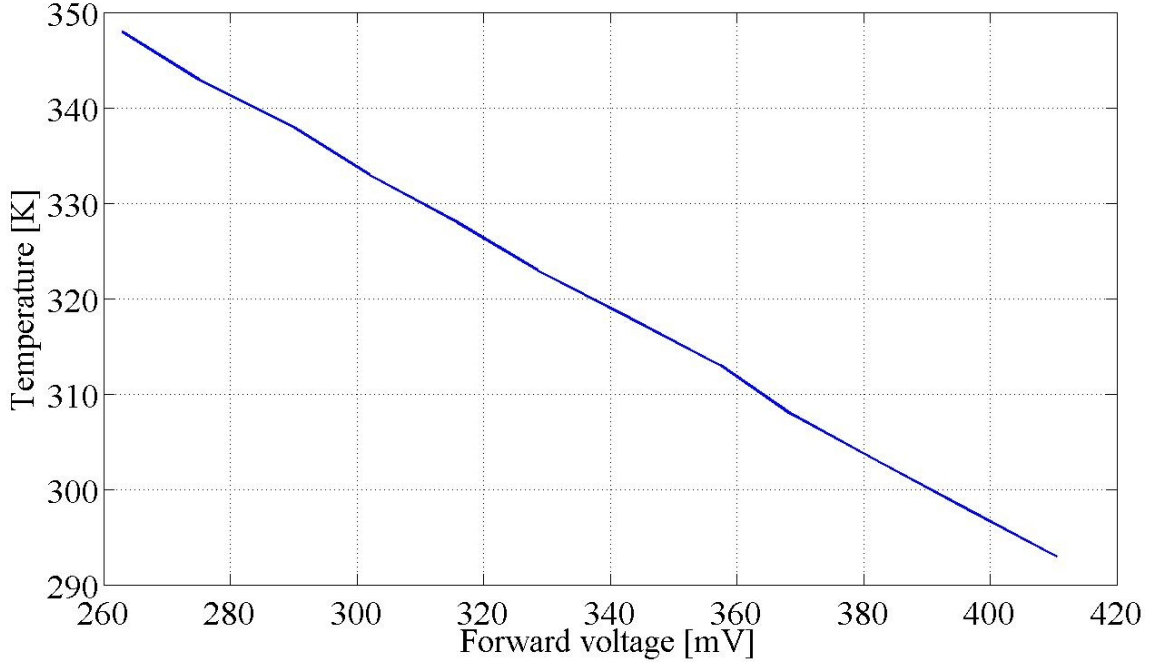


Figure 5.12: Temperature versus forward voltage relation of a lateral ungated PIN diode with forward current of $5\mu A$.

and the impact ionization according to the Selberrherr model (*SELB*), tuned for our SOI technology.

The BOX/substrate interface was parametrized with a surface density of charge $Q_F = -10^{10} cm^{-2}$ (to implement the value of Q_{BOX}) and surface recombination velocities for both carriers of $S = 2.5 \times 10^3 cm/s$ to fit the open-circuit voltage of $482 mV$ at $1000 W/m^2$. Based on equation 5.7, the equivalent capture cross section is of $\sigma_{eq} = 1.5 \times 10^{-17} cm^2$. Values of the fitting parameter σ_{eq} for SOI technologies were comprised between 5×10^{-18} and $4 \times 10^{-17} cm^2$ in [8] which confirms thus the possible explanation of the phenomenon.

We choose to compare the P-V curves because the short-circuit currents are different between simulation and measurements. Indeed, a single finger was simulated in Atlas. Thus, simulations do not take into account the generation outside the solar cell finger within a diffusion length distance for example. The comparison of P-V measured and simulated curves at $T = 320 K$ for an irradiation of $1000 W/m^2$ with an *AM1.5G* solar spectrum is presented in figure 5.13.

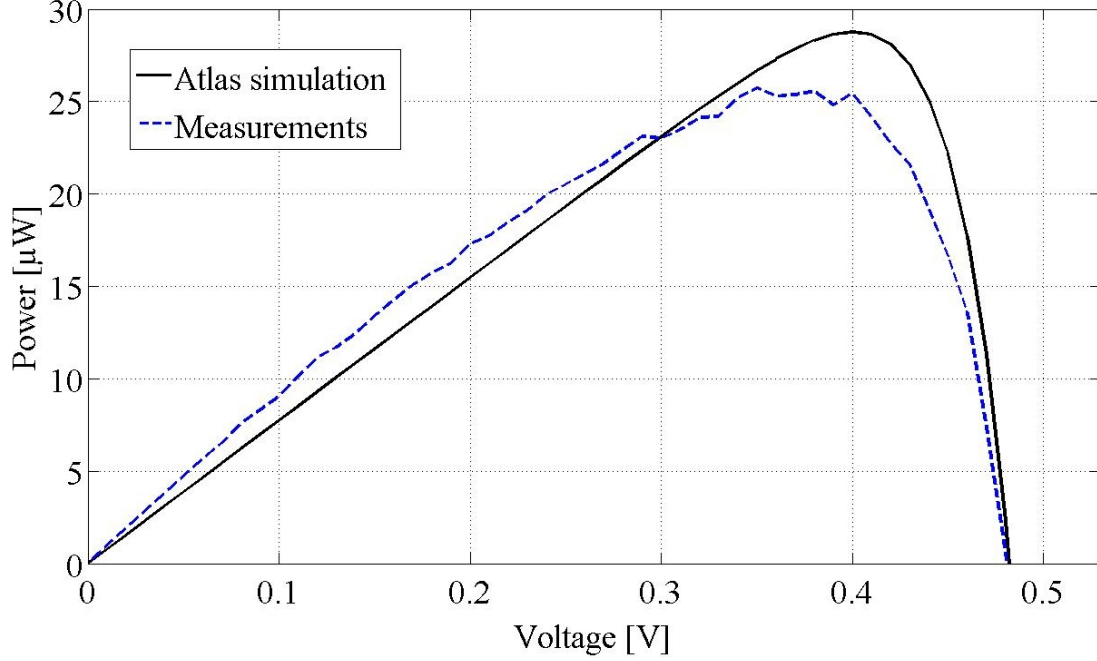


Figure 5.13: P-V simulated (continuous line) and measured (dashed line) curves at $T = 320K$ for an irradiation of $1000W/m^2$. The measured solar cell features the following dimensions: $L_i = 34\mu m$, $L_N = L_P = 10\mu m$, and $L_F = 500\mu m$.

Even if the curves have similar shape, differences occur between simulation and measurements for different reasons. Like explained here above, the short-circuit current is slightly different from simulation to measurements, i.e. $I_{SC} = 77.6\mu A$ in Atlas compared to $I_{SC} = 95\mu A$ in measurements. Secondly, the Atlas simulation is based on one finger of interdigitated solar cell. Thus, the series resistance which is mostly composed of fingers and the metal lines is underestimated. Concerning the figures of merit, the efficiency is 11.6% with Atlas simulations while it was 10.3% during the characterization, thus a slight difference of only 1.3%. Similarly, the fill factor is 63.3% in Atlas simulations and 54.3% in measurements which corroborates our hypothesis due to incomplete value of the real resistances.

Similar observations can be made for the lower irradiances but the differences increase due to the photocurrent estimation. Indeed, we mentioned previously an abnormal to high value of the measured photocurrent at $500W/m^2$ and $100W/m^2$.

The impact ionization model was activated in Atlas but does not reveal the phenomenon. This can be due to a particular mesh of the structure for ionization impact simulation. Indeed, in order to obtain convergence for the electrical characteristic under illumination, the grid space has to be increased. This may cause the mesh to be inadequate for taking into account the impact ionization at the junctions where the electric field is though in the order of magnitude of $10^6 V/m$.

To conclude this analysis, the ungated solar cell cannot be fully described with a Matlab or Atlas approach : both simulations must be used in parallel. A circuit modeling may be an asset and will be described later in this chapter.

5.6 Gated Lateral PIN Diode

5.6.1 Design and fabrication

For this second kind of device, the solar cell is embedded under an active region of the SOI wafer. The thin silicon film is thus superposed over the intrinsic zone of the solar cell. The anode and cathode regions of the solar cell are implanted during the same step as the source and drain regions of the active circuitry of the thin silicon film. Then, the process continues like a standard CMOS process.

It has been introduced that thin silicon film can be used as a gate to modulate the charges in the intrinsic region of the solar cell. To realize this gate, a lateral PIN diode was fabricated. The device in the thin film behaves optically like the UV sensors described in the second chapter. To distinguish both lateral photodiodes in this section, we will refer to the lateral PIN photodiode in the substrate as the *solar cell* while the lateral PIN photodiode in the thin film is the *UV photodiode*.

Since the thickness of the film is not large, i.e. $80nm$, only a small part of the light is absorbed in it, leaving the greatest part of energy being absorbed by the solar cell in the substrate. As a matter of bias, the UV photodiode is short-circuited to apply a constant bias on the frontgate. As a matter of design, the N^+ and P^+ regions of the UV photodiode have to be the smallest as possible, since as they are

covered with metal, they reflect light and thus reduce the photosensitive area of the solar cell.

5.6.2 Modeling

When the photodiode is fabricated under an active area, the thin silicon film lies above the buried oxide. This may absorb a part of light (constituted mostly of UV and blue light as demonstrated in chapter 2) and then reduce the efficiency of the photodiode. However by applying a voltage on this front gate, it is possible to modulate the space charge below the BOX. Indeed, like in classical MOS capacitor, a negative voltage will create an accumulation layer of holes while a large positive gate voltage will induce an inversion layer. A depletion layer occurs when the gate voltage is null or slightly positive as demonstrated during the C-V characterization.

A two-dimensional schematic of one gated solar cell is presented in figure 5.14. Due to design rule convenience, the minimal distance between the electrodes of the

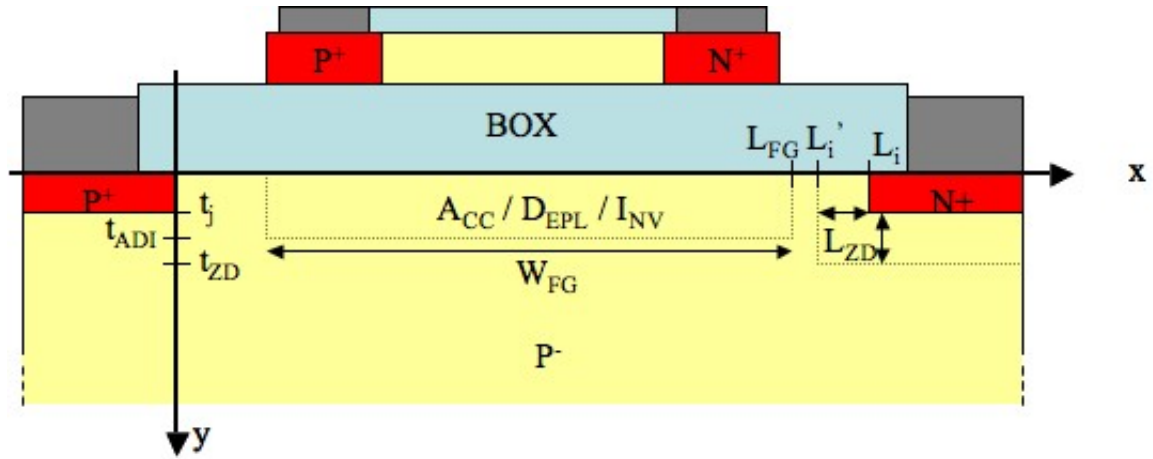


Figure 5.14: Schematic of the gated solar cell in SOI substrate.

two different devices is $6\mu m$. The depletion region is still present around the cathode while a charge area is located below the BOX interface. The width of the charge region induced by the front gate is denoted W_{FG} and its thickness is $t_{A,D,I}$ according to the accumulation, depletion or inversion layer. When modeling the photocurrent of the ungated solar cell, it was demonstrated that a geometrical analysis was more

The photocurrent is then the integration of the generation term on the quarter-circle surface with radius $r = L_n + L_{ZD}$ as described by :

$$I_{ph,\lambda} = q \cdot G_0(\lambda) \cdot L_F \cdot \int_0^{L_n+L_{ZD}} \int_0^{f(x)} e^{-\alpha \cdot y} dy dx, \quad (5.15)$$

where $f(x) = L_n \sin\left(\arccos\left(\frac{x-L_n}{L_n}\right)\right)$ is the function describing the quarter-circle in which the generation term is integrated. This equation must be resolved by numerical simulation due to integration of the function $f(x)$. For a solar cell with a supposed effective lifetime of $\tau_{eff} = 0.1\mu s$ (i.e. $L_n = 18\mu m$), an intrinsic length of $L_i = 34\mu m$ and a width of $500\mu m$, the photocurrent under an irradiance of $1000W/m^2$ is estimated at $32.5\mu A$ while it has been measured at $37\mu A$ when a negative frontgate of $-10V$ was applied. This estimation takes into account the real photosensitive area of the solar cell, including the generation outside the solar cell at a distance of L_n and considering the reflections due to metal lines of the solar cell and the UV diode and the absorption in the thin film. As for the ungated solar cell, there is a slight underestimation, probably due to the simplicity of our geometrical approach and the estimation of the diffusion length.

Depletion

When no voltage is applied on the frontgate, the solar cell interface with the BOX is in depletion everywhere below the frontgate. This bring us to a geometrical model identical to the ungated diode : a depletion layer is under the BOX and the absorption term has to be vertically integrated along the photosensitive area at a distance $L_{ZD} + L_n$. The presence of the thin silicon film and the metal lines of the UV diodes reduces the $95\mu A$ short-circuit of the ungated by a factor 1.55 for the gated case, i.e. $I_{SC} = 57\mu A$ with the geometrical model. The measurements were of $I_{SC} = 63\mu A$, thus a ratio of 1.62 was observed compared to the $98\mu A$ measured in the ungated case.

Inversion

The inversion case is more complicated when using a geometrical approach. Indeed, as a first point of view, the inversion layer simply increases the width of the N^+ region, then the photocurrent would be the same as in depletion mode. But in measurements the photocurrent straightly rises up to values of $140\mu A$ for a $+50V$ frontgate voltage. Even if the thickness of the inversion layer increases, the main possible reason would be a reduction of the surface recombination velocity S at the interface. Another reason could be an impact ionization phenomenon due to high electric field of $5 \times 10^7 V/m$ if $V_{FG} = 50V$. However, this phenomenon is too difficult to be only described by a geometrical model and the Atlas simulation does not seem able to put it in evidence.

5.6.3 Characterization

The gated solar cells were characterized under the Oriel solar simulator with $AM1.5G$ terrestrial spectrum and irradiances of 100, 500 and $1000W/m^2$ like for the ungated solar cell measurements. The front gate was biased with the backgate as a ground reference, and the anode of the solar cell was grounded too. Figures 5.16 and 5.17 show the I-V and P-V curves of the gated solar cells for a front gate voltage of $+5V$ since it has been showed that a $0V$ voltage would be near the edge of the three modes.

A similar behavior as the ungated solar cells can be observed in those figures. Finally, the evolution of the measured fill factor and efficiency of the solar cell under solar illumination of $1000W/m^2$ are presented in figure 5.18.

Analysis

Concerning the I-V and P-V curves, some observations identical to the case of the ungated solar cells can be made. The efficiency is at its best for the lowest solar irradiances. A record efficiency of 22% is even achieved for a $50V$ front gate voltage at $100W/m^2$. The open-circuit voltage is logically decreasing with light power as for

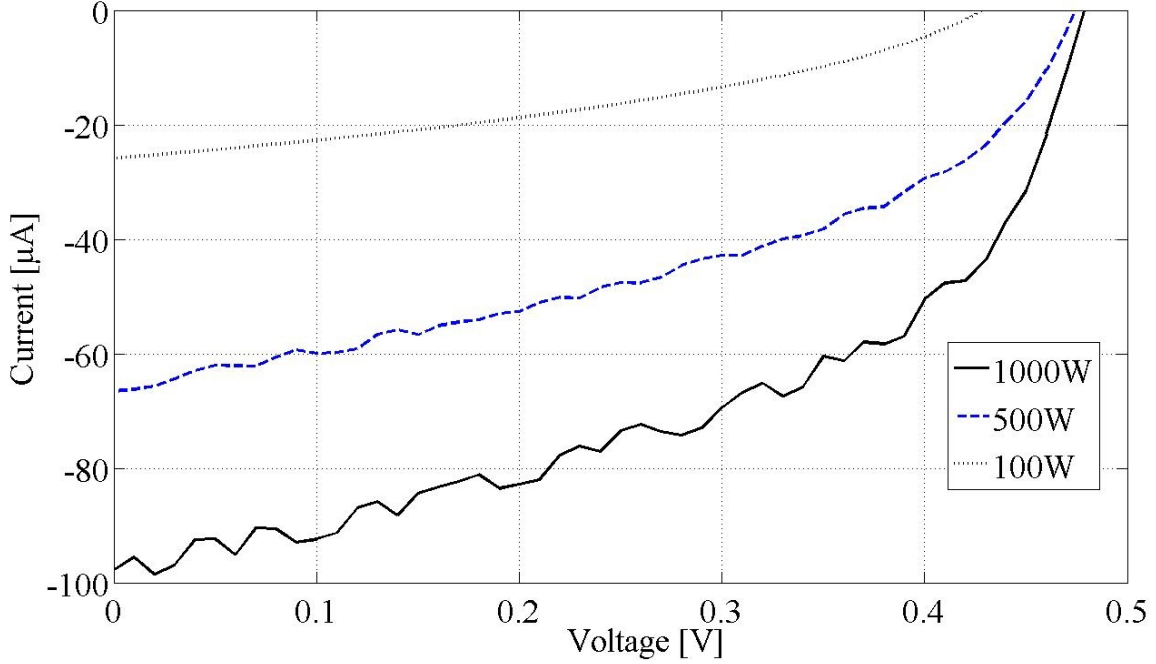


Figure 5.16: Measured I-V curves of lateral PIN diodes implanted in the substrate with $V_{FG} = +5V$. For the solar cell, $L_i = 34\mu m$, $L_N = L_P = 10\mu m$, and $L_F = 500\mu m$. For the UV diode, $L_i = 10\mu m$, $L_N = L_P = 10\mu m$, and $L_F = 500\mu m$. The light power densities were of $1000W/m^2$ (solid line), $500W/m^2$ (dashed line) and $100W/m^2$ (dotted line) for AM1.5 solar spectrum.

the short-circuit current.

It can be seen that fill factor and efficiency evolve oppositely with the front gate voltage. Indeed, the efficiency is increasing with the front gate voltage and the fill factor is straightly decreasing to reach very poor values as soon as $V_{FG} = 0V$. This can be explained in particular by the rise of current with the frontgate voltage increase. The loss voltage on the series resistances is then high enough and the fill factor reaches the same values as for the ungated solar cell.

The table 5.2 summarizes the main parameters of the gated solar cells for front gate voltages of 0 and $+5V$.

5.7 Equivalent Circuit Model

The solar cell being often connected to circuitry for maximum power point tracking or energy harvesting, a circuit equivalent model is needed to simulate the behavior

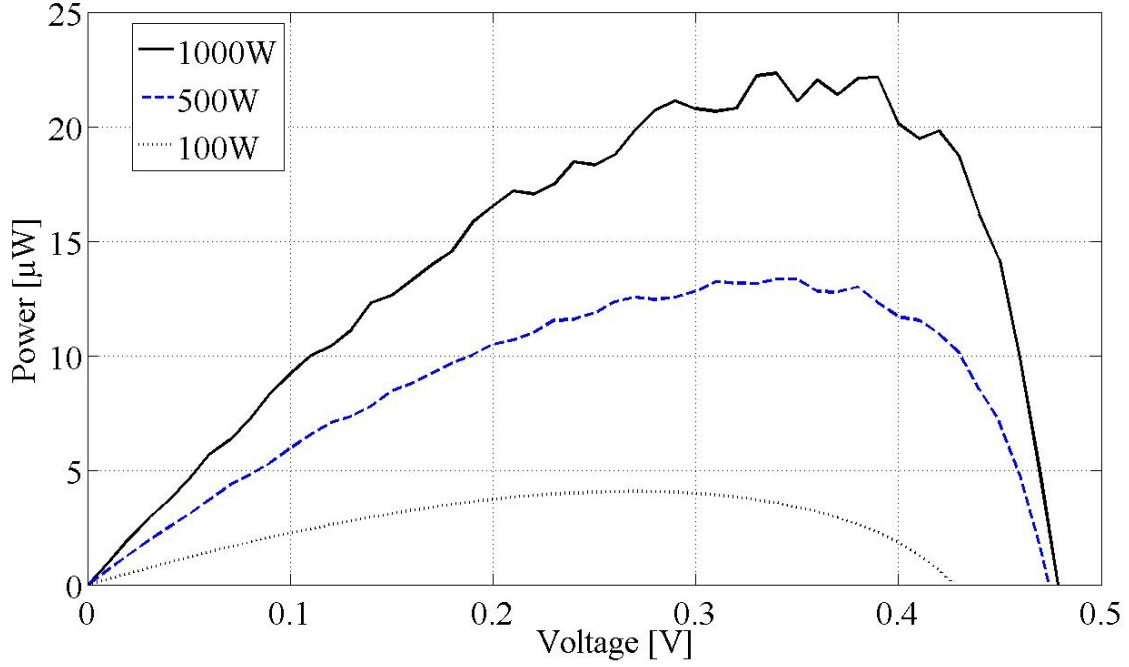


Figure 5.17: Measured P-V curves of lateral PIN diodes implanted in the substrate with $V_{FG} = +5V$. For the solar cell, $L_i = 34\mu m$, $L_N = L_P = 10\mu m$, and $L_F = 500\mu m$. For the UV diode, $L_i = 10\mu m$, $L_N = L_P = 10\mu m$, and $L_F = 500\mu m$. The light power densities were of $1000W/m^2$ (solid line), $500W/m^2$ (dashed line) and $100W/m^2$ (dotted line) for AM1.5 solar spectrum.

of the complete system. The most used model consists in a current source corresponding to the photocurrent I_{Ph} , two diodes modeling the dark characteristic of the solar cell (for Shockley-Read-Hall and space charge region recombination mechanisms at low and high injection levels), a parallel resistance R_P which represents the edge effects and surface recombination losses and finally a series resistance R_S corresponding to the resistance of the fingers and metal layers. The multi-diodes model can even be extended to six diodes according to different recombination mechanisms occurring in the diode, but a two-diodes model is sufficient for low open-circuit voltages and Si solar cells. A third diode can be used for Auger recombination mechanism [13], but it is mostly used for LED modeling.

The circuit equivalent is showed in figure 5.19. The two diodes have ideal factor of $n = 1$ and saturation current $I_{S,1}$ for diode $D1$ which holds for SRH and surface recombination at low injection and of $n = 2$ and $I_{S,2}$ for diode $D2$ which

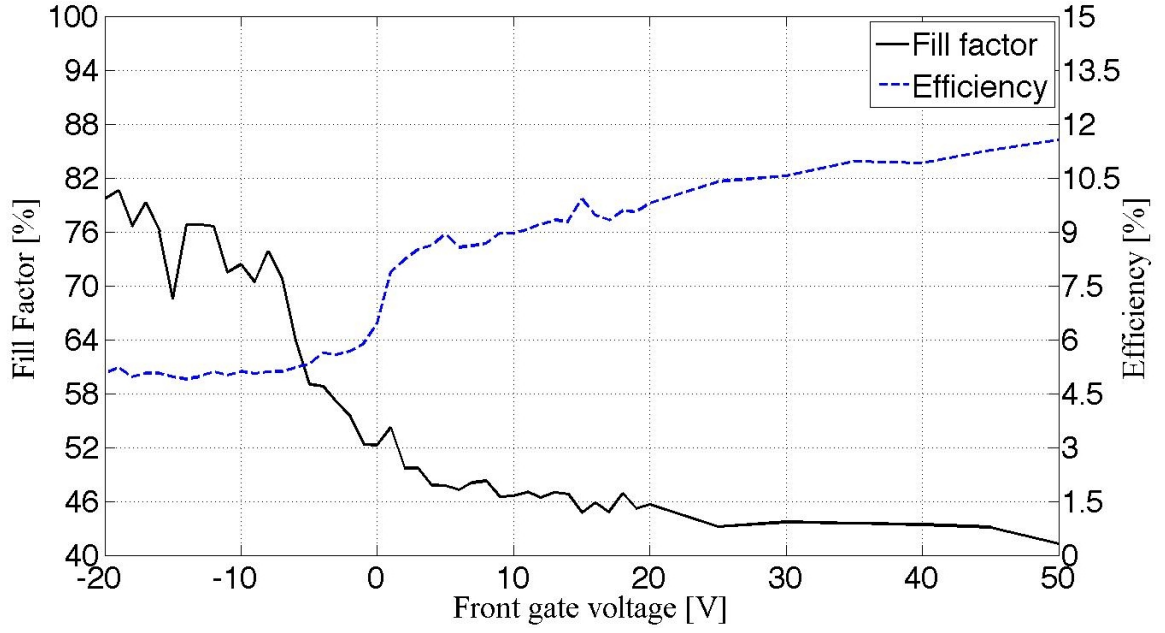


Figure 5.18: Evolution of the gated solar cells efficiency and fill factor as a function of the Si thin-film bias referred to back side at $1000\text{W}/\text{m}^2$. For the solar cell, $L_i = 34\mu\text{m}$, $L_N = L_P = 10\mu\text{m}$, and $L_F = 500\mu\text{m}$. For the UV diode, $L_i = 10\mu\text{m}$, $L_N = L_P = 10\mu\text{m}$, and $L_F = 500\mu\text{m}$.

Irradiance [W/m^2]	$V_{FG}[\text{V}]$	$I_{sc}[\mu\text{A}]$	$V_{oc}[\text{V}]$	$FF[\%]$	$\eta[\%]$
1000	0	63	491	52.3	6.5
500	0	47	470	45.9	8.2
100	0	19	432	35.3	11.5
1000	5	98	479	47.7	8.9
500	5	66	475	42.3	10.7
100	5	26	428	37.8	16.4

Table 5.2: Performance comparison of the gated solar cells.

represents the same recombination mechanisms at higher injection. The values of R_P and R_S must be compared to the characteristic resistance of the solar cell R_C defined by the ratio $\frac{V_{oc}}{I_{sc}}$. In order to have a high FF value, the values of R_S and R_P must be significantly small and high compared to R_C respectively to avoid losses [18].

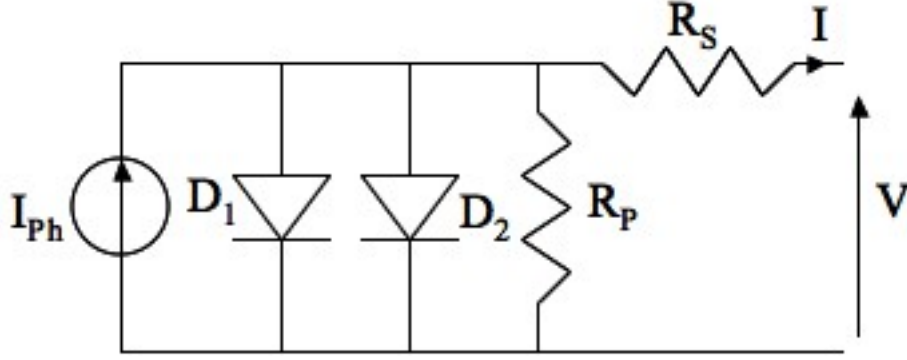


Figure 5.19: Equivalent circuit model of a solar cell with two-diodes implementation.

The equation of the current defined as positive when flowing out of the solar cell is :

$$I(V) = I_{Ph} - \left[I_{S,1} \cdot \left(e^{\frac{V+I \cdot R_S}{V_T}} - 1 \right) + I_{S,2} \cdot \left(e^{\frac{V+I \cdot R_S}{2 \cdot V_T}} - 1 \right) + \left(\frac{V + I \cdot R_S}{R_P} \right) \right]. \quad (5.16)$$

The resolution of this equation is made numerically but some of the unknowns can be pre-estimated. At the open-circuit point, the measured current is $I = 0$ for which $V = V_{OC}$. We can then express I_{Ph} in equation 5.16 by :

$$I_{Ph} = I_{S,1} \cdot \left(e^{\frac{V_{CO}}{V_T}} - 1 \right) + I_{S,2} \cdot \left(e^{\frac{V_{CO}}{2 \cdot V_T}} - 1 \right) + \frac{V_{CO}}{R_P}. \quad (5.17)$$

The saturation currents can be estimated by equations 5.10 and 5.11 which will constitute an initial condition for the resolution of equation 5.16. The series resistance is the sum of the resistance of the metal lines and of the fingers which dominates this term. Nevertheless, the metal lines resistance has been estimated to 25Ω while the finger resistance is more complicated to calculate due to the non-uniform distribution of the current in the structure. The resolution of the system leaving a minimal error between the modeling and the experimental curves gives the following values for the ungated solar cell and the gated solar cell with $V_{FG} = 5V$ at $1000W/m^2$, $500W/m^2$ and $100W/m^2$: $I_{S1} \simeq 3 \times 10^{-13}A$, $I_{S2} \simeq 6.7 \times 10^{-10}A$ and $R_S \simeq 250\Omega$. Concerning the series resistance, its value is dominated by the finger resistance but due to the microcurrents of the solar cells, the voltage loss in it is almost negligible.

The figure 5.20 illustrates the comparison between the extracted and the measured I-V curves for the three irradiances.

The values of the parallel resistance are very variable and are listed in table

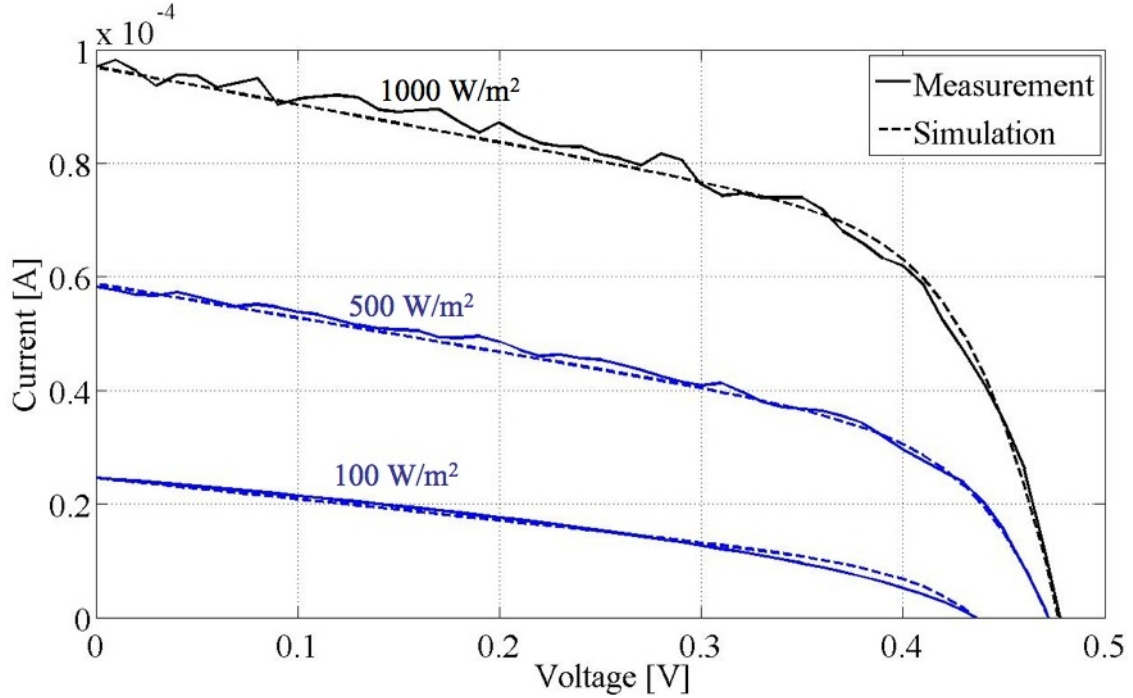


Figure 5.20: Comparison of the measured (continuous line) and extracted I-V curves (dashed line) of the ungated solar cell for irradiances of $1000\text{W}/\text{m}^2$, $500\text{W}/\text{m}^2$ and $100\text{W}/\text{m}^2$.

5.3 for the ungated solar cell and the gated solar cell with frontgate voltages of 0 and 5V along with the characteristic resistance R_C . We presented in figure 5.18 the evolution of the fill factor and the efficiency of the gated solar cell as a function of its frontgate voltage. The fill factor was decreasing when the frontgate voltage was increasing. This phenomenon can be explained by surface conditions changes and thus a decrease of the parallel resistance. The extraction of the parallel resistance of the measurement I-V curves of the gated solar cell gave parallel resistance values which are plotted in figure 5.21 along with the fill factor evolution. The poor fill factor results can thus be explained in particular with the slow values of the parallel resistance which are in the same order of magnitude as the characteristic of R_C as can be seen in table 5.3. By increasing the frontgate voltage, the parallel resistance

Solar cell type	Irradiance [W/m^2]	$R_P[k\Omega]$	$R_C[k\Omega]$
Ungated	1000	14.8	4.9
Ungated	500	16.5	8
Ungated	100	26.5	17.5
Gated and $V_{FG} = 0V$	1000	20	7.8
Gated and $V_{FG} = 0V$	500	19.5	10
Gated and $V_{FG} = 0V$	100	30.5	22
Gated and $V_{FG} = 5V$	1000	10	4.9
Gated and $V_{FG} = 5V$	500	12	7.2
Gated and $V_{FG} = 5V$	100	22.5	16.5

Table 5.3: Extracted parallel resistance and characteristic resistances of equivalent circuit modeling for the SOI ungated and gated solar cells at $V_{FG} = 0V$ and $V_{FG} = 5V$ under an irradiance of $1000W/m^2$.

decreases quickly from $V_{FG} = 5V$ and reaches value of $10k\Omega$ or less while the characteristic resistance is just twice times smaller. This can explain the decrease of the fill factor.

5.8 Comparison with Other Technologies and Improvements

5.8.1 Comparison

Solar cells have been fabricated for many years and record of efficiencies have been achieved in various technologies. The table summarizes the efficiencies of different silicon technologies and other semiconductor and organic technologies in the table 5.4. The table lists the top efficiencies of industrial process and the efficiencies achieved by CMOS compatible process. We achieve results comparable with other CMOS SOI technology and industrial amorphous silicon even if the efficiencies are well below results of classical industrial Si solar cells.

Moreover, under indoor illumination, i.e. $100W/m^2$, the solar cells feature higher efficiencies. For example, our photodiodes reach an efficiency of 15.5% and 22% for ungated and gated (with $V_{FG} = 50V$) solar cells respectively. The benefit for indoor daily use is indisputable.

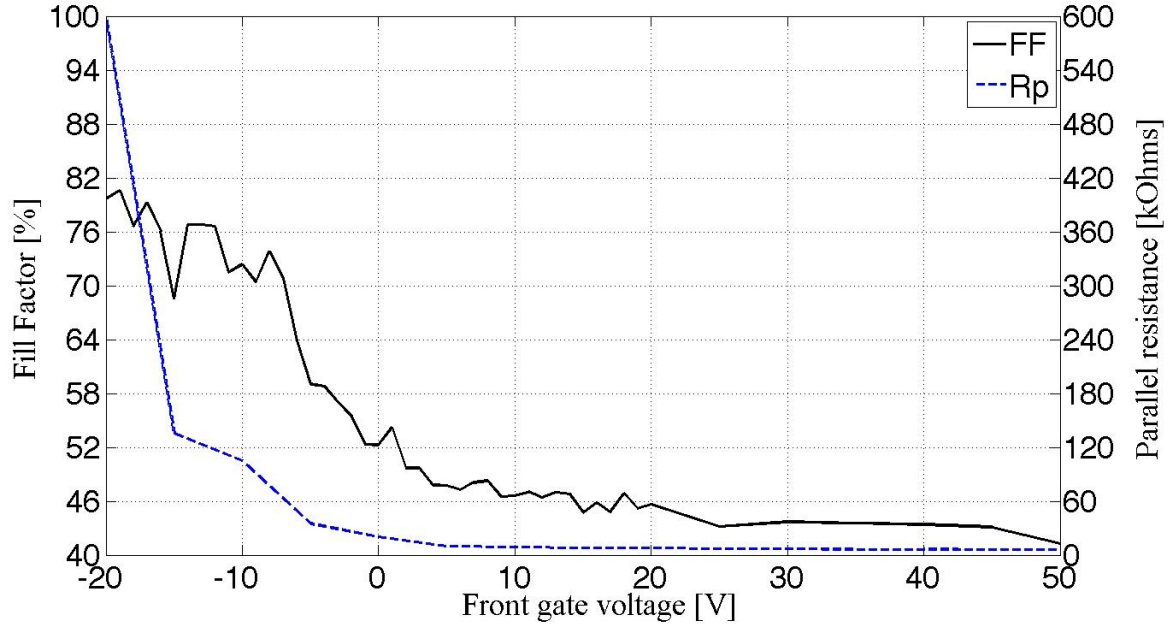


Figure 5.21: Evolution of the measured fill factor and the extracted parallel resistance for the gated solar cell as a function of the frontgate voltage.

5.8.2 Improvements

As it has been shown here above, SOI solar cells have great potential but still suffer from poor fill factor which decreases the efficiency drastically. This is mainly due to the bad BOX/substrate interface. Particularly, in our first design, the parasitic resistances are not negligible, as it can be deduced from the low fill factor.

The fabrication process could also be improved to approach the state of the art efficiency limit of 25% in c-Si. A first step is to improve the silicon quality which imply a higher lifetime of the carrier. A better anti-reflective layer (e.g. in silicon nitride) could also improve the efficiency. Passivating the substrate interface would be the better solution and is possible if the solar cell is ungated. However it requires more steps if the solar cell is fabricated under an active region. Fortunately, the efficiency can be improved if the solar cell is gated but still with a poor fill factor.

Finally, reducing the metal lines width and length would allow for increasing the photosensitive area and thus the efficiency. Moreover, following our perspectives, an improvement to significantly increase efficiency (or fill factor) would be to thin the silicon substrate allowing for backside illumination, to avoid the optical losses

Technology	$\eta[\%]$
Multi Si (Industrial ; record) [21]	20.3
Mono Si (Industrial ; record) [22]	24.7
a-Si (Industrial ; record) [23]	12.1
CdTe (Industrial ; record) [13]	16.7
Thin film CIGS (Industrial ; record) [24, 25]	19.9
Organic (Industrial ; record) [13]	6.8
SOI (CMOS ; SmartDust) [1]	12
a-SI (CMOS) [26]	5.2
CIGS (CMOS) [26]	7.1
Ungated SOI (CMOS) - This work	10.3
Gated SOI (CMOS ; $V_{FG} = 50V$) - This work	11.6

Table 5.4: Performance comparison of the state-of-the art solar cells in various technologies at $1000W/m^2$.

in the oxides, metallic contacts and interfaces. The backside could also be textured to change its bandgap and absorption properties.

5.9 Conclusion

Low-cost and high-efficiency SOI-based solar cells were designed, fabricated and characterized. After describing the context and interest of integrated solar cells in silicon-on-insulator technology, we reviewed the main figures of merit in photovoltaics and re-demonstrated the thermodynamic limit of the photocurrent to be of $420A/m^2$. We then described how two types of solar cells can be embedded in SOI technology by simply adding one mask/step compared to our classical CMOS process. Both devices are embedded in the substrate but can be either ungated if they are fabricated outside an active zone or gated under an active zone. For the last case, the active circuitry can be used as a gate to modulate the photocurrent inside the solar cell.

As a first step, we characterized the interface between the BOX and the Si substrate by C-V measurements. It allowed for calculating the total net oxide charge of $Q_{BOX} = -10^{10}cm^{-2}$ and the DIT of absolute charge density of $2.2 \times 10^{10}cm^{-2}/eV$.

Then, the ungated solar cells were extensively described. Their dark character-

istic was analyzed by comparison with the UV sensors of chapter 2 and with the influence of the DIT extracted before. The illuminated characteristic has then be modeled by an intuitive geometrical approach giving a simulated photocurrent of $95\mu A$ under an irradiance of $1000W/m^2$ while the measured short-circuit current was of $98\mu A$. The solar cells were then measured and the I-V and P-V curves have been presented and yielding an efficiency of 10.3, 10.5 and 15.5 for irradiances of 1000, 500 and $100W/m^2$ respectively. From the curves, an operating temperature of $320K$ in the solar cell was observed at $1000W/m^2$ and the estimation of the DIT combined with the measured open-circuit voltages allowed us for calculating a surface recombination velocity of $2.5 \times 10^3 cm/s$ at the interface.

Afterwards, the gated solar cell was studied. Since the diode can be modulated according to the frontgate voltage, the three modes of the solar cells were modeled with the same geometrical approach as for the ungated solar cells. We presented measurements of the structure which achieved efficiencies up to 11.6% and 22% with $V_{FG} = 50V$ for irradiances of $1000W/m^2$ and $100W/m^2$ respectively. However increasing the frontgate voltages increases the short-circuit current but also decreases straightly the fill factor.

To finalize the modeling of the SOI solar cells, the equivalent circuit model based on two diodes, a current source and the series and parallel resistances was investigated. The values of the saturation current of the diodes and the series resistances were of $I_{S1} \simeq 3 \times 10^{-13} A$, $I_{S2} \simeq 6.7 \times 10^{-10} A$ and $R_S \simeq 250\Omega$. The parallel resistance being the main fitting parameter of the model, its value varies from $5k\Omega$ to $22k\Omega$. A clear relation was established between the fill factor bad values and the low values of the parallel resistance compared to the characteristic resistance of the solar cell.

Finally, we compared our results to those obtained in the literature for integrated solar cells and we proposed some perspective to improve the efficiency and increase the fill factor of our solar cells. This proves that a high efficiency solar cell can be implemented at marginal cost in a complete SOI CMOS process.

References

- [1] B.A. Warneke et al., "An autonomous 16mm^3 solar-powered node for distributed wireless sensor networks," *Proceedings of IEEE Sensors*, Vol. 2, pp. 1510-1515, 2002.
- [2] URL: <http://spie.org/x33847.xml?ArticleID=x33847>
- [3] A. Luque and A. Marti, "Theoretical Limits of Photovoltaic Conversion", *Handbook of Photovoltaic Science and Engineering*, Chap. 4, Wiley and Sons, Edited by A. Luque and S. Hegedus, 2003.
- [4] M. Bruel, B. Aspar and A.-J. Auberton-Herve, "Smart-cut : A new silicon on insulator material technology based on hydrogen implantation and wafer bonding", *Japanese journal of applied physics*, Vol. 36, No. 3B, pp. 1636-1641, 1997.
- [5] S. Cristoloveanu, D. Munteanu and M.S.T. Liu, "A review of the pseudo-MOS transistor in SOI wafers: operation, parameter extraction, and applications", *IEEE Transactions on Electron Devices*, Vol. 47, No. 5, pp. 1018-1027, May 2000.
- [6] I. Ionica, A. El Hajj Diab, Y.H. Bae, X. Mescot, A. Ohata, F. Allibert, and S. Cristoloveanu, "Advances in the pseudo-MOSFET characterization method", *2010 International Semiconductor Conference (CAS)*, pp. 45-51, October 11-13, 2010.
- [7] T. Rudenko, A. Rudenko, V. Kilchytska, S. Cristoloveanu, T. Ernst, J.-P. Colinge, V. Dessard and D. Flandre, "Determination of film and surface recombination in thin-film SOI devices using gated-diode technique", *Solid-State Electronics*, Vol. 48, No. 3, pp. 389-399, 2004.
- [8] T. Rudenko, V. Kilchytska, V. Dessard and D. Flandre, "A revised reverse gated-diode technique for determining generation parameters in thin-film silicon-on-insulator devices and its application at high temperatures", *Journal of applied physics*, Vol. 97, No. 9, pp. 093718.(1-9), 2005.

- [9] D.K. Schroder, "Semiconductor Material and Device Characterization - Third Edition", *John Wiley and Sons*, 2006.
- [10] D. Flandre et al., "Fully-depleted SOI CMOS technology for low-voltage low-power mixed digital/analog/microwave circuits", *Analog Integrated Circuits and Signal Processing*, Vol. 21, pp. 213-228, 1999.
- [11] M. A. Pavanello, J. A. Martino and D. Flandre, "Analog Performance and Application of Graded-Channel Fully Depleted SOI MOSFETs", *Solid-State Electronics*, Vol. 44, No. 7, pp. 1219-1222, 2000.
- [12] I.V. Antonova, "Modification of Si/SiO₂ interface in SOI structures by hydrogen implantation: radiation tolerance", *Proceedings of the 207th ECS Meeting*, pp. 137-142, Quebec City, May 15-20, 2005.
- [13] P. Verlinden, "Photovoltaics : from Device Physics to Manufacturing", *Lecture - Graduate School MUSICS*, Louvain-la-neuve, May 31 - June 2, 2010.
- [14] A. Afzalian and D. Flandre, "Physical Modeling and Design of Thin-Film SOI Lateral PIN Photodiodes", *IEEE Transactions on Electron Devices*, Vol. 52, No. 6, pp. 1116-1122, June 2005.
- [15] A. Afzalian, "Optical Detectors in SOI CMOS Technologies for Blue DVD and Short Distance Optical Communication", *PhD Thesis*, Université catholique de Louvain, pp. 29-34, 2006.
- [16] A. Alexandre, F. Dadouche and P. Garda, "Two dimensional model for lateral photodiode", *Proceedings of the conference on Design and Test of Integrated Systems in Nanoscale Technology 2006*, pp. 294 - 298, Tunis, September 5-7, 2006.
- [17] O. Bulteel and D. Flandre, "Optimization of blue/UV sensors using p-i-n photodiodes in thin-film SOI technology", *Proceedings of the International Symposium on Silicon on Insulator Technology and Devices*, Vol. 19, No. 4, pp. 175-180, San-Francisco, May 2009.

- [18] M.A. Green, "Solar Cells: Operating Principles, Technology and System Applications", *Prentice-Hall series in solid state physical electronics*, University of New South Wales, Australia, 1982.
- [19] J. Gray, "The Physics of Solar Cells" A. Luque and S. Hegedus, "Handbook of Photovoltaic Science and Engineering", *Handbook of Photovoltaic Science and Engineering*, Chap. 3, Wiley and Sons, Edited by A. Luque and S. Hegedus, 2003.
- [20] J. O. Schumacher, "Numerical simulation for silicon solar cell with novel cell structures", *PhD Thesis*, Fraunhofer Institute for Solar Energy Systems, Freiburg, 2000.
- [21] O. Schultz, S.W. Glunz and G.P. Willeke, "Multicrystalline silicon solar cells exceeding 20% efficiency", *Progress in photovoltaics*, Vol. 12, No. 7, pp. 553-558, 2004.
- [22] Z. Jianhua, W. Aihua and M.A. Green, "24.5% Efficiency silicon PERT cells on MCZ substrates and 24.7% efficiency PERL cells on FZ substrates", *Progress in photovoltaics*, Vol. 7, No. 6, pp. 471-474, 1999.
- [23] G. Yue, B. Yan, G. Ganguly, J. Yang, S. Guha, C.W. Teplin and D.L. Williamson, "Performance Improvement of Hydrogenated Nanocrystalline Silicon Solar Cells by Hydrogen Dilution Profiling", *Record of the 2006 IEEE 4th World Conference on Photovoltaic Energy Conversion*, Vol. 2, pp. 1588-1591, 2006.
- [24] I. Repins, M. A. Contreras, B. Egaas, C. DeHart, J. Scharf, C. L. Perkins, B. To, and R. Noufi, "19.9 %-efficient $ZnO/CdS/CuInGaSe_2$ solar cell with 81.2 % fill factor", *Progress in Photovoltaics : Research and Applications*, Vol. 16, 2008.
- [25] M. A. Contreras, M. J. Romeroa, and R. Noufia, "Characterization of $Cu(In,Ga)Se_2$ materials used in record performance solar cells", *Thin Solid Films*, Vol. 511-512, pp. 51-54, July 2006.

- [26] J. Lu, W. Liu, C.H.M. van der Werf, A.Y. Kovalgin, Y. Sun, R.E.I. Schropp, and J. Schmitz, "Above-CMOS a-Si and CIGS solar cells for powering autonomous microsystems", *Proceedings of the 2010 IEEE International Electron Devices Meeting*, San Francisco, December 6-8, 2010.

CONCLUSION AND PERSPECTIVES

The silicon-on-insulator technology has proven its advantages with regards to classical bulk technologies for integrated circuits performances. In this work, we described the components of complete UV photosensors for biomedical and environmental applications and we studied integrated solar cells for micropower solar energy harvesting. We first demonstrated the feasibility of fabrication of two different types of devices on a classical SOI wafer : the UV sensor in the thin film and the photovoltaic cell in the substrate. Then, we presented optically optimized structures for the UV sensors in SOI technology which achieve high responsivity in the UV range. We also described a design of a performant signal processing integrated circuit for transducing the photocurrent into frequency. The complete photosensor has been used to measure biological material concentration by UV absorbance within a complete miniaturized system that overpass the current laboratory equipments performances. In the end, innovative solar cells fabricated in the SOI substrate have been extensively investigated, characterized and modeled.

The first chapter consisted in a review of the optoelectronic principles of semiconductor especially applied to SOI technology. In particular, since the silicon absorbs light as a function of its thickness, the thin Si film (with thickness of $80nm$) of the SOI wafer would be dedicated to low wavelengths absorption and constitutes thus an excellent choice for embedding UV sensors. Contrarily, the silicon substrate (with thickness of $800\mu m$) is preferably chosen for a large spectrum harvesting and is used to fabricate solar cells. Moreover, the particular multilayer structure of the SOI wafers thus allows for operating autonomous ultra-low-power circuits integrated in the thin silicon film of the wafer.

In the second chapter we briefly reviewed the basics of DC performances of the lateral PIN diodes embedded in the thin Si film. They act as UV sensors with high

efficiency around $\lambda = 400nm$ and are fully compatible with a CMOS process. The main purpose of the chapter was the optimization of the optical performance of the photodiodes, mostly thanks to the addition of anti-reflection coatings. In UCL SOI technology, the devices have been fabricated with ARC in silicon nitride (Si_3N_4) and alumina (Al_2O_3). The photodiodes with both ARCs have been characterized and the measured curves fit with the simulations for the responsivities which reach values of $0.08A/W$ at $\lambda = 400nm$ for an intrinsic length of $8\mu m$, anode and cathode lengths of $10\mu m$, a CMOS process oxide thickness of $280nm$ and the ARC thickness of $40nm$. A SOI industrial technology (from *OKI Semiconductor*) would increase the responsivity thanks to a reduction of the widths of the metal lines but will suffer from a thicker passivation oxide due to numerous metal layers. In our classical SOI technology, the better choice would be a dual anti-reflection coating layer with a $48nm$ silicon nitride over a $6nm$ silicon oxide which could increase the responsivity to $0.18A/W$ with a intrinsic length of $18\mu m$ and anode/cathode lengths of $1\mu m$ while being still fully compatible with a CMOS process. For future investigations, the responsivities of silicon-on-nothing and membrane structures were simulated and both feature a value up to $0.27A/W$. The mathematical model implemented for the ARC is easily adaptable for applications in biomedical and environmental fields which often require specific target wavelengths comprised from 200 to $450nm$. We performed simulations for the realization of UV sensors in ultra-thin SOI technology (e.g. such as IBM with a $10nm$ thin Si film thickness). The photodiodes would achieve a flat and high responsivity of $0.18A/W$ from $240nm$ to $360nm$, which is very accurate for deep-UV instrumentation.

In order to interface the UV photodiodes, we designed current-to-frequency processing signal circuits in the same SOI technology. Basically, the circuit consists in an integrator followed by a comparator. The integrator has been realized with a Miller operational amplifier looped by a $10pF$ capacitance and a NMOS switch while the comparator has been implemented by a Schmitt trigger for noise robustness. The amplifier has been designed with the UCL $\frac{g_m}{I_D}$ methodology and yields a $74dB$ open-loop gain, a $300kHz$ GBW and a total power consumption of $25\mu W$ for

a 2V supply voltage. A comparison of three implementations of the Schmitt triggers has pointed out that a low power and guaranteed hysteresis architecture was the most convenient in terms of surface and power consumption as well as in term of precision. A deep analysis of the noise performances of the circuit allowed us to set the minimum detectable photocurrent to 200pA which can be reduced to 10pA by increasing the power consumption. The behavior of the circuit with respect to the temperature has been discussed and it has been showed that a calibration would be enough to conserve its expected operation. The optical dynamic of the circuit is currently of 3 orders of magnitude and could be improved to 6 decades during which the circuit keeps a linear output with respect to the photodiode responsivity. Finally, we proposed a flow diagram of design for photosensors including a photodiode and a current-to-frequency converter for biomedical or environmental instrumentation.

A concrete application of the UV photodiodes is described in the fourth chapter. We measured biological material concentration in solution by UV transmittance with our photosensor. As many biological substances feature an absorption peak in the UV (for example DNA absorb light at 260nm), our system includes light emitting diodes with low wavelength emitting peak (i.e. 260 and 280nm). We first calibrated the system with quartz microcuvettes to demonstrate the validity of the measurement principle. We proposed a modeling of the complete microsystem to predict the photocurrent as a function of the biological material concentration. Then, the first measurements were performed on solutions contained in PCR tubes. A monotonic relation between the concentrations and photocurrents was obtained for DNA concentrations ranging from 400ng/ μ L to 4pg/ μ L at 280nm and from 6×10^{11} spores/ml to 6×10^7 spores/ml for bacteria. A study of the three main parameters of the system (i.e. the photodiode bias, the LED-to-tube distance and the emitting wavelength of the LED) was performed to tune the microsystem at its optimum. The complete UV photosensor including a UV photodiode and the current-to-frequency integrated circuit in our SOI technology was then used to perform similar measurements. The DNA concentration was quantified in a range from 400ng/ μ L to 40fg/ μ L at 260nm with in-tube measurements. Moreover, BSA was quantified in a range from 10 μ g/ μ L

to $1pg/\mu L$ in well-microplates and a monotonic relation was again established for influenza concentrations in a range of three decades in the same microplates. Afterwards, the complete photosensor was coupled with a microfluidic PDMS channel acting as biological material container. For this last case the DNA was quantified in a range from $10\mu g/\mu L$ to $10pg/\mu L$ while the BSA quantification range was spread a decade lower. Finally, a comparison of the most currently used lab equipments for DNA concentration quantification allowed for pointing out that our system was able to quantify DNA on a concentration range of at least two decades wider in the worst case when the samples were contained in PCR microtubes.

Finally, the last chapter opens a new field of discussion about the solar cells embedded in the SOI substrate. The photovoltaic devices are lateral PIN diodes implanted under the BOX and their fabrication is fully compatible with a standard CMOS process. According to the particular structure of the SOI wafer, two kinds of device can be fabricated : the gated solar cells if the device is implanted under an active region of circuitry, and the ungated solar cells otherwise. The MOS structure of the SOI wafer was characterized by a C-V analysis which allowed for finding a flatband voltage of the structure of $0V$ and a threshold voltage of $2.2V$ due to a total oxide charge of $Q_{BOX} = -10^{10}cm^{-2}$. A defect interface trap charge density of $D_{IT} = 2.2 \times 10^{10}cm^{-2}C/eV$ was also calculated during those measurements. The ungated solar cell was then described. Its dark characteristic is similar to the UV PIN diode and the illuminated characteristic was modeled according to a geometrical intuitive approach. A photocurrent of $95\mu A$ was simulated while the measured one was of $98\mu A$. The solar cells were characterized with the *AM1.5G* terrestrial spectrum and the efficiencies obtained were of 10.3%, 10.5% and 15.5% for irradiances of $1000W/m^2$, $500W/m^2$ and $100W/m^2$ respectively. An internal temperature of $320K$ was extracted from measurements and a surface recombination velocity of $S = 2.5 \times 10^3cm/s$ was extracted with the values of the DIT and the comparison between Atlas model and measurements. The gated solar cell was then studied and modeled with the same method as for the ungated one combined with the C-V measurements. The devices were measured under illumination and the efficiencies were

of 8.9%, 10.7% and 16.4% for irradiances of $1000W/m^2$, $500W/m^2$ and $100W/m^2$ respectively and a frontgate voltage of $V_{FG} = 5V$ ensuring an inversion layer in the device under the BOX. The top efficiencies that we reached were of 12%, 13.6% and 22% for the same previous irradiances when a maximal frontage voltage of $50V$ was applied. A circuit equivalent modeling was used to model the solar cells with electronic circuit components (i.e current source, diodes and resistances). The current source models the photocurrent and the diodes model the Shockley-Read-Hall and surface recombination phenomenons at low and high injections. Two resistances are also used in the equivalent circuit : a series resistance models the resistance of the fingers and of the metal lines inner resistances while a parallel resistance models edge and surface effects. A strong correlation was established between the parallel resistance value and the fill factor for gated solar cell as it was mentioned in the literature.

We also proposed improvements for the different parts of the work. For the UV photodiodes, the main improvements would come from a reduction of the anode and cathode lengths since they are covered with metal and thus reflect light to decrease the total photosensitive area. Another major improvement useful for increasing the photodiode responsivity is to decrease the silicon dioxide thickness down to a minimum, i.e. $6nm$ in the UCL SOI technology.

Concerning the integrated circuit for signal processing of the UV photodiode, an auto-calibrating circuit could be added in the same chip to adapt the measurements and in particular to regulate the Schmitt trigger thresholds if a temperature change is observed. A battery with an integrated low dropout voltage regulator would also allow for resisting to the voltage variations of the circuit. Finally, some improvements have been proposed to reduce the noise of the circuit in order to feature an optical dynamic up to 6 orders of magnitude.

The most recent advanced version of the microsystem used to quantify biological material concentrations integrates a PDMS channel as biological sample container. This allows for reducing the dimensions and the portability of the equipment. However, currently the LEDs and the circuit are supplied with large sized I-V sources.

The complete miniaturization and portability would include battery cells for the whole system and voltage regulators for example.

To finish, we proposed some guidelines to improve the solar cells fill factor which is currently bad. The main influencing factor is the BOX/substrate interface. One solution is for example to passivate this interface, but it would require more steps compared to the current CMOS process. A final goal is to reduce the substrate thickness down to a few tenth of micrometers and to illuminate the solar cell from its backside which could be texturized.

As a perspective, we propose to calculate the area of a SOI solar cell array required to supply complete integrated circuits. As first example, we consider the complete UV sensor composed of the PIN lateral diode in thin Si film of chapter 2 and the signal processing circuit of chapter 3. The specifications are to supply $27\mu W$ which is possible to obtain with the ungated and gated solar cells alone.

For ungated solar cells, the current at the maximal power point is approximately of $75\mu A$ for which the voltage is $V_{MAX} = 0.375V$. This would thus require a total area of $0.26mm^2$ for an irradiance of $1000W/m^2$. Of course the result can be adapted for the lower irradiances, i.e. $0.51mm^2$ at $500W/m^2$ and $1.74mm^2$ for indoor irradiances of $100W/m^2$. By using gated solar cells, we will consider that the frontgate is biased at a positive voltage of $50V$ to reach its best efficiency, the total area needed is then of $0.21mm^2$ at $1000W/m^2$, $0.37mm^2$ at $500W/m^2$ and $1.14mm^2$ if the illumination is of $100W/m^2$.

Other specific integrated circuits have been realized and detailed in the literature. We propose to calculate the area of both type of SOI solar cell needed to supply these ICs at each irradiance. The chips chosen for this example are firstly two examples of commercial state-of-the-art microcontrollers (MCU) with power consumption less or equal to $5mW$ [1, 2]. The second example is an ULP nearly perpetual environmental sensor with $7.7\mu W$ power consumption [3]. Finally, an intraocular pressure monitor has been fabricated in [4] and its average power consumption is reduced to $80.6nW$. Each of them features a chip size of a few mm^2 . The table 5.9 summarizes

the different areas of solar cells for our work and the other applications. They can be compared to the size of the circuitry for each realization.

IC	Diode type	Irradiance [W/m^2]		
		1000	500	100
This work - $27\mu W$ ($0.5mm^2$)	Ungated	$0.26mm^2$	$0.51mm^2$	$1.74mm^2$
	Gated ($@V_{FG} = 50V$)	$0.21mm^2$	$0.37mm^2$	$1.14mm^2$
$5mW$ MCU [1, 2] ($4.4mm^2$)	Ungated	$48.5mm^2$	$95mm^2$	$3.23cm^2$
	Gated ($@V_{FG} = 50V$)	$41.6mm^2$	$73.5mm^2$	$2.27cm^2$
$7.7\mu W$ Sensor [3] ($5.9mm^2$)	Ungated	$0.08mm^2$	$0.15mm^2$	$0.49mm^2$
	Gated ($@V_{FG} = 50V$)	$0.07mm^2$	$0.11mm^2$	$0.35mm^2$
$80.6nW$ Sensor [4] ($3mm^2$)	Ungated	$782\mu m^2$	$1535\mu m^2$	$5200\mu m^2$
	Gated ($@V_{FG} = 50V$)	$672\mu m^2$	$1185\mu m^2$	$3660\mu m^2$

Table 5.5: Area of SOI solar cells needed to supply different IC

However, this would imply that the solar cells are always biased at their maximum power point and that an adequate combination of series and parallel diodes is possible to achieve the requirements of the supply current of $75\mu A$ and voltage of $2V$. Sometimes, boost circuits can be used to increase the voltage. The second appendix describes the use of charge pumps dedicated to solar cell power management in SOI technology.

At the end, to conclude this dissertation, we have demonstrated the ability of the silicon-on-insulator technology for embedding optoelectronic components for bio-environmental applications and micropower solar energy harvesting. On one hand, the blue/UV photosensors in the thin Si film can reach high responsivity thanks to its $80nm$ film thickness and to an adequate choice of anti-reflection coatings. On the other hand, micropower solar cells can reach efficiencies from 10% to nearly 12% for outdoor irradiances and from 15% to 22% for indoor illuminations when they are embedded in the substrate which is currently useless in that technology. Integrated circuits can be designed and fabricated in the SOI thin film and interface the UV sensors with a current-to-frequency converter. It has been showed that excellent results were achieved concerning the quantification of biological material

CHAPTER 5. DESIGN AND MODELING OF SOLAR CELLS IN SOI SUBSTRATE

concentration by UV transmittance with a microsystem consisting in a complete UV photosensor in SOI and deep UV light-emitting diodes.

References

- [1] D. Bol, S. Boyd and D. Dornfeld, "Application-Aware LCA of Semiconductors: Life-Cycle Energy of Microprocessors from High-Performance 32nm CPU to Ultra-Low-Power 130nm MCU", *IEEE International Symposium on Sustainable Systems and Technology 2011*, pp. 1-6, Chicago, May 16-18, 2011.
- [2] M. Zwerg et al., "An 82 μ A/MHz Microcontroller with Embedded FeRAM for Energy-Harvesting Applications", *IEEE International Solid-State Circuits Conference 2011 Digest of Technical Papers*, pp. 334-336, February 20-24, 2011.
- [3] G. Chen et al., "Millimeter-Scale Nearly Perpetual Sensor System with Stacked Battery and Solar Cells", *IEEE International Solid-State Circuits Conference 2010 Digest of Technical Papers*, pp. 288-289, February 7-11, 2010.
- [4] G. Chen et al., "A Cubic-Millimeter Energy-Autonomous Wireless Intraocular Pressure Monitor", *IEEE International Solid-State Circuits Conference 2011 Digest of Technical Papers*, pp. 310-312, February 20-24, 2011.

A-1 : LIGHT MODELING IN SOI MULTI-LAYER STRUCTURE

This appendix summarizes the light modeling implementation presented in Afzalian's PhD thesis [1]. The responsivity, as defined from chapters 1 and 2, is the ratio between the photocurrent and the incident light power and can be written as :

$$R = \frac{q \cdot \lambda}{h \cdot c} \cdot A \cdot QI \cdot \eta_{SOI}, \quad (5.18)$$

where A is the total area of the diode, QI is the internal quantum efficiency (see equation 1.12) and η_{SOI} is the efficiency of the thin silicon layer regarding the whole structure. The thin Si film efficiency has then to be calculated as a fraction of the incident light power P_{in} . To solve the problem, we modeled and simulated mathematically the reflection, transmission and absorption of electromagnetic waves in a multi-layer multi-material structure as in [2]. Each layer of the structure is defined by its thickness and refractive index N_i as in figure 5.22. The figure represents the structure of a simple lateral diode in SOI technology covered with one ARC layer over the SiO_2 as in figure 2.3.

We assume that the first (layer 0) and the last media (layer 5) are semi-infinite and that each layer features its refractive index defined by equation 1.3. Then, we can write a recursive formula to compute the electric fields from medium $i + 1$ (E_{i+1}) back to medium i (E_i) :

$$E_{i+} + E_{i-} = E_{(i+1)+} \cdot e^{j \cdot \delta_{i+1}} + E_{(i+1)-} \cdot e^{-j \cdot \delta_{i+1}} \quad (5.19)$$

$$N_i \cdot (E_{i+} - E_{i-}) = N_{i+1} \cdot (E_{(i+1)+} \cdot e^{j \cdot \delta_{i+1}} - E_{(i+1)-} \cdot e^{-j \cdot \delta_{i+1}}), \quad (5.20)$$

where δ_{i+1} is defined by :

$$\delta_{i+1} = \frac{2\pi}{\lambda} \cdot N_{i+1} \cdot d_{i+1}. \quad (5.21)$$

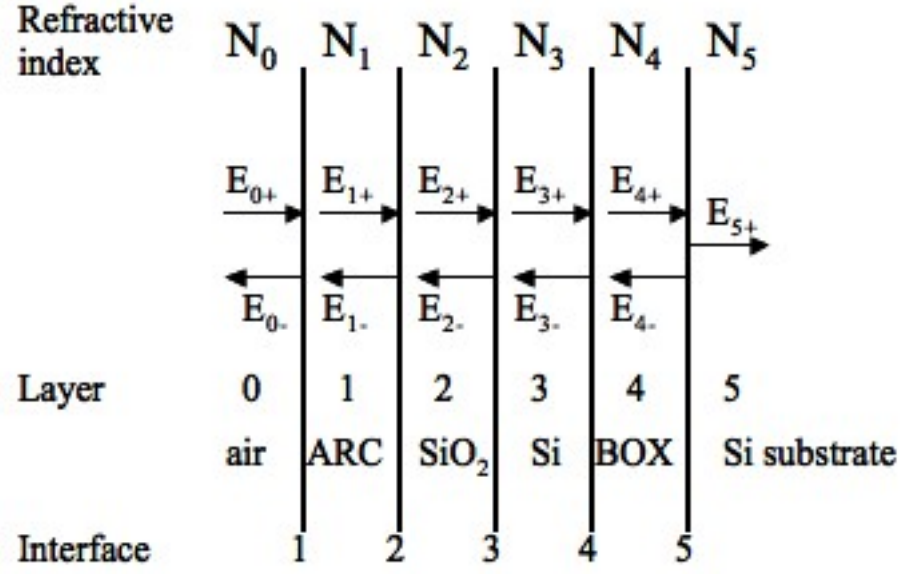


Figure 5.22: Equivalent multi-layer model for a standard lateral PIN photodiode in SOI technology with one ARC.

In equation 5.21, d_{i+1} is the distance travelled by the waves from interfaces $i + 1$ to i , i.e. the thickness of layer i .

Then, following the electromagnetic theory, we can express the average power of the electromagnetic wave (P_{av}) as the cross product of the electric and magnetic fields related to the wave:

$$P_{av} = \frac{c}{8\pi} \text{Re}(E \times H^*). \quad (5.22)$$

Now, we can define the light absorbed in a medium i by :

$$P_{abs,i} = T_i - T_{i+1}, \quad (5.23)$$

in which T_i is the light transmitted in the medium i , expressed by :

$$T_k = \frac{c}{8\pi} \{ n_{k-1} (|E_{(k-1)+}|^2 - |E_{(k-1)-}|^2) + \text{Re}[N_{k-1}^* 2j \text{Im}(E_{(k-1)+} \cdot E_{(k-1)-})] \}. \quad (5.24)$$

Concerning the layer 0, we can define the incident power to the device, P_{in} , by :

$$P_{in} = n_0 \cdot |E_{0+}|^2. \quad (5.25)$$

According to figure 5.22, we can write for the efficiency of the SOI film :

$$\eta_{SOI} = (1 - r) \frac{P_{abs,3}}{T_3}, \quad (5.26)$$

where r is the equivalent reflection of the first layers before the thin silicon film (in that case, the double-layer of ARC/SiO_2). $P_{abs,3}$ is the power absorbed in the thin Si film and T_3 is the power transmitted into it. Of course, the model can be adapted for SON and membrane structures by adding the associated different layers since the model is recursive and allows as many layers as wanted. The same results can be obtained by ensuring the continuity of electric and magnetic fields at each interface of the structure according to the Maxwell equations.

References

- [1] A. Afzalian, "Optical Detectors in SOI CMOS Technologies for Blue DVD and Short Distance Optical Communication", *PhD Thesis*, Université catholique de Louvain, pp. 29-34, 2006.
- [2] P. Jespers, F. Van De Wiele and M. White, "Solid State Imaging", *NATO Advanced Study Institutes Series - E. Applied Sciences*, Noordhoff International Publishing, 1976.

A-2 : ENERGY HARVESTING

CIRCUITS FOR SOI SOLAR CELLS

Power Management Consideration

Even if a solar cell can provide enough power to supply an applicative circuit, an intermediate circuitry is necessary to regulate a constant supply voltage to the load for any illumination. A circuit with feedback loop is then required for tracking the maximum power point on the P-V curve of the solar cell according to the variations of the illumination and hence supply the load. A typical energy management circuit is schematized in figure 5.23 and has been designed in classical silicon CMOS technology in [1, 2]. Our future goal is to design a similar circuit in SOI technology with integrated solar cells in the silicon substrate.

In this circuit, the voltage of the solar cell is increased by the charge pump to

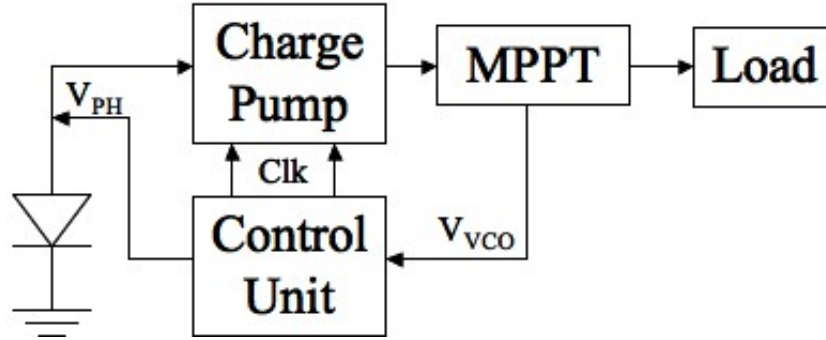


Figure 5.23: Schematic of the solar energy management circuit.

supply a maximum power point tracking (MPPT) unit. The MPPT is an algorithmic circuit that senses the output current of the charge pump to determinate if the solar cell is at its maximum power point or not. The MPPT circuit features two outputs : the first one is connected to the load, typically a battery cell or a low power circuit. The second one (V_{VCO}) is provided by an intern voltage controlled oscillator and is the input of a control unit block. This last circuit generates the clocks for the charge pump and adjusts the voltage bias of the solar cell if the maximum power

point is not currently reached according to V_{VCO} .

The Charge Pump

The first stage of this circuit is the charge pump and allows for increasing the voltage delivered by the solar cells. Of course, the current at the output of the charge pump is decreased due to the power efficiency of the circuit. The schematic of a three-phases charge pump (and its clock generator) implemented with MOSFET diodes is showed in figure 5.24. This type of charge pump has been described in [3, 4] where

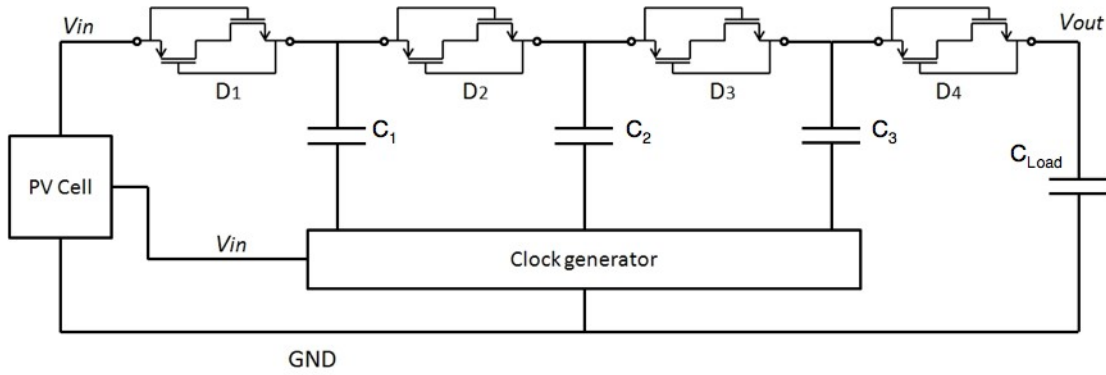


Figure 5.24: A three-phases charge pump architecture implemented with ULP MOS diodes [3].

the MOS diodes have been realized in ULP technology [5]. The output voltage of the charge pump is described by the following equation [6] :

$$V_{out} = (V_{in} - V_D) + N \cdot (V_{in} - V_D) + \frac{N \cdot I_{out}}{f \cdot C_{Load}} \quad (5.27)$$

where N is the number of pumping capacitances (i.e. the number of stages), V_{in} is the output voltage of the solar cell, V_D is the voltage drop across the ULP diode, I_{out} is the output current of the charge pump, f is the operating frequency of the charge pump and C_{Load} is the total capacitance at the output node of the charge pump. For our three-phases charge pump, it implies a maximal output voltage of $V_{out} = 4 \cdot V_{in}$ in the ideal case where the voltage drop across the MOS diode is null when $I_{out} = 0$.

Preliminary Measurements

A realization of the charge pump has been fabricated in UCL SOI CMOS technology. The diodes were implemented by ULP diodes for which the NMOS and PMOS transistors yield an identical size ratio of $\left(\frac{W}{L}\right) = \frac{100\mu m}{2\mu m}$, the pumping capacitances are $C_{1,2,3} = 5pF$ and $C_{Load} = 20pF$. The clock generator has not been integrated on the same chip, we then generated the clock signals with an extern equipment as described hereafter.

Two ungated solar cells for which $L_i = 34\mu m$, $L_N = L_P = 10\mu m$ and the area is $0.25mm^2$ for each were connected in series under an irradiance of $100W/m^2$. According to figure 5.10 and table 5.1, the total open-circuit voltage is $V_{OC} = 872mV$ and the short-circuit current is $25\mu A$. For their total size of $0.5mm^2$ and the efficiency of 15.5%, the power at the maximal power point is of $7.7\mu W$ and is achieved for $I_{MAX} = 14.3\mu A$ and $V_{MAX} = 540mV$ as observed during the characterization. The power provided by the solar cell was plotted, relatively to its maximal value, as a function of the load current of the charge pump in figure 5.25.

Two cases are illustrated : the solar cells alone (continuous line), for which the maximum is obtained at $I_{Load} = 14\mu A$ as measured, and the solar cells connected to the charge pump without any clock (dashed line) for which the maximum is obtained at $I_{Load} = 12\mu A$. For the second case, one can observe the weaker power delivered by the solar cell and the negative shift of the maximum which corresponds to a positive delta voltage of $36mV$ of the maximal power point of the cell (corresponding to a difference of $2\mu A$).

We then measured the output voltage of the charge pump as a function of the load current. The clocks were generated externally with an amplitude equal to the voltage delivered by the solar cells at each load current. This way, we emulate a perfect ring oscillator for which the frequency of the clocks was fixed to $10MHz$. The current provided by the clock generator was determined experimentally to be of $450nA$ at $I_{Load} = 0A$ but is supposed to increase with a rise of the load current. The figure 5.26 summarizes the voltage gain (continuous line) and the voltage magnitudes

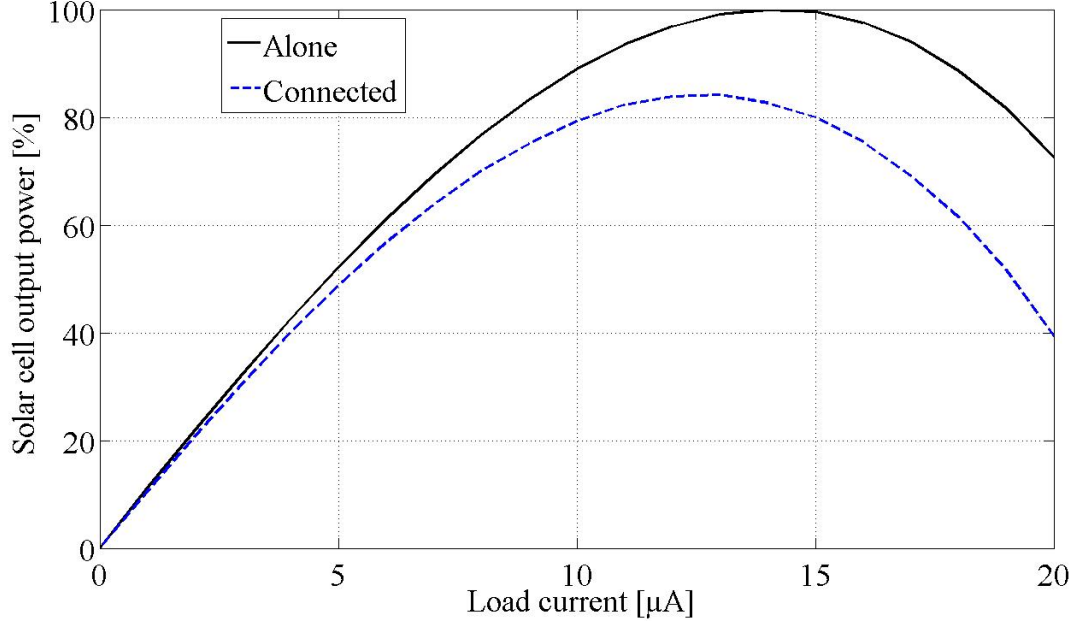


Figure 5.25: Measurements of the relative power of the solar cell alone (continue line) and connected to the charge pump (dashed line) as a function of the load current.

at the input (doted line) and output (dashed line) of the charge pump.

Currently, the voltage gain for $I_{Load} = 0$ is 2.88 and is equal to 1 for a load current of $10.5\mu A$. However, due to unknown currents injected by the clocks, it is actually impossible to quantify the efficiency of the charge pumps. According to equation 5.27, we can deduce at $I_{Load} = 0$ that the average threshold voltage of the ULP diode is of $230mV$. This large value is due to a preliminary design that do not take into account the influence of the source-backgate voltage. Indeed, it has been showed in [7], that the ULP diodes yield a different I-V characteristic according to the backgate voltage referred to the source of the transistors. It would then be possible to reduce considerably this threshold voltage and hence reduce the leak current of the transistors.

Conclusion

The benefit of a charge pump is of course an elevation of the voltage to supply CMOS circuitry which needs voltage values around $2V$ in the UCL SOI $2\mu m$ technology.

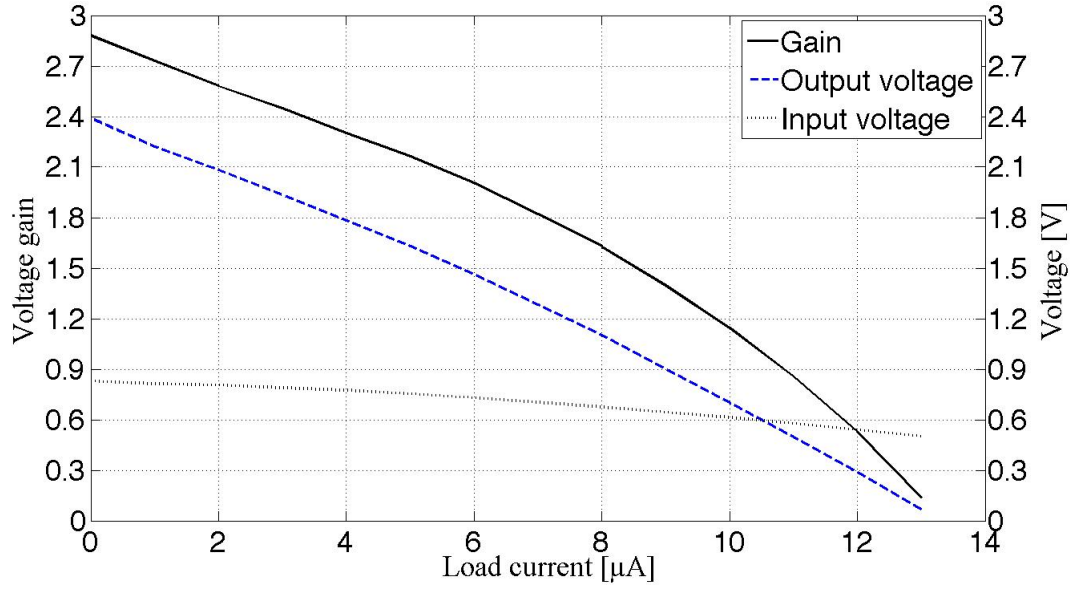


Figure 5.26: Measurements of the evolution of the voltage gain of the charge pump (continue line) and of the voltage magnitudes of the connected solar cell (doted line) and of the output of the charge pump (dashed line) as a function of the load current.

Nevertheless, the diodes have to be carefully designed to maximize the efficiency of the charge pump in order to feature an adequate voltage gain while keeping a sufficient load current.

References

- [1] H. Shao, C.-Y. Tsui and W.-H. Ki, "A Micro Power Management System and Maximum Output Power Control for Solar Energy Harvesting Applications", *Proceedings The International Symposium on Low Power Electronics and Design 2007*, Portland, August 27-29, 2007.
- [2] H. Shao, C.-Y. Tsui and W.-H. Ki, "An Inductor-less MPPT Design for Light Energy Harvesting Systems", *Proceedings of Design Automation Conference 2009*, Yokohama, January 19-22, 2009.
- [3] D. Flandre, O. Bulteel, G. Gosset, B. Rue and D. Bol, "Disruptive ultra-low-leakage design techniques for ultra-low-power mixed-signal microsystems", *Proceedings of FTFC 2011*, Marrakech, May 31-June , 2011.
- [4] G. Gosset, O. Bulteel, P. Baijot and D. Flandre, "Ultra-High-Efficiency Co-Integrated Photovoltaic Energy Scavenger", *Proceedings of SOI Conference 2011*, Tempe, October 3-6, 2011.
- [5] V. Dessard, "SOI specific analog techniques for low-noise, high-temperature or ultra-low power circuits", *PhD Thesis*, Université catholique de Louvain, Belgium, 2001.
- [6] J. F. Dickson, "On-chip high-voltage generation in MNOS integrated circuits using an improved voltage multiplier technique," *IEEE Journal of Solid-State Circuits*, Vol. SC-11, No. 3, pp. 374-378, June 1976.
- [7] G. Gosset, B. Rue and D. Flandre, "Very High Efficiency 13.56 MHz RFID Input Stage Voltage Multipliers Based On Ultra Low Power MOS Diodes", *2008 IEEE International Conference on RFID*, pp.134-140, Las Vegas, April 16-17, 2008.

A-3 : LOW TEMPERATURE MEASUREMENTS

In collaboration with the *Centro Universitario da FEI* in Brazil, low-temperature measurements were performed on the lateral PIN diodes in both SOI thin film and substrate in the range from $100K$ to $400K$.

UV Photodiodes

According to publications [1, 2], the UV photodiodes have been measured for both dark and illuminated characteristics. Concerning the dark current, a straight decrease of four decades has been observed for a temperature decrease from $400K$ to $100K$ as well for reverse as for positive voltages. A slighter decrease is also observed for the illuminated characteristic. The main advantage is a higher signal-to-noise ratio and thus an increased responsivity for the photodiodes at lower temperatures. According to the Atlas simulation, the reduction of the total photocurrent is due to bandgap narrowing at low temperatures while the rise of current at higher temperatures can be explained by the doping and temperature dependency on the carrier lifetime.

Solar Cells

The main figures of merit of the ungated solar cells (I_{SC} , V_{CO} , FF and η) have also been studied along a temperature range from $100K$ to $380K$. The open-circuit voltage increases with a lowering of the temperature as predicted in the literature while the short-circuit current also decreases with the temperature due to recombination the intrinsic region. As a matter of power, P_{MAX} also increases at lower temperature which can be explained by the larger carrier mobility. Finally, an increase of the fill factor is observed below $250K$ that can be related to an increase of the

parallel resistance and thus a reduction of the surface recombination velocity at the BOX/substrate interface.

References

- [1] M. de Souza, O. Bulteel, D. Flandre and M.A. Pavanello, "Temperature Influence on the Behaviour of Lateral Thin-Film SOI PIN Photodiode in the Blue and UV Range", *Proceedings of the EuroSOI Conference 2010*, Grenoble/France, January, 25-27, 2010.
- [2] M. de Souza, O. Bulteel, D. Flandre and M.A. Pavanello, "Analysis of Lateral SOI PIN Diodes for the Detection of Blue and UV Wavelengths in a Wide Temperature Range", *ECS Transactions*, Vol. 31, No.1, p. 199-206, 2010.
- [3] M. de Souza, O. Bulteel, D. Flandre and M.A. Pavanello, "Electrical Characterization of SOI Solar Cells in a Wide Temperature Range", *Proceedings of the SOI Conference 2010*, San Diego - CA/USA, October 11-14, 2010.