INVITED PAPER

Engineering SOI Substrates for RF to mmWave Front-Ends

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5G and Wi-Fi 6(E) are creating new user experiences that require unprecedented network capacity with on-demand data throughput at record low latencies. To address these requirements, spectral resources from 100s of MHz to mmWave frequencies have been assigned to these standards. Gbps data rates are offered at these bands using record high waveform complexity, tightening RFIC linearity specifications to minimize signal distortion.

Over the last two decades, silicon on insulator (SOI) has proven to be the semiconductor solution of choice for highly linear, power efficient, integrated wireless systems. At the same time, the world's near to endless CMOS capacity and the demonstrated large-scale manufacturability of RF-SOI substrates have enabled cost effective solutions for 4G/LTE and Wi-Fi. Today, 5G and Wi-Fi 6(E) are benefiting from this demonstrated capability. This article reviews the continuous innovation of SOI engineered substrates to address the challenges of today's and future wireless systems.

HR-SOI TO TRAP-RICH SOI

Compared to bulk silicon technology, SOI's key advantages for RF applications have led to its general adoption in smartphone front-end modules over the past decade, spearheaded by RF switches. SOI wafers are composed of a thin silicon layer, usually 50 to 150 nm where the active devices are built, fully isolated from the underlying or "handle" wafer by a buried oxide (BOX) layer.

This configuration has major benefits. First, the shallow trench isolation reaches the BOX and effectively eliminates any conduction path between devices. This, in turn, enables transistor stacking to a level unsustainable using junction isolation. It also drastically improves the isolation between circuit blocks. The second benefit is the ability to engineer the handle wafer specifically for communication applications without degrading the quality of the active device layer, leading to high resistivity (HR) silicon being implemented as the handle wafer material. Decreasing the concentration of free carriers in the handle wafer reduces the attenuation or insertion loss (IL) of the propagated signal, resulting in better power transmission efficiency. It also reduces the power of the parasitic signals generated at the harmonic frequencies of the carrier signal, i.e., harmonic distortion (HD) or, when multiple signals are involved, intermodulation distortion (IMD).

TABLE 1
300 MM RF-SOI SUBSTRATE SPECIFICATIONS

	HR-SOI	RFeSI	RFeSI_T Low Linearity Drift vs. Temperature	Trap Rich RF-SOI >10 GHz
Substrate Type	High Resistivity 1-3 kΩ·cm	High Resistivity 1-10 kΩ·cm	Low Resistivity p-type	High Resistivity 1-10 kΩ·cm
Trap-Rich	N/A	Thin to Thick	Ultra-Thick	Ultra-Thin to Thick
BOX Thickness (nm)	100 to 1000	200 to 400	200	30 to 200
Top Si Thickness (nm)	75 to 145	75 to 145	75 to 145	50 to 75
Top Si Thickness Uniformity (nm)	±3.5	±3.5	±3.5	±3.5
2nd Harmonic Power (dBm)	<–50	–70 to –90	–70 to –120	–60 to –90

Though the HR handle is highly beneficial, the HR-SOI wafer has an inherent capacitor-like configuration, which results in the possible creation of a low resistivity, free carrier accumulation or inversion layer underneath the BOX, dubbed the parasitic surface conduction (PSC) layer.[1] This issue can be circumvented with an engineered layer between the BOX and HR handle containing a high density of electrically active traps.[2,3] Three game-changing effects of this trap-rich (TR) layer are the Fermi level pinning induced by the traps, the trapping of free carriers from the base wafer and the reduction of mobility. A higher level of signal fidelity can be achieved: the isolation is improved because the conductive coupling below the BOX is suppressed, leaving only capacitive coupling. The fluctuation of carrier concentration below the BOX is suppressed, as the Fermi level is pinned close to the middle of the semiconductor's gap, linearizing the handle's resistance and capacitance and drastically reducing HD. Finally, the constant HR further reduces IL.

The following section discusses Soitec's TR SOI family of substrates and how the RF performance compares to HR-SOI for different wireless applications (see ***Table 1***). The measurements shown throughout the article, unless otherwise stated, are performed on 2.1 mm long coplanar waveguide (CPW) at a fundamental frequency of 900 MHz. The DC bias refers to the bias applied between the central line and ground lines; the latter connected to the substrate backside. The second harmonic power levels are referenced to a fundamental frequency output power of 15 dBm at a default DC bias of 0 V.

RF-SOI SUBSTRATES FOR RF FRONT-ENDS

Depending on the intended function in the RF front-end (RFFE), the diverse RF circuits impose different requirements on the RF-SOI substrate, i.e., for large signal (linearity, power handling) or small signal and immunity to interferers (crosstalk, digital noise).[4–6] Given the increasing complexity of the RFFE, high density integration of digital logic, memory and RF functions must also be carefully considered. The final system application—such as infrastructure or mobile user equipment (UE)—will also dictate specifications including ruggedness and robustness.

Large-signal switching, shaping and amplification can introduce signal distortion because of the inherent nonlinear nature of active RF circuits. Soitec's RFeSI™ substrates help minimize distortion by reducing parasitics, as previously explained. ***Figure 1*** shows the harmonic and intermodulation products generated on three RFeSI TR SOI substrates with guaranteed second harmonic power below -100 dBm (RFeSI100), -90 dBm (RFeSI90)

and -80 dBm (RFeSI80). The IMD performance is measured with two 20 dBm tones at 900 and 955 MHz.[7]

The complexity of the digital and control content of the RFFE has been steadily increasing. For example, several 26 MHz—up to 52 MHz—MIPI RFFE[SM] bus instances are required to control the radios in the modern smartphone, including 5G, Wi-Fi, Bluetooth, GNSS and NFC. Even with the complexity, the control and digital signals must not interfere with the RF and vice versa. A good RF substrate should help prevent unwanted signals conducting from one part of the system to another—whether control, digital or RF—as they can disrupt system operation. Crosstalk and digital noise immunity are very important when designing RF and mmWave front-ends, and the design starts with the substrate (see ***Figure 2***).[5]

Smartphone antenna impedance and aperture variation due to external elements, such as the position of the user's hand, have been widely studied, leading to the use of antenna tuners (AT) in the RFFE to dynamically compensate such variation. ATs are implemented as close to the antennas as possible and are the first RFFE elements that must withstand large VSWR. Depending on the design, ATs may require the RF-SOI substrate BOX to withstand voltages greater than 100 V. Some RFeSI substrates offer BOX soft breakdowns greater than 150 V by tuning the BOX layer thickness appropriately (see Table 1).

When comparing RF, mmWave and integration capabilities, Figures 1 and 2 show a clear advantage of TR SOI over HR-SOI. TR RF-SOI has greatly contributed to the success of CMOS in RF and mmWave front-ends. As RFFEs evolve, TR SOI substrates must also evolve to address more stringent requirements. Higher frequency measurements, substrate modeling and material developments are being pursued for future applications, and these are described in the following sections.

MMWAVE CHARACTERIZATION

Signal attenuation in transmission lines, particularly CPW lines, is strongly affected by the free carriers in the underlying substrate. The total propagation loss, which comprises metallic losses in the lines as well as losses from the substrate, is often used to compare the RF per-

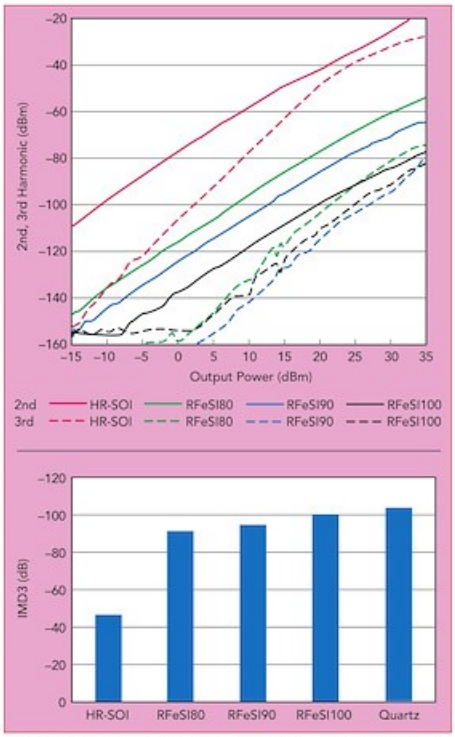


Fig. 1 RF-SOI substrate second and third harmonics (a) and 845 MHz IMD3 (b).

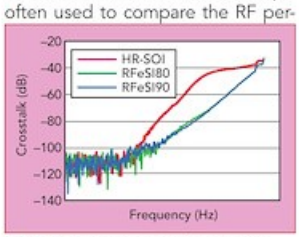


Fig. 2 RF-SOI substrate crosstalk immunity.

Fig. 3 Measured insertion loss on HR-SOI and RFeSI90 substrates (a) compared to simulated HR-SOI substrate model (b).

formance of different substrates. *Figure 3* plots the propagation loss (α) versus frequency of CPW lines on different silicon substrates, showing the separate contributions from the metallic and substrate losses. For a 50 Ω transmission line, α is equivalent to the IL per unit length.

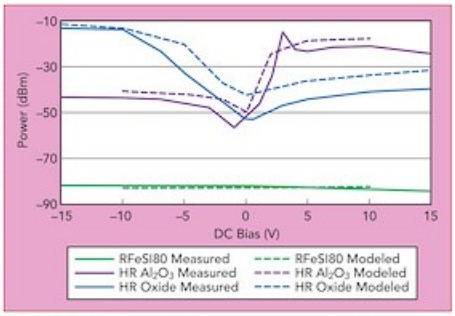


Fig. 4 Measured vs. simulated second harmonic power.

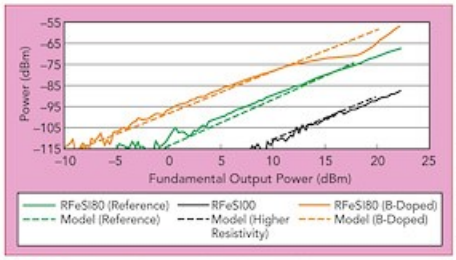
CPW lines with different lengths (i.e., 426, 906, 2106, 2526, 2826 µm) and the same cross section were measured and the multiline thru-reflect-line (mTRL) algorithm applied to extract the propagation constant.[8] The mTRL algorithm with redundant line measurements increases the extraction accuracy by reducing the measurement noise, which is inherently larger at mmWave frequencies. The separation of the metallic and substrate losses was obtained using a procedure described by L. Nyssens et al.[9], which is valid at mmWave frequencies.

The different samples were manufactured with the same CPW pattern, such that they have similar metallic losses versus frequency. The increasing IL with frequency is caused by the skin effect, a metallic loss mechanism. The introduction of HR silicon improved the IL by reducing the number of free carriers in the handle substrate. Nevertheless, the presence of the PSC at the oxide-silicon interface degrades the IL. This is suppressed when a TR layer is used, as with the RFeSI90 wafer. Therefore, the TR SOI substrates combining a HR handle silicon substrate and TR layer have negligible substrate-related losses. At sufficiently high frequencies, when the slow-wave mode is suppressed—above a few tens of MHz for TR substrates and above 10 to 20 GHz for HR substrates—the substrate losses are frequency independent and agree with the substrate model. The improvement in IL for the RFeSI substrates is valid across the entire mmWave frequency range.

SIMULATING RF-SOI SUBSTRATES

Developing engineered materials for advanced applications is a complex, time- and resource-consuming process, which is more efficient with calibrated simulation. Accurate small-signal modeling has been developed using a combination of electromagnetic (EM) and technology computer-aided design (TCAD) tools to account for the lossy nature of the silicon substrates and conductive interfaces.[10,11] While simulating a semiconductor substrate's large-signal behavior is more of a challenge, the authors have developed the capability to link material properties to RF performance. To model the distortion induced by the substrate on a CPW line's signal, modeling is based on simplified EM propagation models which are complementary to solving the semiconductor transport equations and trapping phenomena in a transient, large-signal, time-domain TCAD approach. The model has been validated with several HR and TR samples having key differences in material parameters, enabling the relative importance of such differences on the linearity of the RF substrates to be assessed.

Figure 4 shows the second harmonic power levels versus DC bias for three substrates, comparing measured and modeled performance. The DC bias induces a mirror charge below the BOX. An RFeSI80 TR wafer is shown for reference; the other two wafers are HR,



▲ Fig. 5 Measured vs. simulated second harmonic power of two modified trap-rich wafers and the reference RFeSI80 sample.

each with a different BOX material: the first oxide, the second alumina (Al2O3). Oxide-silicon interfaces are known to have a positive, fixed interfacial charge density, reflecting the creation of an electron PSC,[1,3] while the charge density is negative at alumina-silicon interfaces, reflecting creation of a hole PSC. The interfacial fixed charge densities of the HR Oxide and HR Al_2O_3 samples were extracted from low frequency CV measurements of classical MOS capacitor devices at 8 × 10^{11} and -6 x 10^{11} cm^{-2}, respectively (not shown), and the same values were used in the model. The model correlates well with the measured data, accurately capturing the strong dependence on bias voltage and fixed charge.

By introducing trap energy states in the polysilicon TR layer, modeling predicts the increase in effective resistivity, as well as the decrease in power of the generated harmonic. ***Figure 5*** plots the second harmonic versus fundamental output power for three RFeSI substrates, comparing measured and modeled performance. One primary material parameter difference distinguishes each substrate from the others, and the model captures the relative impact of each parameter on the harmonics generated by that substrate. As a reference, the RFeSI80 substrate was modeled and measured. Using a more resistive polysilicon layer and handle wafer, an RFeSI100 was fabricated and modeled. Tailoring the resistivity in the model is almost sufficient to justify the 20 dB difference in the second harmonic power levels between these two substrates. Finally, the RFeSI80, introduced significant Boron contamination within the polysilicon layer, confirmed by SIMS and SRP data (not shown). Boron degrades the substrate impedance and raises the harmonic levels; adding the Boron profile into the model generates accurate estimates of harmonic performance.

This physical modeling gives key insights into the effect of the fundamental material parameters on RF loss and linearity performance and is a useful tool when designing substrates to meet given RF specifications.

BETTER PERFORMANCE AND TEMPERATURE STABILITY

RF-SOI substrates need to evolve to support new and more stringent RF requirements. Today, RFFE linearity is often not limited by the substrate, yet a large field of RF applications would benefit from RF-SOI substrates with better HD and IMD specifications. RFeSI linearity may be enhanced by improving the handle wafer resistivity and polycrystalline silicon trapping efficiency (see RFeSI100 in Figure 1). However, there are limits to the resistivity level that can be achieved with bulk silicon while guaranteeing stability, mechanical strength and affordability.

Other limitations of HR silicon are its relatively small bandgap and high dielectric constant. A 1.1 eV bandgap implies that the number of intrinsic carriers in the bulk silicon, which increases with temperature, becomes higher than the residual wafer doping in the range from 50°C to 90°C. Above this temperature, the resistivity and associated RF performance start degrading (see ***Figure 6***). While this is not an issue for most applications, some require performance stability to 150°C, such as grade 1 and 2 automotive. These applications require materials with resistivity independent of temperature.

Soitec has built SOI wafers with

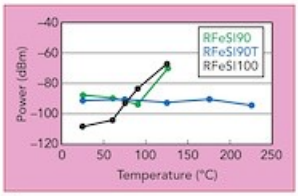


Fig. 6 RFeSI second harmonic power vs. temperature.

Fig. 7 Second harmonic vs. ε for porosification setups yielding steep and shallow trade-offs.

a porous silicon layer, which can be viewed as thin silicon membranes separated by gaps. It presents a huge surface area, on the order of 500 m^2/cm^3, so the many dangling bonds and surface states act as traps. Because the silicon membranes are so thin, all carriers are within trapping distance of the surface and are also subject to coulomb scattering. This ensures a low free carrier concentration and mobility, even when the temperature rises. The benefits of porous silicon for RF applications are well known, with demonstrated temperature stability on relatively thick layers, usually greater than 50 µm.[12,13]

Using SOI wafers and a thin buried porous silicon layer, to our knowledge, Soitec is the first to demonstrate very low HD levels and complete independence versus temperature up to 200°C, as shown in Figure 6. This performance has an added benefit: because porous silicon is essentially a composite material of silicon and empty spaces, its permittivity is lower than the usual 11.7. Thus, the transmitted signal sees a material with a reduced effective permittivity, which benefits HD, IL and signal isolation.

The effective RF performance and permittivity of porous silicon layers is dependent on the porosification process and material properties, such as porosity level, structure type, pore size, surface state and thickness. This is illustrated in ***Figure 7***, which shows second harmonic power versus permittivity when different trade-off configurations are used to fabricate the porous silicon layer. The figure shows obtaining adequate performance, temperature stability and low permittivity requires the proper fabrication process.

CONCLUSION

This article illustrates how substrate engineering brings additional linearity and value for RF and mmWave applications. Measurement setup and extraction procedures enable evaluating the substrate performance through representative metrics. With a physical understanding of material properties, the EM behavior of the sub-