Planar Leaky-Wave Antenna Design on Thick Substrate by Radiating Surface Waves Using Strip Rings

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***Abstract*—This paper presents a comprehensive analysis of a 75 GHz dipole-slot antenna on ultra-low loss Silicon (Si) combined with metallic strip rings to allow surface wave (SW) conversion into leaky-wave (LW) radiation. First, the influence of the die dimensions on the radiation pattern (RP) is studied on a simple dipole-slot antenna. Then, the design of surrounding metallic ring strips is performed. Through both measurements and simulations, an improvement of the antenna gain and a reduction of uncontrolled radiation from the chip edges are demonstrated. The results show an enhancement of the antenna gain of more than 5 dB by adding the rings, to reach more than 7.9 dBi for each test structure, and an impedance bandwidth of 10 GHz. This study provides valuable insights on the design of metallic strip rings for SW conversion into LW for planar antennas solutions at mm-wave frequencies on thick substrates.**

Keywords—dipole-slot antenna, trap-rich substrate, low profile antenna, chip-size insensitivity, surface waves, leaky wave

I. Introduction

On-chip Si antennas enable direct integration with front-end circuitry, reducing connection loss and parasitic effects while facilitating co-design. Yet, they often suffer from poor radiation efficiency and low gain due to the high permittivity and loss of commonly used substrates. A widely used strategy is to shield the substrate with a metal layer in between but this leads to reduced bandwidth and efficiency due to the proximity of such a reflector [1]. An alternative solution is to place a metal plane below the substrate. In this case, the use of an ultra-low loss trap-rich high-resistivity (TR HR) Si substrate suppresses substrate losses and leads to an increase in antenna efficiency [2]. However, the unshielded thick Si substrate also implies the excitation of SWs which lead to uncontrolled radiation from the chip edges. This effect is exacerbated when using TR-HR substrates due to the very low attenuation of the SW. Solutions have been proposed in the literature to reduce such SW on electrically thick substrates, including via fences [1], air cavities [3], or artificial magnetic conductors [4]. However, these methods require additional processing steps that are not part of conventional CMOS processes. The simplest and more common solution is to use an Si-lens to avoid SWs and increase the antenna gain [5]. This solution is however not compatible with planar applications. Another emerging option is to use antenna arrays in a configuration that leads to a partial cancellation of SW modes [6], but this solution constrains the array geometry based on the SW distribution and would lead to high ohmic losses when using a single thin metal layer, as in this study.

In this paper, we present a new planar solution to reduce the RP dependence on the chip dimensions for a single metal layer antenna on an ultra-low loss unshielded Si substrate, making it compatible with most Si-based processes. A dipole-slot antenna is first designed to demonstrate the strong gain dependence on the die dimensions. Then, a new holographic-based solution is proposed by adding metallic strip rings [7] around the antenna on the same metal layer to convert part of the trapped SW into LWs. Finally, the measurement setup is described and comparisons between simulated and measured S_{11} and RP for the two studied structures on several die dimensions are conducted.

II. Design of Antennas

Fig. 1(a) shows the designed 75 GHz dipole-slot antenna with its dimensions. The antenna has been processed on a 300 µm-thick metal-backed TR HR Si substrate with a 1 µm-thick layer of aluminum. On such a low-loss substrate, the fundamental SW mode TM_0 is excited and scatters at the edges of the chip. This causes constructive and destructive interference in the radiation mechanism in the far-field of the antenna and induces chip size-dependent variations of the antenna gain, as shown in Figs. 2 and 3, where simulated RP are plotted at 75 GHz for several values of DieX and DieY (pink curves). The variation of the antenna RP with the die dimensions is a challenge for on-chip antenna design, as these dimensions depend on the active circuit configuration. Means of reducing this effect are therefore coveted.

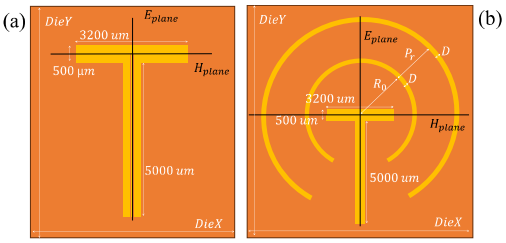

Fig. 1. (a) Dipole-slot antenna. (b) Dipole-slot antenna with strip rings.

To reduce the RP dependence on the die dimensions and increase the gain, a holographic-based design variation is proposed by placing 2 metallic strip rings around the antenna (Fig. 1(b)). These periodic rings convert the SWs into LWs, which are defined by an elevation beam angle θ that is well known for off-broadside angles [7]:

$$\theta \approx \sin^{-1}\left(\frac{\beta_{TM0}}{2\pi/\lambda_0} - \frac{\lambda_0}{P_r}\right)$$

Where β_{TM0} is the phase constant of the SW mode, P_r the period of the metallic strip rings in the radial direction and λ_0 the free space wavelength. The beamwidth can be controlled by the strip width (i.e. D in Fig. 1(b)) [7]. Contrary to [7], the SW launcher lies on the same layer as the strips, which is an essential advantage in terms of fabrication. Using these design principles and extracting the SW propagation constant [6], the dimensions have been fixed to P_r = 2000 µm, D = 200 µm and R_0 = 2500 µm using 2 rings, leading to a maximum gain around $\theta \approx -8°$ at 75 GHz. Figs. 2 and 3 show the simulated RP of the dipole-slot antenna with rings at 75 GHz for several values of DieX and DieY (blue curves). A reduced RP dependency on the die dimensions is demonstrated as well as an increase of the gain by more than 5 dB for all the dies compared to the simple dipole-slot solution. For each die, the gain reaches values above 8.5 dBi with deviation value below 1 dB at $\theta \approx -8°$.

III. Measurement Results

For the on-chip antenna measurements, the spherical system presented in [8] was used. The setup is depicted in Fig. 4(a).

To reduce the effect of the on-wafer probe and the metal chuck on the measured RP, the frontside of the probe and the chuck were covered with mm-wave absorbers (see Fig. 4(c)). Their effect is sketched in Fig. 4(d). To account for these phenomena, a 3D probe model was included in the simulation as shown in Fig. 4(b).

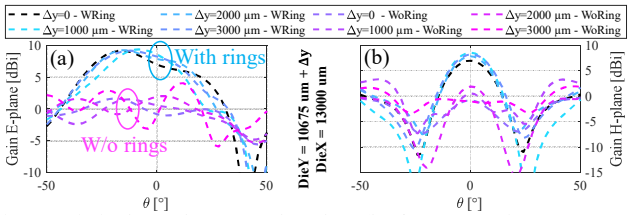

Fig. 2. Gain in the E-plane (a) and H-plane (b) @75 GHz; DieY Sweep.

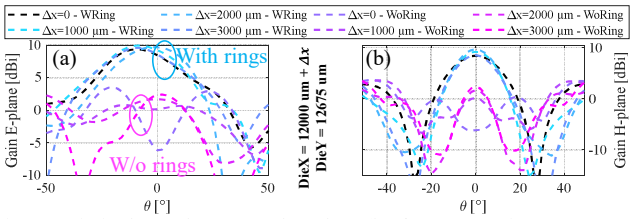

Fig. 3. Gain in the E-plane (a) and H-plane (b) @75 GHz; DieX Sweep.

The probe body was modeled as a PEC and the HFSS-IE hybrid solver from Ansys was used. The gain of the antenna under test (AUT) was extracted by comparing the measured S_{21} parameter with a known horn antenna and compensating for the losses of the mm-wave probe by determination of the error terms using on-wafer calibration.

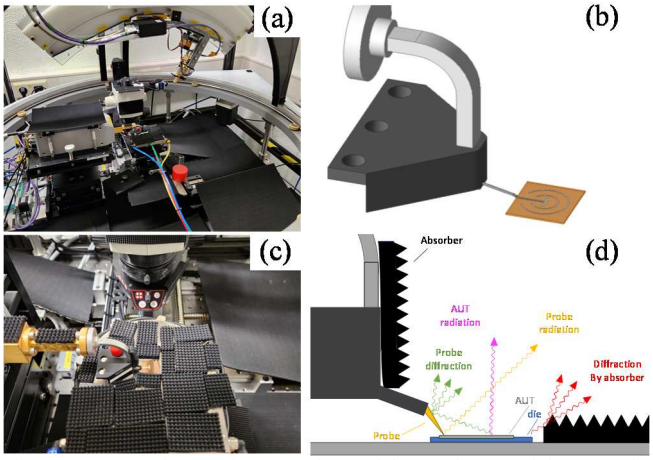

Fig. 4. (a) Setup picture. (b) 3D probe model. (c) Closeup of the on-wafer probe and absorbers. (d) Sketch of the effect of the absorber and the probe.

Both antennas with and without metallic rings were processed on dies of variable DieY values = {10675 µm, 11675 µm, 12675 µm, 13675 µm} and fixed DieX = 13000 µm, for a total of 8 test structures. The RP on the E- and H-planes (defined in Fig. 1) at 75 GHz are compared with simulations in Fig. 5. The return loss (not shown here) was also obtained through both measurements and simulations and was observed to be dependent on chip dimensions for the AUTs without rings while giving the same response on all chips when the rings are present. That confirms depletion of the SW before reaching the chip edges. Those data (not shown) confirm that the antennas reach an impedance bandwidth of 10 GHz around 72.5 GHz and good correlation between measured and simulated S_{11} parameter is obtained. For the characterization of the RP, the E-plane cut only covers a range of -10° ≤ θ ≤ 50°, since smaller angles suffer from shadowing from the probe. In the H-plane, very good agreement between measured and simulated gains is observed, as depicted in Fig. 5(b), while it is only the case for -10° ≤ θ ≤ 0° in the E-plane. For higher elevation angles, a deviation is observed between simulation and measurements, likely due to the probe that affects the gain by reflection and scattering of the antenna radiation as well as direct radiation, as observed in [9]. This deviation is still increased for the test structures without rings, likely due to the absorbers close to the AUT that scatter the radiated waves at the edges of the die (see Fig. 4(d)), which is not considered in the simulations. The measured gain at $\theta = -5°$ ranges from 7.9 to 9.5 dBi for the test structures with metallic rings. An overall gain improvement of more than 5 dB is also observed in this direction compared to the test structures without rings, as well as a reduced RP dependence on the die dimensions, in accordance with the simulation results.

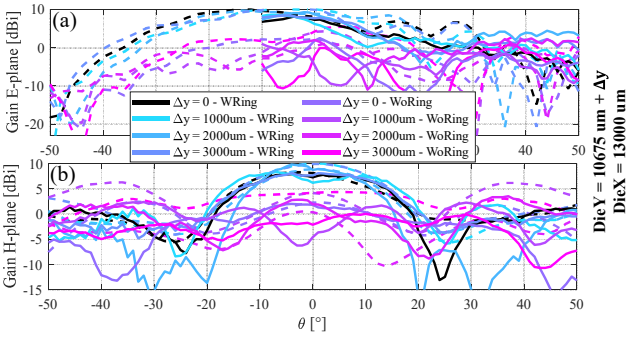

Fig. 5. Gain vs θ in E-plane (a) and H-plane (b) @75 GHz. Dotted lines are simulations (with the probe) and continuous ones are measurements.

IV. Conclusion

In this article, a 75 GHz dipole-slot antenna was designed and tested to demonstrate the dependence of the RP on die dimensions suffered by antennas on ultra-low loss metal-backed Si substrates. The most common techniques for reducing the stray radiation due to SW diffraction at the chip edge were reviewed. Then, we presented a new holographic-based solution by adding metallic strip rings around the antenna to convert part of the trapped SW into LWs. Based on simulation and measurements results, a clear gain improvement of more than 5 dB is observed as well as a reduction of the RP dependence with die dimensions. Consequently, this single metal layer design is an efficient solution for reducing the undesirable effect of SWs for planar antennas on thick substrates without using additional wafer treatment such as vias through the silicon or backside etching.

References

[1] S. -Y. Tang et al., IEEE Trans. Antennas Propag., vol. 71, no. 9, pp. 7184-7195, Sept. 2023.
[2] N. André et al., IEEE Journ. Electron Devices Soc., vol. 7, pp. 393-397, 2019.
[3] A. E. I. Lamminen et al., IEEE Trans. on Antennas Propag., vol. 56, no. 9, pp. 2865-2874, Sept. 2008.
[4] D. Sievenpiper, et al., IEEE Trans. Microwave Theory and Techn., vol. 47, no. 11, pp. 2059-2074, Nov. 1999.
[5] A. Krysl et al., 47th IRMMW-THz, Delft, Netherlands, 2022, pp. 1-2.
[6] V. Lammert, et al., IEEE Trans. Antennas Propag., vol. 70, no. 8, pp. 6683-6691, Aug. 2022.
[7] S. K. Podilchak, et al., IEEE Antennas Wireless Propag. Lett., vol. 7, pp. 155-158, 2008.
[8] B. Sievert, et al., IEEE Access, vol. 8, pp. 89680-89691, 2020.
[9] L. Boehm, et al., 46th EuMC, London, UK, 2016, pp. 552-555.