Wafer-Scale Nanoimprint Lithography Process Towards Complementary Silicon Nanowire Field-Effect Transistors for Biosensor Applications

*Achim Müller, Xuan T. Vu, Vivek Pachauri, Laurent A. Francis, Denis Flandre, and Sven Ingebrandt**

The authors present a combined, p- and n-type fabrication process for silicon nanowire field-effect transistor (SiNW FET) biosensors on a 4" wafer format with nanowire widths down to 100 nm and a height of only 42 nm. The full wafer design includes various SiNW FET combinations with metal or electrolyte gate contacts. A top-down fabrication protocol on high-quality silicon-on-insulator wafers is developed. Down-thinning of Si is done by a modified CMOS cleaning solution, which gives the possibility to control the resulting thickness with sub-nm precision. The structuring of SiNW FETs is realized by nanoimprint lithography (NIL) applying a special temperature/pressure profile. The authors fabricate nano-scale sensor structures and micro-scale contact lines in the same NIL step. Precise control of the imprinting procedure is important for complete filling of the structures. In this project, the authors aim towards complementary device combinations and therefore they characterize the threshold voltage dependency on the device structures. Back-gate contacts at the front-side of the chips enable a control of surface potential shifts. The new SiNW FET sensors can be utilized for biomedical applications, where they are operated in a liquid environment under double-gate configuration using parallel front gating and back gating.

1. Introduction

The ion-sensitive field-effect transistor (ISFET) was firstly described in 1970 by P. Bergveld.[1] Downscaling of this device concept to silicon nanowire field-effect transistors (SiNW FETs) found a wide field of potential applications such as pH sensing,[2–6] drug discovery,[7,8] DNA,[4,9] protein,[10,11] and virus detection.[12,13] Fabrication of such devices can be realized by either bottom-up or top-down methods, where most of the bottom-up techniques show poor growth control and alignment problems in the resulting sensor chips. Top-down methods, e.g., electron-beam,[14] nanoimprint-[5] and dip-pen lithography[15] are easier to control and are suitable for industrial upscale. Electron-beam and dip-pen lithography have disadvantages be cause of long writing times and high fabrication costs, which makes them unsuitable for medium scale fabrication in an academic setting. In contrast to this, nanoimprint lithography (NIL) is a very promising technique that, however, requires a predefined mold and does not offer the same flexibility as electron-beam processing. As a big advantage it offers rapid, wafer-scale structuring of micro- and nano-structures in one-step. In this report, we describe a combined p-type and n-type, top-down fabrication protocol using NIL as primary structuring technique for parallel fabrication of 352 chips on a 4" wafer scale format. All following structuring steps were done by photolithography and the alignment of the NIL structures to the following steps was a technological challenge. We present nanowires (NW) structured via NIL down to 100 nm in top width and only 42 nm in height with a length of 7 μm. Before structuring the NWs out of the top Si layer of the silicon-on-insulator (SOI) wafers, the Si was thinned down using a standard cleaning solution of a CMOS process. This method of top Si thinning is therefore fully CMOS compatible. Compared to our earlier used sacrificial oxidation process it poses less thermal and mechanical stress, it enables very precise thickness control, low surface roughness, and a hole carrier mobility close to the one of bulk silicon.[16] In a previous publication of our group we showed stable pH sensing for n- and p-type SiNW FET devices, where devices without ion implantation of the contact lines already showed an n-type characteristics.[9] In the process

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described here, we realized n-type and p-type SiNW FETs by implantation of their contact lines using phosphorous- or boron-doping, respectively. In our project we are aiming toward complementary device combinations for biosensors with signal pre-amplification on chip. In this first wafer design, we varied nanowire dimensions and combinations of n-type and p-type devices in order to extract parameters and to later simulate the device performance for future designs with the desired combinations. To balance and precisely control the nano-scale devices, we included back-gate contacts to the Si substrate in all designs, where the buried oxide (BOX) was opened and etched through to the handle silicon layer of the SOI wafers for further implantation and metallization. After metallization, these back-gate contacts were accessible on the same side as all the other contacts. In earlier works, it was shown that a precise control of the back-gate potential is crucial for stable operation of SiNW FET devices in a liquid environment.[9]

For the fabrication process described here, we used thermally grown, ≈7 nm thick SiO_2 as gate dielectric and a photoresist as simple passivation layer to enable first electrical characterizations. We present the transfer characteristics of nanowire ion-sensitive and metal-oxide-semiconductor field-effect transistors (ISFETs and MOSFETs), which will be used as control sensors for the liquid-gate operation of the n–p combinations. In a follow-up fabrication run, we will include other gate dielectric materials in order to achieve reliable ISFET performance of our SiNW biosensors.

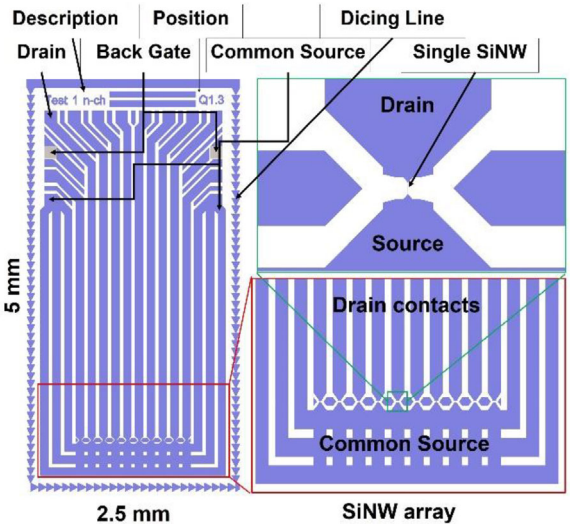

Figure 1. Design of the SiNW FET arrays: on the left side a single dipchip is shown. One chip measures 2.5 × 5 mm^2 and typically contains eight individually addressable SiNWs, located at the bottom of the chip, while sharing a common source contact. Contacts for wire bonding are located on top of the chip. Filling structures with no electrical function were integrated between the contact lines to guarantee a conformal filling of the resist during NIL. All chips and their position on the wafer are labeled (description and position). Two back-gate contacts are included at the front-side of the dies. At the right bottom a closer look to a SiNW array is shown. A further zoom on top shows an example of an individual SiNW transistor contacted by drain from the top and source from the bottom. The structures at the left and right are the filling structures for NIL. In other designs of our full wafer process, different combinations of n-type and p-type SiNWs were included, while in other designs as discussed below, the SiNWs were contacted by metal gate contacts (compare Figure 7).

2. Experimental Section

2.1. Sensor Design

The design of the SiNW FET devices included chips with a dipchip configuration (5 × 2.5 mm^2). A typical dipchip design is shown in **Figure 1**a. The nanowires are placed at the bottom of the chip, which can be dipped into the analyte solution. We varied nanowire dimensions and included several n–p test combinations. In total 26 different designs were resulting in 324 dipchips per wafer. The main goal of our test design was to realize n- and p-type FETs with metal and liquid gates for comparison of their electronic performance. Here we present SiNW FET designs having a metal gate contact with wires of physical length of 7 µm (5 µm electrical length, due to alignment gap of the implantation mask) or simple opening in the passivation down to the gate oxide material for electrolyte gate contacts. SiNWs had different widths from 1 µm down to 100 nm (mask measures) for characterizations.

2.2. Process Flow

The fabrication of the SiNW FETs was done in the clean room of the University of Applied Sciences Kaiserslautern, Zweibrücken, Germany. Prime grade, 200 mm SOI wafers were purchased from SOITEC, France. Two different batches were used, while the first batch had a starting device layer thickness of 205 nm and a resistivity of 8–22 Ωcm and second batch had a 142 nm device layer thickness and 14–18.9 Ωcm resistivity. Both had a BOX thickness of 400 nm and a crystallographic orientation of (100) ± 0.5°. The 200 mm wafers were too large for our 100 mm process line. Prior to fabrication, we cut them down to a diameter of 100 mm by an Nd-YAG laser available in our facilities. Before cutting we used a protective coating on both sides of the wafers. After cutting, the wafer edges needed to be polished by hand with sand paper and DI-water. The applied process flow for the chip fabrication is illustrated in **Figure 2** and was very similar to the one shown earlier in our group[5] with some modified steps, which will be discussed in Section 3.

The thinning effect of Si using the standard cleaning one (SC1) solution of a CMOS process was presented earlier.[17] Tang and co-workers[16] presented a modified SC1 solution for SOI wafer thinning for MOSFET fabrication. Here we used solutions of (NH_4OH:H_2O_2:H_2O) with different ratios and different temperatures as detailed in Section 3. All chemicals for the wet chemical processes had VLSI grade in order to avoid metal contaminations of the Si. After down thinning, a 35 nm thick, thermal SiO_2 was grown on the top Si layer in dry O_2 conditions at 1000 °C for 30 min. This SiO_2 layer was later used as hard mask for anisotropic wet etching.

The second step was NIL structuring of the nano-scale SiNW structures and the micro-scale contact lines in one step as illustrated in Figure 2d. The structure transfer from the NIL

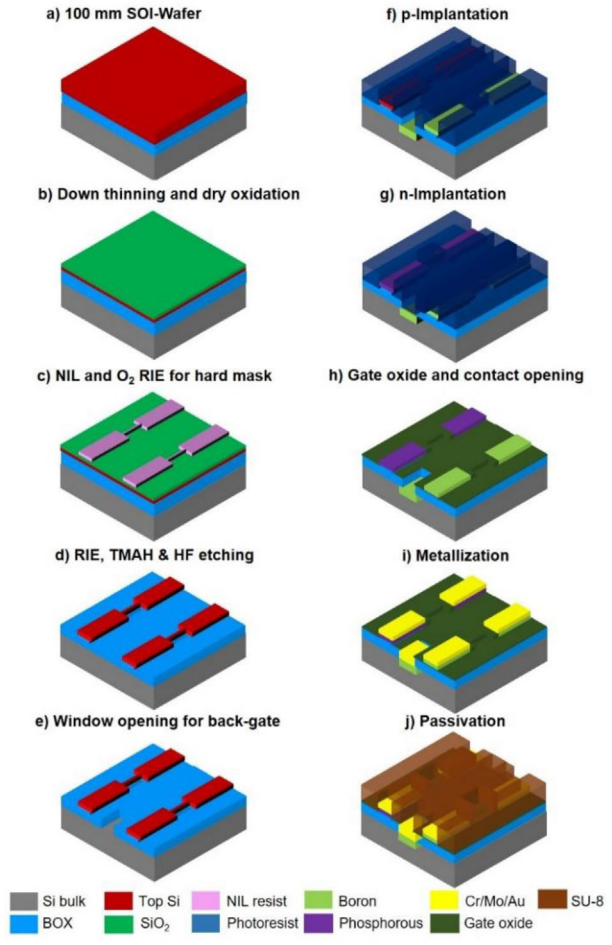

Figure 2. Process flow of our combined SiNW process (from top to bottom): after wafer cutting, down thinning and oxidation the micro- and nanostructures were formed in one step by NIL, RIE, and wet etching. Then back-gate contacts were defined followed by two implantations for p- and n-type devices. After forming the gate dielectrics by dry oxidation of Si, the contact lines were metallized by a sandwich layer of Cr, Mo, and Au and passivated with a photoresist for initial characterization of the devices in liquid environments and for comparison to their MOSFET counterparts.

resist into the SiO_2 hard mask was done by CHF_3 RIE etching. The silicon wet etching was then done by tetra methyl ammonium hydroxide (TMAH) at 70 °C. After TMAH etching, the hard mask was removed by hydrofluoric acid (HF), resulting in the SiNW device structures with contact lines.

The technique for NIL was already presented in 1995.[18] Since then many variants using thermal or UV curing of the resist were described. Nowadays NIL is widely used for nanostructuring in academic setting as well as in some industrial processes.[19] We used a 6 inch silicon mould with 200 nm deep structures based on our design, which was fabricated by the Institut für Mikroelektronik (ims chips) Stuttgart, Germany. NIL was done on our Eitre 6 Nanoimprint Lithography system from Obducat Technologies, Sweden with a thermoplastic NIL-resist (mr-I 7030, Micro Resist Technology, Germany) of 300 nm thickness. Wafer bending during NIL can occur while imprinting or demoulding.[20–23] We had problems with the wafer holder in our system, which also caused wafer bending and left the alignment of the following photolithography masks a technological challenge. For better control of the imprinting time, our optimized NIL procedure differed significantly from the one recommended in the resist datasheet. The difference of both processes and the adaptation of the NIL protocol to successfully realize the wafer-scale process in a high yield will be discussed in Section 3.

For the back-gate opening, which was done by HF etching, we used a positive resist as mask layer structured by photolithography. The back-gate contacts give the possibility to operate the devices in dual-gate configuration. This configuration can be used to shift the working point of a single device and to improve its electrical stability during detection.[24–26]

All following implantation steps were done at Ion Beam Service (IBS), France. We used boron doping and a positive resist (≈1.5 µm thickness) as masking material. This is usually not allowed in a CMOS process, but for us it was the easiest procedure to protect the nanostructures without posing additional thermal or mechanical stress during processing. Due to the low energy implantation, we had no problem with eventual resist hardening during implantation. The boron implantation was realized with low energy of 10 keV, a dose of 10^{15} atoms cm^{-2}, and a tilt of 0°. The back-gate contacts were also opened for this p-implantation to reduce the contact resistance. Annealing was done in a high temperature furnace at 850 °C (for 30 min) in a nitrogen atmosphere. N-type implantation was done in a second implantation step with phosphorous ions. An energy of 15 keV, a dose of 10^{14} atoms cm^{-2}, and a tilt of 7° were used here.

As gate dielectric material, a 7 nm thick SiO_2 was grown in dry O_2 conditions at 820 °C for 45 min. After gate dielectric formation, the contact lines were opened by HF and a metal stack of 10 nm Cr, 150 nm Mo, and 200 nm Au was deposited by evaporation and structured by lift-off. This metal stack was used for the gate metal contacts of the MOSFET structures and as bond pad material for all contacts. Cr was necessary to ensure adherence to the silicon, Mo was necessary to avoid interdiffusion of the metal on the MOSFET structures, and Au was used to lower the contact line resistances and for reliable wire bonding. Passivation of the contact lines was realized by a 1 µm thick SU-8 layer to enable first functional tests in an electrolyte solution.

The device encapsulation was done after die-and wire-bonding by polydimethylsiloxane (PDMS, 96-083, Dow Corning, Germany). **Figure 3** shows a finally encapsulated dipchip. It can be seen that the chip's sidewall and back side were also encapsulated by PDMS to reduce leakage currents when the whole chip was dipped into the analyte solution. Pin connectors were soldered to the PCBs for first electrical characterizations as discussed in Section 3.

2.3. Methods of Threshold Voltage Extraction

Ortiz-Conde and co-workers[27] compared several extraction methods for the threshold voltage V_{TH} and showed that 7 out of 11 tested methods showed very similar results. For this work we

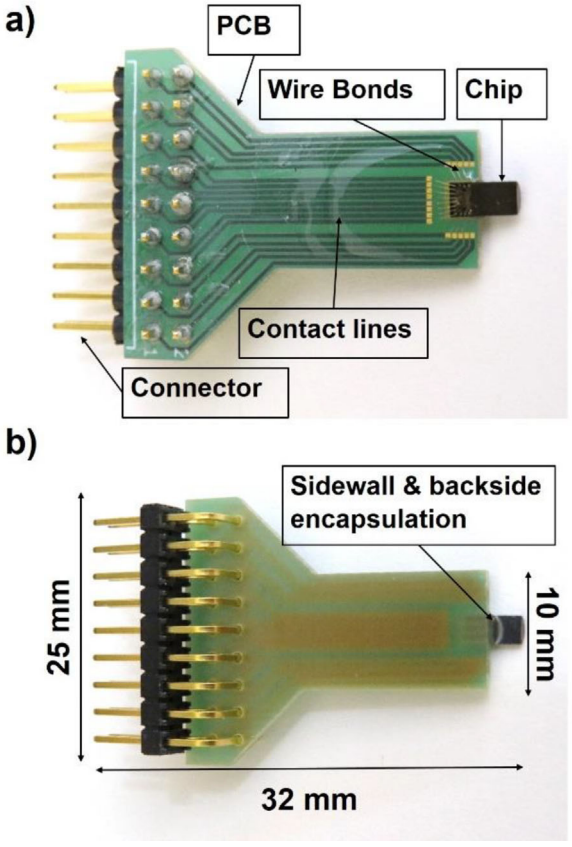

Figure 3. a) Top- and (b) bottom-view of an encapsulated dipchip with a total length of 32 mm, a small width of 10 mm (right) and a big width of 25 mm (left). On the right side, the silicon die can be seen which was contacted onto a PCB by wire bonding. The wire bonds, the side walls, and the back side of the chip were encapsulated by PDMS.

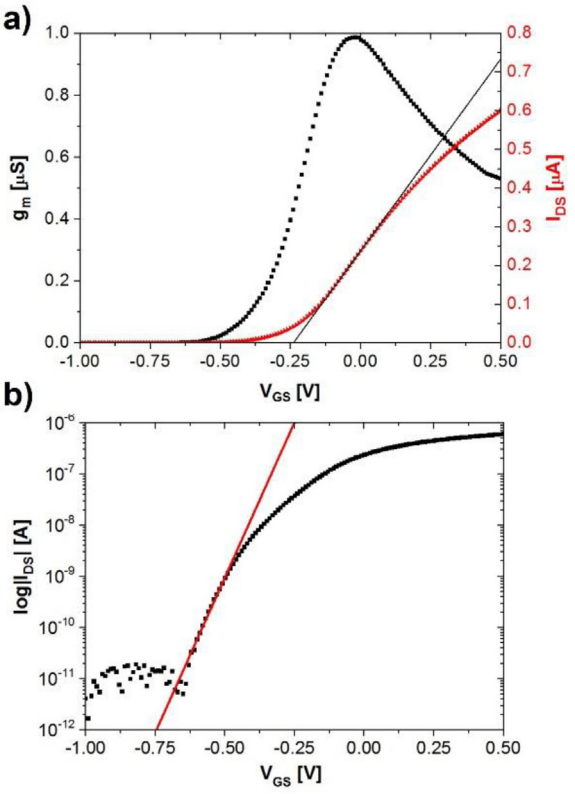

Figure 4. Extrapolation methods shown on two different, exemplary SiNW devices: (a) extrapolation method for the threshold voltage V_{TH} in linear regime. the left axis is showing the transconductance g_m and the right axis the drain-source current I_{DS}. The *x*-axis intercept of the linear extrapolation corresponds to V_{TH} and its slope to the k factor. b) Extrapolation method for the threshold voltage using the subthreshold slope *S*. This example was taken from a n-type SiNW ISFET where the back-gate was grounded.

applied the "extrapolation in linear region" method, meaning that around the point of highest transconductance a linear regression was realized and the *x*-axis intercept of this linear function was defined as the V_{TH} as illustrated in **Figure 4**a.

In linear mode the drain-source current is given by the following equation:

$$I_{DS} = k \cdot (V_{GS} - V_{TH}) \cdot V_{DS} \quad (1)$$

with I_{DS} is the drain to source current, k the slope, V_{GS} the gate-source voltage, V_{TH} the threshold voltage, and V_{DS} the drain-source voltage.

In total 11 measurement points were used for extrapolation fits resulting in a fitting range of 100 mV. For electrical characterization, a dual sweep procedure (from negative to positive and vice versa) was applied to work out eventual hysteresis effects. The measurements were done on a wafer prober with high resolution supply and measurement units (HRSMU) integrated in the Agilent 4156C parameter analyzer. The extrapolation for the subthreshold slope (S) was realized from I_{DS} values of $2 \times 10^{-11}\,A < I_{DS} < 2 \times 10^{-9}$, where *S* is the inverse of the extracted slope (Figure 4b) in units of $mV\,dec^{-1}$.

3. Results

3.1. Optimization of the Fabrication Protocol

For wafer thinning we used NH_4OH (28–30%):H_2O_2 (30%): H_2O (1:1:5) at 68 °C and we observed an etch rate of $0.35\,nm\,min^{-1}$. A composition of 1:4:20 at 74 °C resulted in a slightly smaller etch rate of $0.32\,nm\,min^{-1}$ and a composition of 1:2:10 at 74 °C in a larger rate of $0.46\,nm\,min^{-1}$. Tang and co-workers[16] presented an etch rate of $0.66\,nm\,min^{-1}$ with a composition of 1:8:64 at 70 °C. Nakajima and co-workers[28] reported an etch rate of $0.4\,nm\,min^{-1}$ with a ratio of 2:2:5 at 70 °C. This etch rate fits better to our results. However, we found that when increasing the amount of NH_4OH in the solution the etch rate increased, which also fits well to another report.[29]

In order to counteract the mentioned bending problems in our NIL tool and to reach a complete filling of all nano- and microstructures of our wafer design, we needed to adjust the protocol for imprint. In **Figure 5**, it is shown that in this modified NIL protocol the pressure was reset to ambient pressure before cooling down. This resulted in a fast and precisely controllable imprinting time. With the imprinting procedure recommended

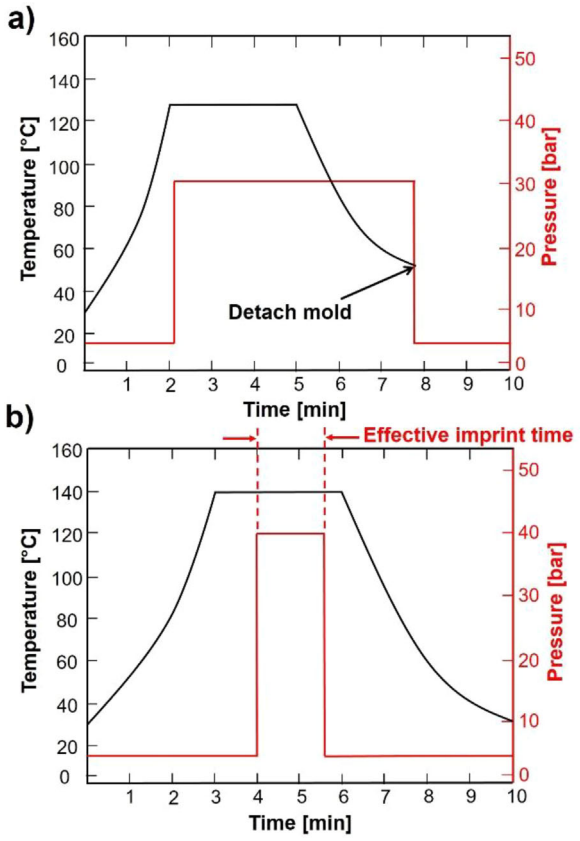

Figure 5. a) Nanoimprint protocol as recommended in the datasheet of the imprint resist mr-I 7030 and (b) our optimized imprint procedure (bottom) to fill the micro- and nanostructures of our design in a single NIL step. In our protocol the effective imprinting time can be much more precisely controlled, which was particularly important for complete filling of the microstructures.

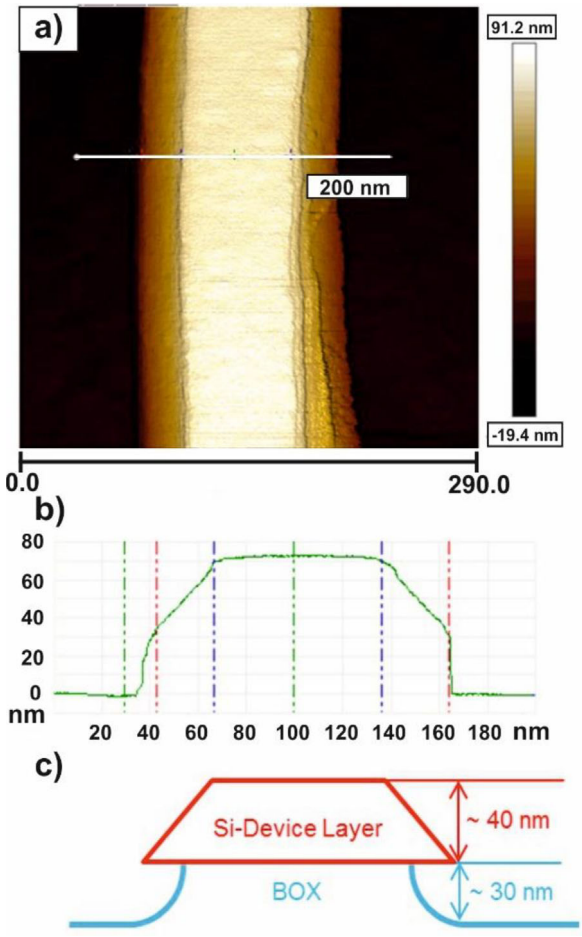

Figure 6. AFM characterization of a 100 nm wire after TMAH etching: (a) shows the AFM image of 290 nm width. The line scan in (b) shows the top profile. As it is known from our previous processes, the real cross section would look like it is depicted in (c) resulting from an under etching of the BOX.[9]

in the datasheet of the resist, the effective imprinting time was strongly dependent on the cooling time, which was difficult to control in our NIL tool. As long as the temperature was higher than the glass transition temperature of the resist, the standard protocol resulted in uncontrollable behavior with high risks of over-imprinting and hence non-functional nanowires after etching.

We also observed that finding the ideal imprinting parameter for SOI substrates was even more difficult than for Si bulk substrates. This is most likely due to the different thermal conductivity and mechanical properties of the wafers. The thickness of the BOX layer had an influence to the ideal imprinting time as well. This we observed when using a dummy SOI wafer with thinner BOX (144 nm instead of 400 nm), where a much higher imprinting time was needed compared to the thicker BOX layer wafers. Also the wire width played a significant role for the over-imprinting effects. The narrower the wire, the easier an over-imprinting occurred.

The resulting nanowires were characterized by AFM and a typical scan image of a 100 nm wire is shown in **Figure 6**. The AFM measurement shows a top and bottom width of ≈75 and ≈125 nm of the trapezoidal structure, respectively. The height of the silicon after hard mask removal was 42 nm, meaning that about 16 nm of Si was consumed by the thermal SiO_2 growth, which fits well with our oxide hard mask thickness of 35 nm. Figure 6c illustrates the cross section of a wire with its typical trapezoid structure resulting from the anisotropic wet etching with TMAH as earlier described.[9]

3.2. Electrical Characteristics

Figure 7 is illustrating schematics, microscopic pictures, and transfer and output characteristic for p- and n-type and MOS- and ISFETs, respectively. For this characterization 300 nm wide SiNW devices were used. In general, higher I_{DS} currents are visible for the n-type devices due to the higher mobility of electrons compared to holes as expected from silicon transistors. Also for the n- and p-MOSFET pairs the characteristics is not fully symmetrical in terms of V_{TH}. In order to gain complementary p–n combinations of devices, we would need to scale the SiNW width to counteract for the different mobilities as in classical CMOS processing.

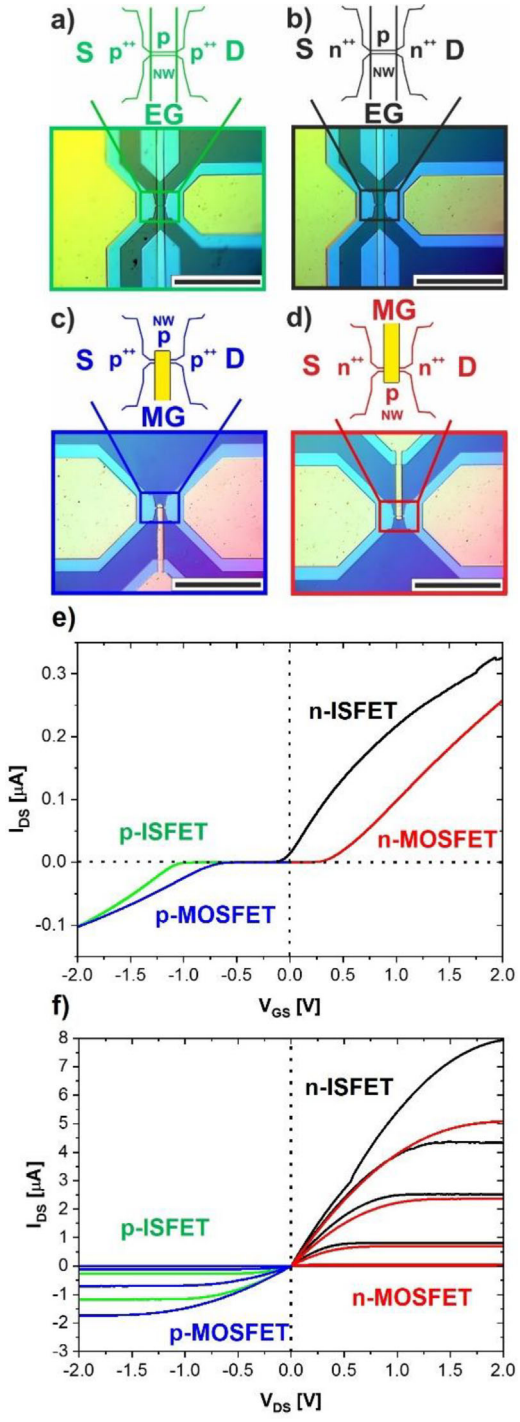

Figure 7. Schematic and microscopic image of SiNWs as (a) p-type ISFET, (b) n-type ISFET, (c) p-type MOSFET, and (d) p-type MOSFET (scale bars 100 µm). Note that the structures in the images are rotated by 90° compared to the layout shown in Figure 1. ISFET SiNWs are contacted by an electrolyte gate (EG), while MOSFET SiNWs s are contacted by a metal gate (MG) as indicated in the schematics. e) Transfer characteristic and (f) output characteristic of the different types with same width of 300 nm for the SiNWs (mask measures). For the transfer characteristics a V_{DS} of 50 mV (−50 mV) was used. For the output characteristic V_{GS} was stepped from 0 to 2 V for n-type and from 0 to −2 V for p-type devices with a step size of 0.5 V.

As expected, the threshold voltage of the ISFETs is shifted to the left compared to the MOSFETs due to different work functions and the offset potential of the Ag/AgCl reference electrode. It can also be seen that the n-type ISFET has the largest currents, while already showing small kinks in the characteristic lines. In this configuration the SiO_2 gate dielectrics can become unstable and for a reliable biosensor operation in liquid environments other gate dielectric materials need to be used. When other gate oxide material are applied, as planned in our project, the shift in V_{TH} will be dependent on the type of material used. To control these bias voltage shifts due to work function and surface potential differences, the back-gate contacts of the SOI structures can be used.

3.3. Back Gating

Figure 8 shows the influence of the back gating to a 5 µm long and 1 µm wide, n-type MOSFET nanowire. Figure 8a illustrates the transfer characteristics for different back-gate voltages V_{BS} demonstrating that the devices behave as fully depleted SOI MOSFETs. Figure 8b illustrates the extracted threshold voltage V_{TH} and subthreshold slope S for a given back-gate voltage including a linear fit to extract the slope.

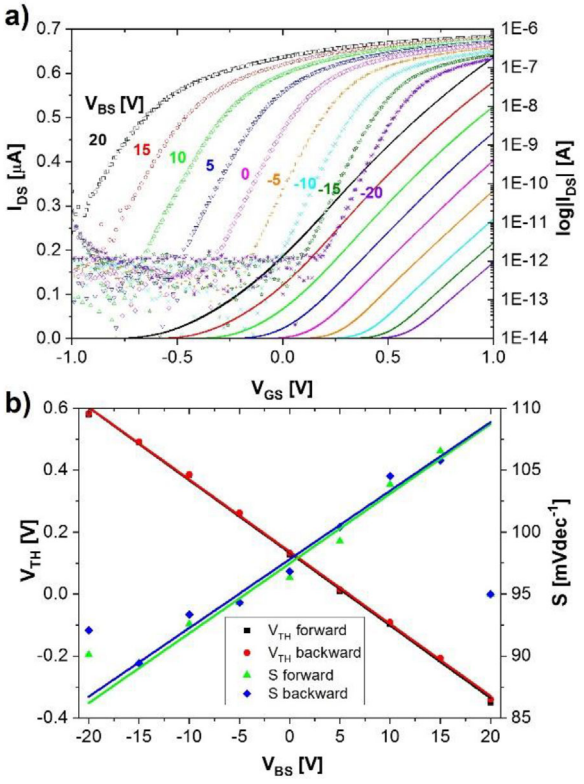

Figure 8. a) Transfer characteristics for different back-gate voltages V_{BS} and b) V_{TH}- and S-V_{BS} dependence including a linear fit for a 5 µm long and 1 µm wide n-type MOSFET nanowire with metal-gate contacts. Forward and backward scan show no hysteresis in V_{TH}. The drain-source voltage V_{DS} was 50 mV in all cases. Logarithmic and linear scales are bullets and lines, respectively.

It can be seen that the slopes of the threshold voltage in dependence to changes in back-gate voltage $\frac{\Delta V_{TH}}{\Delta V_{BS}}$ for forward and backward scans were 23.4 and 23.3 mV V^{-1}, respectively, showing that the threshold voltage is independent from electrical hysteresis in our devices. By the *y*-axis intercept of the linear fit, an offset of 4.14 mV in threshold voltage between forward and backward scan can be extracted representing a very small hysteresis. For the subthreshold slopes a back-gate voltage dependence $\frac{\Delta S}{\Delta V_{BS}}$ of 97.5 and 97.8 mV dec^{-1} V^{-1} for forward and backward scan can be extracted, respectively.

This characterization shows that the back-gate contacts of our devices are fully functional and can be easily used to balance bias voltage shifts due to different work functions of the gate dielectrics and different surface potentials in ISFET configurations for later n–p device combinations.

3.4. Width Dependency of FETs

In **Figure 9**a the dependency of V_{TH} to the SiNW width for different devices is shown. It can be seen that there is a difference of 415 ± 42 mV between MOSFET and ISFETs for the same SiNW width, which is too high to only account the offset potential of the reference electrode for this (DRIREF-2SH from World Precision Instruments). This behavior was also observed in earlier reports.[30–33] It was discussed that this effect is resulting out of trapped charges.[31,33]

Milgrew and co-workers[33] proposed a UV-light treatment to reduce this mismatch. Hammond and co-workers[32] reduced the mismatch between an ISFET and a reference FET (REFET) realized in a CMOS process run from 320 down to 15 mV. Further reading for an explanation of the difference in V_{TH} for MOSFETs and ISFETs can also be found in literature.[34]

Figure 9b shows the SiNW width dependence of the subthreshold slope. *S* was about 100 mV dec^{-1} for all devices and only for the very narrow SiNWs it decreased most likely caused by reduced carrier mobility due to scattering effects. Figure 9c illustrates the linear slope dependency on the mask width. It is shown that *k* is decreasing with decreasing width. This dependency, however, is not as linear as known from bulk MOSFET technology. However, for our planned n–p combinations, scaling of the device widths can be done to reach a better level of complementarity as the one shown in Figure 7. Subramanian and co-workers[35] showed an increasing effect of the sidewalls on the mobility degradation and postulated the following equation for the carrier mobility in FinFET structures:

$$\mu_{peak} = \mu_{v,peak} \cdot f_v + \mu_{h,peak} \cdot f_h \quad (2)$$

with $\mu_{v,peak}$ and $\mu_{h,peak}$ the mobility of the vertical and horizontal surfaces, respectively. f_v and f_h are the fractions of current flow along the vertical and horizontal surfaces which are given by

$$f_h = \frac{W_{fin}}{W_{fin} + 2 \cdot H_{fin}} \quad (3)$$

$$f_v = \frac{2 \cdot H_{fin}}{W_{fin} + 2 \cdot H_{fin}} \quad (4)$$

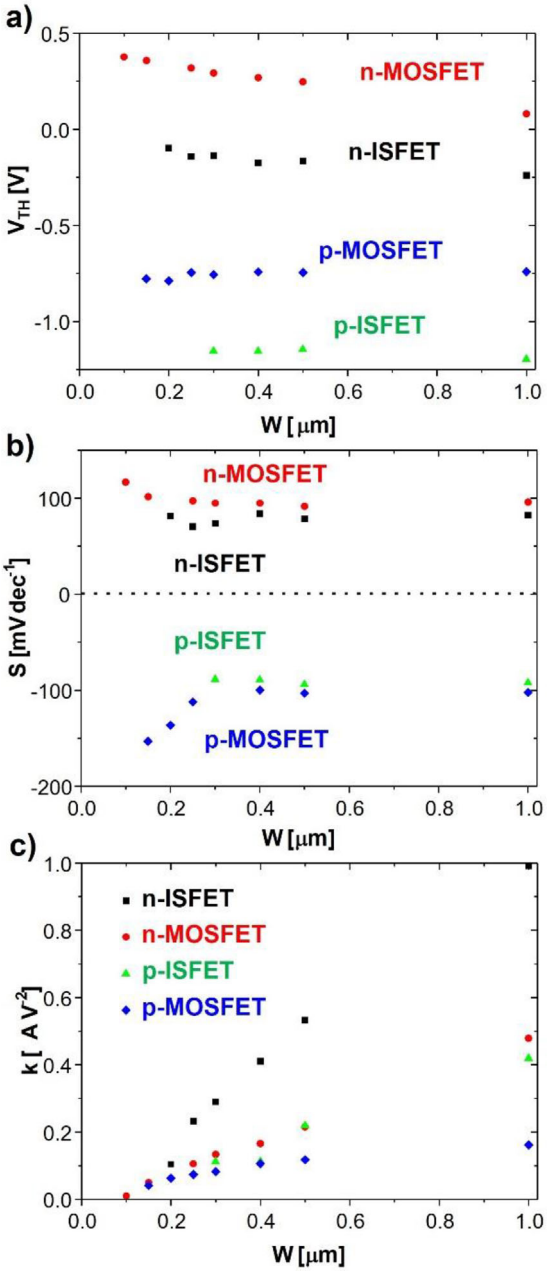

Figure 9. a) Threshold voltage (V_{TH}), (b) subthreshold slope *S*, and (c) the linear mode slope (k) dependence in relation to the SiNW width. It can be seen that the V_{TH} values for both device types shift to more negative voltages by about 0.4–0.5 V independent of the SiNW widths, which is more than the expected value caused by an offset potential of the Ag/AgCl reference electrode. The analyte solution used for the ISFET characterizations was a phosphate buffer at pH 7 and a concentration of 100 mM. The subthreshold slope *S* was about 100 mV dec^{-1} for all devices. Only for very narrow SiNWs it decreased most likely due to scattering effects.

with W_{fin} the width of the top surface and H_{fin} the height of the side wall. This relation is valid for FINFETs with 90° sidewalls that are etched by anisotropic dry etching methods. As we used an anisotropic wet etching process, the effect of the resulting geometry has to be added and the fin height has to be divided by the sine of 54.7° to get the length of the sidewall:

$$f_h = \frac{W_{fin}}{W_{fin} + 2.45 \cdot H_{fin}} \tag{5}$$

$$f_v = \frac{2.45 \cdot H_{fin}}{W_{fin} + 2.45 \cdot H_{fin}} \tag{6}$$

These equations are illustrating that this effect is higher for anisotropically etched NWs. In addition the sidewalls are in the (111) plane, where mobility is generally lower than in the (110) plane.

For all our n-type and p-type ISFETs, no front-gate leakage was observed within the applied voltage ranges. The n-type ISFETs had a depletion mode character with its point of highest transconductance at $V_{GS} = 0$ V, what makes them highly suitable for biosensing. In all characterizations, negligible electrical hysteresis was observed. Therefore, all fabricated devices are promising candidates for high performance biosensing applications.

3.5. Wafer-Scale Characterization

For such biosensor experiments, it is very important to have a reliable fabrication process with minimum sensor-to-sensor variation (on one chip) and minimum chip-to-chip variation, when using the same mask design. We characterized the quality of our full wafer fabrication process using the smallest structures of 100 nm SiNWs (mask measures). For the 100 nm wide, n-type MOSFET devices, 38 FETs distributed all over the wafer were characterized. A number of 26 devices worked without notable leakage currents resulting in a yield of 72.2% over the entire wafer for these smallest structures. The extracted threshold voltage was 0.65 ± 0.30 V with a maximum and a minimum value of 1.40 and 0.30 V, respectively.

The k-factor in linear regime was $5.6 \pm 2.9 \times 10^{-7}\,AV^{-2}$, whereas the maximum and minimum values were 11.5 and $1.1 \cdot 10^{-7}\,AV^{-2}$, respectively. The mean value and the standard deviation were calculated as follows:

$$\bar{x} = \frac{1}{n} \cdot \sum_{i=1}^{n} x_i \tag{7}$$

$$\sigma = \sqrt{\sum_{i=1}^{n} \frac{(x_i - \bar{x})^2}{n-1}} \tag{8}$$

where $\bar{x}$ is the arithmetic mean, σ the standard deviation, and n the number of samples.

Figure 10 shows a histogram of V_{TH} values and the k-factors in relation to the NW widths. The bins were always centered to the median value so that the measured data can be compared with the calculated Gaussian distribution. The width of the bins was calculated by Equation (9):

$$w = \frac{x_{max} - x_{min}}{\sqrt{n}} \tag{9}$$

where w is the width of the bin, x_{max} and x_{min} the maximum and minimum values, respectively.

The Gaussian distribution in Figure 10 is then given by Equation (10):

$$rf = \frac{1}{\sqrt{2 \cdot \pi}} \cdot e^{-\frac{(x-\mu)^2}{2 \cdot \sigma^2}} \tag{10}$$

where rf is the relative frequency, μ the median, and σ^2 the variance. They show an agreement with the calculated Gaussian distribution meaning that the threshold voltage and the slope are controlled by the process and should also be reproducible in a later fabrication processes.

4. Discussion

The novel protocol for down thinning of the Si top layer in the beginning of the process enabled a very precise thickness control

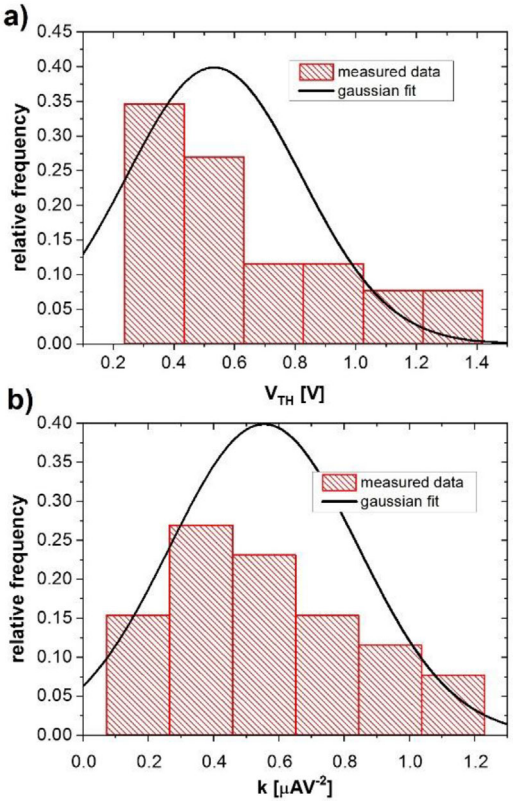

Figure 10. Histogram of the mean values between forward and backward scans for (a) V_{TH} and (b) k-factors ($n = 26$) including a plot of the Gaussian distribution as calculated by Equation (10).

of the Si top layer. In our process the etching rates differed compared to an earlier work.[16] We observed an overprinting effect in many test experiments, which we were able to overcome by a modified NIL protocol. In our university clean room setting we maximized the fabrication yield on 4" wafers with our NIL tool and reached 72.2% for the 100 nm silicon nanowires, which were evenly distributed over the wafers. The electrical characterizations for our SiNW MOSFET and ISFET devices with different width showed reproducible performance with negligible electrical hysteresis. The different absolute drain–source current values of the n- and p-type devices, when selecting symmetric bias voltages, could in future designs of n-p combinations be compensated by scaling the nanowire widths similarly to what is usually done in CMOS designs. The n- and p-type devices showed already a good level of complementarity with an expected shift between the threshold voltages of MOSFETs and ISFETs. We successfully realized back-gate contacts on the front sides of the chips, which can reliably be used to adjust eventual bias voltage shifts. This is particularly important when in future different gate dielectric materials for realization of stable biosensors are introduced in the process.

5. Conclusions

We realized a fabrication protocol for complementary n- and p-type SiNW FETs using a wafer scale top-down fabrication process with sub-100 nm features, with a thickness of ≈40 nm and a mechanical length up to 7 μm for the wires. SiNW FET devices showed reproducible electrical characteristics. Many different designs were fabricated in parallel for future biosensing experiments.

With the 4" wafer-scale process described here we successfully established a platform technology. We reached a good yield for a university clean room process, which is high enough to supply researchers in future projects with reliable and reproducible biosensor devices.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

complementary metal-oxide-semiconductor process, nanoimprint lithography, silicon nanowire field-effect transistor biosensor, wafer-scale process

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[1] P. Bergveld, *IEEE Trans. Biomed. Eng.* **1970**, *BM17*, 70.
[2] S. Y. Chen, J. G. Bomer, E. T. Carlen, A. van den Berg, *Nano Lett.* **2011**, *11*, 2334.
[3] Y. Cui, Q. Q. Wei, H. K. Park, C. M. Lieber, *Science* **2001**, *293*, 1289.
[4] T. C. Nguyen, M. Schwartz, X. T. Vu, J. Blinn, S. Ingebrandt, *Phys. Status Solidi A-Appl. Mat.* **2015**, *212*, 1313.
[5] X. T. Vu, J. F. Eschermann, R. Stockmann, R. GhoshMoulick, A. Offenäusser, S. Ingebrandt, *Phys. Status Solidi A-Appl. Mat.* **2009**, *206*, 426.
[6] S. Zafar, C. D'Emic, A. Afzali, B. Fletcher, Y. Zhu, T. Ning, *Nanotechnology* **2011**, *22*, 6.
[7] X. X. Duan, Y. Li, N. K. Rajan, D. A. Routenberg, Y. Modis, M. A. Reed, *Nat. Nanotechnol.* **2012**, *7*, 401.
[8] W. U. Wang, C. Chen, K. H. Lin, Y. Fang, C. M. Lieber, *Proc. Natl. Acad. Sci. USA* **2005**, *102*, 3208.
[9] X. T. Vu, R. GhoshMoulick, J. F. Eschermann, R. Stockmann, A. Offenhausser, S. Ingebrandt, *Sens. Actuator B-Chem.* **2010**, *144*, 354.
[10] T. W. Lin, P. J. Hsieh, C. L. Lin, Y. Y. Fang, J. X. Yang, C. C. Tsai, P. L. Chiang, C. Y. Pan, Y. T. Chen, *Proc. Natl. Acad. Sci. USA* **2010**, *107*, 1047.
[11] R. H. Tian, S. Regonda, J. M. Gao, Y. L. Liu, W. Hu, *Lab Chip* **2011**, *11*, 1952.
[12] P. L. Chiang, T. C. Chou, T. H. Wu, C. C. Li, C. D. Liao, J. Y. Lin, M. H. Tsai, C. C. Tsai, C. J. Sun, C. H. Wang, J. M. Fang, Y. T. Chen, *Chem. Asian J.* **2012**, *7*, 2073.
[13] G. J. Zhang, L. Zhang, M. J. Huang, Z. H. H. Luo, G. K. I. Tay, E. J. A. Lim, T. G. Kang, Y. Chen, *Sens. Actuator B-Chem.* **2010**, *146*, 138.
[14] D. E. Presnov, S. V. Amitonov, V. A. Krupenin, *Russ. Microelectron.* **2012**, *41*, 310.
[15] A. R. Gao, N. Lu, P. F. Dai, T. Li, H. Pei, X. L. Gao, Y. B. Gong, Y. L. Wang, C. H. Fan, *Nano Lett.* **2011**, *11*, 3974.
[16] X. H. Tang, N. Reckinger, G. Larrieu, E. Dubois, D. Flandre, J. P. Raskin, B. Nysten, A. M. Jonas, V. Bayot, *Nanotechnology* **2008**, *19*, 7.
[17] G. K. Celler, D. L. Barr, J. M. Rosamilia, *Electrochem. Solid State Lett.* **2000**, *3*, 47.
[18] S. Y. Chou, P. R. Krauss, P. J. Renstrom, *Appl. Phys. Lett.* **1995**, *67*, 3114.
[19] S. V. Sreenivasan, *Microsyst. Nanoeng.* **2017**, *3*, 19.
[20] P. Forsberg, M. Karlsson, *Diam. Relat. Mat.* **2013**, *34*, 19.
[21] S. Landis, N. Chaix, C. Gourgon, T. Leveder, *Nanotechnology* **2008**, *19*, 13.
[22] S. Landis, N. Chaix, C. Gourgon, C. Perret, T. Leveder, *Nanotechnology* **2006**, *17*, 2701.
[23] R. H. Pedersen, O. Hansen, A. Kristensen, *J. Micromech. Microeng.* **2008**, *18*, 9.
[24] O. Knopfmacher, D. Keller, M. Calame, C. Schönenberger, in *Proceedings of the Eurosensors XXIII Conference* (Eds: J. Brugger, D. Briand), Elsevier Science Bv, Amsterdam **2009**, Vol. 1, p. 678.
[25] O. Knopfmacher, A. Tarasov, W. Y. Fu, M. Wipf, B. Niesen, M. Calame, C. Schonenberger, *Nano Lett.* **2010**, *10*, 2268.
[26] C. M. Lim, I. K. Lee, K. J. Lee, Y. K. Oh, Y. B. Shin, W. J. Cho, *Sci. Technol. Adv. Mater.* **2017**, *18*, 17.
[27] A. Ortiz-Conde, F. J. G. Sanchez, J. J. Liou, A. Cerdeira, M. Estrada, Y. Yue, *Microelectron. Reliab.* **2002**, *42*, 583.

[28] A. Nakajima, H. Aoyama, K. Kawamura, *Jpn. J. Appl. Phys. Part 2 – Lett.* **1994**, *33*, L1796.
[29] M. Itano, F. W. Kern, M. Miyashita, T. Ohmi, *IEEE Trans. Semicond. Manuf.* **1993**, *6*, 258.
[30] J. C. Chou, L. P. Liao, *Thin Solid Films* **2005**, *476*, 157.
[31] P. Georgiou, C. Toumazou, *Sens. Actuator B-Chem.* **2009**, *143*, 211.
[32] P. A. Hammond, D. Ali, D. R. S. Cumming, *IEEE Sens. J.* **2004**, *4*, 706.
[33] M. J. Milgrew, P. A. Hammond, D. R. S. Cumming, *Sens. Actuator B-Chem.* **2004**, *103*, 37.
[34] A. A. Poghossian, *Sens. Actuator B-Chem.* **1997**, *44*, 551.
[35] V. Subramanian, A. Mercha, B. Parvais, J. Loo, C. Gustin, M. Dehan, N. Collaert, M. Jurczak, G. Groeseneken, W. Sansen, S. Decoutere, *Solid-State Electron.* **2007**, *51*, 551.