SleepRider: a 5.5µW/MHz Cortex-M4 MCU in 28nm FD-SOI with ULP SRAM, Biomedical AFE and Fully-Integrated Power, Clock and Back-Bias Management

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Abstract

Ultra-low-power microcontrollers (ULP MCUs) face a performance trade-off between energy-efficient computing during activity periods and low sleep power, associated with limited wake-up time and energy. Adaptive back-biasing in FD-SOI, along with near-threshold operation at ultra-low voltage, has brought significant improvements by dynamically shifting the minimum energy point (MEP) along the frequency axis. This work introduces a highly-integrated 64-MHz ULP Cortex-M4 MCU with 96-kB SRAM in 28nm FD-SOI. A clock and power management unit (CPMU) generates all internal supplies and clocks from a 1.8-V supply, while unified frequency and back-bias regulation (UFBBR) performs PVT compensation. Custom 16-kB ULP SRAMs achieve low read/write access energy, 1.2/0.84pJ/32-bit access respectively, and provide 0.98nW/kB ultra-low-leakage data retention. A low-power biomedical analog front-end enables biopotential monitoring. The MEP is 5.5µW/MHz (8.2µW/MHz including conversion losses). Sleep power is 7.7µW with retention of logic state and 32-kB memory.

In highly-integrated MCUs, power savings across all chip components are required as any sub-optimal component may ruin the average applicative power. The architecture of the proposed MCU, codenamed SleepRider, is built around an ARM Cortex-M4 processor with several digital interfaces (Fig. 1). The memory includes two 16-kB custom ULP SRAMs with ultra-low leakage (ULL) in sleep and two 32-kB high-density (HD) foundry SRAMs for increased memory capacity. The analog front-end (AFE) includes an instrumentation amplifier (IA) and a dual ADC with a differential input. The CPMU generates all clocks and ultra-low-voltage supplies from internal references, and performs adaptive back-biasing (ABB) for PVT compensation.

Switched-capacitor voltage regulators (SCVRs) generate three internal voltage supplies from the main 1.8V, respectively at 0.4V (VDDL) for the logic, 0.5V (VDDM) for the ULP SRAMs and 0.8V (VDDH) primarily for HD SRAMs. Negative charge pumps (CPs) generate a negative supply at -0.2V (VSSN) in active mode used by the ULP SRAMs. The comparators, control logic and local oscillator (LO) of the SCVRs use an auxiliary 0.9V supply voltage (VDDI) from a high drop-out linear regulator. In sleep mode, the SCVR clock switches from the LO to a 500-kHz reference clock. Given the lack of MiM capacitors in this process, MoM capacitors geometry optimization mitigates the impact of the parasitic capacitance of the flying capacitors on the power conversion efficiency (PCE) in the switched-capacitor network (SCN) which is mostly critical for high-division ratio SCNs (Fig. 2).

The UFBBR technique efficiently compensates for PVT variations that affect both logic speed and N/PMOS imbalance [1]. However, the coupling between BBN and BBP (i.e. NMOS/PMOS BB voltages) due to the parasitic well capacitances threatens the stability of independent BBN/BBP control loops. Instead, we propose a unified dual-output frequency-locked loop (FLL) architecture (Fig. 3), avoiding the need for off-chip capacitors. Logic speed and imbalance are respectively sensed by a tunable ring oscillator (TRO) – also used as the main system clock in active mode – and N/PMOS-sensitive ROs. Digitally-controlled oscillators (DCOs) driving switched-cap CPs perform fast proportional current actuation. The proposed UFBBR is stable in all PVT corners and locks in 16µs. In comparison, the ABB from [2] performs only one control cycle in 14.9µs which leads to a much longer lock time.

Negative-differential-resistance (NDR) latches have been used in ULP SRAMs for their ABB compatibility and ULL data retention. Compared to [1], the ULP SRAM (Fig. 4) uses a modified 7T ULL bitcell with uniform 32-nm gate length and a PMOS-only write port, providing 2.1× area and 15× power reduction. 2D sub-banking in 0.5-kB local arrays (LAs) decreases the read access time by 1.5× and brings the mean read (resp. write) access energy at 64MHz down to 37 (resp. 26) fJ/bit. In order to ensure 0.03-ppm hold stability and writability, the local write word line (LWWL) signal uses boosted voltage levels at 0.8 (hold) and -0.2V (write). Finally, power gating (PG) of the SRAM periphery brings its sleep power down to 0.98nW/kB.

In the AFE, the IA relies on a chopped architecture with transconductance (TC) and transimpedance (TI) stages [3] with a gain of 37dB. It is supplied at 1.8V to increase the input dynamic range to 1.5V (Fig. 5), avoiding potential saturation due to high-amplitude artefacts. Two parallel 12-bit time-based ADCs combining a voltage-controlled oscillator and an asynchronous counter digitize the IA differential output [4]. Using a back-bias-controlled oscillator (BBCO) provides a wider dynamic range up to 1.8V allowing high IA gain and improved linearity compared to a current-starved (CS) RO (Fig. 5). The AFE can operate in sleep mode with a power overhead of 3.5µW for the IA and 1µW for the dual ADC.

SleepRider was manufactured in 28nm FD-SOI (Fig. 8). The measurements show the highest level of computing performance and integration compared to other ULP MCUs, with low power in sleep and active modes (Table 1). The logic and SRAM MEP is 4.8µW/MHz at 56MHz (CoreMark). This results in a peak energy efficiency similar to our previous ULP MCU [1] while providing 1.7× higher computing performance. Sleep power is 5.8µW with 32-kB memory retention, excluding SCVR conversion losses. Each wake-up cycle from sleep to active mode takes 39µs and has an energy overhead of 18.7nJ (Fig. 6). In an applicative use case of ECG-based arrhythmia classification, the total power including CPMU conversion losses is 19.8µW, broken down in Fig. 7 among different tasks. This represents a 3.2× reduction factor compared to the best commercial ULP MCU [5].

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References

[1] D. Bol, JSSC, 2021 (in press). [2] S. Höppner, TCAS-II, 2019, pp 2159-63. [3] N. Van Helleputte, JSSC, 2015, pp 230-44. [4] M. Baert, JSSC, 2019, pp 1577-87. [5] AmbiqMicro, Apollo3 datasheet, on-line.

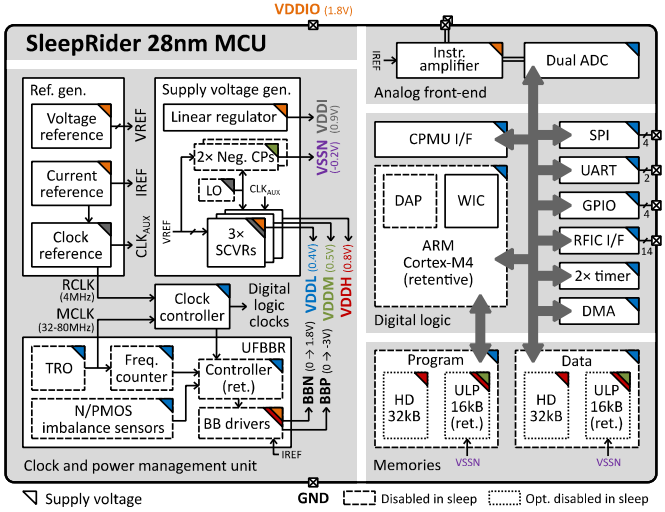

Fig. 1 – MCU architecture showing voltage domains and sleep-mode status. Digital logic and ULP SRAMs retain data in sleep mode.

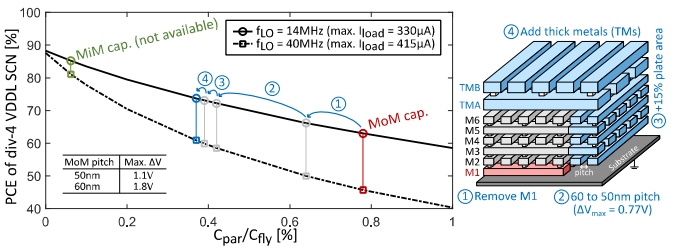

Fig. 2 – PCE of the div-4 SCN in the VDDL SCVR with reduction of the ratio between parasitic capacitance (C_{par}) and SCN flying capacitor (C_{fly}).

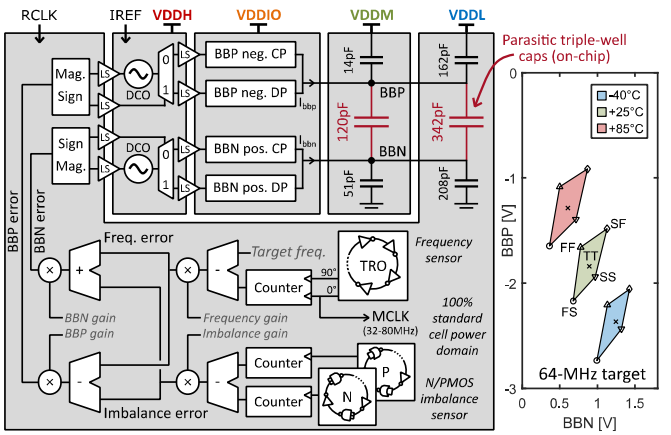

Fig. 3 – UFBBR FLL architecture and in-lock BB voltages. The target frequency and loop gains are configurable in software.

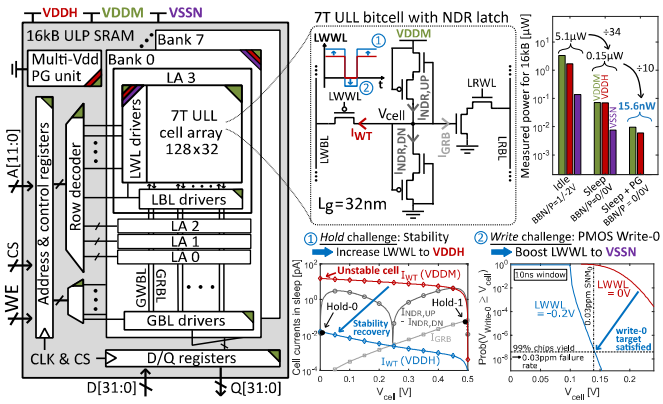

Fig. 4 – Custom ULP SRAM: architecture, bitcell, design challenges of PMOS-only write port and measured static power by supply rail.

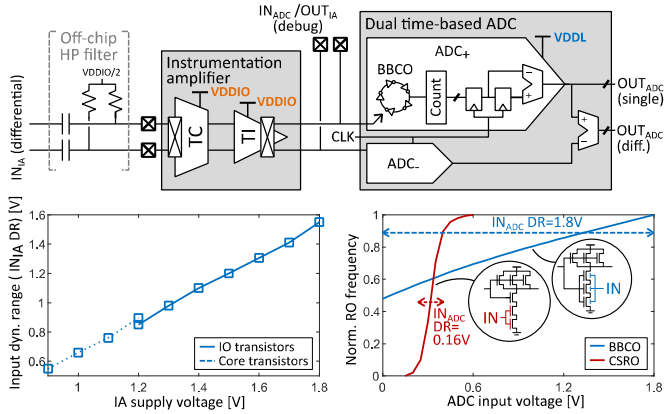

Fig. 5 – Biomedical AFE schematic and simulated performance.

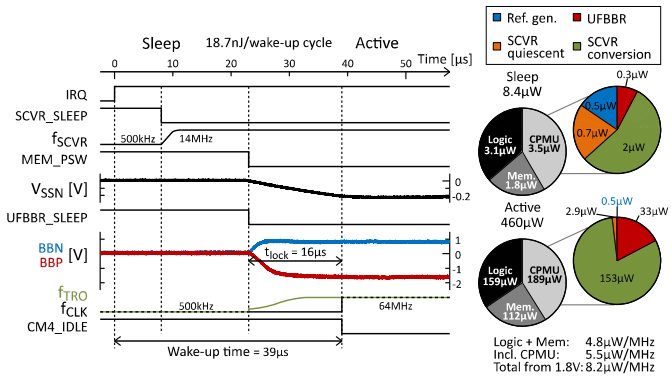

Fig. 6 – CPMU wake-up sequence and power breakdown. Measured power is provided with 64-kB memory retention in sleep and at 56MHz (MEP) in active mode.

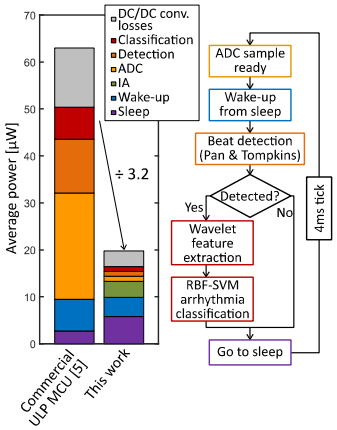

Fig. 7 – Measured applicative power on ECG monitoring use case.

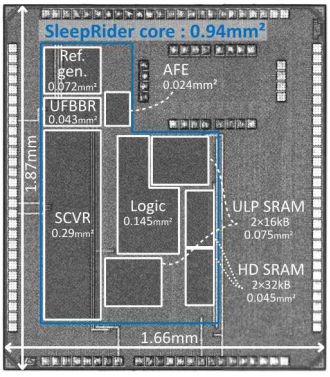

Fig. 8 – Chip microphotograph with post-shrink dimensions.

TABLE I
COMPARISON WITH THE STATE OF THE ART

	Ambiq Apollo3	Myers VLSIC, 2017	Prabhat ISSCC, 2020	Lallement SSCL, 2018	Lee JSSC, 2020	Song TBioCAS, 2019	Bol JSSC, 2021	This work
Technology	40nm ULP eFlash	65nm LP	65nm LP	22nm FD-SOI	55nm DDC	55nm CMOS	28nm FD-SOI	28nm FD-SOI
CPU	CM4F	CM0+	CM33	CM0+	CM0	CM4F	CM0	CM4
Memory	384kB RAM 1MB Flash	2kB ROM 12kB SRAM	128kB ROM 20kB RAM	12kB SRAM	8kB SRAM	192kB SRAM	64kB SRAM	96kB SRAM
Embedded PCM	Main clock int. supplies	All clocks Int. supplies	All clocks Int. supplies	Back bias	All clocks Int. supplies Back bias	Main clock int. supplies	Main clock Int. supplies Back bias	All clocks Int. supplies Back bias
External comp.	1.8V supply Crystal osc. 1L + 2C (Buck)	1.2V supply	1-1.5V supply 1L+1C (Buck)	0.4-0.8V supply Main clock	1.2/2.4/-1.2V supplies	1.4V supply Crystal osc. 2C (LDO) + 4C (VREF) 2C (AFE)	1.8V supply Ref. clock 3C (SCVR) 1C (UFBBR)	1.8V supply 3C (SCVR) Opt. 2C+2R (AFE)
PVT compensation	N/A	AFS	UFVR	Limited ABB	AVS + ABB	×	UFBBR	UFBBR
AFE	ADC	×	×	×	×	(IA + ADC) x 8ch.	×	IA + ADC
Max freq. at MEP supply [MHz]	96	0.2	2.35	20	0.5	80	80	80
Active power at MEP [µW/MHz]	32.8* @48MHz	7.6 @0.2MHz	20 @2.35MHz	1.13 @20MHz	4.7 @0.5MHz	23† @80MHz	3.5 @48MHz	5.5 @56MHz
Wake-up time [µs]	25	N/A	180	0.3	N/A	N/A	20	39
Lowest power state with ret. (DC/DC conv. incl.) [µW]	1.8 (8kB) 6.7 (384kB)	0.14 (4kB)	0.01 (4kB)	N/A	0.7 (8kB)	N/A	12.7 (64kB)	7.7 (32kB) 9 (96kB)
Peak efficiency [CoreMark/mW]	104 @164 CM	324 @0.5 CM	201 @9.4 CM	× (not enough RAM)	495 @1.2 CM	149 @273 CM	666 @112 CM	622 @192 CM

* Including DC/DC conversion losses. † Digital only.
Red and blue fonts highlight MCU limitations and top performance respectively.
AFS: adaptive frequency scaling - AVS : adaptive voltage scaling - UFVR : unified frequency and voltage regulation - CM : CoreMark