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Low Power K- and Ka- Wideband LNA Design in 22 nm FD-SOI Using Transformer-Tuned Input

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***Abstract*—This paper presents a wideband two-stage low-noise amplifier (LNA) covering continuously from 21 GHz up to 47 GHz. The design employs a feedback technique using a transformer-based network at the input common-source stage which introduces poles and manipulates Γ_{opt} (by modifying the noise correlations between the input and output), allowing for an eased implementation of simultaneous power- and noise-match over a wide band. The design was fabricated in the low power 22 nm FD-SOI node from GlobalFoundries. At nominal bias, the measured LNA achieves a gain of 15.5 dB over the entire K- and Ka-bands with 2-dB-ripple, and a minimum noise figure of 2.2 dB for 9.1 mW of power. The bias point can also be effectively modulated through the use of back-gate biasing, allowing overall for more than 10 dB of gain-control.**

Keywords— LNA, wideband, transformer, 5G, CMOS, FD-SOI, matching network, mm-wave integrated circuit, variable gain.

I. Introduction

At mm-wave frequencies, front-ends exhibiting wideband characteristics are of particular interest to address transceiver needs over the large spectrum. The interest in wideband transceivers lies in their coverage of multiple standards including 5G and automotive radar such as the n258 (26 GHz) K-band, the n257 (28 GHz) and n260 (39 GHz) Ka-bands, or the n259 (41 GHz) and n262 (47 GHz) V-bands.

The low-noise amplifier (LNA) is a critical link in the receiver signal-chain, and its design is a challenge when targeting flat gain and low noise-figure (NF) over large fractional bandwidths while simultaneously maintaining low return loss (below -10 dB). Indeed, compared with narrowband designs there is usually a trade-off in at least some portion of the band between input power-matching and achieving minimal noise-figure performance.

In this paper, we propose a transformer-feedback that modifies Γ_{opt} – the optimal source reflection coefficient to minimize noise – facilitating simultaneous noise- and power-match over a wide band. At the same time, the load impedance at the output is carefully tailored to obtain a flat gain response.

The technology employed in this work is the 22 nm FD-SOI node from GlobalFoundries (22FDX®), which offers devices that reach transit- (f_t) and maximum oscillation- (f_{max}) frequencies up to 350 GHz [1], along with low noise and low power, making it a technology of choice for mm-wave and sub-THz front ends. On top of that, it also offers state-of-the-art digital and baseband circuitry, supporting an efficient monolithic single-chip integration of a full communications system. Finally, 22FDX® offers a rich back-end-of-line (BEOL) metal stack build-up, featuring three thick copper layers and one thick aluminium layer that allow for the designs of high-quality passives up to mm-wave.

This paper leverages the technology to design a wideband and low-power LNA covering the entire K- and Ka-bands.

Section II presents the circuit design considerations and choices, with a focus on (i) the input transformer-feedback's Γ_{opt}-impact and pole-tuning to achieve wideband matching while maintaining excellent noise performance, and on (ii) the gain-flattening through the output stage network.

Section III then presents the on-wafer measurement results. Overall, at nominal bias, the LNA achieves 2.2 dB of NF and 15.5 dB of gain with less than 2 dB of ripple over the n257 through n260 bands of the 5G network (21-47 GHz).

Finally, we highlight that the back-gate node unique to FD-SOI technology can be employed to effectively modulate the gain of the LNA, that is of interest for optimizing a receiver's behaviour to the received power level, and reduced gain modes have the benefit of consuming less DC power.

II. Circuit Design

The full schematic of the 2-stage LNA is presented in Fig. 1. The first stage is a common-source employing inductive feedback to provide wideband input matching along with low NF response, while the second stage is a cascode design to efficiently boost and flatten the gain of the overall LNA.

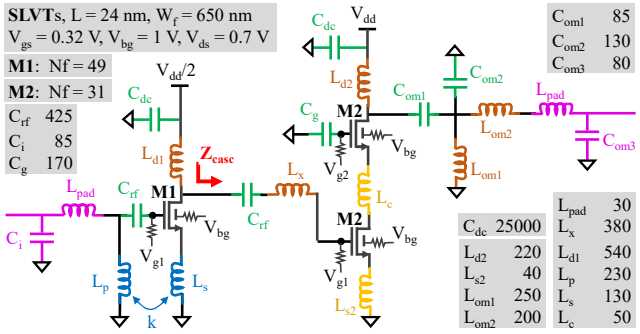

Fig. 1. Schematic of the overall 2-stage LNA. C and L values in fF and pH.

A. Transistors

All transistors in the LNA are *super-low threshold-voltage* (SLVT) N-FETs of 24 nm gate length, and are sized with 650 nm finger width, which provides a good trade-off point between available minimal noise figure (NF_{min}) and available gain. FET M1 of the first stage employs 49 fingers while the FETs M2 and M3 in the second cascode stage are each implemented using 31

fingers. A source to drain voltage (V_{ds}) bias condition of 0.7 V is chosen for each FET of the design. The gate bias points were set to V_{gs} = 0.32 V for all devices in the LNA. The back-gate voltage V_{bg} is nominally set to 1.0 V for all FETs, and V_{bg} can be varied to implement a variable gain function for the LNA.

The nominal V_{bg} value of 1.0 V was chosen in order to implement a flexible design, capable of varying its performance metrics (gain, P_{dc}, NF) by controlling the overdrive voltage on the devices through the modulation of V_{bg} from -0.4 V to 2.5 V. This leads to an LNA design that can efficiently trade-off power for performance, targeting more than 10 dB of gain control through the V_{bg} tuning.

B. Inductive Feedback and Γ_{opt}-Tuning

Noise at the input and at the output of a two-port device are made up of several physical contributions. Those different contributions are usually uncorrelated, though the total noise at the input is generally partially correlated with the total noise at the output, as they share common origins from the device physics. It is then possible to intelligently manipulate and feed-through the input noise to the output to cancel out part of that correlated noise. The typical way to do this is to present an optimal source impedance Z_{opt} to the device, from which the input noise will reflect, changing its amplitude and phase before being transferred through to the output. This approach however does not allow for simultaneous optimal noise- and power-match at the input (i.e. $\Gamma_{opt} \neq \Gamma_{in}^{*}$, Fig. 2). One way to manipulate the required Γ_{opt} to attain the minimal noise figure (NF_{min}) is to introduce feedback from the output to the input, changing the noise budget at the different nodes [2]. Such feedback can then be used to adapt Γ_{opt} (by adapting the noise correlation between input and output noise) to achieve noise- and power-match simultaneously from the input network [3]. In the present case, this comes at the price of a small penalty in attainable NF_{min}, that remains acceptable to achieve good power match (and therefore increased gain).

In this work, inductive feedback was chosen between the source degeneration inductor and a second inductor placed as a shunt element at the input, as depicted in Fig. 2.

Fig. 2 illustrates the principle of noise manipulation through the chosen inductive feedback. A single noise source is represented for simplicity: the thermal channel noise current, that is often the dominant contributor for short-channel MOSFETs [2], and the resulting induced c_1 and c_2 noise voltages at the source and drain nodes are depicted.

The following is a simplified and intuitive analysis of the circuit. The noise voltage present over L_s is fed back to the input through inductive coupling with L_p, depicted as the green noise c_{fb}. When k is equal to zero, then Γ_{opt} is determined by the correlation of c_1 to c_2. However, when introducing some inductive coupling, some noise c_{fb} is added to the input, and Γ_{opt} is then determined by the correlation of this new noise signal ($c_1 + c_{fb}$) to c_2. Note that the phases of the depicted noise signals c_1, c_2 and c_{fb} are arbitrarily depicted in Fig. 2, since they depend on the load impedance Z_L and on the transfer function through the device (affected by g_m but also by parasitic capacitances of M1 at mm-wave). In the case of the considered M1 transistor (parameters of M1 given in Fig. 1), the feedback network is overall positive in nature for the output signal, and the result is that G_{max} increases with larger (negative) values of k, as shown in Fig. 2. This comes at the price of a reduced stability factor μ (as expected for positive feedback).

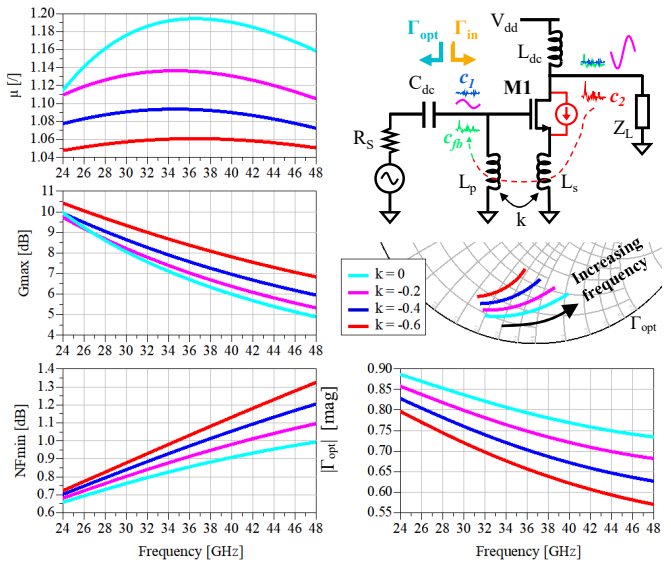

Fig. 2. Impact of inductive feedback technique on the input stage's stability factor μ, maximum available gain G_{max}, minimum noise figure NF_{min} and corresponding optimal source reflection coefficient Γ_{opt}.

The idea of the feedback is to manipulate Γ_{opt} to bring it closer to Γ_{in}^{*}, in order to alleviate trade-offs between noise and power matching at the input. This will be highlighted in the next section, when considering the appropriate load impedance (i.e. the input impedance of the 2nd cascode stage). Furthermore, reducing the magnitude $|\Gamma_{opt}|$ has the effect of easing the input matching, particularly over a wide band.

We note that including the feedback network comes at the price of a slightly increased NF_{min} value. This is due to the feedback of some uncorrelated noise to the input, which overall leads to NF_{min} degradation with feedback introduced [2]. Fig. 2 shows that the penalty in NF_{min} is contained to a few tenths of a dB, which is a worthwhile trade-off allowing for a broader input match close to optimal noise performance.

C. Input Pole Tuning Towards Wideband Input Match

When replacing Z_L in the schematic of Fig. 2 by the input impedance of the designed cascode network Z_{casc} (represented in Fig. 1), the S_{11} parameter response of the overall circuit is that of Fig. 3a. It exhibits resonant behavior due to an additional pole introduced in the response through the feedback network [3]. Fig. 3a demonstrates how the magnitude of the coupling

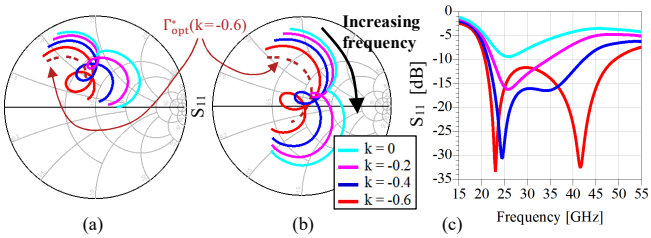

Fig. 3. Return loss seen at first stage input for several values of coupling factor k. (a) without C_i or L_{pad} (see Fig. 1). (b) and (c) with C_i (84 fF) and L_{pad} (30 pH).

factor k affects this behavior, with large coupling factors allowing for a stronger impact of the additional pole that broadens the S_{11} response. A wideband matching then becomes achievable thanks to this inductive feedback providing resonant behavior in S_{11}. A full analytical analysis of the transformer-based pole-tuning technique employed can be found in [3] describing the input pole-splitting for a wideband input match response. Finally, the response in Fig. 3b is that of the overall 2-stage LNA, obtained from the responses in Fig. 3a by adding the input network L_{pad} and C_i to rotate S_{11} in the Smith chart and place the resonance at the center. The result is that S_{11} can be made very wideband with a response below -10 dB from 24 to 53 GHz, as illustrated in Fig. 3c.

Fig. 3 also plots the Γ^*_{opt} response for the case k = -0.6 (dashed lines). This highlights that conjugate power match is attained at the input (i.e. maximal power-transfer). Furthermore, Γ_{opt} passes close to the Smith center after matching (Fig. 3b), i.e. that a near-NF_{min} response is *simultaneously* achieved. Overall, transformer- feedback allows for a manipulation of Γ_{opt} that permits a wideband matching in power and noise at the input simultaneously.

In the final LNA, a large capacitor C_{rf} placed prior to the gate of the 1st stage's FET serves for DC bias decoupling (Fig. 1). C_{rf} is placed after inductor L_p in order for the LNA's input pad to have a DC path to ground for ESD protection through L_{pad} and L_p (similar protection present at the output RF pad).

D. Output Stage Network and Overall Gain Flattening

The 2nd stage cascode is designed along with its matching networks to peak its gain response at high frequency.

The gain of the first stage exhibits a roll-off in frequency of approximately 3 dB from 28 GHz to 45 GHz, and this is in accordance with its G_{max} trend plotted in Fig. 2, meaning that wideband power match is well achieved for stage 1.

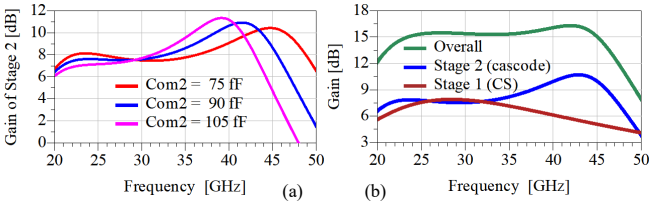

Fig. 4. (a) Gain of the second stage for different values of C_{om2}. (b) Gain of 1st and 2nd stage and overall gain of the wideband LNA.

Stage 2 compensates for this roll-off by providing higher gain in the higher band part. This is achieved by introducing mismatch in the output stage for selective gain-peaking. The result is that overall, a wideband response is achieved for the 2-stage LNA, as demonstrated by the green curve in Fig. 4b through a flat gain spanning approximately 23 to 45 GHz.

III. Measurement Results

The LNA was measured on-wafer (GSG probes) using a noise-figure setup (NF and gain) under 50 Ω based on a UXA-X-N9042B signal analyzer from Keysight and a noise-source up to 50 GHz. S-parameter measurements were performed up to 67 GHz using a Keysight N5291A VNA.

The layout of the fabricated LNA is depicted in Fig. 5, and

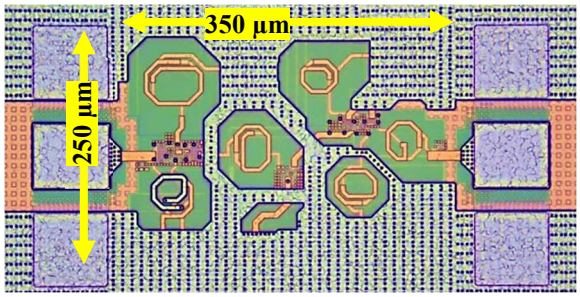

Fig. 5. Chip photograph of the fabricated two-stage wideband LNA.

although multiple inductors are present in the design, a compact layout area of 0.087 mm² is still achieved.

A. Nominal Bias Operation

The RF results are plotted in Fig. 6. The design exhibits an ultrawide gain response that peaks at 15.5 dB, and is very flat, with a measured 2-dB gain bandwidth spanning from 21.3 to 47.2 GHz, and a return loss better than -10 dB from 20.6 to 49.4 GHz. The measured NF has a minimum value of around 2.2 dB at 28 GHz and remains below 3 dB from 20.4 to 42.0 GHz.

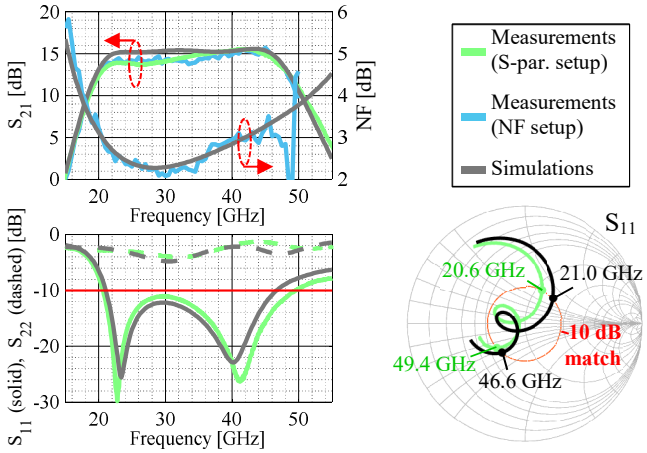

Fig. 6. Measured and simulated performance of the wideband LNA.

Excellent correlation to the predictive simulations (that include a full electromagnetic solve of the overall layout) is demonstrated; a difference in the gain response in the lower part of the band being the main slight discrepancy. The LNA is verified to be unconditionally stable from 1 kHz to 67 GHz.

B. Variable-Gain Operation

The LNA's V_{bg} (see Fig. 1) can be tuned to trade-off performance (gain and NF) for DC power consumption. Measurement results pertaining to those states are plotted in Fig. 7, demonstrating that the targeted 10 dB of variable-gain control is easily achieved through the proposed tuning of the back-gates. Indeed, a peak gain of 18.0 dB is achieved using a V_{bg} of 2.5 V or above, while a peak gain of 8.9 dB is observed at a V_{bg} of 0 V, and this gain can be further reduced drastically by employing negative V_{bg} values (down to below 5 dB).

The overall NF is affected, particularly in the low-gain settings, and increases up to a value of 4 to 6 dB for the lowest-gain modes, which remains acceptable for frequencies approaching 45 GHz, especially considering that low gain settings are to be employed when the input signal is large, i.e.

when the input signal-to-noise ratio (SNR) is high.

Fig. 7 also highlights the decreased power-consumption at lower gain settings, with the LNA drawing a reduced power of around 2 to 3 mW for V_{bg} values in the range of -0.4 to 0 V.

Finally, the LNA is demonstrated to maintain its wideband and low gain-ripple performance in all considered bias states.

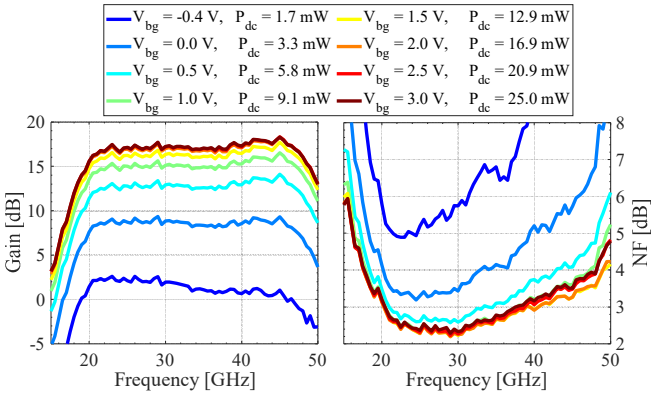

Fig. 7. Measured (signal analyzer) gain, NF, and P_{dc} over applied V_{bg}.

C. Benchmarking

Table I benchmarks the obtained results (at nominal bias) against state-of-the-art CMOS LNAs at K- and/or Ka- band from the published scientific literature [3]-[13]. Overall, the proposed LNA offers amongst the highest bandwidth and lowest NF at low power consumption, decent gain and low area.

TABLE I. BENCHMARK OF WIDEBAND K-/KA-BAND CMOS LNAS

Ref.	Technology	Freq. [GHz]	Gain (peak) [dB]	NF (min.) [dB]	P_{dc} [mW]	Area$ [10^{-3} mm^2]
[3]	65 nm CMOS	19.2-38.9	13.5	3.1	6.4	130
[4]	45 nm RFSOI	24-44	20	4.2	58	200
[5]	22 nm FD-SOI	24-43	23	3.1	20.5	217
			18.2	3.4	12.1	
[6]	45 nm RFSOI	27-46	21.1	2.4	25.5	380
[7]	22 nm FD-SOI	36.7-43.3	19.9	2.5	21	112
			14.8	3.3	7.5	
[8]	22 nm FD-SOI	23.7-28.5	23.1	2.1	5.6	92
[9]	22 nm FD-SOI	19-36	20.1	1.7	17.3	56
		20-36	17.0	2.1	5.6	
[10]	28 nm FD-SOI	21.3-41.1	20.3	2.9	27.5	128
[11]	65 nm CMOS	18-44	19.5	2.6	17	160
[12]	40 nm CMOS	19-46	12.4	3.4	4.4	96
[13]	65 nm CMOS*	21.8-30.3	26.3	3.6	19.2	97
		32.6-45.1	25.5	3.8		
This	22 nm FD-SOI^	21.3-47.5	15.5	2.2	9.1	87

$Core area without pads. *Dual output design (high / low band). ^At nominal bias.

IV. CONCLUSION

This paper describes the design and implementation of a wideband and low-power LNA covering continuously the entire K- and Ka-bands using GlobalFoundries' 22 nm FD-SOI technology. The design makes use of inductive feedback based on a transformer between the source degeneration inductor of the first amplification stage and a shunt-mounted inductor at the RF input. This technique allows for an engineering of Γ_{opt} by manipulating the noise contributions present at the first stage's input and output nodes, which in turn leads to a network for which *simultaneous* match in noise and power over a wideband is eased, which comes at a small (acceptable) penalty in overall attainable NF_{min}. Furthermore, this matching is facilitated over a broad band thanks to the poles introduced by the inductive feedback network.

Overall, at nominal bias, the low-power design (9.1 mW) is shown to exhibit an ultra-wideband response, achieving a minimum of 2.2 dB noise figure along with 15.5 dB of gain with less than 2 dB of ripple from 21-47 GHz, with an input match continuously better than -10 dB.

On top of that, the LNA can be configured as a variable-gain device by making use of the unique back-gate bias node of the 22FDX® technology. In that case, a gain control of more than 10 dB is achieved over a 3 V bias range at the back-gates, while maintaining a good NF value.

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