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Figures of merit of nanoscale transistors at cryogenic temperature: 28nm UTBB FD SOI nMOSFET case study

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Outline

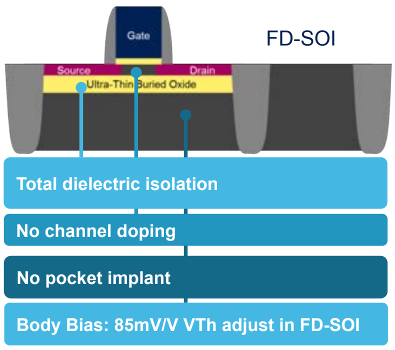
- Introduction : context – **motivation**
- Device and **technology** description
- **Experimental methodology** and results
  - DC performance
  - Analog / RF FoMs
  - Equivalent circuit elements extraction
  - Self-heating
- **Conclusions**

Context

Ultra Thin Body & BOX = Ultimate scaling of the planar fully-depleted (FD) SOI (Silicon-on-Insulator) MOSFET

28 nm FD SOI CMOS node (UTBB)

- Very good control of the short channel effects (low S, DIBL, I_{off}, mismatch, noise…)
- Low power consumption
- Tunability of the electrical performance via the back gate electrode (and PVT adjustments)
- **Very good analog & RF performance**
- ***Tunnel-FET and qubit integration demonstrated***



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FD SOI is foreseen as a competitive technology platform for low power wireless applications,… Internet of Things, 5G,…

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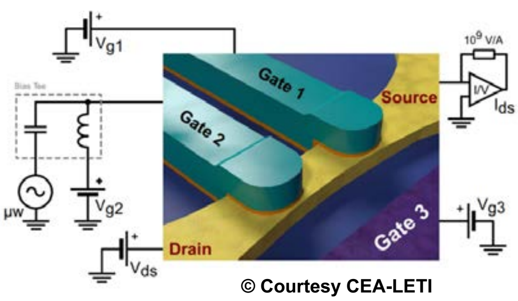
Motivation

BUT today FD SOI technology is also a technology of choice for low-temperature applications :

Space applications – mm-waves communication between satellites

Quantum computing – qu-bits (quantum dots and nanowires) as well as their control and readout circuitry



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NEED for high speed and low power (do not increase qubits temperature) integrated circuitry operating **in RF** and at **cryogenic temperature**.

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Analog / RF performance

Key factors of merit for any FET

@ transistor-level

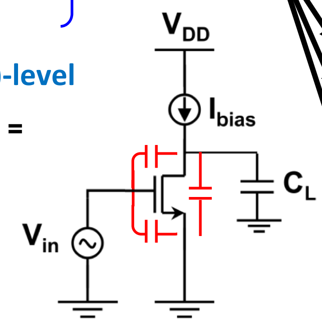
- $f_T = g_m/(2\cdot\pi\cdot C_{gg})$
- f_{max} α f_T, R_g
- $A_{v0} = g_m/g_d = (g_m/I_d)\cdot V_{EA}$ ≠ const (f)

⇨ *depends on*

- ❑ Transconductance g_m
- ❑ Drive current, I_d
- ❑ Output conductance, g_d
- ❑ Early voltage, V_{EA} ($V_{EA} = I_d/g_d$)
- ❑ g_m/I_d ratio
- ❑ Gate capacitance, C_{gg}
- ❑ Parasitics (C, R)

@ circuit (amplifier)-level

- $GBW = g_m/(2\cdot\pi\cdot C_L) = (g_m/I_d)\cdot(I_d/(2\cdot\pi\cdot C_L))$



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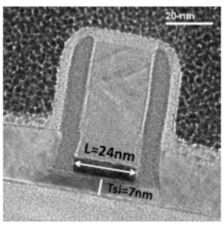
Device description



[N. Planes *et al.*, VLSI Symp. 2012]

life.augmented

- **28 nm FD SOI UTBB**
- **L_g = 25, 30 ··· 150 nm**
- ground plane is well-type
- gate stack
- HfSiON of 2.3 nm (EOT=1.3 nm) + TiN
- T_{Si} : 7 nm
- T_{BOX}: 25 nm
- no intentional channel doping

  → N_A~10^{15} cm^{-3}

@ IBM, CEA-LETI, ST 28nm, GF 22nm, Samsung 14nm

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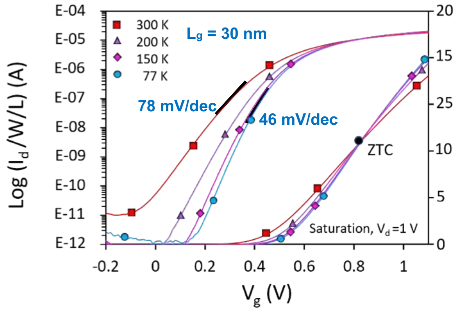
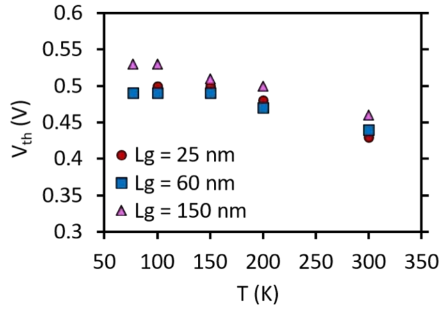
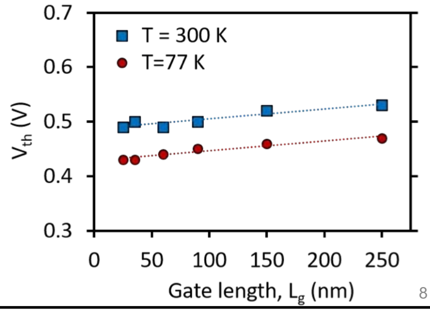
DC experimental results







SS↓ improves with **T** ↓

but not fully linearly due to traps

[A. Beckers *et al.*, EuroSOI-ULIS 2018]

V_{th}↑ (≈ 0.5 mV/K) with **T**↓

ZTC point as **µ**↑ with **T**↓

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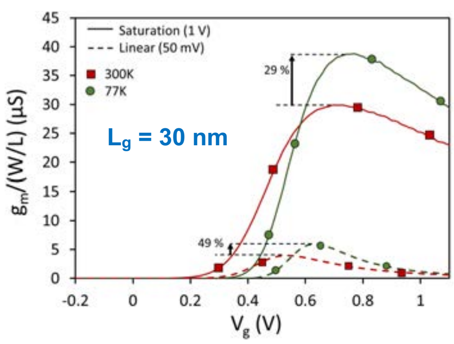
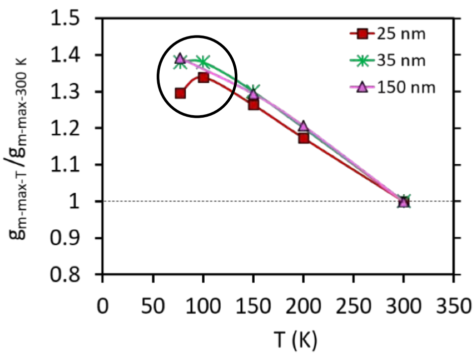
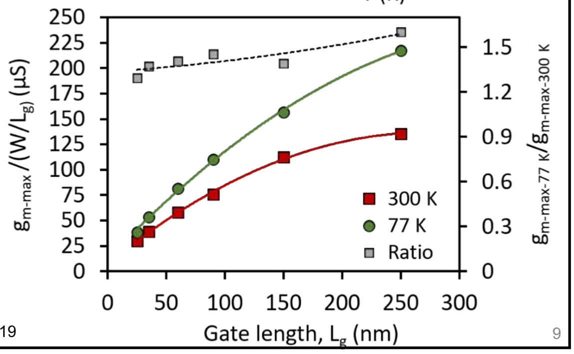
8







g_{m-max}↑ (**29% in saturation** below ZTC, vs 49% in linear, for **L = 30 nm**) with **T** ↓

But the improvement is lower for short lengths and below 100 K in relation with ***µ***

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9

In short-channel devices

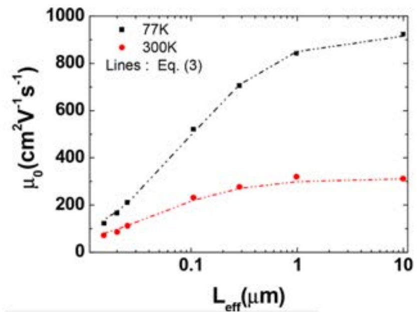
Carrier mobility

Mobility μ_0 temperature dependence is impacted by 2 balancing mechanisms

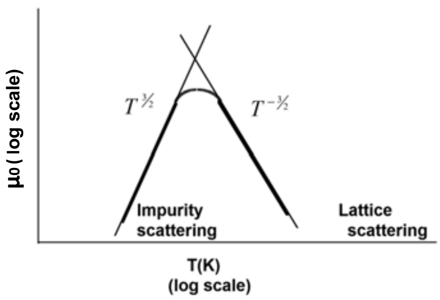
1. **Coulomb scattering** on the defects, ↓ $\mu_{coulomb}$ at ↓ **T**
2. **Phonon scattering**, ↑ μ_{phonon} at ↓ **T**

Larger impact of S/D junctions defects & impurities for shorter devices

[Grenoble INP, Ghibaudo]



$1/\mu_0 = 1/\mu_{phonon} + 1/\mu_{Coulomb}$



Callister, Materials Science and Engineering: An Introduction, Chapter 19.6-19.12

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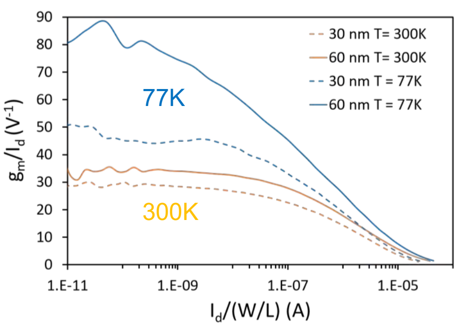
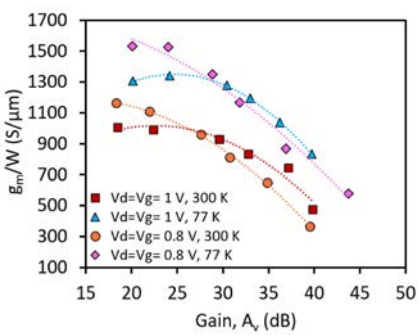
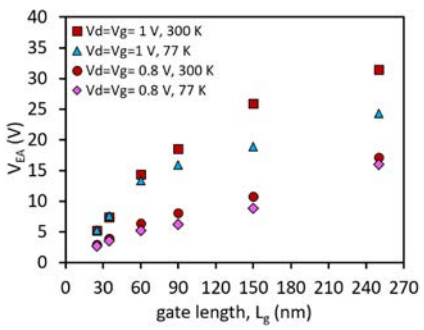




Analog FoM

$$A_v = \frac{g_m}{g_d} = \frac{g_m}{I_d}.VEA$$



g_m/I_d ↑ and V_{EA} ↓ with **T** ↓

⇒ **Gain** ↑ at constant g_m

or g_m ↑ at constant gain **!**

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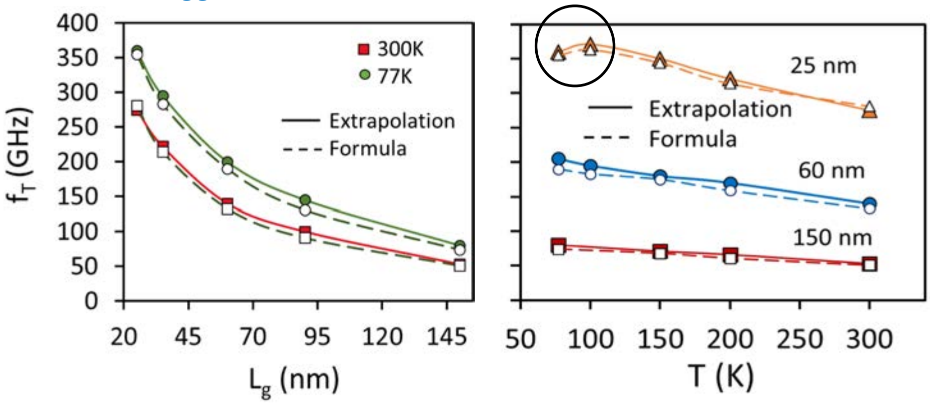
RF measurements

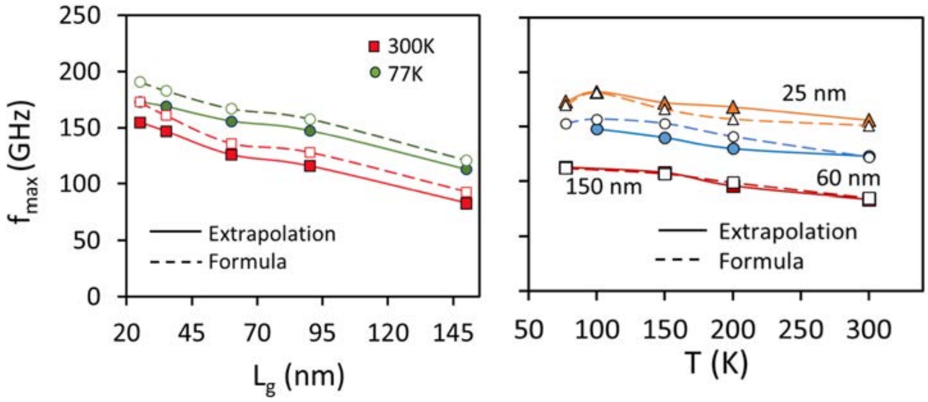
$$f_T \cong \frac{g_m}{2\pi C_{gg}}$$



- Improvement of $\mathbf{f_T}$ with **T** reduction

  85 GHz increase of $\mathbf{f_T}$ for the shortest device (**30% increase**)
- No increase of f_T below 100 K for the shortest device

$$f_{max} \approx \frac{f_T}{2\sqrt{(R_s + R_g)g_{ds} + 2\pi f_T R_g C_{gd}}}$$



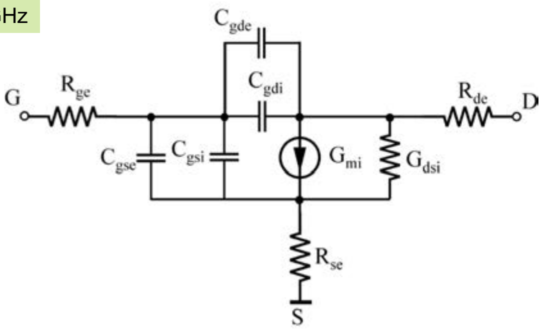
- **30 GHz improvement of $\mathbf{f_{max}}$** with **T** reduction (**17% increase**)
- Similar trends for $\mathbf{f_T}$ and $\mathbf{f_{max}}$ temperature dependence,
  but weaker improvement of $\mathbf{f_{max}}$

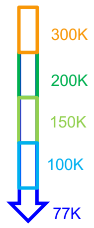
Equivalent circuit extraction

$\begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix}$

[S] ⇨ [Y] or [Z]

From DC up to 67 GHz





g_{mi} : **intrinsic** transconductance

g_{me} : **extrinsic** transconductance (**including the access resistances**)

$C_{gg} = C_{gs} + C_{gd}$ R_{ge} , R_{de} & R_{se}

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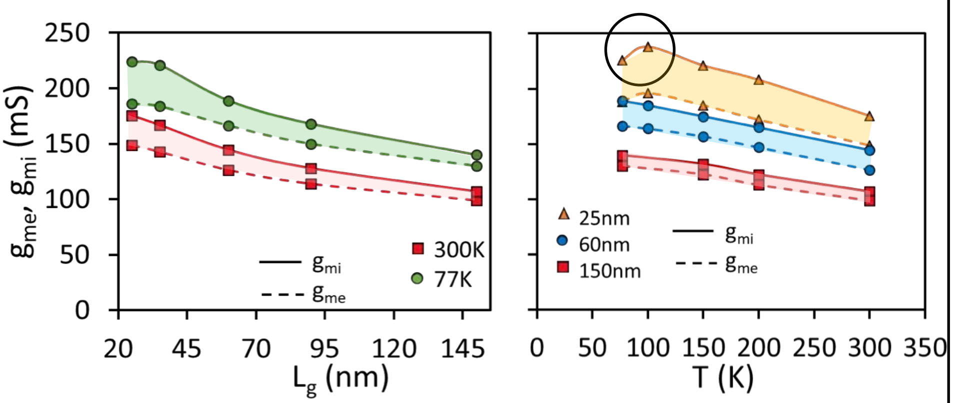
g_m improvement



- g_{me} << g_{mi}, **large impact of series resistances for shorter devices**
- g_{mi} increases with temperature reduction

  but again shows the peak at 100 K, confirming **μ** dominant effect

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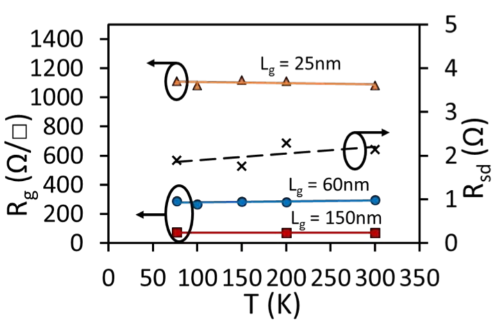
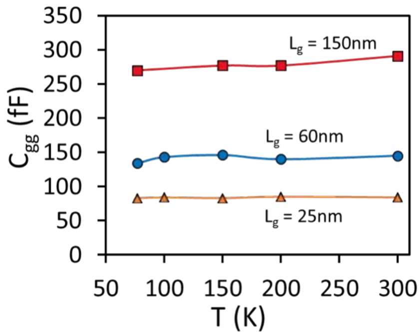
Gate capacitances and access resistances

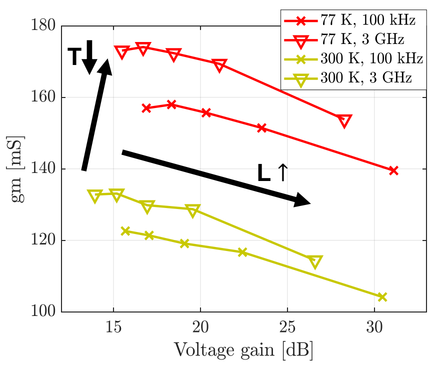


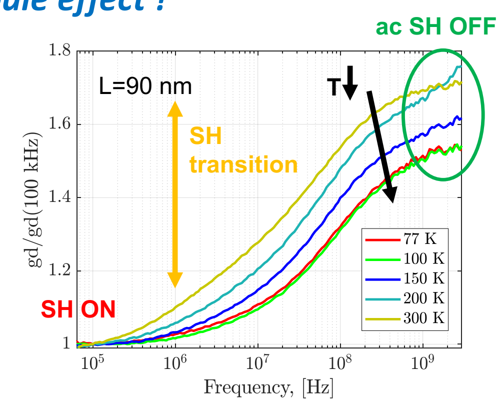


- Only a **weak decrease** of $\mathbf{R_{sd}}$ with temperature reduction and $\mathbf{R_g}$ **nearly unchanged** (degenerated, metallic behavior)
- $\mathbf{C_{gg}}$ **stays almost constant** with temperature decrease

Self-heating

High V_G & V_D (1V), I_D → Joule effect !





- ☐ Relative effect of SH on g_m & g_d(f) smaller at low T (mostly long channel FETs)
- ☐ Increased R_{th} at cryo wrt 300 K
- ☐ Larger T rise at 77K (+100→65K for L=25→90nm) than 300K (+65→36K)
- ☐ Av follows gm and gd trends : smaller degradation at low temperature
- ☐ Characteristic frequency of SHE shifts (~x4) to higher frequencies as T↓

Conclusions

- Potential of **28nm UTBB FD SOI MOSFETs for future cryogenic** applications has been demonstrated
- **Small-signal equivalent circuit elements** are extracted from I-V and S-parameters measurements **versus temperature and length**
- **Analog and RF FoMs at low temperatures** are explained in terms of **increases of μ, g_m and V_{EA}**, whereas **C and R parasitics ≈ cst**
- Temperature reduction down to **77 K** results in **improvements of gain (by ~ 5-10 dB)**, **f_T (by ~ 85 GHz)** and **f_{max} (by ~ 30 GHz)** as well as **g_{m_max}** and **I_d** (by ~ 20-70%), but **with an optimum at 100 K**
- **Self heating** is important to study (using same method).
- This work is now (S3S conference, 15 Oct. 2019) extended to the temperature range **down to 4.2 K**

Acknowledgements

EU projects

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welcome

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