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Impact of gate to source/drain alignment on the static and RF performance of junctionless Si nanowire n-MOSFETs

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ABSTRACT

We present experimental results for junctionless nanowire transistors (JNTs) with different gate alignments to the nanowire. Devices with nanowire source/drain extensions (NSDE) show high series source/drain resistance due to the low doped nanowire extensions, which causes lower drive current and larger device performance variations comparing with devices in which the gate electrode overlaps with the source/drain contact pads (GSD). Due to the improved on-current GSD devices exhibit much higher cutoff frequency. The high fringing field in the NSDE JNT results in degradation of SS. An optimized "dumbbell" shape JNT structure is proposed to further improve the device performance. Our preliminary simulations demonstrate higher on-currents but also larger parasitic capacitances for the dumbbell JNT. However, the RF performance of the dumbbell JNT is still improved with a factor similar to our experiments. Much smaller fringing field for the dumbbell JNT is expected from the simulation, which can cause less device variations.

1. Introduction

Junctionless nanowire transistors (JNTs) provide an alternative route to ultimately scaled MOSFETs for sub-10 nm technology [1–4]. The source (S), drain (D) and channel of a JNT are doped uniformly with a typical doping concentration of approximately 1×10^{19} cm^{-3} in order to achieve an enhancement-mode operation with a high I_{ON}/I_{OFF} ratio and a steep subthreshold swing [5–10]. In such a structure, PN junctions at the source/channel and drain/channel are avoided which leads to a simple fabrication process and a great immunity to short channel effects. JNTs also show higher reliability due to smaller electric field at the channel interface [4]. Because the doping concentration of S/D regions is relatively lower compared with standard MOSFETs high series resistance is expected for JNTs [5]. Additional S/D implantation to achieve a higher doping ($> 1 \times 10^{20}$ cm^{-3}) in S/D regions can reduce the series resistance [6,7].

In general, there are two different JNT architectures by considering the gate to the source/drain alignment. In the first architecture, as illustrated in Fig. 1(a) for a cross section view with only the top gate, the gate covers part of the nanowire (NW) with nanowire source/drain extensions (NSDE) to the large contact pads which can be considered as the elevated S/D. The NSDE corresponds to the nanowire regions under gate spacers with a length of L_{NSE} at the source side and L_{NDE} at the drain side, having the same doping concentration as the channel. The additional S/D implantation as reported in [6,7] cannot introduce dopants into the NSDE regions because of the presence of spacers and the difficulty to remove the damage and to activate the dopants in narrow and short nanowires. Due to the relatively low doping concentration and possible dopant deactivation in the NSDE, high series S/D resistance is expected [6–13]. In the second architecture with gated S/D (GSD), as shown in Fig. 1(b), the gate overlaps the S/D contact pads with overlapped lengths of L_{GS} to the source and L_{GD} to the drain. JNTs with GSD structure can reduce the S/D resistance [13–15], but unfortunately increases the parasitic gate-to-source and gate-to-drain capacitances.

In this paper, we present the DC characteristics including on-current, subthreshold swing (*SS*), threshold voltage V_T, and the RF cutoff frequency for the experimental NSDE and GSD JNTs. The comparison indicates weaker variabilities and higher cutoff frequency for the GSD JNTs.

2. Device fabrication

Si nanowire array JNTs were fabricated on Silicon-on-Insulator

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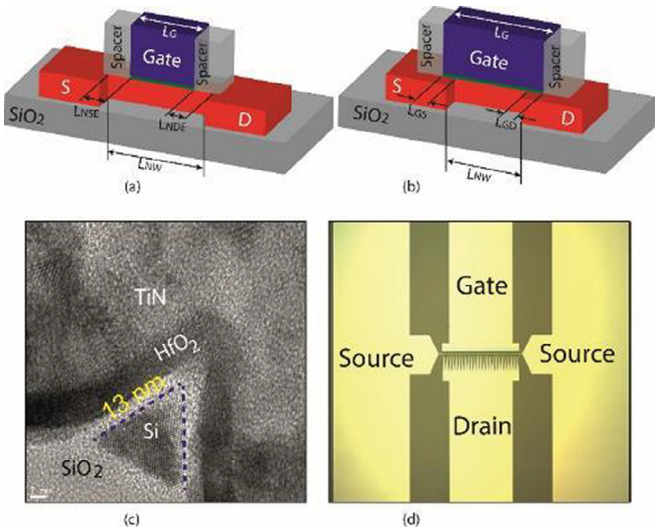

Fig. 1. Cross sectional schematics with only the top gate on a single Si nanowire for (a) NSDE, and (b) GSD JNT. (c) A TEM image shows a triangular shape Si nanowire. (d) A microscope image of the final device showing the GSG structure for RF measurements.

(SOI) substrate with a 60 nm-thick top silicon and a 145 nm-thick buried oxide (BOX). Firstly, the substrate was implanted with phosphorus ions to a dose of 2×10^{14} atoms/cm^2, and then annealed at 1000 °C for 30 s to activate the dopants, targeting a doping concentration of $\sim 2 \times 10^{19}$ cm^{-3} as estimated from simulations. The isolated mesa with NWs were defined by e-beam lithography and reactive ion etching (RIE). Each NW array consists of a sufficient number of nanowires in parallel (625 NWs) to be able to extract accurately the small-signal equivalent circuit of each architecture by on-wafer RF measurements. The length of NWs between two pads is defined as the nanowire length L_{NW}, as indicated in Fig. 1(a). The fabricated NWs are about 25 nm-wide. Then, NWs were thinned down by well controlled chemical etching. A gate stack consisting of 5 nm HfO_2 and 60 nm TiN was deposited by atomic layer deposition (ALD) and sputtering, respectively, and then patterned by e-beam lithography and RIE. After SiO_2 spacer formation (100 nm in width), nickel silicide was formed at source and drain regions. Finally, a passivation layer was deposited and metal contacts to gate and S/D were fabricated after opening contact windows through the passivation layer. Fig. 1(c) shows a cross sectional TEM image for a single Si nanowire with gate stack. The nanowire shows a triangular shape with a side length of 13 nm. A SiO_x interfacial layer (~2 nm-thick) is clearly seen in the image, resulting in a large EOT of gate oxide. The interfacial layer is formed during our processing. Multi-gate fingers and coplanar Ground-Signal-Ground (GSG) structures for RF measurements were fabricated as shown in the optical image of Fig. 1(d). Four sets of devices with NSDE and GSD structures as listed in Table 1 were fabricated on the same chip. Because JNT operates in enhancement-mode, the effective channel length is determined by the nanowire length under the gate.

The fabricated devices were characterized in DC and at high frequencies. RF performances are extracted from measured scattering parameters (S-parameters) in the frequency range from 0.1 to 40 GHz.

Table 1
List of fabricated JNTs with different geometries which were measured by scanning electron microscopy (SEM).

Definition	L_{NW} (nm)	L_G (nm)	Gate-S/D
SET 1	115	80	NSDE
SET 2	80	120	GSD
SET 3	110	120	GSD
SET 4	65	120	GSD

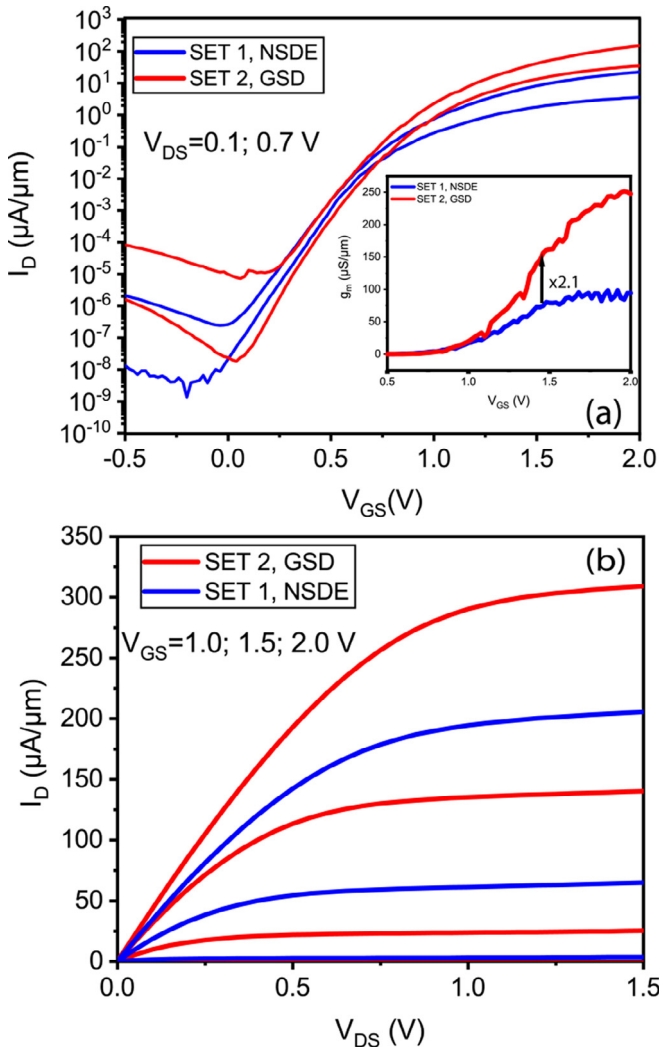

Fig. 2. Comparison of the measured (a) I_D-V_{GS} transfer and (b) I_D-V_{DS} output characteristics for a GSD JNT and a NSDE JNT with the same effective channel length, showing a better performance of the GSD JNT. The inset in Fig. 2(a) compares the transconductance g_m for the corresponding two JNTs at V_{DS} = 0.7 V.

3. Results and discussion

Fig. 2(a) shows the I_D-V_{GS} transfer characteristics for JNTs with a NSDE (SET 1) and a GSD (SET 2) architecture, respectively. For the SET 1 and SET 2 JNTs the effective channel length is the same because the device is switched off by depletion of the gated nanowire region where stronger electrostatics are present. This means for SET 1, only the NW below the gate (L_G = 80 nm) and for SET 2, only the NW between the S/D pads (L_{NW} = 80 nm) are easily switched off by the stronger gate control. Thus, the comparison between SET 1 and SET 2 JNTs can offer us a better understanding about the impact of NSDE and GSD gate on the device performance. For the SET 1 JNT, the total length of the NSDE, $L_{NSDE} = L_{NSE} + L_{NDE}$ = 35 nm. For the SET 2 device, $L_{GSD} = L_{GS} + L_{GD}$ = 40 nm. Fig. 2 clearly indicates a smaller subthreshold swing of *SS* = 90 mV/dec for the GSD JNT in comparison of *SS* = 106 mV/dec for the NSDE device. The higher *SS* than the ideal value for both devices could be caused by the larger EOT and the triangular shape of the nanowire, where the electrical field cross the nanowire is not uniform leading to different V_T at different positions of the nanowire. Furthermore, the NW dimension variations in the array

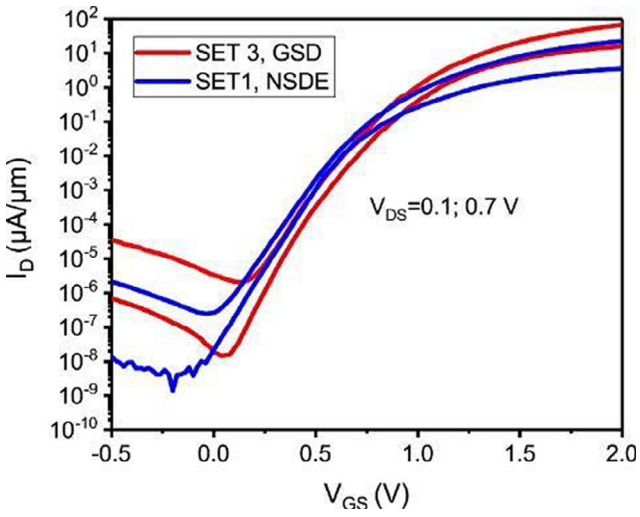

Fig. 3. Comparison of the measured I_D-V_{GS} transfer characteristics for a GSD JNT and a NSDE JNT with similar NW length, showing a better performance of the GSD JNT.

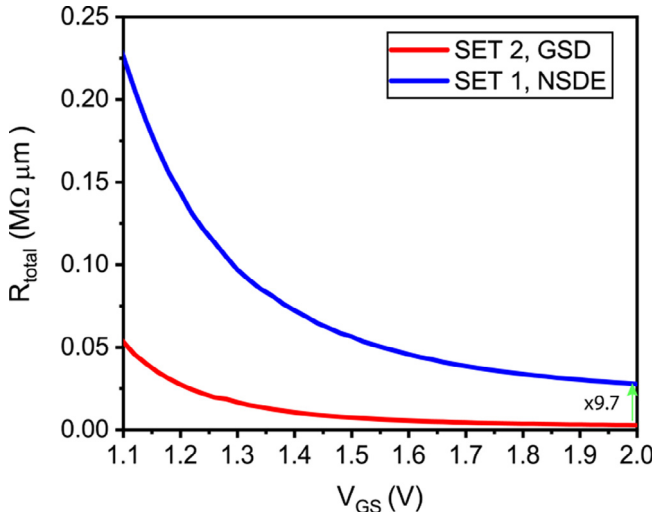

Fig. 4. Extracted total resistance at V_{DS} = 0.1 V, showing that the series R_{SD} for NSDE device is much larger than the GSD device.

could also lead to *SS* variation for each single NW, and thus degrade the final *SS* of NW array JNT. The threshold voltage V_T for these two measured JNTs are almost the same at V_{DS} = 0.7 V, corresponding to V_T = 0.46 V which are extracted at a constant drain current of $I_D = 1 \times 10^{-3}$ μA/μm in Fig. 2(a). Higher gate induced leakage (GIDL) currents are clearly seen for the GSD device, where the larger overlap between the gate and drain increases band-to-band tunneling area thus resulting in larger GIDL. The GSD JNT shows also higher transconductance g_m (in the inset) with an increase factor of 2.1 at V_{GS} = 1.45 V, V_{DS} = 0.7 V compared with the NSDE JNT. The higher on currents of GSD JNT are further demonstrated by the I_D-V_{DS} output characteristics in Fig. 2(b). Good saturation is also shown in Fig. 2(b) for both devices. The average output conductance g_d in the saturation region (V_{DS} > 0.9 V, V_{GS} = 1.5 V) is extracted to be 9.5 μS/μm for the GSD and 7.3 μS/μm for the NSDE JNTs. At V_{DS} = 0.7 V, V_{GS} = 1.5 V, $g_d = 16\mu S/\mu m$ for the NSDE JNT, and $g_d = 22\mu S/\mu m$ for the GSD device, thus the voltage gain (g_m/g_d) is calculated to be 7.36 for the GSD JNT and 4.9 for the NSDE JNT. The GSD device shows a higher voltage gain with a factor of 1.5 than the NSDE JNT at V_{DS} = 0.7 V, V_{GS} = 1.5 V.

Fig. 3 compares the I_D-V_{GS} transfer characteristics for the SET 1 and SET 3 JNTs, which have almost the same NW length. The GSD JNT of SET 3 still shows higher drive currents than the NSDE JNT even though the GSD device has a longer gate length. The large difference of the on-current is mainly due to the high series source/drain resistance for the NSDE JNT. Fig. 4 presents the total resistance R_{total} at on-state for the NSDE and GSD JNTs (SET 2), where R_{total} is extracted at V_{DS} = 0.1 V using:

$$R_{total} = \frac{V_{DS}}{I_D} = R_{ch} + R_{SD} \tag{1}$$

where R_{ch} is the channel resistance which decreases with increasing gate voltage, R_{SD} is the S/D series resistance including source resistance R_S and drain resistance R_D. At very high gate voltage R_{total} is dominated by R_{SD}. We can see at V_{GS} = 2.0 V, R_{total} for the NSDE device is almost one order of magnitude higher than that of the GSD JNT, thus causing lower on-currents.

The source resistance R_S lowers the effective gate voltage by:

$$V_{GS} = V_{eGS} + R_S I_D \tag{2}$$

where V_{eGS} is the effective gate voltage with negligible R_S value.

Then the subthreshold swing *SS* is changed to:

$$SS = \frac{d(V_{GS})}{d(\log_{10} I_D)} = \frac{d(V_{eGS})}{d(\log_{10} I_D)} + \frac{d(R_S I_D)}{d(\log_{10} I_D)} = SS' + R_s I_D ln10 \tag{3}$$

where SS' is the subthreshold swing with negligible R_S.

We can see from Eq. (3) that high R_S increases *SS* mainly at large I_D, which is demonstrated by the experimental results shown in Fig. 5. At $V_{GS} > 0.5V$, *SS* increases much faster for the NSDE device because of the higher R_S.

Moreover, the measured average *SS* at very small I_D (from 10^{-13} to 10^{-11} A/μm) at V_{DS} = 0.1 V shows higher values with a larger variation for the NSDE JNTs (SET 1), as indicated in Fig. 6. JNTs in SET 4 present the smallest *SS* variation in which the L_{GSD} is much larger than the other sets of devices. The large variation of *SS* for such small I_D cannot be attributed to the high R_S for the NSDE JNTs as seen from Eq. (3) and Fig. 5. The high fringing field in the NSDE JNT results in the degradation of *SS* and the increase of the *SS* variation as reported by theoretical simulations [16,17], which will be discussed also in the simulation section in this paper. For the GSD JNTs, the large planar gate contact on the large pads lowers the fringing field.

The impact of the gate alignment on the device performance for JNTs is further reflected by the V_T and DIBL (drain induced barrier lowing). The NSDE JNTs (SET 1) show higher average V_T value and

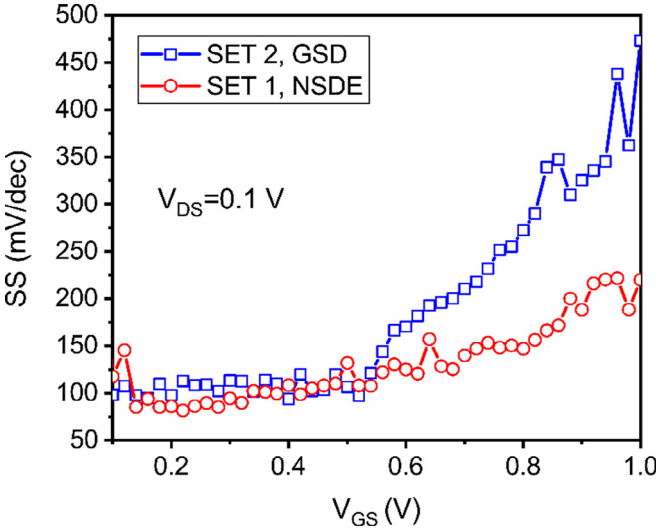

Fig. 5. Measured *SS* for a NSDE JNT and a GSD JNT, showing faster *SS* increase for the NSDE device at V_{GS} > 0.5 V due to the large source resistance.

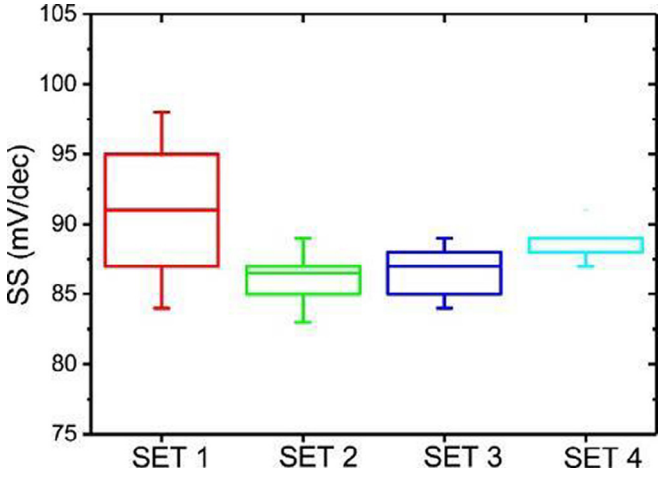

Fig. 6. Measured *SS* in the small I_D range for the four sets of JNTs listed in Table 1, showing a larger *SS* variation for the NSDE devices (SET 1).

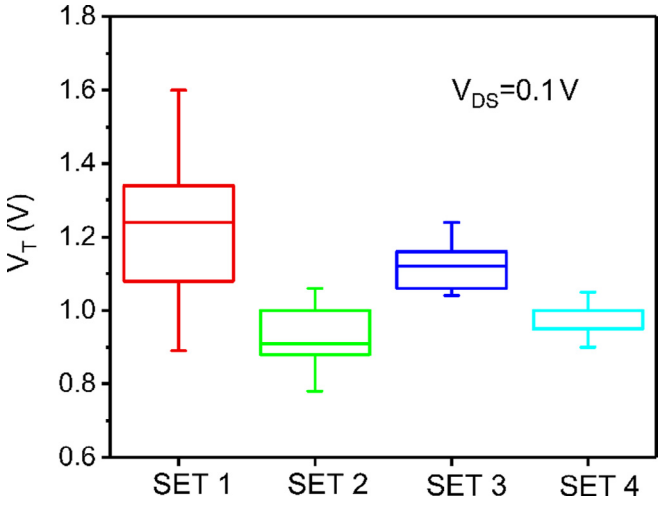

Fig. 7. Measured V_T for the four sets of JNTs listed in Table 1, showing larger V_T variation for the NSDE devices (SET 1).

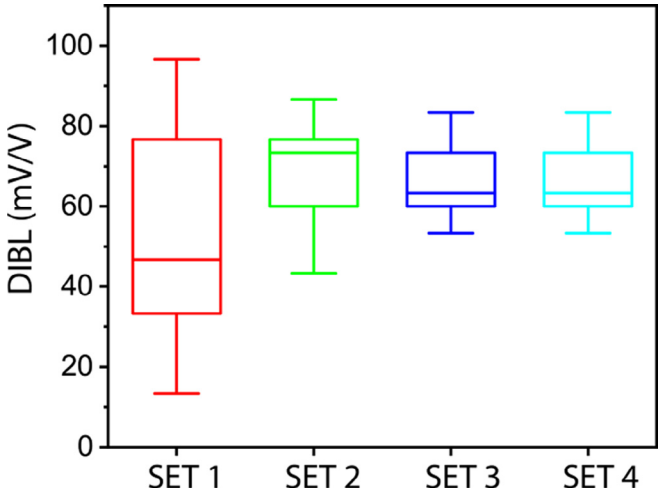

Fig. 8. Measured DIBL for the four sets of JNTs listed in Table 1, showing larger DIBL variation for the NSDE devices (SET 1).

much larger variations than the GSD JNTs as demonstrated in Fig. 7. The measured DIBL, as presented in Fig. 8 presents similar variations as V_T. From Eq. (2), we can see a larger Rs of NSDE JNT causes a smaller

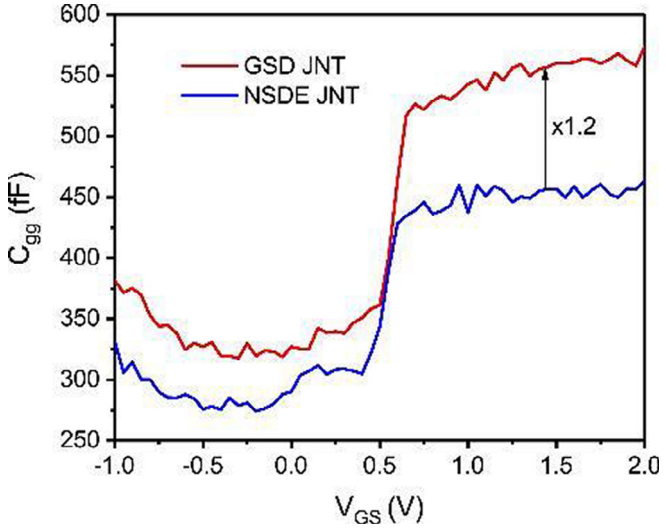

Fig. 9. Measured C_{gg}-V_{GS} curves of NSDE JNT (SET 1) and GSD JNT (SET 2), showing higher parasitic capacitance for the GSD JNT due to the large gate to source/drain overlap.

effective gate voltage V_{eGS} than that for the GSD device, thus needs higher V_T to switch the device. As reported in [18,19] DIBL is proportional to the effective V_{eDS}.

$$V_{eDS} = V_{DS} - I_D R_{SD} \tag{4}$$

Therefore, a higher R_{SD} causes smaller DIBL, which is demonstrated in Figs. 2 and 8 for the NSDE device. However, the large R_{SD} variation of the NSDE JNTs results in larger DIBL variation, as shown in Fig. 8. In addition, the high fringing field for the NSDE JNT can also increase the V_T and DIBL [16,17]. For NSDE JNTs the misalignment of the gate with variations of L_{NSE} can further increase the variation of R_S. The nanowire dimensions variation in the extension regions causes R_{SD} variation. All these effects result in large variations of V_T and DIBL for NSDE JNTs.

The gate capacitances C_{gg} of NSDE and GSD (SET 2) JNTs were measured and extracted. Fig. 9 shows the results at a frequency of 100 kHz. It is clear that the gate capacitance C_{gg} for the GSD JNT is larger than NSDE JNT (with a factor of 1.2 at V_{GS} = 1.45 V) because of the larger gate/source overlap area.

RF measurements can provide a unique insight into the transistor dynamic behavior [20–22]. A direct figure of merit we can get from the S-parameters is the cutoff frequency (f_T) of the current gain. The tradeoff between the improved on-current and larger gate capacitance can be characterized by f_T since,

$$f_T = \frac{g_m}{2\pi C_{gg}} \tag{5}$$

where g_m is the transconductance proportional to the on-current and C_{gg} denotes the total gate capacitance [23]. The S-parameters for a NSDE (SET 1) and a GSD JNT (SET 2) were measured at V_{DS} = 0.6 V and de-embedded using their associated open structure [24]. The current gains (H_{21}) are calculated from the S-parameters. f_T is extracted from the frequency at which the current gain equals to 0 dB, as shown in Fig. 10. f_T of the GSD JNT reaches 29 GHz, while f_T = 16 GHz for the NSDE JNT which is comparable with our enhancement-mode gate-all-around nanowire MOSFETs with NSDE architecture [25]. An increase factor of 1.8 for the f_T of GSD JNT is in agreement with the measured g_m in Fig. 2 and the capacitance in Fig. 9 considering Eq. (5). The result of f_T unambiguously proves the advantage of GSD JNTs over NSDE JNTs in respect of the transistor dynamic performance. The improvement of on-current in GSD JNTs surpasses the increase of the gate capacitance. The 29 GHz f_T is also comparable with the reported f_T of nanowire MOSFETs from other groups [25–27].

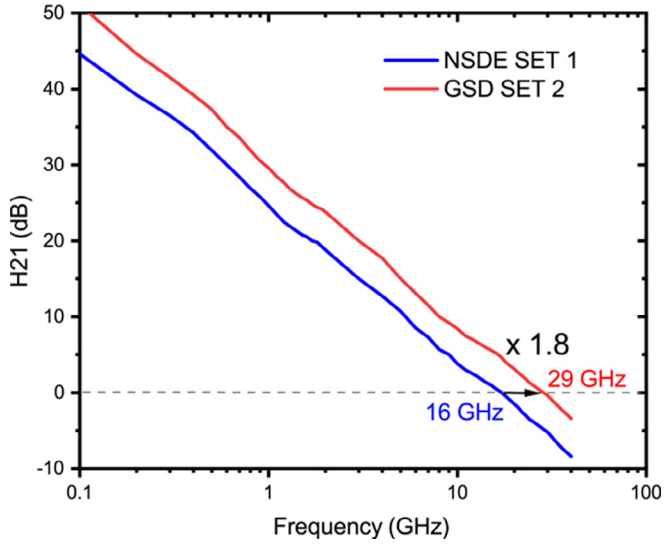

Fig. 10. Current gain of GSD and SDE JNTs extracted at V_{DS} = 0.7 V, V_{GS} = 1.45 V, indicating a cutoff frequency of 29 and 16 GHz for the GSD and NSDE JNTs, respectively.

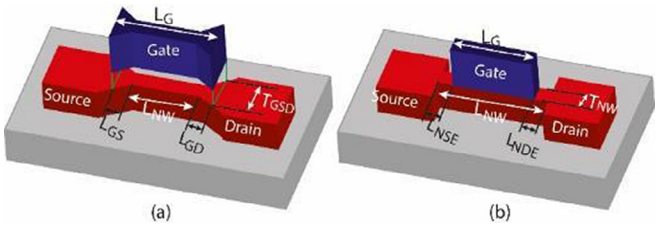

Fig. 11. Proposed dumbbell JNT structure (left) in comparison with a NSDE JNT for TCAD simulation.

Table 2
Device dimensions for TCAD simulation.

JNT	L_{NW} (nm)	L_G (nm)	T_{NW} nm	L_{GS}/L_{NSE} (nm)	L_{GD}/L_{NDE} (nm)	T_{GSD}(nm)
Dumbbell	50	70	10	10	10	30
NSDE	90	70	10	10	10	

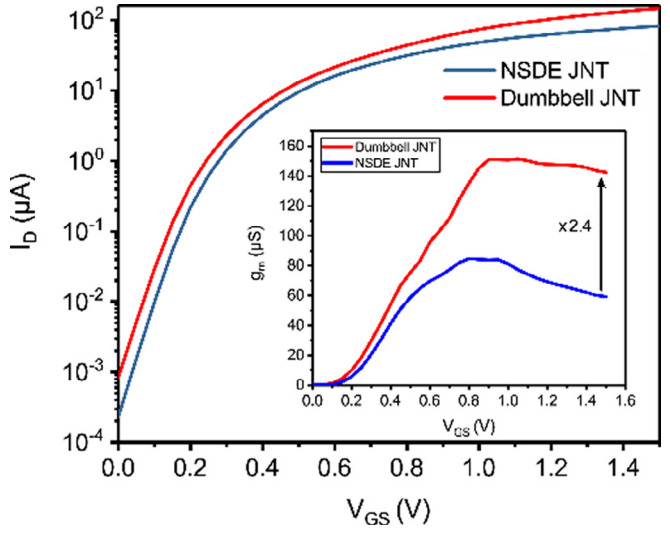

Fig. 12. TCAD simulated results for the proposed "dumbbell" JNT with a single nanowire at V_{DS} = 0.7 V, showing higher on-current and transconductance g_m compared with the reference NSDE JNT.

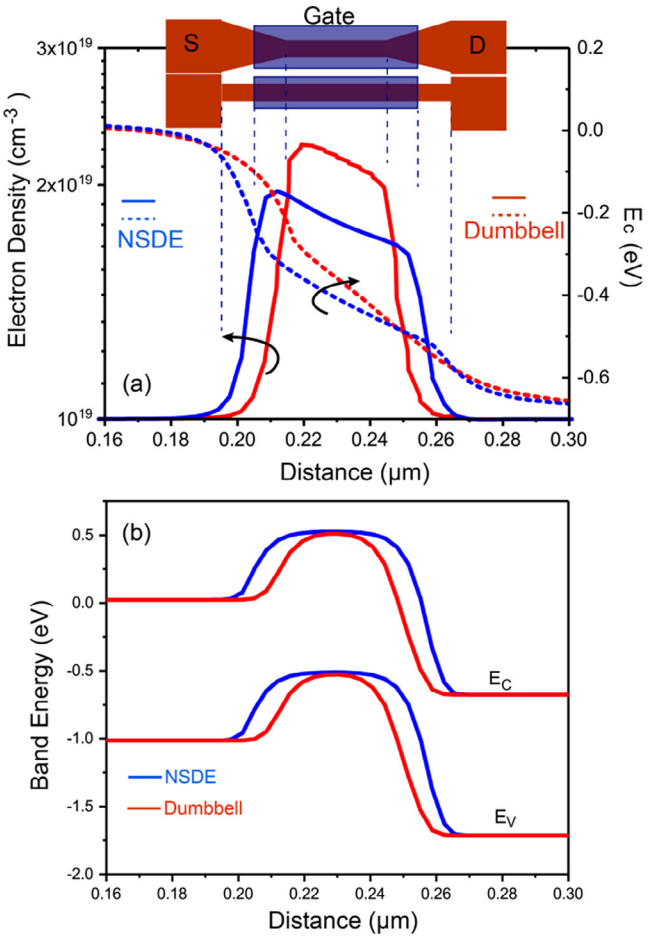

Fig. 13. (a) TCAD simulated electron density in on-state (V_{DS} = 0.7 V and V_{GS} = 1.5 V) and the corresponding conduction band diagram of NSDE (blue line) and Dumbbell (red line) JNTs at the center of the NW shown in Fig. 10. The lower conduction band energy at the source side of the channel for the NSDE device is caused by the high fringing electrical field. (b) The simulated band energies in the off-state (V_{DS} = 0.7 V, V_{GS} = − 0.3 V) indicate the NW extension regions for the NSDE JNT are depleted due to the fringing field.

Based on the experimental results we propose a "dumbbell" JNT structure as shown Fig. 11, which is similar to the conventional FET structures as proposed in [28,29]. The wider extension reduces the series source/drain resistance and suppresses the fringing field effects. Detailed dimensions of the simulated device are listed in Table 2 with a NSDE JNT as a reference. The NW has a fin shape with a width T_{NW} = 10 nm and a height of 50 nm and a doping concentration of 1×10^{19} cm^{-3}. Tri-gate with 3 nm-thick HfO_2 is used for both simulated JNTs. Models including quantum confinement, doping-dependent mobility model, the high-field velocity saturation model, a doping-dependent band-gap-narrowing model and the Shockley-Read-Hall generation/recombination models are used for the Sentaurus TCAD simulation. The first TCAD simulation demonstrates higher on-current and transconductance g_m (with a factor of 2.4 at V_{DS} = 0.7 V and V_{GS} = 1.45 V) as shown in Fig. 12 in comparison with the NSDE JNT.

Fig. 13(a) shows the simulated electron densities and also the conduction band energies from source to drain at on-state (V_{DS} = 0.7 V, V_{GS} = 1.5 V) for both the dumbbell and the NSDE JNTs at the center of the NW. The lower conduction band energy at the source side of the channel for the NSDE JNT is caused by the higher fringing field which results in accumulation of electrons at on-state. The high fringing field leads to degradation of *SS* and DIBL [16,17], as also experimentally confirmed in Figs. 6 and 7. Fig. 13(b) presents the simulated band energies for the off-state at V_{GS} = -0.3 V. The NW extension regions for

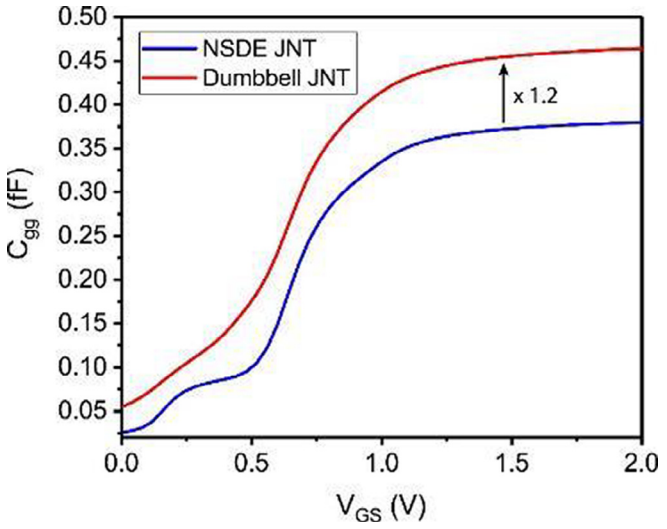

Fig. 14. TCAD simulated comparison of C-V at 1 MHz for the proposed single "dumbbell" nanowire with the reference NSDE JNT.

the NSDE JNT are depleted by the strong fringing fields, causing a longer effective channel length in off-state. For the dumbbell JNT the gate/source (drain) overlapped regions are less depleted than the NSDE JNT. It is thus clear that for the dumbbell JNT the device is switched on/off mainly in the gated very thin nanowire channel region.

Fig. 14 shows the simulated C-V results for a "dumbbell" JNT in comparison with a NSDE JNT. Similarly to the experimental results shown in Fig. 9, the larger gate to source/drain overlap areas in the "dumbbell" JNT result in higher gate capacitance with a factor of 1.2 at V_{GS} = 1.45 V. Finally, an increase factor of ~ 2 is thus expected for f_T at V_{DS} = 0.7 V, V_{GS} = 1.5 V by estimation from Eq. (5), showing superior RF performance of "dumbbell" JNTs.

4. Conclusion

We have experimentally investigated the effects of the gate alignment in JNTs. Devices with NSDE gate alignment show high series source/drain resistance due to the lowly doped narrow nanowire extensions, thus causing lower on-currents and larger variations in terms of *SS*, and V_T in comparison with GSD JNTs. We have also found that the high fringing field in the NSDE JNT results in degradation of *SS*. Due to the improved on-current GSD devices show much higher cutoff frequency. Optimizations of gate to source/drain overlap, fringing field effect reduction with a dumbbell-shape nanowire structure to lower the series NSDE resistance and to minimize parasitic gate capacitance have been proposed and demonstrated with simulations.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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