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Structural and nanomechanical properties of porous silicon: Cheap substrate for CMOS process industry

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The surface topology of porous silicon (PSi) is a relevant parameter that decides the compatibility of such substrate with CMOS process. Using standard resistivity (1–10 Ω·cm) of Si substrate to fabricate PSi-S is a low cost solution for the industry. In this paper, through an atomic force microscopy (AFM) analysis, the root mean square (RMS) roughness, the power spectral density and the correlation length were determined for different PSi layers. Furthermore, the measured hardness, Young's modulus, and stress have been made for different thicknesses of PSi: 5, 10, 50, and 200 μm. The obtained results demonstrated that very interesting properties have been achieved with the 50 μm-thick PSi-S layer with a maximum porosity around 65%, a surface roughness less than 1 nm and a hardness value of (∼1 GPa). The realized results encourage the utilization the PSi-based substrate into the industry process and thus the development of a Systems-on-Chip (SoC).

KEYWORDS

hardness, porous silicon (PSi), power spectral density, System-on-Chip (SoC)

1 | INTRODUCTION

Due the increased demand for next generation wireless communication, a huge market is advertised for the development of both active and passive integrated circuits. However, it is difficult to integrate the passive and active devices in the same sample due to bad insulating properties of the involved substrates.[1,2] Various solutions have been investigated to replace the bulk silicon by innovative substrates, for instance, glass substrate,[3] high resistivity (HR-Si) substrates,[4,5] or high resistivity trap-rich substrate.[6] Nevertheless, the proposed solutions have encountered difficulties in their achievements such as the high cost or the long process time. In the last years, a great interest was focused on PSi fabricated by the electrochemical anodization of silicon in hydrofluoric acid (HF)-based electrolytes. This solution aimed to provide solution to reduce the cost and the fabrication process complexity. Thanks to its large surface area and the control of its layer properties through various characterizations, most of the works related to PSi as substrate have been devoted to different applications such as electronic,[7] photonic crystal sensors,[8] and magnetic sensing.[9] However, the compatibility of the PSi with industrial processes remains questionable, and the study of its mechanical characteristics should be performed while accounting this issue.

The morphology of substrate is important in order to produce high performance of integrated devices. Therefore, the study of structural and mechanical properties of the post-anodization process of PSi is inescapable. To address this issue, an important number of articles have been devoted to the investigation of mechanical properties of PSi on Si bulk substrate.[10–16] However, a focus should be performed on the layer uniformity with anodization, and the complete cancellation of etch residue products and moderate pore volumes.[17,18] Indeed, the latter aspect should be highlighted because the porosity, stress, and roughness of the PSi layer could affect the integration devices. For this reason, it becomes essential to characterize precisely the mechanical behavior of PSi to optimize the manufacturing process in order to reach mechanical requirements for industry process integration.

Contrary to our previous papers where we have focused on substrate electrical performances,[19–21] in this article, we figure out the structural and mechanical properties of PSi substrates, these characterizations are undertaken with the aim of better adapting the porosification parameters in the idea of integrating the PSi with the standard processes of the industry. So we have investigated the nanomechanical properties and the structure analysis of the PSi layer with different thicknesses formed on p-type Si substrate with two resistivities. The PSi layers formed by anodization are characterized by scanning electron microscopy (SEM), atomic force microscopy (AFM), and nanoindentation. The main objective is to explore the influence and the relationship between the nanomechanical properties, namely, stress, and roughness of the analyzed structure of the PSi layer, without losing sight of PSi integration in industrial processes.

2 | EXPERIMENTAL

Electrochemical etching platform is used inside a fume-hood at room temperature for the porosification of p-type silicon substrates doped B with resistivities of (ρ = 1–10 Ω·cm, PSi-S) and (ρ = 5–20 mΩ·cm, PSi-M). The electrolyte used for the anodic etching process for the PSi-S substrates was based on a 2:1 mixture of (50%) HF and ethanol, and a current density of 10 mA·cm^{-2} was applied during different etching times leading to the various PSi thicknesses. On the other hand, the sample with 50 μm thickness, PSi-M, was etched in HF : ethanol (1:1 in vol.), at current density 75 mA·cm^{-2} during 40 min. In addition, another Si-based substrate is introduced for comparison with PSi, it is trap-rich substrate, where a layer rich in traps was introduced between n-type silicon bulk doped P and silicon oxide (see Figure 1A).

The surface morphology, roughness, and spectral analysis were characterized by AFM. The microstructure of PSi samples was observed by a field emission scanning electron microscope (FE-SEM, GEMINI Ultra 55 Zeis). The porosity is calculated by gravimetry method by weighting the sample before anodization (m_1), after anodization (m_2) and after a KOH etching of the PSi layer (m_3) using the following equation:

$$P = (m_1 - m_2)/(m_1 - m_3). \quad (1)$$

The hardness and elastic modulus were measured using Agilent Nano Indenter G200 system equipped with a Berkovich indenter by the load–depth-sensing nanoindentation method. The hardness was calculated according to the Oliver–Pharr method as an average from 16 indents.[22] The stress of different thickness of PSi was deduced from Stoney's formula (Equation 2) after measuring the radius of curvature using an Alpha-Step profilometer by considering average measurements.

$$\sigma \approx \frac{E_{Si}}{6(1-\gamma_{Si})}\frac{t_{Si}^2}{t_{PSi}}\left(\frac{1}{R_1}-\frac{1}{R_2}\right), \quad (2)$$

where σ is the stress of the PSi film after anodization, E_{Si} is Young's Modulus of silicon substrate (171.2 GPa), γ_{Si} is Poisson's ratio (0.22), t_{Si} is thickness of silicon (381 ± 20 μm), t_{PSi} is thickness of PSi film, R_1 is curvature radius of the silicon substrate before anodization, and R_2 is curvature radius of the silicon substrate after anodization.

3 | RESULTS AND DISCUSSION

The microstructure top-view of PSi samples, sketched in Figure 1B, is mesoporous with a pore diameter (at the surface) ranging from 1 to

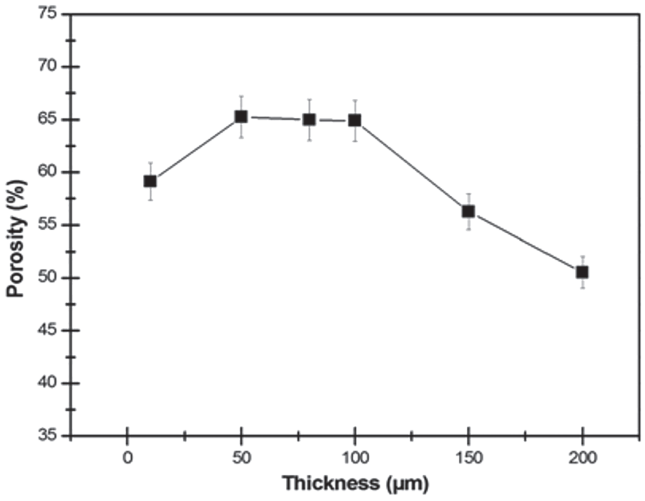

FIGURE 2 Variation of porosity with thickness for PSi-S

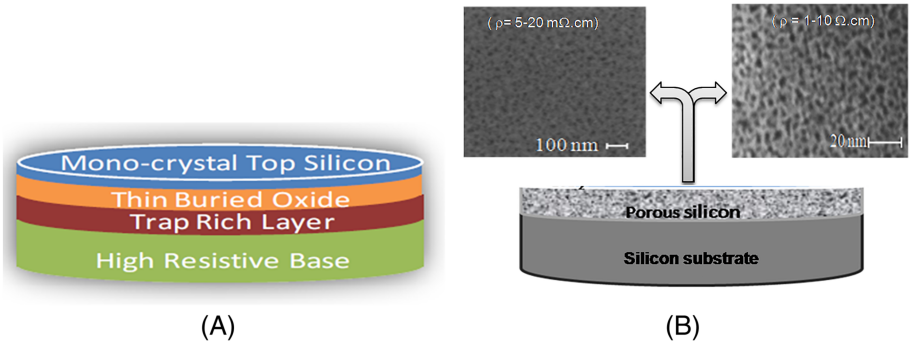

FIGURE 1 A, Trap-rich substrate and B, top-view microstructure of PSi samples (S at the left and M at the right)

TABLE 1 Comparison between two nominal resistivity

Sample	ρ (Ω·cm)	t_{PSi} (μm)	d_{pores} (nm)	P (%)
PSi-M	0.005–0.02	50	10–12.5	≈50
PSi-S	1–10	50	3–14	≥65

5 nm and from 10 to 12 nm for a PSi-S and PSi-M substrates, respectively.

The variation of porosity with thickness is related to the chemical dissolution of the porous material during its formation. According to Herino et al,[23] the porosity and pore size increase with increasing current density or decreasing HF concentration.

Therefore, it could be concluded that the porosity of PSi-M substrate increases with the increasing of thickness as it is observed in Fakiri et al,[16] on the other hand, for the same thickness (50 μm), the porosity increases with the increase of the resistivity.

In addition, the same observation is made for PSi-S substrate, the porosity increases with thickness until reaching saturation, which seems to be the highest porosity of 65% for 50 μm thickness as it is shown in Figure 2. This saturation is due to the edge effect, a large front of engraving (more area) for a constant total current, thus the current density is reduced implying a decrease in porosity with thickness. Thereafter, the PSi develops cracks and small pores start growing. All results corresponding to the two nominal resistivities are summarized in Table 1.

The PSi surfaces obtained after anodization and oxidation must own similar characteristics to those of monolithic silicon to withstand deposits, etching, and high temperature annealing of a standard process in microelectronics; in this way, the morphology of the PSi has been investigated.

From AFM image (Figure 3A), a change in the PSi structure is observed, and for a PSi-S substrate (1–10 Ω·cm), the size of pores

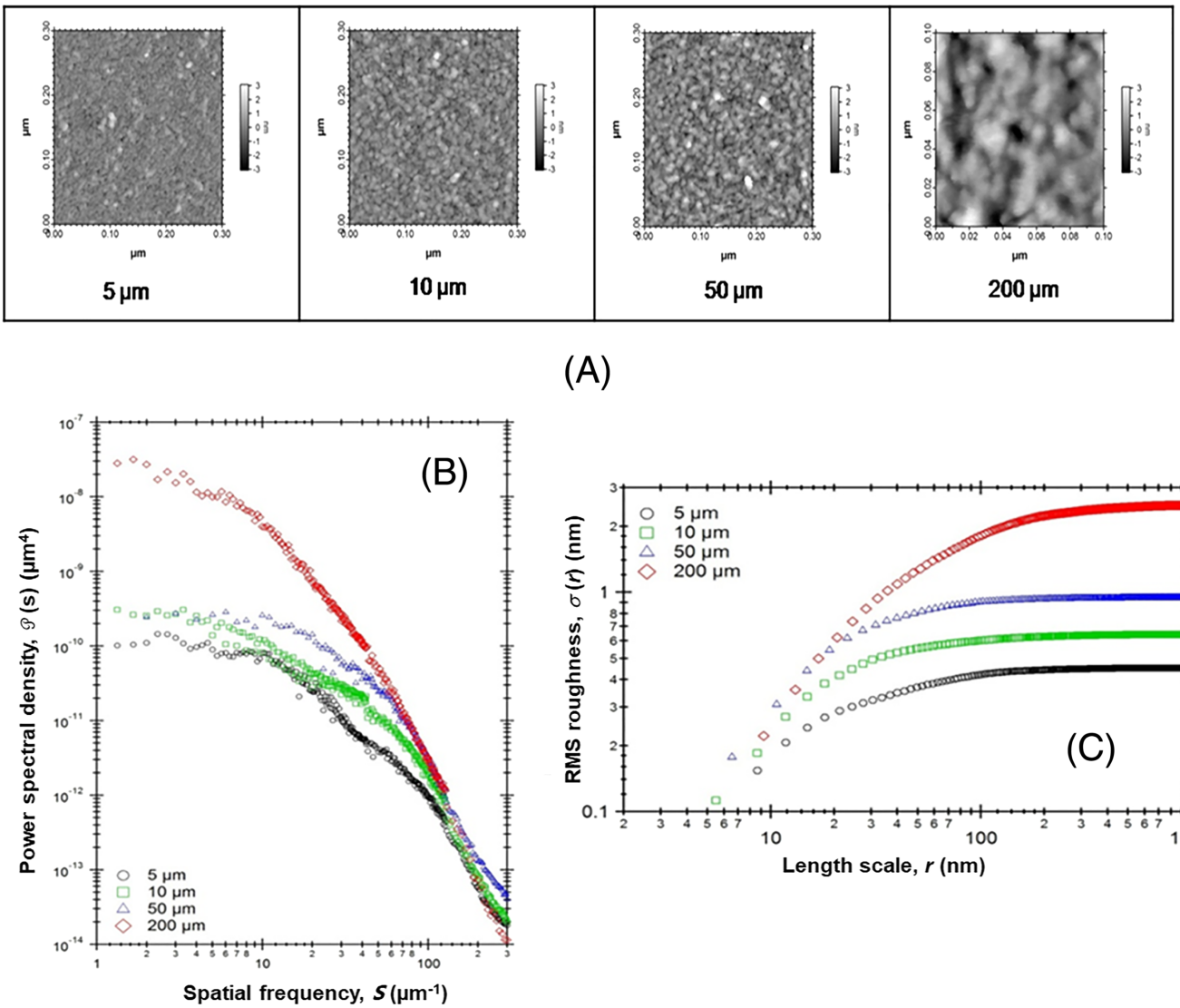

FIGURE 3 A, Atomic force microscopy (AFM) image of different thicknesses of PSi-S substrate, B, superposition of power spectral density versus spatial frequency, and C, superposition of root mean square (RMS) roughness versus length scale of (5, 10, 50, and 200 μm) thickness of PSi-S substrate

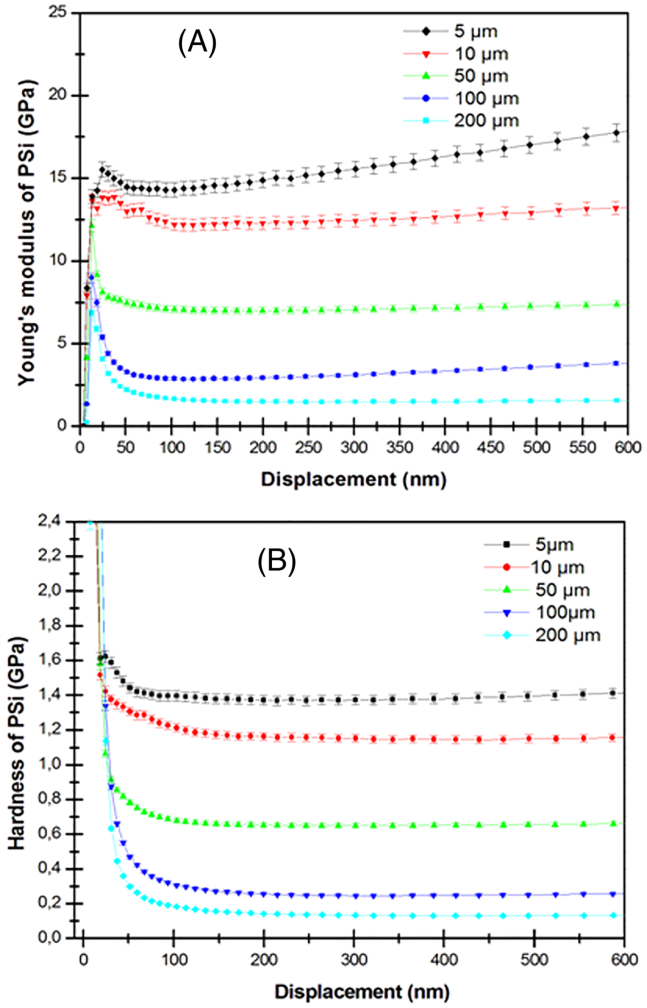

FIGURE 4 A, Variation of the Young's modulus. B, Hardness versus displacement in porous silicon for different thickness

increase with the time spent in the electrolyte, varying from 3 to 14 nm.

The power spectral density is the frequency response of a random or periodic signal. Figure 3B presents the superposition of power spectral density versus spatial frequency for different thicknesses of PSi: 5, 10, 50, and 200 µm. At the lower spatial frequency, flat curves with constant values are observed, whereas a significant variation is shown for a PSi thickness of 200 µm; this indicates where the average power is distributed according to the frequency.

Figure 3C shows, at small-scale, a roughness that is quite identical regardless the thickness of the PSi layer. However, at large-scale, the roughness increases with the thickness of the PSi layer. The root mean square (RMS) roughness becomes constant above 100 nm scan; this indicates that it is necessary to scan at least 100 nm to avoid losing information on the surface roughness. Therefore, one of the main benefits and advantage of PSi compared with Std is having large specific surface area despite a rougher surface.

According to Figure 3C, when the roughness is close to value of 1, this indicates a smooth surface.[13,14] From this result, we can conclude that the porous layer due to the electrochemical etching of silicon surface leads to an increase of the surface roughness. Despite this, the roughness reach 0.9 nm for 50 µm, so the surface of PSi still smooth, whereas it reaches 2.5 nm for 200 µm thickness of PSi because the pores of PSi are continuously etched to form large diameter of pores and that part of the fluorine molecules existing in the solution will find a difficulty to penetrate through the already formed pores associated of the porous layer to reach the Si bulk. Next, these molecules will stay on surface of the PSi layer which will undergo second time the etching.

Let us discuss the measurement of Young's modulus (E) and Hardness (H). Before starting this, it is important to measure them for bulk silicon. The average modulus of Si bulk is about 171.2 GPa with an average hardness of 12.3 GPa. These results fit well with those of Sun et al.[14] Figure 4A,B compares the E and H of five PSi-S samples with spongy structure for different thicknesses, and it reveals very low H and E values [e.g., the measured E of PSi (50 µm-thick) being equal to 8 GPa, this value is approximately 20 times lower than for bulk silicon (171.2 GPa)]. It is observed that, at the shallow indentation of surface, between (5 µm, 10 µm) and (100 µm, 200 µm) samples, the values of H and E have ~10% and 7% difference, respectively, but for the 50 µm sample, the value of H and E are in the middle, that is, about 50% difference. When tip exceeds 50 nm penetration depth, a slight difference is observed for all the samples. At early stage, an increase in hardness versus contact depth is observed until the hardness reaches a maximum value due to the finite value of the real tip.[24] So the change of thickness induces an inverse change of the Young's modulus, which can be explained physically by the amount of air (vacuum) due to the creation of paths in PSi layer induced after

TABLE 2 Comparison of PSi structures to the state-of-the-art

Refs	ρ (Ω·cm)	t_{PSi} (µm)	P (%)	d_{pores} (nm)	σ (nm)	E (GPa)	H (GPa)	Stress (MPa)
This work	0.005–0.02	50	50	10–12.5	2.04	43.5	3.3	–
	1–10	50	65	3–14	1	10.5	1	–20
Charitidis et al[13]	0.005	47	–	15–25		19	2.4	–
	1–3	42	–	–		4	0.3	–
Sun et al[14]	0.08–0.12	2.5 ± 0.1	71–87	–	–	0.8–4	–	7.9 ± 0.09
								0.8 ± 0.01
Dariani and Nazari[15]	1–5	–	20	14	–	38	–	–

porosification. This behavior indicates a higher wear resistance of the PSi sample.

The stress measurement based on radius of curvature measurements of PSi film is expressed using a Stoney's formula (Equation 2) stated in Section 2. The measurements revealed that the stress values of PSi layers are negative, which leads to a compressive stress, and that this stress decreases with increasing thickness of PSi and attains the value of −20 MPa for 50 μm thickness. A high wafer bending level could influence the stress measurements if the devices are integrated on PSi, so these wafers are incompatible for the integration within process of industry; for this reason, we have chosen the wafers with the low radius of curvature in order to minimize the stress of wafers.

Finally, to figure out the interest of the reached properties of the proposed PSi, we have drawn Table 2. This latter summarizes the comparison of PSi-S substrate versus works reported in the state-of-the-art. As it is observed through this table, for PSi-S sample, the smaller pore size and the smooth surface structure with 1 nm roughness have induced an important hardness with two times greater than that the highest measured one in literature, in addition, a smaller Young's modulus.

Concerning the electrical properties of PSi, they were investigated in Rack et al,[21] where the evaluated performances are summarized and highlighted the merits of PSi and, in particular, the PSi-S substrate. The latter provides the highest RF electrical performances, with very strong linearity, low relative effective permittivity (3.5), and high effective resistivity (5 kΩ·cm), it maintains its high performance all the way up to 175°C. Thus, the PSi-S substrate can be considered for the integration of high quality passives devices (results to be found in Belaroussi et al[20]).

4 | CONCLUSION

Material features of PSi substrate are investigated. The results obtained show especially for a 50 μm thickness of PSi-S substrate a maximum porosity around 65% with a high insulating surface area, a surface roughness less than 1 nm and a hardness value of (∼1 GPa). Both Young's modulus and hardness of the PSi films increase with decreasing film thickness. These observations can be attributed to changes in the PSi microstructure as the thickness is decreased. Radius of curvature measurements were used to study the stress of PSi films. In particular, the stress is influenced by the pore size, which scales with film thickness. The proposed PSi-S with all of those microstructural, nanomechanical properties, and highest radio-frequency (RF) electrical performances shows the highest specific structure quality that demonstrates an inexpensive basic substrate for the industry process.

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