An Ultra-Low-Power Read-Out Circuit for Interfacing Novel Gas Sensors Matrices

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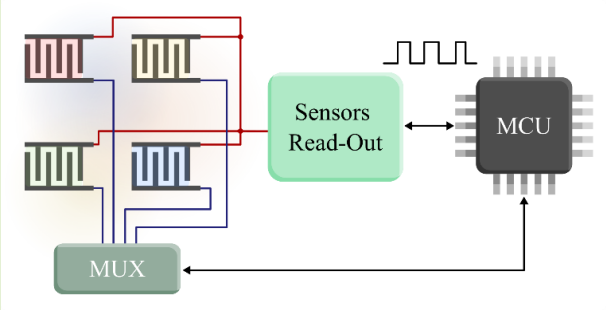
***Abstract*—New gas sensing materials, like conductive polymers and nanomaterials-based composites, together with integrated circuit advancements have enabled a new paradigm in gas sensing where a matrix of different types of sensors is used to improve selectivity and sensitivity. In this paper we present a highly flexible read-out circuit for acquiring the dc resistance of the sensors in the matrix. It can measure values from 1 kΩ up to 33 MΩ, with a minimum SNR of 57 dB. It also offers a wide range of input configuration in terms of resistance and bias voltages to select the optimal bias point for each sensor and to accommodate a large range of sensor types. It achieves very low power consumption at a maximum current consumption of 194 μA and an energy per conversion ranging from 1.21 nJ up to 188 nJ thanks to the optimization of the frequency of operation. The circuit was fabricated in a 180 nm bulk CMOS process and a complete characterization of the circuit is presented including current consumption, signal-to-noise ratio, and transfer function. Finally, the circuit was tested in a real application for the measurement of NH_3 and NO_2 using two different types of sensors validating the design objectives and the capability of the read-out circuit for system-on-chip integrations.**



***Index Terms*— Gas detectors, sensor systems, resistive read-out, relaxation oscillator.**

I. Introduction

IN THE beginning of the 1960's the first chemiresistive sensor was demonstrated by Seyama using ZnO as sensing layer, shortly after Taguchi fabricated and patented the first metal-oxide (MOx) sensor using SnO_2 as the sensitive material [1]. Since then, MOx gas sensors have continuously improved, and a better knowledge of their performances was acquired. New materials, miniaturization, and decades of testing have made these sensors arguably one of the main choices for gas sensing. Despite such progress, MOx sensors have proven challenging to integrate in ultra-low power and internet of things applications (IoT). This is mainly because the sensing element operates at high temperatures, in the order of hundreds of degrees Celsius, requiring a power-hungry heating element [2].

During the last three decades research on other types of sensing materials has taken place in parallel [3], [4]. Graphene and its derivates have shown to be a good candidate for gas sensors, many authors have fabricated and tested sensors for NO_2, CO_2 and NH_3 [5], [6], [7]. Another field that has produced significant results is that of the conductive polymers (CP), where polyaniline (PANI) [8] and polypyrrole (PPy) [9] stand out [10]. Other polymers, like polystyrene sulfonate (PEDOT:PSS) have been studied but to a lesser degree [11]. These polymers, by means of doping, nanostructuration or other treatments can be made sensitive to a wide range of gases including volatile-organic compounds (VOCs), NH_3 and CO [12]. Graphene and CP work at room temperature, thus eliminating the need for a heater. The reaction with the gas is frequently fully reversible, although exceptions have been reported with graphene [13].

From the signal point of view, these novel sensing materials present several challenges. To begin with, CP are poorly selective, so doping has been widely used to alter the selectivity and the sensitivity. Additionally, the baseline conductivity spans a

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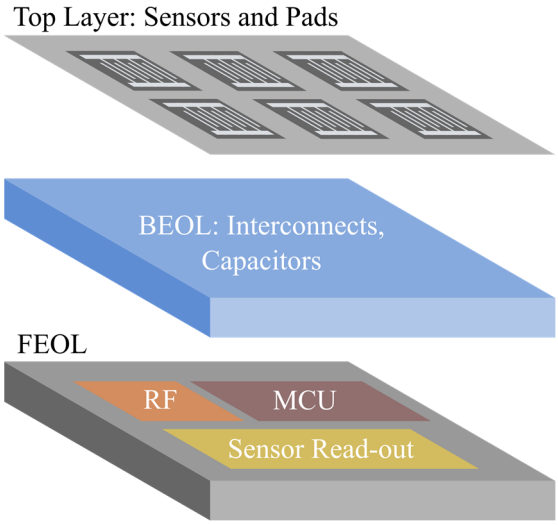

Fig. 1. Concept of a system-on-chip for gas monitoring with signal processing and communication.

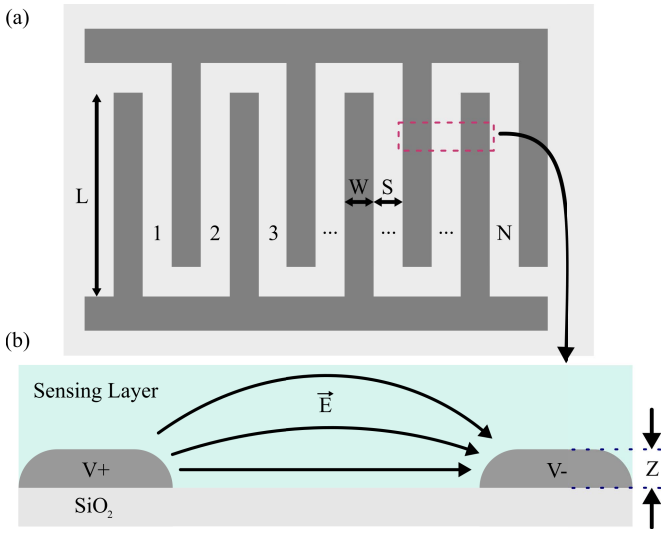

Fig. 2. Dimensions of IDE electrodes. (a) Top view, (b) Cross-section view of the inter-finger space with sensing layer and electric field.

very wide range for different formulations, so sensors tend to have very dissimilar nominal resistances. Significant amount of noise has been observed for the three types with flicker noise being predominant [14], [15], [16].

For creating a modern and flexible gas sensing platform, like in Fig. 1, we believe the inclusion of different types of materials such as Graphene, PANI, and PPy offers best results [17]. These sensors can be made with different chemistry and geometries to expand the sensing capabilities even further.

For the estimation of concentration of gases, a two-step procedure is needed. First, the sensors have to be interfaced with a read-out circuit to convert the physical, analog, resistance value into a digital one. Each electrode should be polled periodically, by means of a multiplexer and secondly, the estimated measure for each gas should be calculated by using the correlated values between sensors. To obtain the resistance estimations a dynamic and flexible read-out circuit is needed, one that can handle a wide range of input resistances, bias voltages while keeping power consumption at a minimum.

In this paper we present a read-out circuit to interface modern gas sensors that can meet the mentioned requirements. It offers very high dynamic range, ultra-low power, and is adaptable to each sensor requirements dynamically, making it ideal for interfacing a gas sensor matrix.

The paper is structured in the following way. In section II, we begin by a brief overview of the state of the art of CP and graphene sensors with the aim to establish the range of resistances that the interface must be able to accommodate. Then, in section III, the proposed sensor interface is explained with a detailed description of its working principle and the technology used. Section IV presents the results from measurements and finally we offer some conclusions and perspectives.

II. Sensors Overview

A. Construction

To ease the integration with traditional CMOS processes, the use of planar interdigitated electrodes (IDE) is preferred as they are built using only the top metal layer and make optimal use of the area that is exposed to the ambient air. In terms of electrodes dimensions, there are four degrees of freedom for the design: width (W), spacing (S), length (L), number of fingers (N), as shown in Fig. 2. Assuming a perfect coverage of the fingers by the sensing material, the resistance of the sensor can be approximated with (1) derived from the resistance of two parallel half-cylinders. This approximation is valid for a non-polarizable sensing layer that extends infinitely upwards, in practice, a layer with a thickness of 2Z already contains 90 percent of the current.

$$R = \frac{2 \cdot \ln\left(\frac{S}{Z} + 1\right)}{\sigma \cdot N \cdot L \cdot \pi} \tag{1}$$

The total width of the sensor is $L + 3 \cdot W$ and the length $(2 \cdot N + 1) \cdot W$. The maximum area per sensor is limited by the size of the chip and the number of sensors employed.

The conductivities for some sensing materials are listed in Table I. Even though, the electrodes dimensions can help equalize the final sensor resistance, the conductivity range is considerably larger than what dimensions can compensate, resulting in sensors with baseline resistance spanning several decades.

TABLE I
Properties of PANI, PPy and Graphene

Material	Doping / Treatment	σ (Scm^{-1})	Gas	Ref.
PPy	None	3.2 m	NH_3	-*
PPy	ClO_4	10.95	NH_3	[18]
PPy	ClO_4	65.34	NH_3	[18]
PPy	None	9.33 n	-	[19]
PANI	None	44 p	N_2, NO_X	[20]
PANI	$1HNO_3$	16.3 µ	CO, N_2	[21]
PANI	CSA	7.99	CO, N_2	[21]
PANI	-	256 µ	NH_3	-*
Graphene	None (Pristine)	5 m	NO_2	-*
Graphene	rGO	118 µ	NO_2	[22]
Graphene	rGO-1100°C	210	NO_2	[23]

*Have been measured in our laboratory.

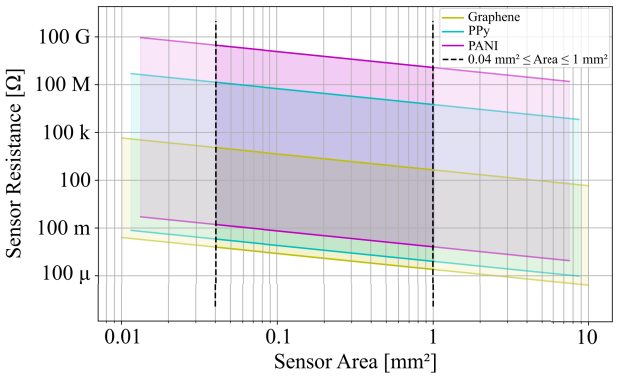

Fig. 3. Range of resistances for different formulations of sensing materials as a function of area. Finger width and spacing equal to 3 μm.

We have experimented with sensors with an area up to 1 mm^2 with W and S in the range of 2 μm up to 4 μm, Z fixed to 2 μm. The lower limit in sensor area is not set by the possibility of making such small electrodes but by the difficulty of accurately and reliably depositing the sensing layer. Our smallest sensors made by drop casting are 200 μm by 200 μm. Considering these values, for the same conductivity, we obtain a ratio of 400 between the largest and smallest resistances by only changing electrodes dimensions. Other mechanisms for applying the sensing layer, like inkjet printing, can be used to fabricate smaller sensors. Fig. 3 shows the resulting dc resistance for sensors made with the constraints imposed by the electrode area and the conductivities of Table I. Many sensing layer formulations with different properties fall in between the extremes, for this reason it is very important, and one of the objectives of this work, to make a read-out circuit that can accommodate very dissimilar sensors.

B. Signal Characteristics

The different conduction mechanisms and the specific reaction to each gas demand an individual analysis for every type of sensor. The sensitivity of each sensing material is usually nonlinear, and the sensor resistance can more than double or halve from its base value when exposed to high concentrations of gases in the most extreme cases [8]. Besides this, there is also a dependence on temperature, humidity, aging, cross-sensitivity, and the recovery from recent exposure to gases.

In [15], significant noise in Polyethylenimine doped graphene sensors was observed, and the authors proposed it as an estimation of gas concentration. On the other hand, noise figures reported for PPy are much lower [16]. In our experiments we have observed large noise in PANI sensors as well, as will be discussed in the measurements section. At low frequencies, flicker noise is predominant for all types, still the power spectral density (PSD) does not offer the complete picture, in the time domain fast changing steps are also observed sporadically for graphene and PANI whose origin is yet to be understood.

In relation to the time response, the reaction time is the most variable and important factor. In the literature reaction times of seconds up to tenths of minutes are reported for PANI and polypyrrole [8], [24]. The changes in reaction time are highly variable, similar formulations showing widely different values [8].

In this work we use the sensors dc resistance as an estimation of the gas concentration. To be compatible with the different sensor types and responses, the input dynamic range of the circuit interface must cover a large range of resistances from 1 kΩ up to 33 MΩ.

Other publications take a more sophisticated approach by measuring noise power or performing a spectroscopy, but these methods require considerably more energy since they perform digital signal processing [25], [26].

III. Sensor Interface

A. Architecture

Many solutions have been proposed to interface resistive sensors. Starting from classical approaches like the Wien bridge, or RC charging circuit made with discrete components to more modern approaches designed for VLSI from the start. Relaxation oscillators have been used to interface resistive sensors, their main advantage is that they can handle a very large input dynamic range which, as we explained, is needed for the cointegration of diverse gas sensors and a single read-out interface. By means of careful design, relaxation oscillators can also achieve a very good linearity [27]–[30]. The main drawback, which has been addressed by more digital approaches, is that the design is not scalable nor portable between technologies, this is a consequence of being highly analog in nature. They also require a sizeable silicon area because large transistors are used to diminish the nonidealities like mismatch, channel length modulation, noise and leakage. Relaxation oscillators have found a wide range of applications outside the sensor domain. This has resulted in many different approaches and viewpoints applied to the same working principle of the oscillator. and has nurtured the understanding and diversity of available configurations, even beyond CMOS. Recently, relaxation oscillators coupled with ferroelectric field-effect transistors [31] and vanadium oxide devices [32] have been used to generate hysteresis responses towards neuromorphic computing applications.

On the digital side, many read-out circuits have been published and share some common features. Very frequently a current DAC is used for biasing the sensor and the voltage at the sensor is fed to a voltage ADC or to a voltage-controlled oscillator (VCO) [33]–[35]. This type of interfaces can reach high signal-to-noise ratios (SNR), as it is a candidate for noise shaping and filtering embedded in the feedback loop, but our review of the literature indicates that they may not be as energy efficient as relaxation oscillators, at least for comparable dynamic ranges or when using similar CMOS processes (Table II). As our objective is to measure small fractional variations of sensor resistance over a very large range of baseline values, this becomes a severe constraint for ADC + DAC-based architectures that need to feature a very large ENOB (equivalent number of bits), calling for precision devices.

TABLE II
COMPARISON OF PUBLISHED READ-OUT INTERFACES

	This work	CICC 2012 [34]	VLSI Circuits 2015 [35]	ICICDT 2018 [27]	JSSC 2020 [33]	IEEE Sens. J. 2021 [30]
Type	Relax. Osc.	IDAC + ADC	IDAC + log + ADC	Relax. Osc.	IDAC + VCO	Relax. Osc.
Resistance Range (Ω)	1 k – 33 M	23 k - 4.6 M	10 k – 10 M	100 – 1 M	6 dec	100 / 300 k – 4.7 M
Area (mm^2)	0.143	2.8	1.23	0.125	0.064	0.24
Supply Voltage (V)	1.8	0.5	1.2/0.6	1.5	1.8	3.3
Technology (nm)	180	130	180	130	180	350
EPC (J)	1.21 n - 188 n**	11.3 n	1.42 n (worst)***	150 p – 675 n*	171 n	296 n (at 4.7 M)**

*Values acknowledged by the authors; the energy needed for the counter is not included.
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*** The biasing of the sensor is applied only during the sampling phase, not considering sensor stabilization.

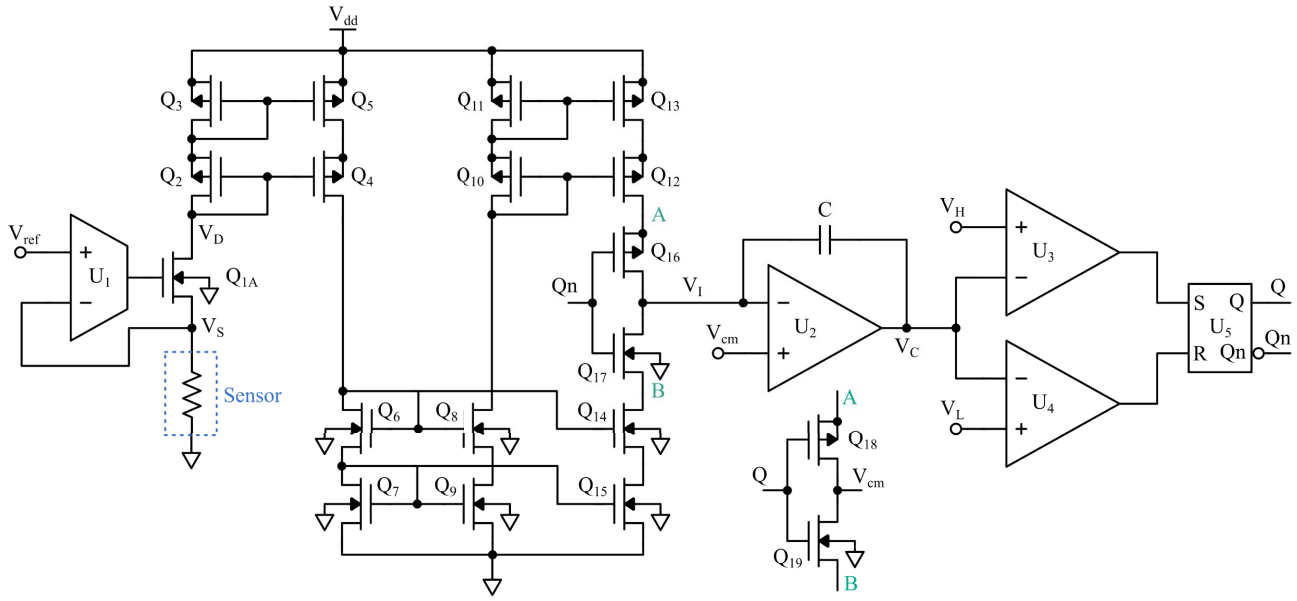

Fig. 4. Schematic of the designed read-out circuit.

Digital interfaces benefit from smaller CMOS nodes, but at the same time, smaller nodes lead to lower core voltages which may be insufficient for biasing sensors with high resistances. If the chip area is mostly determined by the sensors at the top layer, smaller nodes will also impact costs badly.

The last stage of relaxation oscillators-based read-out interfaces is a counter (internal or external) to digitalize the period length value. From an end-to-end perspective, these interfaces are digital converters as well, the key difference is how the analog signal is transformed in the process.

B. Schematic and Principle of Operation

The designed circuit is presented in Fig. 4, it builds on the same general principles as other relaxation oscillators [27], [28], but its components are designed and optimized for the multi sensor approach.

The sensor, with a resistance between 1 kΩ and 33 MΩ, is biased at a constant voltage V_{ref}, between 50 mV and 1 V (chosen so that $R \cdot I_{sensor}$ remains below 60 μA to limit power consumption). V_{ref} is generated by a voltage reference circuit made with an NMOS transistor, Q_{1A}, driven by an operational transconductance amplifier (OTA). The current flowing through the sensor and Q_{1A} is copied and divided by a factor $\gamma = 10$ by the asymmetrical cascode current mirror $Q_{2-3-4-5}$. This current is then copied by NMOS and PMOS cascode current mirrors to feed the integration capacitor C.

The complementary outputs Qn and Q of a set-reset (SR) register, U_5, control the switches Q_{16}-Q_{17} and Q_{18}-Q_{19} that respectively connect the current mirrors to the integrating node, or to a constant voltage V_{cm} to avoid cutting off their bias current. When Q_n is high, the NMOS cascode output is connected to the integrator and the PMOS is connected to V_{cm}, when Q_n is low the connections are permuted.

Assuming the sensor resistance is constant during each measurement cycle, the resulting current is dc, thus the voltage at the output of the integrator raises or decreases with a constant slope until it reaches V_H or V_L, Fig. 5. At this point, the comparators U_3 or U_4 toggle as also does the register, changing the direction of the current that is integrated in C. As a consequence, the waveform at the output of U_2 is a triangle wave where the period T is determined by (2). The value of C is 3.03 pF. The biasing circuit is designed to provide up to 60 μA to the sensor, higher currents would result in higher oscillation frequency, harder to digitalize

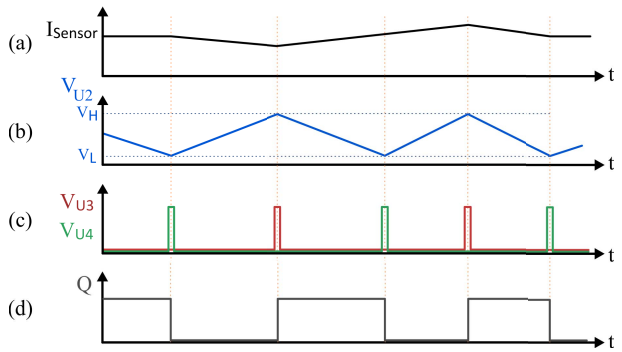

Fig. 5. Current and voltage waveforms for different nodes referred to Fig. 4, from the top: (a) Current flowing through the sensor, Q_{1A}, Q_2 and Q_3. (b) Voltage at the output of operational amplifier U_2. (c) Voltage at the output the comparators U_3 and U_4. (d) Voltage at the Q output of the SR flip-flop.

with a counter.

$$T = \frac{2 \cdot R \cdot C \cdot \gamma \cdot (V_H - V_L)}{V_{ref}} = \alpha \cdot R \tag{2}$$

Finally, the SR register stores the current state of the switches and generates the digital square wave output. A counter measures the period length, it can be either integrated in the read-out circuit, or use one of the counters already available in the microcontroller of the full system, we employ the latter approach here.

C. Technology Comparison

For the implementation of the integrated circuit, we considered three different technologies: 250 nm from TSMC, 180 nm from UMC and 65 nm from TSMC. The core voltages are: 2.5 V, 1.8 V and 1.2 V respectively.

For the current mirrors and the OTA, the benefit of using a smaller node is marginal, the performance of same size transistors in the three technologies is similar. There is an improvement in the Pelgrom's constants, positively affecting mismatch and linearity. A dc gate leakage current of up to 2pA was observed for the 65 nm node for a W = 10 μm, L = 10 μm NMOS device [36]. In the case of 180 nm and 250 nm transistors, the dc gate leakage was not modeled in simulations (virtually 0 A) and no reference to it was found in the documentation.

The operational amplifier and the comparators could benefit from a smaller node because, they could achieve higher frequencies at same power, and this results in a lower energy per conversion (EPC) as explained in the next section. From simulations, to obtain a f_t of 1 GHz with a minimum length transistor, the 250 nm node requires 150 nA of bias, the 180 nm node 100 nA and the 65 nm node 35 nA approximately.

Given that there is a need for a bias voltage of at least 1 V for the sensors, we decided to use the UMC RF-CMOS 180 nm technology for the implementation which provides the best tradeoff between power and maximum oscillation frequency.

D. Power Considerations

To analyze the performance of the read-out circuit in terms of power consumption, the energy per conversion (EPC) is the figure of merit that has been widely adopted in the literature [27], [30], [33], [34], [35]. Although we decided to use it to avoid introducing a new figure which would make comparison with previous work harder, it is worth noting that this figure has some drawbacks like not accounting for power-up energy, off-state current and stabilization time.

TABLE III
EFFECTS OF DESIGN PARAMETERS ON EPC

Parameter	Effect on E_{sensor}	Effect on $E_{interface}$	Effect on EPC	Effect on Frequency
↓ C	↓	↓	↓↓	↑
↓ γ	↓	↓	↓↓	↑
↓ V_H - V_L	↓	↓	↓↓	↑
↓ V_{DD}	↓	↓	↓↓	-
↓ I_{UX}	-	↓	↓	-
↑ V_{ref}	-	↓	↓	↑

To determine the best operating point in terms of power consumption, competing phenomena must be considered simultaneously. We study the two components that compose the EPC separately, the energy dissipated by the sensor and the energy dissipated by the interface (3).

$$EPC = E_{sensor} + E_{interface} \tag{3}$$

The energy dissipated by the sensor is equal to the power on the sensor times the period of the signal (4), but, as the period also depends on R in a proportional way (2), the final value is independent of it. The multiplication factor 1.3 is added to take into account the current flowing through the sensor branch and its three divided (by a factor of 10) copies in parallel branches in the current mirrors.

$$E_{sensor} = 1.3 \cdot \frac{V_{DD}}{R} \cdot T = \frac{1.3 \cdot 2 \cdot V_{DD} \cdot C \cdot \gamma \cdot (V_H - V_L)}{V_{ref}} \tag{4}$$

The energy consumed by the interface is set by the static current consumed by the active components multiplied by the period, plus a constant value for the energy needed to change the state of the SR register

$$E_{interface} = V_{DD} \cdot T \cdot (I_{U1} + I_{U2} + I_{U3} + I_{U4}) + I_{U5} \tag{5}$$

For U_1, the minimum current is limited by the minimum gain needed in the feedback loop. Due to the large range of currents on Q_{1A}, over 3 decades, its transconductance changes greatly thus affecting the loop gain and in turn the capacity to keep the sensor voltage close to the reference voltage. The minimum current for U_2 is set by the required transition frequency and the output current source and sink limits. The current in the comparators, U_3 and U_4, is bounded by the required delay. The current consumed by the SR register is almost concentrated in the transitions and it is insignificant compared to the rest of the circuits.

To minimize the EPC, we can study the impact of each design parameter separately, the effects of increasing or decreasing each one is presented on Table III. The largest

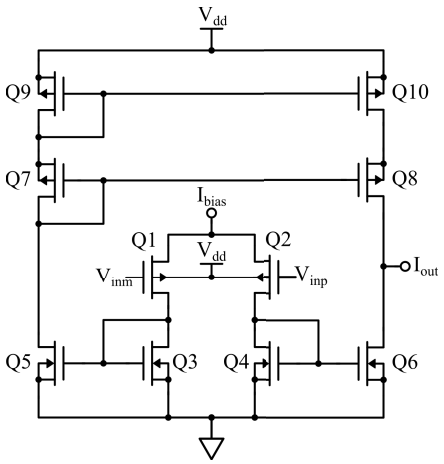

Fig. 6. OTA schematic.

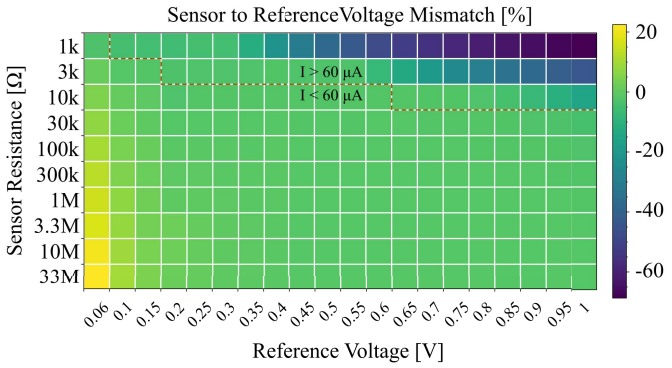

Fig. 7. Heatmap of the mismatch between the sensor voltage and the reference.

benefit comes from decreasing C, increasing γ or decreasing V_H-V_L which have a double effect on power consumption at the expense of increasing the oscillation frequency for the same R and V_{ref}. This can be done as long the oscillation frequency to counter frequency ratio is acceptable. Decreasing the supply voltage has also a double effect but there is not a large margin as the circuit is powered with 1.8 V and a minimum of 1 V + 2· V_{DSSAT}, or around 1.6 V, is needed to bias the sensor. Diminishing the current consumed by the devices decreases power consumption and has no effect on frequency emphasizing the importance of optimizing every component. Increasing V_{ref} offers the least benefit from the design point of view as the power reduction is partial and it increases the frequency but on the other hand it can serve as an optimization knob during operation. In other words, it can be used to set the maximum acceptable bias voltage for a given sensor which is the most efficient operating point.

E. Sensor Bias

The sensor is biased by the OTA of Fig. 6 driving a NMOS transistor connected in feedback a loop, Q_{1A} in Fig. 4. The goal of this stage is to cover a wide range of sensor resistance and reference voltage combinations to successfully meet the different sensors requirements. Low threshold voltage transistors were used for N and P channel devices, except for Q_{1A} to decrease leakage.

To be able to reach low voltages at the gate of the Q_{1A} for small sensor currents, the current mirrors Q_5-Q_3 and Q_4-Q_6 are made wide (W = 10 μm, L = 10 μm) and the bias current, I_{bias} is kept low (5 μA), to provide adequate transconductance in the input differential pair but to require the least overdrive voltage in the current mirrors. The differential pair transistors size is W = 10 μm, L = 1μm and they are biased in weak inversion where the highest transconductance is obtained for the same bias current, the large width also reduces the effects of mismatch and consequently offset.

The highest voltage required at the gate of Q_{1A}, for the smallest R_{sensor}, is considerably lower than V_{dd}, this allowed the usage of a PMOS cascode current mirror to reduce offset and increase the output impedance of the OTA.

The circuit is stable, reaching a phase margin of 45 degrees obtained from simulations.

The bandwidth of interest for gas sensing is very low, in the order of mHz, thus it is essential to reduce flicker noise. Firstly, by means of using large transistors in the signal path, Q_{1A} is W = 30 μm, L = 1 μm and the PMOS cascode Q_{2-3} in Fig. 4 has even much larger devices (W = 800 μm, L = 15 μm). Secondly the low bias current of the OTA helps to reduce noise even more, by decreasing the bandwidth of the feedback loop, attenuating undesired high frequency components.

The mismatch of the sensor voltage to the reference voltage was measured for the complete sensor resistance and reference voltage range and is plotted in Fig. 7 achieving good results within the design range (I < 60 μA). Two lateral regions showed significant mismatch. The first, outside the design range, is where the sensor resistance is low and the bias voltage high resulting in a large current that demands a large overdrive voltage in the PMOS current mirror $Q_{2-3-4-5}$ of Fig. 4. The second is where the sensor resistance is highest and the bias voltage lowest, in this region leakage currents play an important role and affect the sensor current significantly. Low voltages are also the most affected by offset.

F. Integrator and Comparators

To keep the voltage at the output of the current mirrors constant and decrease the output impedance for driving the comparators, the integration capacitor is connected to an operational amplifier U_2. The amplifier follows the traditional architecture: an OTA connected to a PMOS common source output stage, Fig. 8. A Miller capacitor of 1.1 pF is added between the output of the OTA and that of the common source to guarantee stability. The bias current of 10 μA is chosen to provide the necessary frequency for the smallest sensor resistance, nominally 641 kHz. As the signal at the output of the comparator is ideally triangular a large bandwidth overhead was needed to avoid smoothing of the discontinuities in the waveform, the achieved values for all corners are included in Table IV. The differential pair (W = 8 μm, L = 4 μm) size was chosen to balance mismatch while not decreasing f_t excessively. The input common mode range is small as both inputs are close to V_{cm} which is V_{DD}/2 (0.9 V). The output

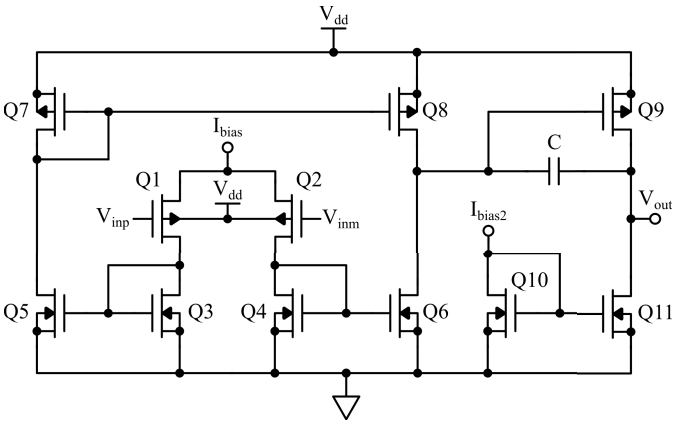

Fig. 8. Operational amplifier schematic.

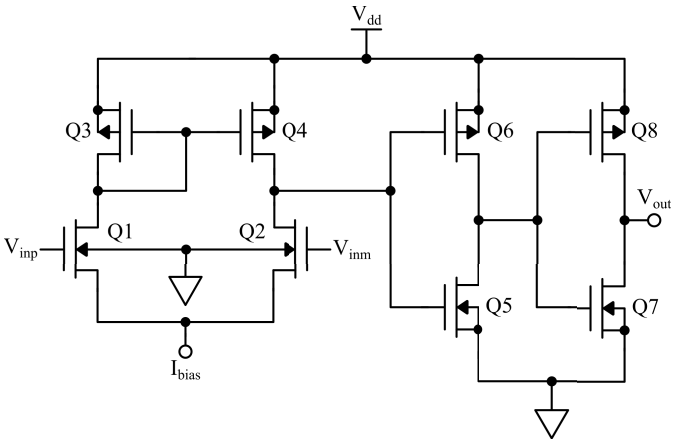

Fig. 10. Comparator schematic.

TABLE IV
OPERATIONAL AMPLIFIER TRANSITION FREQUENCY (Mhz)

Typical	Slow, Slow	Fast, Fast	Slow N, Fast P	Fast N, Slow P
2.795	2.459	3.282	2.755	2.864

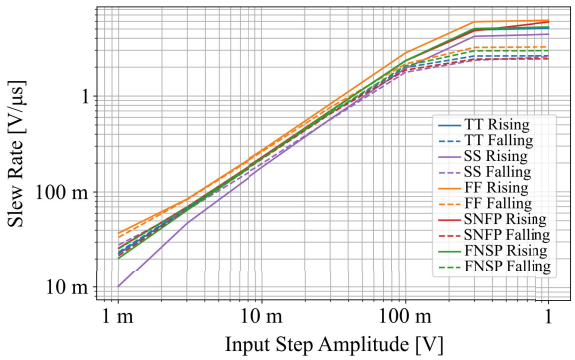

Fig. 9. Operational amplifier slew rate as a function of input differential voltage for all corners.

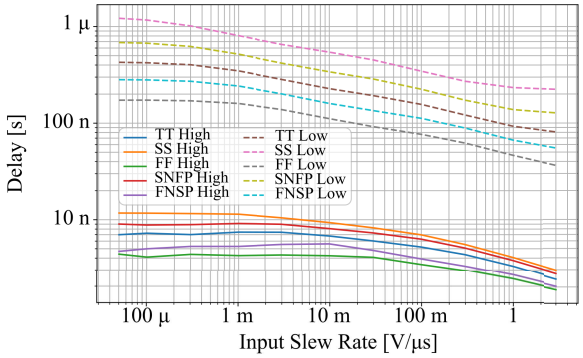

Fig. 11. Comparator delay as a function of slew rate for all corners.

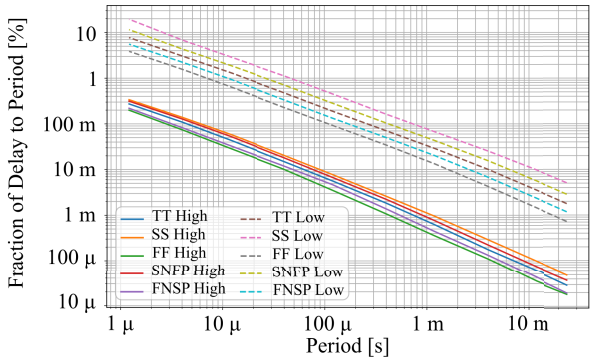

Fig. 12. Fraction of delay to oscillation period for the entire oscillation range.

range is from 0.3 V up to 1.4 V. For the largest frequency the opamp must also have sufficient slew rate to follow generate the triangular waveform. The slew rate was simulated for all corners and input steps with different amplitudes, Fig. 9. The largest required slew rate of 1.3 V/μs generates a difference between the inputs of 60 mV in the typical case and 70 mV in the worst case.

Comparators U_3 and U_4 have three stages. The first one is an active load NMOS differential pair followed by two cascaded minimum-sized inverter stages, providing minimum delay, Fig. 10. The bias current for the differential pair is 20 μA. V_H and V_L are between 0.339V and 1.16V.

Mismatch in the differential pair or the current mirror is not critical as it will appear as a constant offset, or uncertainty in the threshold voltage, but it will affect all frequencies proportionally.

Large decoupling capacitors in the supply and threshold voltages were placed to remove supply ripple which could have a harmful effect especially in the current mirrors and to reduce noise.

The delay of each comparator, U_3 corresponding to the high threshold and U_4 to the low, are depicted in Fig. 11 in relation to the input slew rate. In Fig. 12, the delay is expressed as fraction of the period. The delay of U_4 is intentionally larger than that of U_3, this is done to avoid situations in which the triangle signal reaches V_L, so U_4 output rises. Consequently, the register begins the transition to the other state, and the switches $Q_{16-17-18-19}$ toggle, changing the direction of current in the capacitor. Next, the comparator

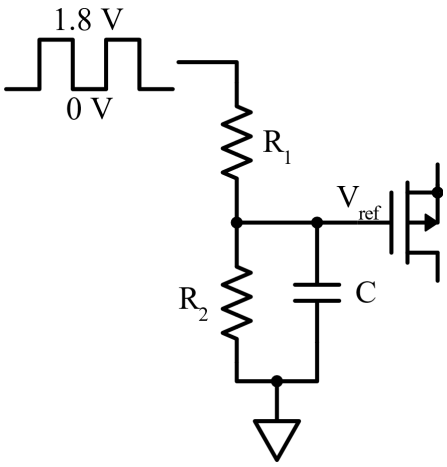

Fig. 13. Reference voltage generator.

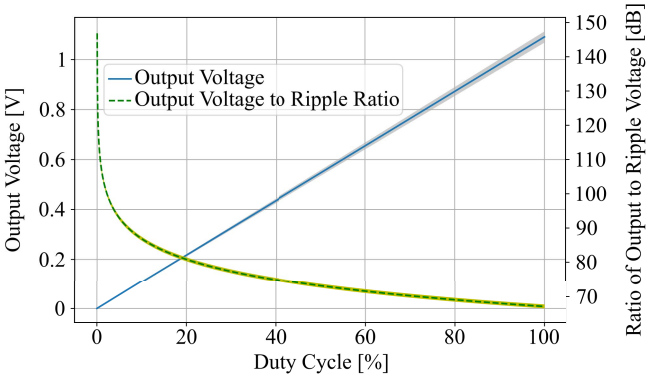

Fig. 14. Reference Voltage and its ratio to ripple voltage as a function of duty cycle.

would reverse to the low state and the inputs of the register are changed but the register has not completed the transition to the other state yet. This could result in additional jitter or malfunctioning.

G. Reference Voltage Generation

Three voltage references are needed for the read-out circuit, one variable for the reference input, which is used to set the sensors biasing point, and two fixed for the comparators of 0.339 V and 1.16 V.

For the reference voltage we decided to use a simple digital-to-analog converter based on on a pulse width modulation (PWM). It provides a sufficiently small step and due to the fact that the voltage is applied to a MOS gate that behaves like a dc open circuit, the generated voltage is not affected by the load, Fig. 13. A resistor divider output is connected to a capacitor and to the reference input, which is the gate of a PMOS transistor. The generated voltage by the divider is unaffected by temperature variations as both resistors change proportionally. The input of the resistor divider is connected to a microcontroller. Most modern microcontrollers, even those for lower power applications, include an output compare or PWM peripheral. This peripheral can create a periodic signal whose duty-cycle can be configured by a setting a value in a register. A crystal is generally used as a clock source for the microcontroller, so the generated digital signal has very consistent frequency.

In our example of Fig. 14, we chose a 10 kHz frequency, thus if the microcontroller runs at least at 1 MHz 100 voltage steps can be defined (the peripheral frequency is usually limited to the maximum frequency of the core). The resistors are $R_1 = 6.5$ MΩ and $R_2 = 10$ MΩ resulting in a maximum current consumption of 100 nA. A capacitor of 22 nF, was chosen to keep the ripple amplitude well below that of the generated dc reference. A 5 % tolerance is standard for discrete resistors as well as 1 %, which was our approach, in the case of integrating the resistors, with the help of common centroid layout techniques a low deviation from the desired resistance ratio can be achieved. In the chart, the uncertainty caused by a 5% tolerance of the resistors is represented by the grey shaded area. The time constant of the circuit is given by its RC value, here 87 ms.

For the fixed references we used high poly resistors, to achieve a very high resistance, thus a very low current. A decoupling capacitor is added again to mitigate supply instability and to reduce resistor noise.

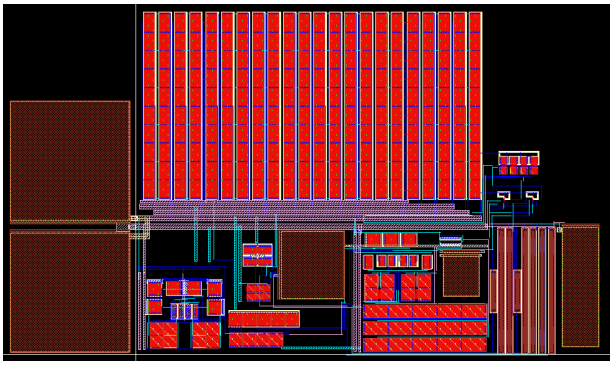

Fig. 15. Layout of the designed read-out circuit.

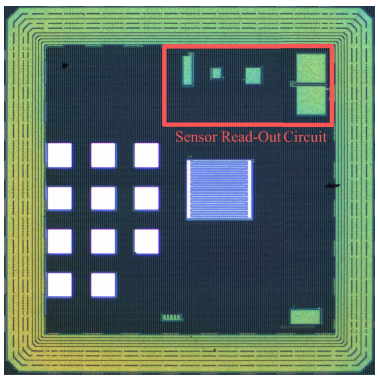

Fig. 16. Photograph of the fabricated integrated circuit.

H. Implementation

The designed layout is shown in Fig. 15. Its width is 497 μm and the height 288 μm (0.143 mm^2). The brown areas correspond to capacitors, the two on the rightmost are for supply decoupling. The cascode PMOS current mirror,

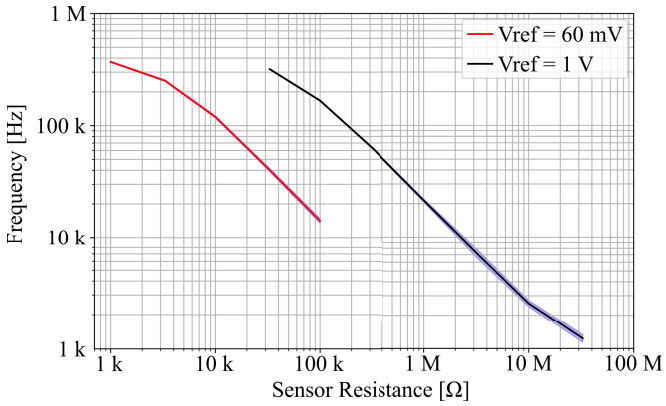

Fig. 17. Output frequency for two bias voltages and a range of sensor resistances. The standard deviation is represented by the blue area.

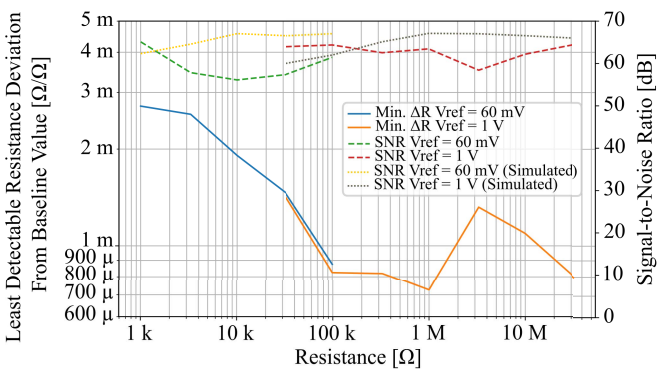

Fig. 18. Signal-to-noise ratio and minimum detectable fractional resistance variation for two bias voltages.

$Q_{2-3-4-5}$ in Fig. 3, requires the most area, covering all the bottom red region. Fig. 16 presents a photograph of the fabricated chip. The devices are not visible because dummy devices have been added to comply with metal densities requirements, the capacitors are still visible. The size of the chip is 1520 μm by 1520 μm. Process, voltage and temperature simulations were carried out prior to fabrication, unfortunately Monte Carlo models were not available for low threshold voltage transistors in this technology, mismatch was evaluated through calculations and good layout practices.

IV. Measurements and Discussion

A. Transfer Characteristics

To make an estimation of the gas concentration, the transfer function of the sensor and that of the read-out circuit must be known. The oscillation period values must then be computationally compensated for obtaining the real measure. The transfer function of the sensors is always non-linear, although at different degrees according to the sensing material and doping. Many models of sensors response and their transfer function are already available in the literature [6], [20].

The read-out transfer function is plotted in Fig. 17 for a set of 9 chips, it was measured in the time domain using a Tektronix MSO56 oscilloscope with a 125 M samples buffer and post-processed with scripts written on Python 3.7. It has a linear range in the middle but at the extremes, several non-linear phenomena become noticeable. At lower frequencies we identify some non-linearity coming from the PMOS and NMOS cascode current mirror connected to the switches. As the drain-source voltage of Q_{13} and Q_{15} becomes smaller, the current mirrors become less effective in copying the current. Furthermore, at low sensor current, below 50 nA, the pads leakage current becomes noticeable, measured values of up to 300 pA were observed. The nonlinearity at high frequencies is partly attributed to the integrator and partly to the comparators, the later having the largest impact, although this has not been backed by simulations as shown in their respective section.

To assess the noise characteristics of the proposed design we plot in Fig. 18 the average signal-to-noise ratio and the minimum fraction of resistance variation that can be measured. The SNR is at least 57 dB for the complete R_{sensor} range for a single measurement, which is higher than the noise processes observed in graphene and polymer sensors [23]. The measured values are close to simulation, for example a simulated SNR of 62 dB is obtained for R = 100 kΩ and V_{ref} = 1V. Because the noise processes present in the read-out circuit are a combination of white and flicker noises, averaging is effective at increasing the SNR. For example, with 10 samples average, the minimum SNR increases to 65 dB and with 100 to 72 dB if such need arises while still handling up to 10 sensors with an individual sampling rate of 1 Hz.

In the field of gas sensors, it is standard to quantify the sensitivity by dividing the resistance of the sensor when exposed to a given gas concentration by the resistance of the sensor when exposed to air. For this reason, we think that a good metric of the uncertainty of a read-out circuit is the minimum discernable change from a baseline resistance calculated for the complete resistance range. The signal-to-noise and distortion ratio is ubiquitous in the ADC literature and could also be applied here. Still distortion in the transfer function is not itself a problem as long as it is predictable and that it does not diminish the gain α from (2) significantly, that in turn would lead to an increase in the minimum detectable resistance deviation.

We have measured PPy sensors for ammonia and found a Rg/Ra value of 1.048 for low concentrations (1.85 ppm NH_3) and a noise of 739 Ω_{RMS}, yielding a limit of detection of 142 ppb with a requirement of detecting variations of 0.37% from the baseline resistance, which is withing the read-out range.

To keep quantization noise below the SNR of the read-out circuit, the timestep of the counter in the microcontroller must be small enough to provide 9.6 bits (corresponding to a SNR_{min} of 57 dB) of resolution at the highest output frequency of the interface, which translate to a timestep of 3.33 ns or a frequency of 301 MHz. This value is close to what is found in commercially available, high-end microcontrollers. In the case of integrating the counter in the chip, reaching that frequency in a 180 nm process does not present a challenge. Previously, a 575 MHz counter has been reported for a 250 nm CMOS process [37]. From simulations, we have seen that adding

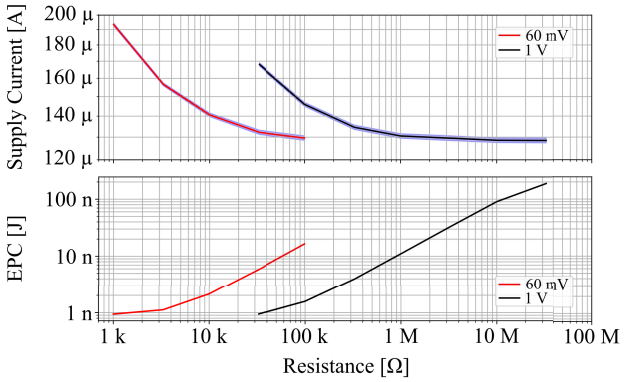

Fig. 19. Supply current and EPC for two bias voltages. Average of 9 chips, the standard deviation is represented by the blue area.

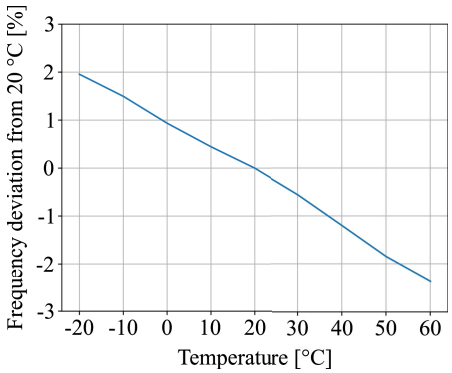

Fig. 20. Dependence of the oscillation frequency with temperature for $R_{sensor} = 330\ k\Omega$, $V_{ref} = 1V$.

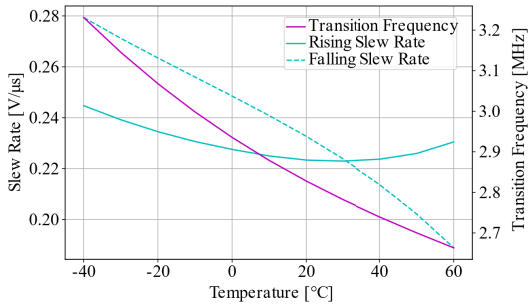

Fig. 21. Simulated opamp slew rate and f_T versus temperature.

a 10-bit counter to the chip would increase EPC by less than 2% in the worst case.

The baseline resistance range spans 60 dB for the 60 mV range and 60 dB for the 1V range (90.4 dB if ranges are combined). From (6), the dynamic range is 117 dB for each subrange, and 148 dB if the whole range is considered. Thus, the microcontroller counter registers must be at least 25 bits wide.

$$DynamicRange = 20 \cdot log_{10}\left(\frac{R_{max}}{R_{min}}\right) + SNR_{min} \quad (6)$$

B. Power Consumption

The supply current was measured for 9 chips, for a set of resistors and two reference voltages: 60 mV and 1 V, Fig. 19. Towards the left, the resistance is lower and the current flowing through it is larger, as its value increases the static current of active components dominates. The EPC follows the expected behavior. The energy dissipated in the sensor is independent of the period, so the longer the period (larger R) more energy is dissipated by the active components and greater is the total EPC. The changes in the trend at both extremes can be explained by the nonlinearity observed in the transfer function.

From Fig. 19 and 4 the EPC for the smallest resistance (1 kΩ) and smallest bias voltage (50 mV) is 1.21 nJ and for the largest resistance (33 MΩ) and largest bias voltage (1 V) is 188 nJ.

In Table II, our design is compared to relevant publication that employed relaxation oscillator or ADC + IDAC. Unfortunately, due to the inherent differences between the two types of approaches it is very difficult to make a fair fully-quantitative comparison, but at least a qualitative analysis is possible. To compare with other relaxation oscillators, it has to be kept in mind that this type of circuit has an EPC according to (3), that is highly dependent on R, so the same R has to be used for comparison. For R = 1 kΩ, the EPC for [27] is 758 pJ while for [30] this value has not been reported. Even though both circuits have a similar α, our value of 1.21 nJ appears higher because [27] is designed to run up to 10 MHz. So, close to 1 MHz their design is only lightly affected by nonlinearity, while in ours it is at the worst point. Reduced linearity imposes small penalties at the extremes in terms of EPC, but the large reduction in supply current translates into a significantly lower EPC for most of the resistance range. For example, at the other extreme, if we consider 4.7 MΩ, which is the highest resistance for [30], the value of our circuit is 45 nJ, for [30] it is 296 nJ, and for [27], even though outside its range, it would be 3.17 μJ if parameters were kept the same. The reason for the difference is that [27] and [30] have a larger static current consumption in the active components, also both circuits have not been designed to use V_{ref} for tuning operation, thus they don't benefit from the reduced EPC achieved by increasing V_{ref}.

With respect to ADC + IDAC architectures, the EPC has a different behavior. In these circuits, the conversion time is fixed or changes moderately. In opposition to relaxation oscillator, the EPC diminishes for larger resistances. Still, this does not have a large impact in [33] because the power consumption is dominated by the read-out circuit. A low EPC is achieved in [35] but the sensor is biased only during the sampling time, not taking into account the stabilization of the sensor. Furthermore, the main limitation of this type of circuits when applied to gas sensing, is that the IDAC is essential to keep the required bits in the ADC at reasonable level, so there is little room to choose the sensor bias voltage.

C. Temperature Response

A climate chamber (Espec SH-241) with controlled temperature and fixed humidity was used to test the variations of the output frequencies for the expected temperature range in typical applications: from -20 °C up to 60 °C, a small deviation

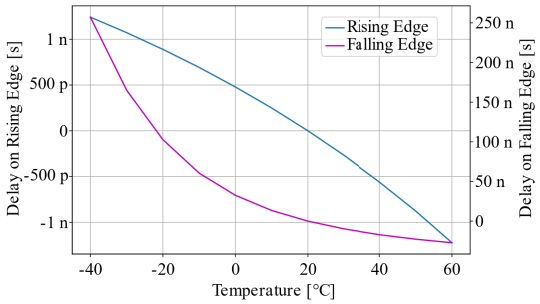

Fig. 22. Simulated comparator delay versus temperature.

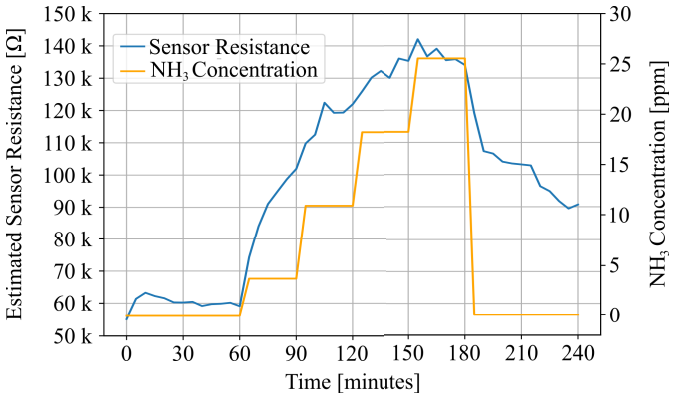

Fig. 23. Estimated resistance, from the output frequency for a sequence of ammonia levels applied to a PANI sensor.

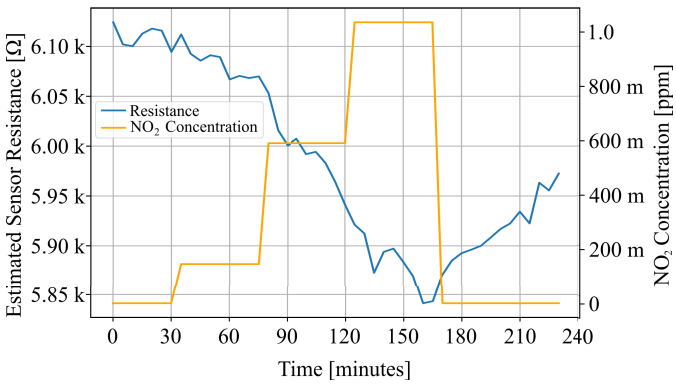

Fig. 24. Output frequency for a sequence of NO2 concentration for a pristine graphene sensor.

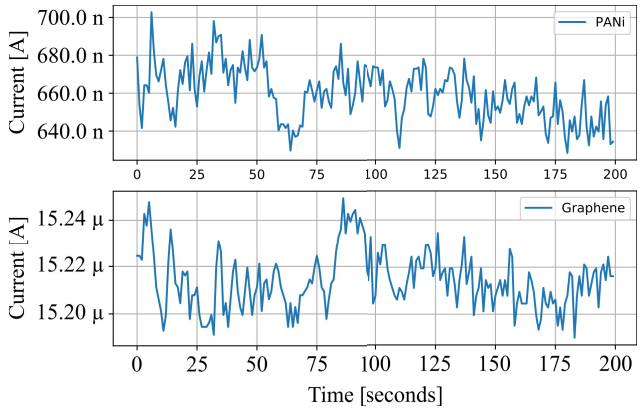

Fig. 25. Current in PANI and graphene sensors under constant bias, the inherent noise is remarkable in both devices. V_{bias} = 100 mV.

of 2 % was seen from the room temperature value for the extremes, Fig. 20. The effect of temperature on the opamp and comparators are plot in Fig. 21 and 22 respectively. The cause of the variation could be attributed to the degradation of slew rate in the operational amplifier with temperature. The change in the transition frequency or the small delay added to the comparators have a lesser impact.

D. Gas Measurements

The read-out circuit was tested in a real case scenario using two types of sensors. The first sensor was built by drop casting of PANI over a set of 1 mm long by 1 mm wide gold IDE's (W = 4 μm, S = 4 μm, N = 125, Z = 1 μm in Fig. 2). This sensor has a baseline resistance of 60 kΩ and was biased with 100 mV. The sensor connected to read-out circuit powered by batteries was placed in a 2.9-liter plastic chamber where a sequence of NH_3 diluted in clean air at different concentrations (nominally 5, 15, 25 and 35 ppm) was applied at a constant flow rate of 2 liters per minute. Humidity and temperature were kept constant. As the thermal mass flow meter (Brooks GF-80 Series) readings are referenced to N_2, a correction factor of 0.73 had to be applied to obtain the real concentration inside the chamber. The results are plotted in Fig. 23. A higher sensitivity is observed for the first step of NH_3, almost saturating for values above 18 ppm.

For the second experiment a pristine graphene sensor was used. It was also built by drop casting using identical electrodes to the first case. The baseline resistance was 6.1 kΩ biased with 60 mV. The sensor was tested with a sequence of NO_2 concentrations (0.2, 0.8 and 1.4 ppm) again diluted in clean air, the response is plotted in Fig. 24. In this case a correction factor of 0.74 for the gas flow measurements was used. The graphene sensor, unlike the PANI, has a negative coefficient, so its resistance decreases for increasing concentration.

The read-out circuit successfully provided estimations of the sensor resistance and values in the ppb range can be measured for both NH_3 and NO_2. In both plots a significant amount of noise is observed, this is not caused by the read-out but by the sensors themselves as seen in Fig. 25 where the current waveform in the sensors for a constant bias is plotted. This highlights the importance of the knowledge of each sensor behavior from a signal point of view to improve concentrations estimates. The cause for these sudden fluctuations seems to be related to sensor interacting with the environment, still noise in conductive polymers is currently a topic of active research.

V. Conclusion

After analyzing the requirements of current state of the art chemiresistive gas sensors and the results obtained with the proposed read-out circuit, we can conclude that it is suitable for interfacing novel sensors designed for ultra-low power applications and most importantly it offers the flexibility to be integrated in a sensor matrix for the detection of several gases in a single SoC with high sensitivity and selectivity.

Remarkably, it can interface sensor with a wide resistance range, from 1 kΩ up to 33 MΩ, and generate bias voltage from 50 mV up to 1 V that allows for the operation of sensors at the optimal point, be it: lowest power or least uncertainty, as required by each application. An extensive analysis of transfer characteristics and power consumption was carried out, reaching a large SNR of at least 57 dB and a minimum EPC of 1.21 nJ. Compared to other published papers, our design achieves very low EPC for the lowest sensor resistance, being the ADC-based implementations more efficient for the highest resistances [34], [35]. This is because, in the second case, the conversion time in relaxation oscillator is much longer. In terms of area, our circuit is one of the smallest even considering the oversized decoupling capacitors. It can also generate the highest bias voltage for the sensor (i.e., 1 V) and handle the largest sensor resistance (i.e., 33 MΩ). With this design as a basis, the effects of constant pole input filters could be studied to provide a consistent frequency response for all sensors, helping to reduce sensors noise and potentially increasing SNR.

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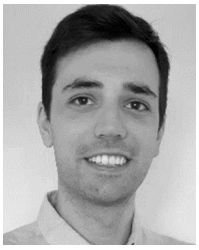

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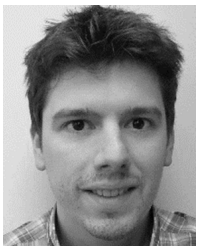

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