Improving Dielectric Constant and Residual Stress in Metal-Insulator-Metal Capacitors Using Different Stacked Thick Dielectric Materials

Najeh Zeidi[1,2], **Nicolas André**[1], **Fares Tounsi**[1,2], **Denis Flandre**[1]
[1]SMALL Research Group, ICTEAM Institute, Université catholique de Louvain, Belgium
[2]SI2E Laboratory, École nationale d'ingénieurs de Sfax, Université de Sfax, Tunisia
***E-mails: [first name].[surname]@uclouvain.be**

2023 International Semiconductor Conference (CAS) | 979-8-3503-2395-5/23/$31.00 ©2023 IEEE | DOI: 10.1109/CAS59036.2023.10303695

***Abstract*—This study aims to analyze and compare the characteristics of Metal-Insulator-Metal (MIM) capacitors, focusing on the effect of the stacking selection of thick dielectric materials, for future applications requiring robustness to high voltages and temperatures. The 300 nm-thick dielectric stacks under investigation include SiO_2 and Si_3N_4 materials deposited using plasma-enhanced chemical vapor deposition (PECVD) at a high temperature (300°C), as well as Al_2O_3 deposited through reactive sputtering at room temperature. The experimental results presented in this work highlight the importance of the stacking choice of these dielectric materials for minimizing the residual stress and the temperature coefficient of capacitance (TCC) and enhancing the overall dielectric constant. These factors contribute to achieving increased capacitance density, with mechanical and electrical resistance to harsh conditions.**

***Keywords*—MIM capacitor; dielectric stacks; dielectric constant; residual stress.**

1. Introduction

The miniaturization of passive components has been a crucial aspect in the development of more compact and efficient electronic devices. Passive components, including capacitors, inductors, and resistors, make up a significant portion (up to 80% of the chip area) of electronic components and analog circuits [1]. Among passive components, capacitors require further development to meet harsh voltage and temperature conditions. The performance of Metal-Insulator-Metal (MIM) capacitors depends on multiple factors, such as design, materials, frequency, and temperature. However, the quality of the dielectric layer remains the most crucial factor, as it significantly affects the capacitance density, residual stress, and breakdown voltage. Plasma-enhanced chemical vapor deposition (PECVD) is widely used for the deposition of silicon dioxide (SiO_2) and silicon nitride (Si_3N_4) dielectrics. These two materials exhibit a high dielectric strength, with 10 MV/cm for SiO_2 and 7 MV/cm [2] for Si_3N_4 at room temperature (RT), with lofty melting points of 1700°C and 1900°C [3], respectively. Furthermore, both materials exhibit low temperature coefficients of capacitance (TCC) of less than 50 ppm/°C. Despite these advantageous properties, the capacitance density of MIM capacitors using SiO_2 and Si_3N_4 is limited due to their low dielectric constants of 3.9 and 7.1, respectively, at RT. To overcome this limitation and reduce leakage current, the incorporation of high-k dielectric materials has been proposed [4], such as Al_2O_3 (k=8.5), TiO_2 (k=95), HfO_2 (k=22), or Ta_2O_5 (k=26). Besides, it is necessary to reduce the total residual stress in the dielectric film, including intrinsic and thermal stresses, to mitigate the wafer curvature, which may degrade the adhesion quality of the stacked insulating layers and lead to the creation of defects and internal cracks [5]. Previous studies [6] have demonstrated that the residual stress in thick films (100 nm to 2 µm) can be effectively controlled by adjusting process parameters such as temperature, pressure, power density, RF frequency, and gas chemistry. Additionally, rapid thermal annealing (RTA) can be employed to reorganize the atomic configuration [5]. Nevertheless, the modification of the deposition recipe directly impacts the refractive index, deposition rate, and etch rate of the film [5], thus causing deviations from the desired stoichiometric structure. The utilization of dielectric material stacks is another strategy adopted to improve the performance of MIM structures. In [7], a 20 nm-thick Al_2O_3 layer, associated with a TiN layer of the same thickness stack, is employed to enhance the dielectric insulation and improve the capacitance density. Similarly, authors in [8] explore the utilization of Al_2O_3 and HfO_2 layers with thicknesses ranging from 15 nm to 30 nm to minimize the leakage current and increase the breakdown voltage and capacitance density. The authors in [9] focus on the implementation of a 12 nm-thick HfO_2 layer as well as a 6 nm-thick SiO_2 layer. This particular combination was chosen to improve the voltage linearity and the thermal coefficient. The present study focuses on the investigation of multilayer dielectrics composed of combinations of low-k (SiO_2 and Si_3N_4) and high-k (Al_2O_3) dielectric layers to form stacks with a total thickness of 300 nm in order to optimize the residual stress, the capacitance density, and the TCC in MIM structures.

2. Microfabrication description

The structure of an MIM capacitor is formed by a dielectric layer sandwiched between two conductive metals. In this study, the MIM capacitor's characteristics are investigated for different dielectric types. Initially, three different generic dielectrics were deposited individually, i.e., ~300 nm of Al_2O_3 by reactive sputtering (wafer-1), ~300 nm of SiO_2 by PECVD (wafer-2), ~300 nm of Si_3N_4 by PECVD (wafer-3), see Table 1. In addition, we achieved different stacking configurations having the same total thickness of ~300 nm by piling up different arrangements of these three dielectrics, each having ~100 nm thickness, resulting in the formation of six different stacking combinations (denoted wafer-4 to wafer-9 in Table 2). The MIM capacitor microfabrication uses <100> 380 µm-thick 3' p-type bulk silicon (Si) wafers as the starting substrate. The deposition of the PECVD SiO_2 and Si_3N_4 takes place in an Oxford Plasmalab System 100 at 300°C, 1 Torr pressure, 30 W RF power, and a frequency of 13.56 MHz. For SiO_2 deposition, the N_2O/SiH_4 gas ratio is set to 7, while for Si_3N_4 deposition, the SiH_4/NH_3 gas ratio is set to 28.5. For the deposition of Al_2O_3, the sputtering chamber is pumped to a low vacuum of 1.2 mTorr before introducing the reactant gas (3 sccm of oxygen) into the system. Argon is used as the sputtering gas (22 sccm) to ablate the target (Aluminium) at RT. To etch and pattern the MIM structure, buffered hydrofluoric acid (BHF) is employed at RT, and finally, the Sentech spectroscopic ellipsometer is used to measure the thickness and the refractive index of each layer individually (Table 1).

To assess the residual stress, the wafer curvature was evaluated before and after each film deposition using the Veeco Dektak 150 profilometer. The latter scanned a distance of 5 cm along the diameter perpendicular to the primary flat for a duration of 60 seconds to generate 18000 points. Then, the average residual stress (σ_f) in the film of interest arising from the deposition process depends on the curvature as expressed in Stoney's formula [5]:

$$\sigma_f = \frac{1}{6}\left[\frac{1}{R_{post}} - \frac{1}{R_{pre}}\right]\frac{E_s\, {d_s}^2}{(1-\nu_s)d_f}, with\ R = \frac{(L/2)^2}{2\, h_{max}} \quad (1)$$

where E_s is the substrate Young's modulus (130 MPa for Si), d_s is the substrate thickness (~380 µm), d_f is the film of interest thickness, ν_s is the substrate Poisson's coefficient (0.28 for Si), R_{post} is the radius of the wafer after deposition, and R_{pre} is the radius of the wafer before deposition. The radius R (R_{post} or R_{pre}) is approximated based on the maximal height, where, as in Fig. 1, R is the radius, L is the length of the measurement, and h_{max} is the maximal deflection of the wafer.

The 428A4 LCR meter along with the PM8PS low signal probe station, equipped with a thermal chuck (up to 300°C) for capacitance-voltage (C–V) measurement, are used to evaluate the variations in capacitance as a function of frequency (100 kHz to 1 MHz) and temperature (25°C to 50°C). The objective of this analysis is to identify the dielectric stack configuration that provides the highest capacitance density and the lowest TCC.

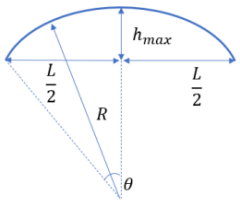

Fig. 1. Illustration of the wafer radius R.

Table 2. Different stacking combinations deposited using the three generic dielectrics.

Wafer reference	Dielectrics stacking (from Bottom to top)
Wafer-4	SiO_2-Si_3N_4-Al_2O_3
Wafer-5	SiO_2-Al_2O_3-Si_3N_4
Wafer-6	Si_3N_4-SiO_2-Al_2O_3
Wafer-7	Si_3N_4-Al_2O_3-SiO_2
Wafer-8	Al_2O_3-SiO_2-Si_3N_4
Wafer-9	Al_2O_3-Si_3N_4-SiO_2

3. Results and discussion

A. Residual stress extraction

The initial curvature of all the wafers was determined, then the deflection after each layer deposition was also measured, and the contribution of residual stress added by each layer was calculated for the six combinations (Table 3). The presence of residual stress in thin films arises from a combination of thermal stress and intrinsic stress developed during film growth and relaxation after cooling [6]. At first sight, when the deposition is performed at RT (i.e., Al_2O_3 sputtering), thermal expansion induced between layers is minimal, resulting in a purely dominant intrinsic residual stress that is significantly lower (+65 MPa) than the residual stress in PECVD SiO_2 or Si_3N_4 (Table 3). On the other hand, Si exhibits a coefficient of thermal expansion of ~2.6 10^{-6}/°C, while SiO_2 has a lower coefficient of ~0.5 10^{-6}/°C, resulting in a

Table 1. Individually deposited dielectrics with measured characteristics.

Wafer reference	Dielectric layer	Refractive index	Deposition rate	BHF etch rate
Wafer-1	Al_2O_3	1.67 /1.50 to 1.67 [18]	11.7 nm/min	136 nm/min
Wafer-2	SiO2	1.45/1.46 [19]	43 nm/min	400 nm/min
Wafer-3	Si_3N_4	2.01/2.08 [20]	24 nm/min	118 nm/min

compressive stress of -214 MPa (Table 3). In contrast, Si_3N_4 has a coefficient of thermal expansion higher than Si of ~3 10^{-6}/°C, resulting in a higher tensile stress of ~517 MPa (Table 3). It is important to note that the specific deposition method and parameters employed can cause variations in the type of stress, whether tensile or compressive. Using the same deposition technique (i.e., PECVD), it can be observed from Table 1 that the BHF etch rate, deposition rate, and refractive index correlate with the density and the residual stress of the film. A higher deposition rate leads to a lower film density, which results in an increased etch rate and reduced residual stress. This relationship is particularly evident when comparing the PECVD SiO_2 and the Si_3N_4 properties, where the hypothesis is true and well validated.

As depicted in Table 3, the 100 nm deposit of SiO_2 exhibits a compressive stress of approximately -60 MPa compared to -214 MPa for 300 nm. On the other hand, a deposition of 100 nm Al_2O_3 yields a tensile stress of around 55 MPa versus 65 MPa for 300 nm, while the deposition of 100 nm Si_3N_4 results in a tensile stress of around 880 MPa versus 517 MPa for 300 nm. These observations highlight the variable stress characteristics associated with each layer and indicate that the presence of residual stress in a film is influenced by various factors, including its thickness. In fact, as the thickness of a film increases, the stress may also increase or decrease, depending on the specific deposition process and material properties. The observed variations in residual stress during the deposition process can be attributed to [6]: *(i)* the difference in atomic distance between the Si substrate and the three dielectric materials, which is for Si, SiO_2, Si_3N_4, and Al_2O_3 equal, respectively, 2.3 Å, 1.62 Å, 1.56 Å, and 1.8 Å; *(ii)* the coefficient of thermal expansion between the Si substrate and the three dielectrics (i.e., 2.6 10^{-6} /°C for the Si substrate, 0.5 10^{-6} /°C for the SiO_2, 3 10^{-6} /°C for the Si_3N_4, and 8.5 10^{-6} /°C for the Al_2O_3); *(iii)* the arrangement and the deposition parameters, especially the temperature. The Al_2O_3-SiO_2-Si_3N_4 (wafer-8) stacking exhibits the lowest overall stress value (124 MPa) compared to the others, which can be attributed to the differences in atomic distance between the three tested dielectrics. Specifically, the atomic distance of SiO_2 is less than that of Al_2O_3. Therefore, when SiO_2 is deposited on Al_2O_3, the insertion of SiO_2 atoms between Al_2O_3 atoms creates a compressive constraint, resulting in a compressive stress. Similarly, when Si_3N_4 is deposited on SiO_2, the insertion of Si_3N_4 atoms between the SiO_2 atoms leads to a compression constraint, thus decreasing the stress associated with the Si_3N_4 layer. Consequently, the overall stress in the stack is reduced to a very low level.

B. Dielectric constant extraction

The dielectric constants of SiO_2, Si_3N_4, and Al_2O_3 were determined by measurements at a frequency of 100 kHz using the 428A4 LCR meter and the MP8MS probe station at RT. For measurement accuracy, three square MIM structures with sides of 500 µm, 1000 µm, and 2000 µm were used. The results confirm that the dielectric constants of the individual 300 nm-thick deposited layers of SiO_2, Si_3N_4, and Al_2O_3 are around 4, 6.2, and 7.1, respectively. Theoretically, the total dielectric constant ε_{tot} in the stack can be determined by considering the thicknesses t and the dielectric constants of each layer, as:

$$\frac{t_{tot}}{\varepsilon_{tot}} = \frac{t_1}{\varepsilon_1} + \frac{t_2}{\varepsilon_2} + \frac{t_3}{\varepsilon_3} \quad (2)$$

This results in an effective dielectric constant of 5.6 for all the stacks formed by the three 100 nm-thick layers, whatever their arrangement. However, the measurement results revealed a noticeable difference in dielectric constants between them, as shown in Table 3. The highest observed discrepancy from the theoretical value is 8.92% for wafer-7 (Si_3N_4-Al_2O_3-SiO_2). In order to determine the stack that exhibits the best frequency and temperature stability and to extract the TCC $\{\Delta C/(C.\Delta T)\}$ and FCC $\{\Delta C/(C.\Delta f)\}$ (frequency coefficient of capacitance), the capacitance of each of the stacks was measured in the temperature range of 25°C to 50°C and the frequency range of 100 kHz to 1 MHz.

Figs. 2 and 3 show the measured results, which validate the theory that capacitance increases gradually with temperature and frequency. The increase in capacitance with frequency (Fig. 2) can be attributed to interfacial polarization. The increase in capacitance with temperature (Fig. 3) is attributed to the space charge polarization induced by the increasing number of free carriers as a result of increasing temperature [10].

Table 3. Measured properties of all the individual/stacked dielectrics materials.

Wafer	Stress after each deposition (MPa)	Average stress (MPa)	Dielectric constant	Capacitance density (fF/µm2)	TCC (ppm/°C)	FCC (ppm/Hz)
Wafer-1	65	65	7.1	0.207	400	0.034
Wafer-2	-214	-214	4	0.119	170	0.035
Wafer-3	517	517	6.2	0.181	140	0.035
Wafer-4	-56/460/100	170	5.7	0.167	608	0.055
Wafer-5	-70/100/330	166	5.7	0.168	374	0.042
Wafer-6	887/-390/183	223	6	0.177	191	0.052
Wafer-7	877/60/-350	195	6.1	0.181	373	0.047
Wafer-8	52/-66/388	124	5.7	0.169	175	0.047
Wafer-9	60/816/-396	160	5.9	0.175	323	0.045

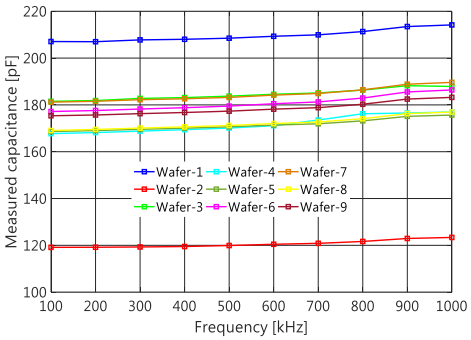

Fig. 2. Variations of the capacitance with frequency.

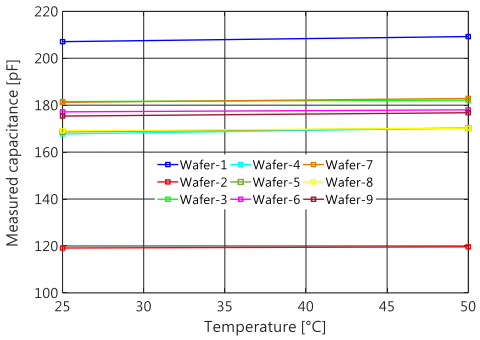

Fig. 3. Variations of the capacitance with temperature.

Based on the findings in Table 3, it can be observed that Al_2O_3 exhibits the highest dielectric constant, a superior capacitance density, and the lowest FCC and residual stress. However, for high-voltage applications, Al_2O_3 is not recommended due to its low breakdown voltage, which is generally inversely proportional to the dielectric constant. Additionally, its TCC is high rated at 400 ppm/°C, making it unsuitable for high-temperature applications. On the other hand, SiO_2 exhibits the lowest dielectric constant, which limits its usage in high-voltage integrated applications that require a large surface area on a silicon chip. Si_3N_4 has an extremely high residual stress attributed to its density, which makes it impractical for high-voltage applications requiring thick dielectric materials (a few µm). In contrast, the measurements carried out confirm that the incorporation of a stack of the three dielectrics (SiO_2, Si_3N_4, and Al_2O_3), with a meticulous adjustment of the thickness parameter and the deposition sequence, makes it possible to reach a compromise with a dielectric constant that can exceed the theoretical value of 5.6. Moreover, it is noteworthy that the Al_2O_3-SiO_2-Si_3N_4 stack (i.e., wafer-8) minimizes the residual stress at 124 MPa, below SiO_2, Si_3N_4, and other stacking arrangements. It further exhibits the lowest TCC value of 175 and an acceptable FCC compared to SiO_2, Al_2O_3, and other stacking configurations.

4. Conclusions

The objective of this research is to address the limitations associated with individual dielectric layers of SiO_2 or Si_3N_4 deposited by PECVD and Al_2O_3 deposited by sputtering by combining them into a stacked arrangement with the aim of optimizing the overall equivalent dielectric characteristics. The study carried out made it possible to investigate the dielectric constant, the residual stress, and the capacitance temperature coefficient (TCC) in MIM structures, with particular emphasis on the influence of the stacking arrangements. By comparing the different characteristics collected, it can be seen that the configuration (Al_2O_3-SiO_2-Si_3N_4) exhibits the lowest residual stress value and the lowest TCC coefficient. Additionally, this particular arrangement demonstrates a stable dielectric constant that closely aligns with the theoretical value.

References

[1] H. Johari and F. Ayazi, "High-density embedded deep trench capacitors in silicon with enhanced breakdown voltage," IEEE Trans. Compon. Packag. Manuf. Technol, vol. 32, no. 4, pp. 808-815, 2009.

[2] A. Farcy, J. Carpentier, M. Thomas, J. Torres and P. Ancey, "Integration of high-performance RF passive modules (MIM capacitors and inductors) in advanced BEOL," Microelectron. Eng., vol. 85, no. 10, pp. 1940-1946, 2008.

[3] M. L. Green, T. W. Sorsch, G. L. Timp, D. A. Muller, B. Weir, P. Silverman, S. Moccio and Y. Kim, "Understanding the limits of ultrathin SiO_2 and Si-O-N gate dielectrics for sub-50 nm CMOS," Microelectron. Eng., vol. 48, no. 1, pp. 25-30, 1999.

[4] D. Kannadassan, R. Karthik, M. S. Baghini and P. Mallick, "Modeling the voltage nonlinearity of high-k MIM capacitors," Solid State Electron, vol. 91, pp. 112-117, 2014.

[5] N. Sharma, M. Hooda and S. Sharma, "Stresses in thin films: an experimental study," Indian J. Phys, vol. 93, no. 2, pp. 159-167, 2019.

[6] J. Klootwijk, K. Jinesh, W. Dekkers, J. Verhoeven, H. Kim, D. Blin, M. Verheijen, R. G. R. Weemaes, M. Kaiser, J. J. M. Ruigrok and F. Roozeboom, "Ultrahigh Capacitance Density for Multiple ALD-Grown MIM Capacitor Stacks in 3-D Silicon," IEEE Electron Device Lett, vol. 29, no. 7, pp. 740-742, 2008.

[7] S. Prasanna, S. Mohan Rao, S. Jayakumar, M. Kannan and V. Ganesan, "Dielectric properties of DC reactive magnetron sputtered Al_2O_3 thin films," Thin Solid Films, vol. 520, no. 7, pp. 2689-2694, 2012.

[8] S. Kim, B. Cho, M. Li, S. Ding, C. Zhu, M. Yu, B. Narayanan, A. Chin and D. Kwong, "Improvement of voltage linearity in high-κ MIM capacitors using HfO_2-SiO_2 stacked dielectric," IEEE Electron Device Lett, vol. 25, no. 8, pp. 538-540, 2004.

[9] B. Olbrechts and J. Raskin, "PECVD oxide as intermediate film for wafer bonding: Impact of residual stress," Microelectron. Eng, vol. 87, no. 11, pp. 2178-2186, 2010.

[10] I. Park, K. Ryu, J. Jeong and J. Ahn, "Dielectric Stacking Effect of Al_2O_3 and HfO_2 in Metal–Insulator–Metal Capacitor," IEEE Electron Device Lett, vol. 34, no. 1, pp. 120-122, 2013.