TCAD Simulation Study on P-type Source-gated CuO TFTs

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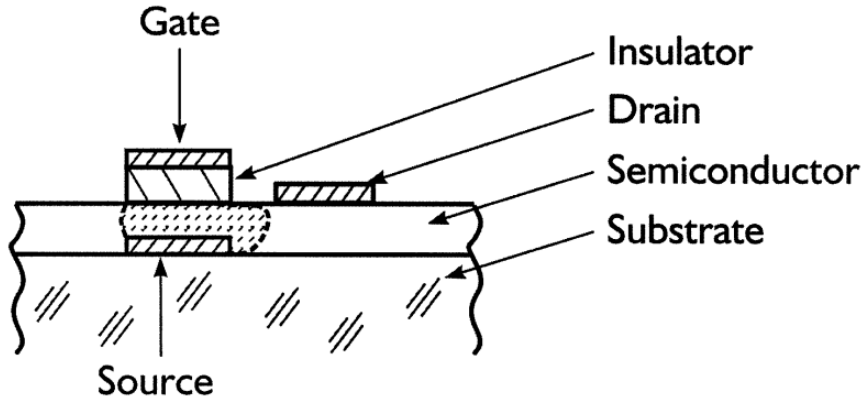
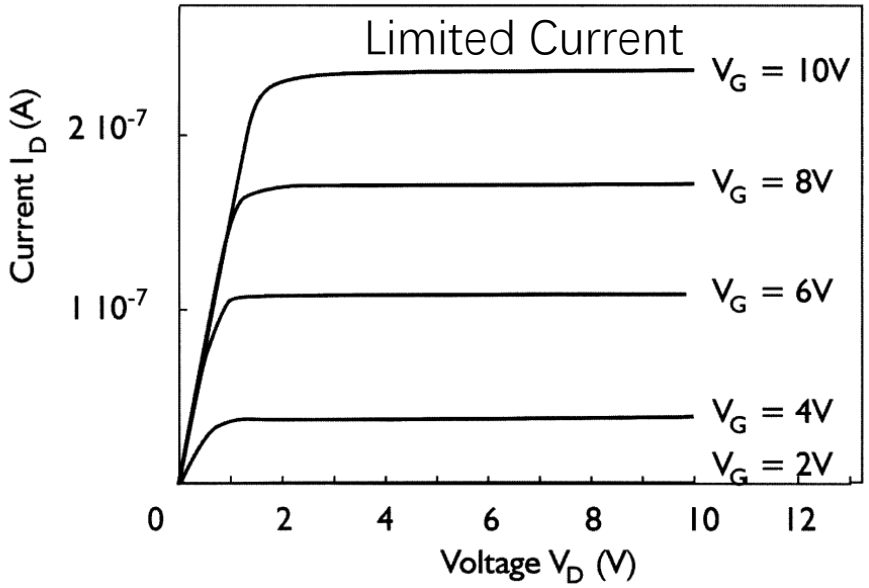
Symposium on Schottky Barrier MOS 2023 "The Schottky barrier transistor in emerging electronic devices"

Concept of the Source-gated Transistor





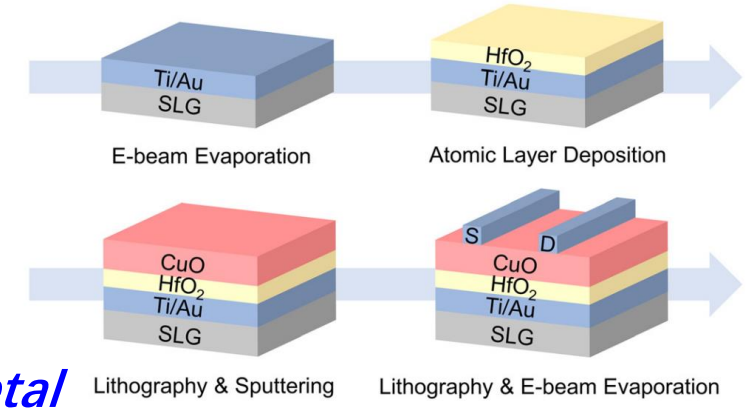
J. M. Shannon *et al.*, IEEE Electron Device Lett., 2003.

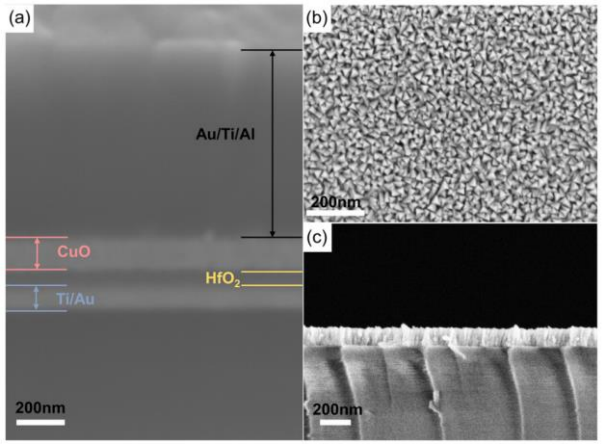
Advantages

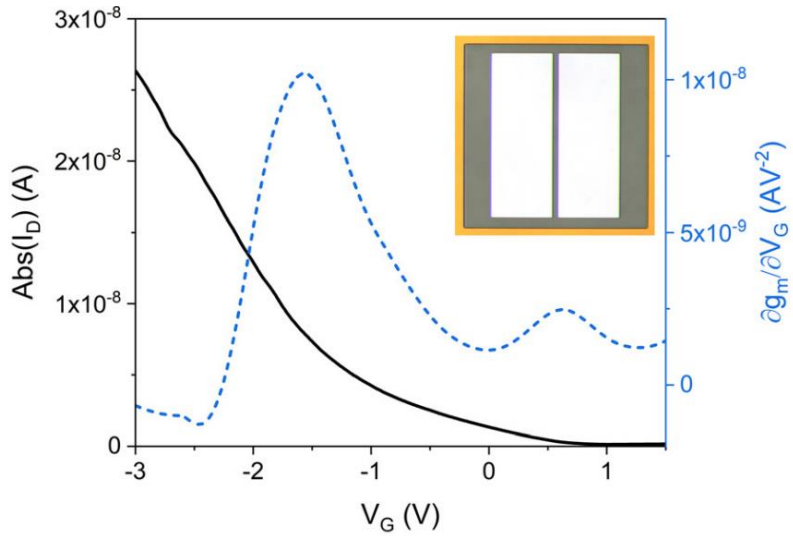
- Low Saturation Voltage V_{DSAT}
- High intrinsic gain
- Tolerance to short channel effects
- Improved bias stress stability

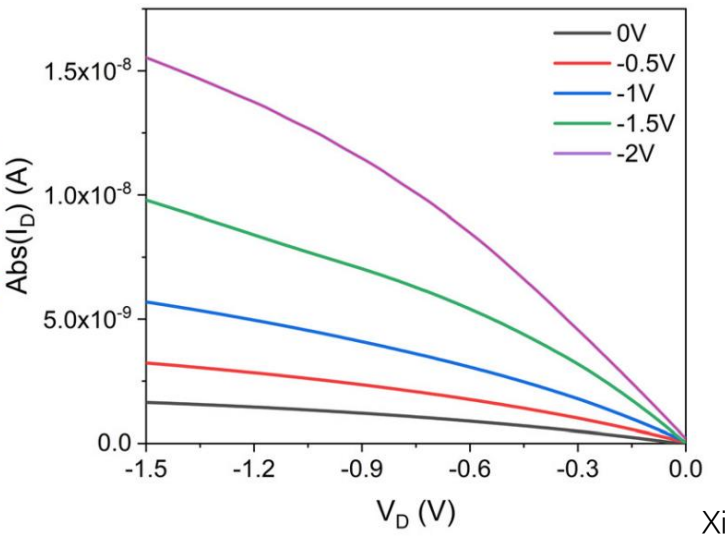
P-type CuO Thin-film Transistor

Potential to realize metal oxide CMOS circuits





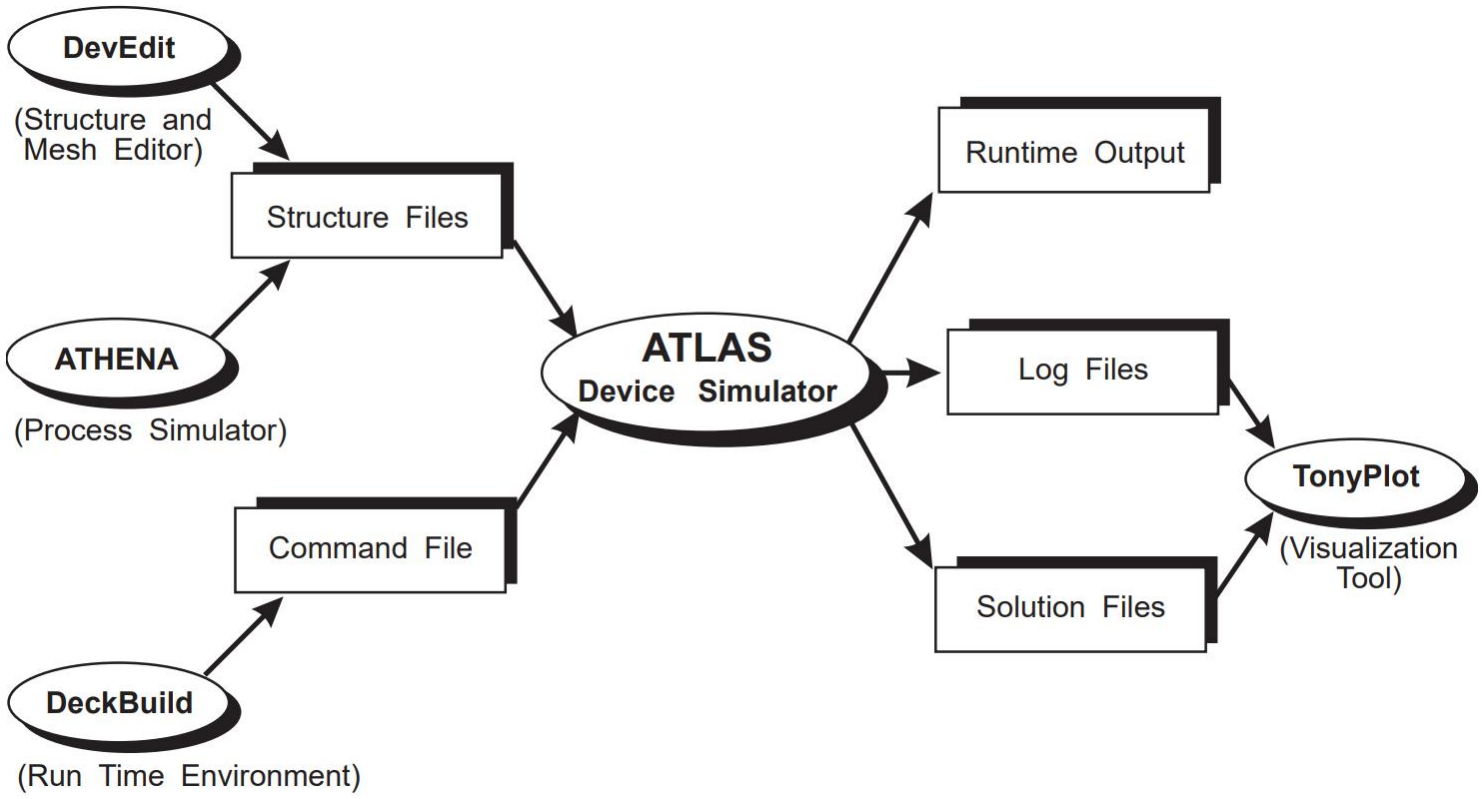




Xi Zeng *et al.*, *Appl. Phys. Lett.*, 2022.

TCAD simulations

TCAD (Technology Computer Aided Design) tool: Silvaco Atlas



- Predictive physically-based simulation
- Provides insight into the internal physical mechanisms associated with device operation
- Visualizes theoretical knowledge.

Objective and Outline

A low V_{DSAT}

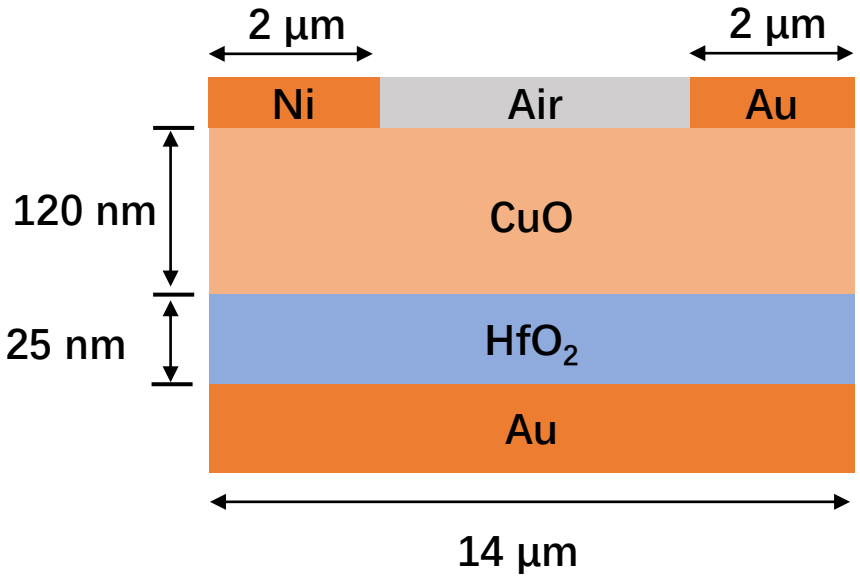
A relatively high saturation current I_{DSAT}

Good analog performance

- Design principle of Source-gated CuO TFT Structure
- Simulations of structure parameters on V_{DSAT} and I_{DSAT}
- Analog performance
- Conclusion

➢ Design principle of Source-gated CuO TFT Structure

Schottky Source Contact



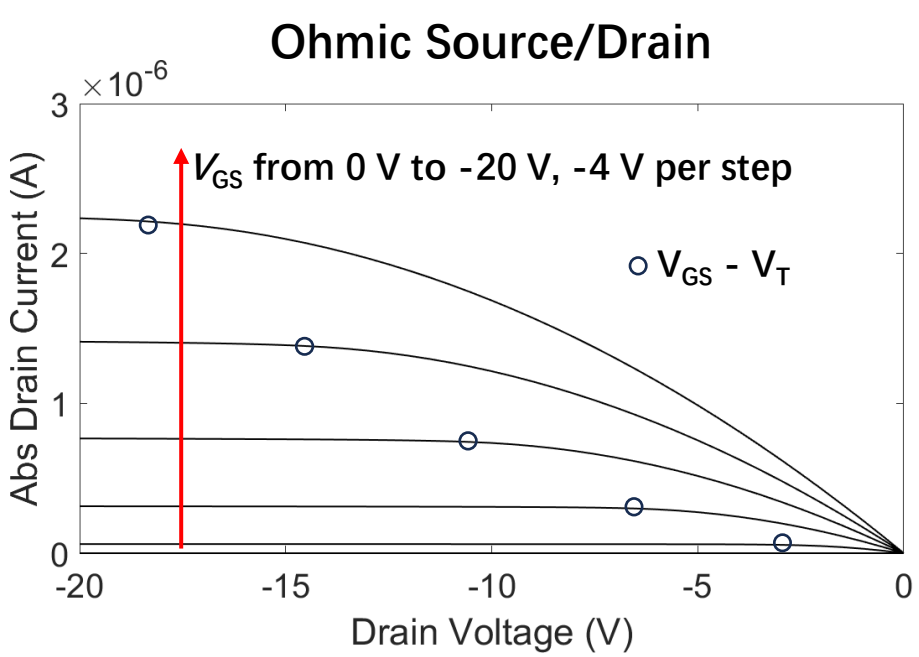
Φ_{Ni} = 5.2 eV < Φ_{CuO} = 5.47 eV

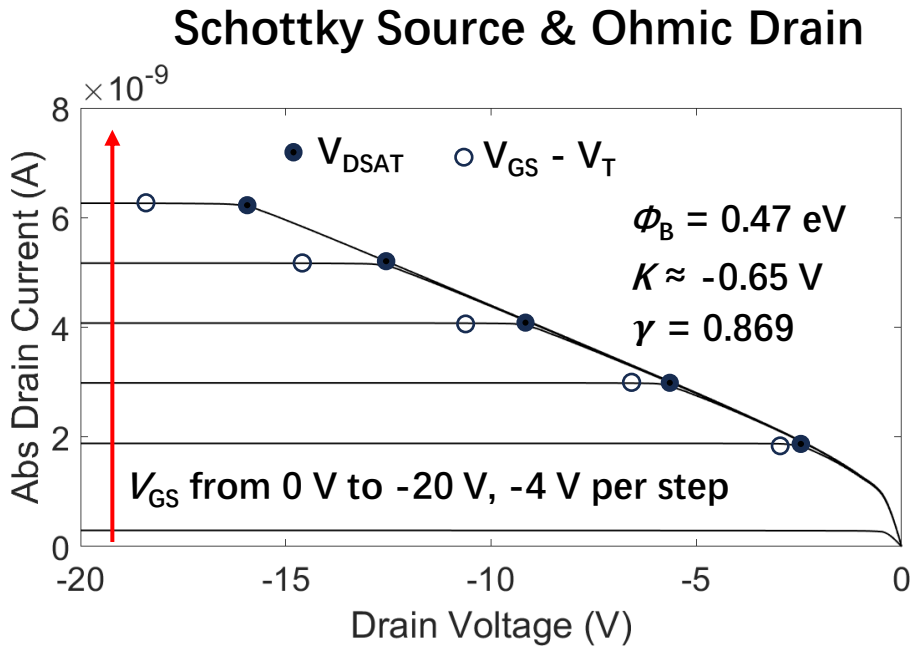
Schottky Barrier Height :

$\Phi_B = E_{g,CuO} + \chi_{CuO} - \Phi_{Ni}$ = 0.47 eV

Parameter from experiments	Value
Width	270 µm
CuO Band gap	1.6 eV
CuO Permittivity	18.1
CuO Affinity	4.07 eV
CuO work function	5.49 eV
Au work function	5.47 eV
Doping	5×10^{17} cm^{-3}
Hole mobility	0.62×10^{-3} $cm^2V^{-1}s^{-1}$
Fixed oxide charge	8.78×10^{12} cm^{-2}
CuO-HfO_2 back Interface defects	6×10^{10} $eV^{-1}cm^{-2}$
CuO-Air front interface defects	3.57×10^{13} $eV^{-1}cm^{-2}$
Threshold voltage	-1.8 V

➢ Design principle of Source-gated CuO TFT Structure





The saturation voltage V_{DSAT}

$$V_{\mathrm{DSAT}} \approx (V_{\mathrm{GS}} - V_{\mathrm{T}}) \cdot \frac{C_{\mathrm{i}}}{C_{\mathrm{i}} + C_{\mathrm{s}}} + K$$

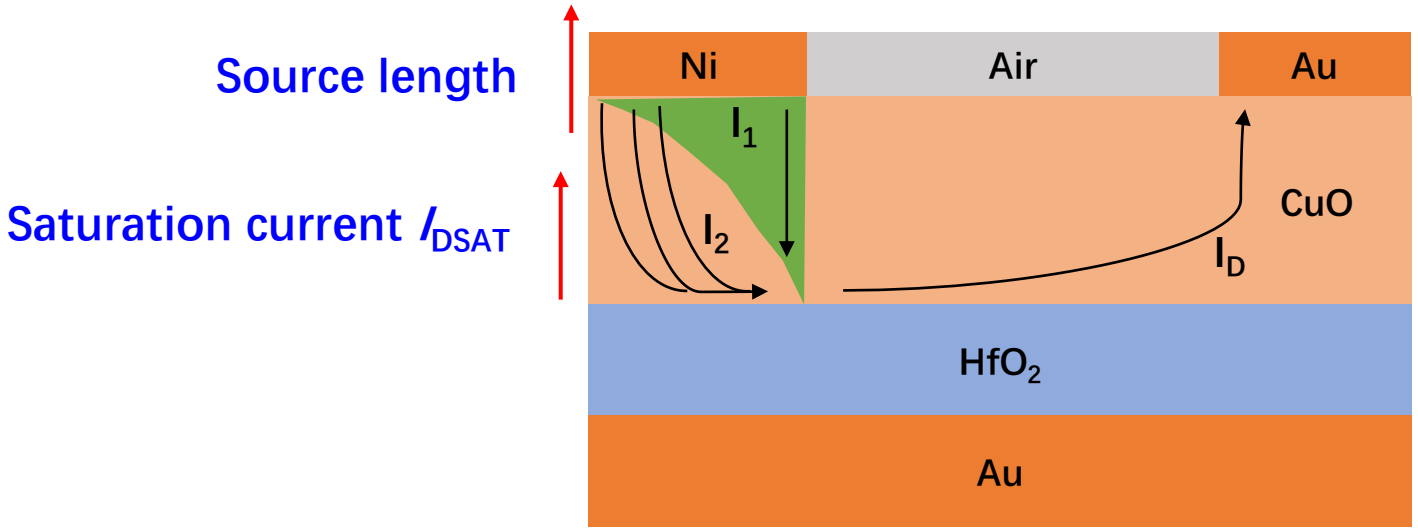
where C_i ($=\varepsilon_i/t_i$) and C_s ($=\varepsilon_s/t_s$) are insulator and semiconductor capacitances per unit aera, respectively, and K is a constant.

The saturation coefficient

$$\gamma = \frac{dV_{\mathrm{DSAT}}}{dV_{\mathrm{GS}}} = \frac{C_{\mathrm{i}}}{C_{\mathrm{i}} + C_{\mathrm{s}}} < 1$$

Eva Bestelink *et al., Adv. Electron. Mater.* 2022

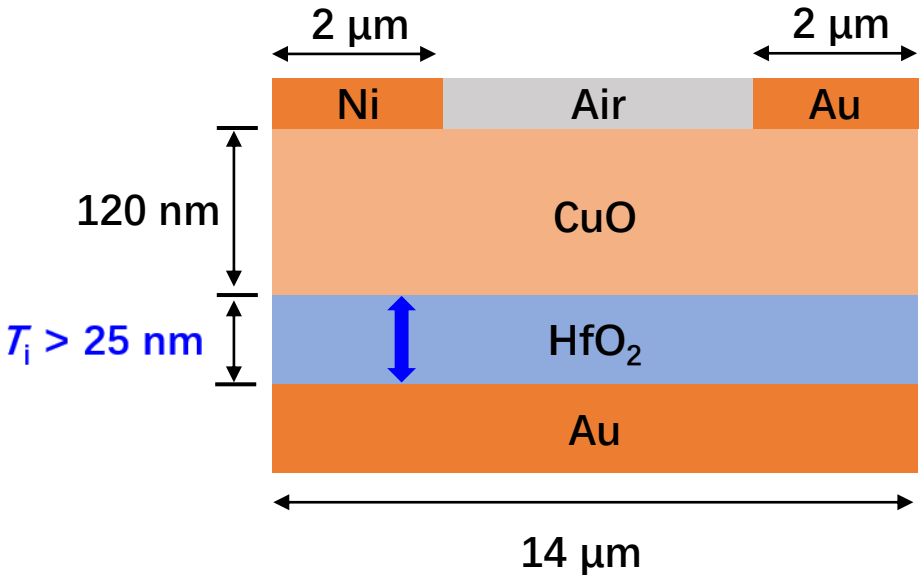
➢ Design principle of Source-gated CuO TFT Structure



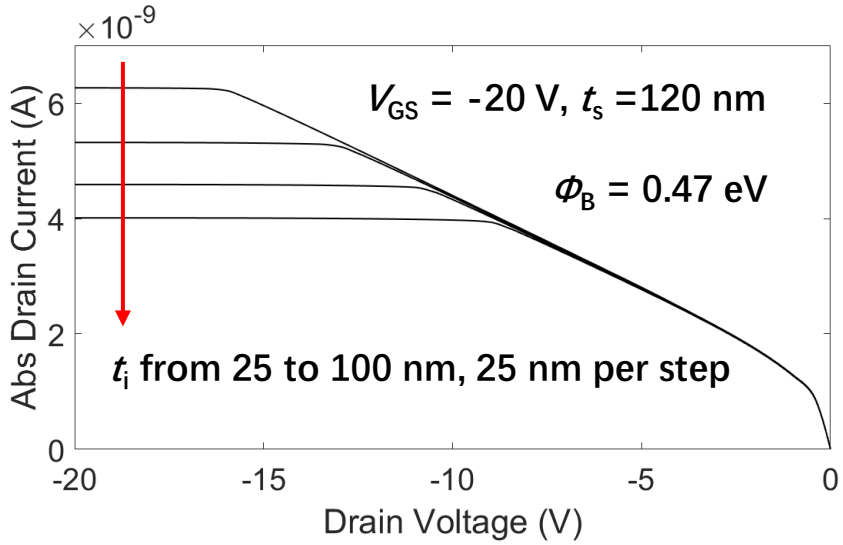
Low-filed JFET-like operation

J. M. Shannon *et al.*, *IEEE Electron Device Lett.*, 2013.

➢ Simulations of structure parameters on V_{DSAT} and I_{DSAT}

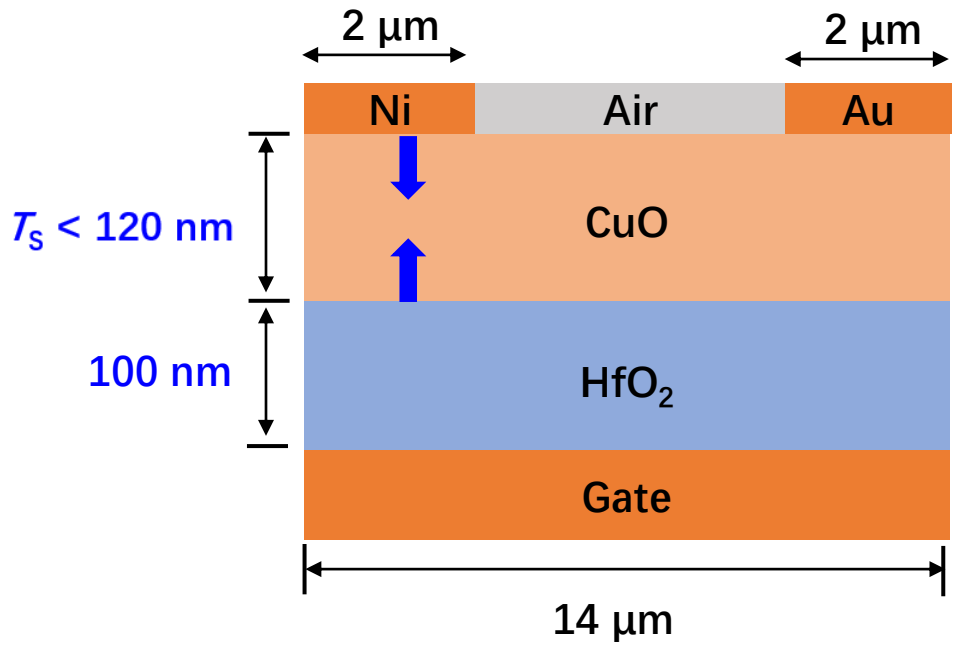


Increase HfO_2 thickness t_i

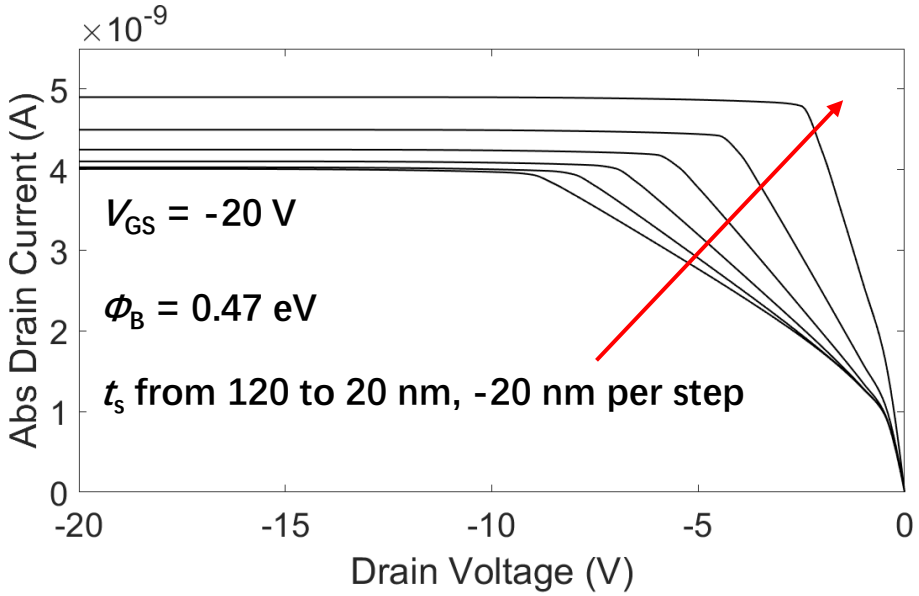


Smaller V_{DSAT} *Lower I_{DSAT}*

➢ Simulations of structure parameters on V_{DSAT} and I_{DSAT}

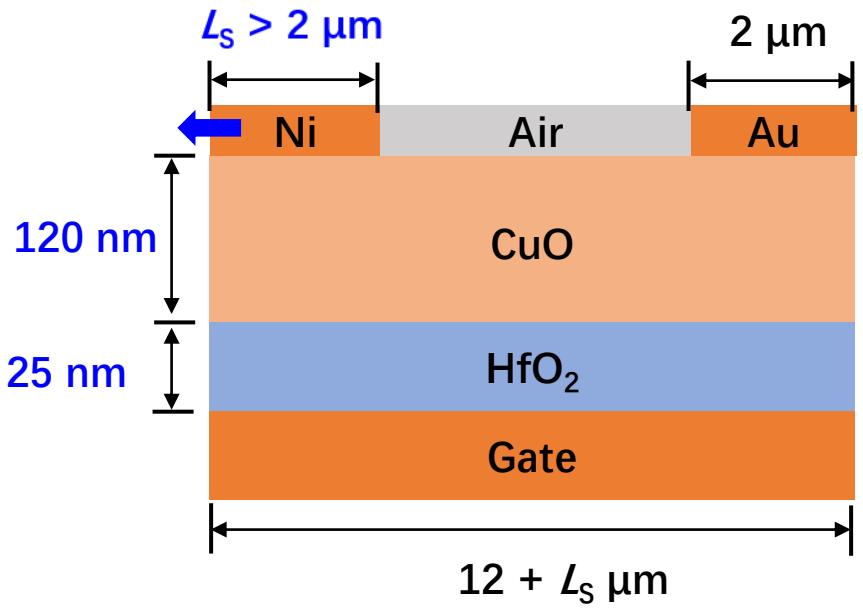


Decrease CuO thickness t_s

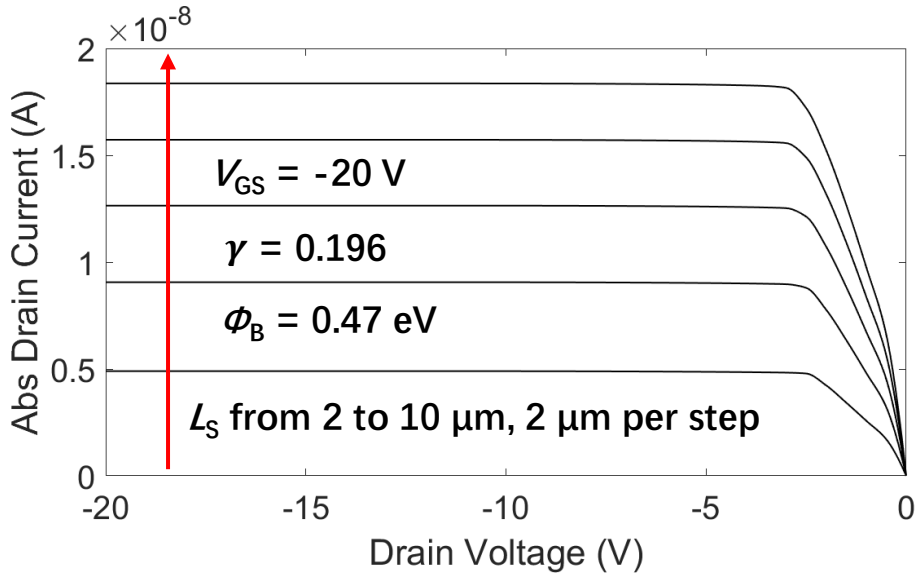


Smaller V_{DSAT} *Higher I_{DSAT}*

➢ Simulations of structure parameters on V_{DSAT} and I_{DSAT}



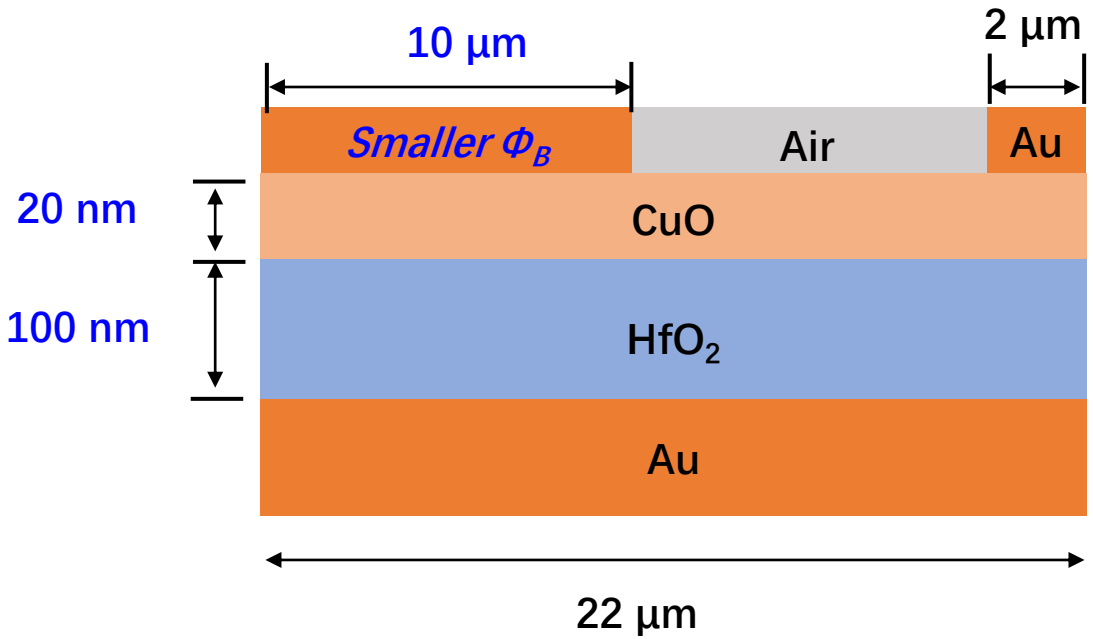
Increase source length L_S



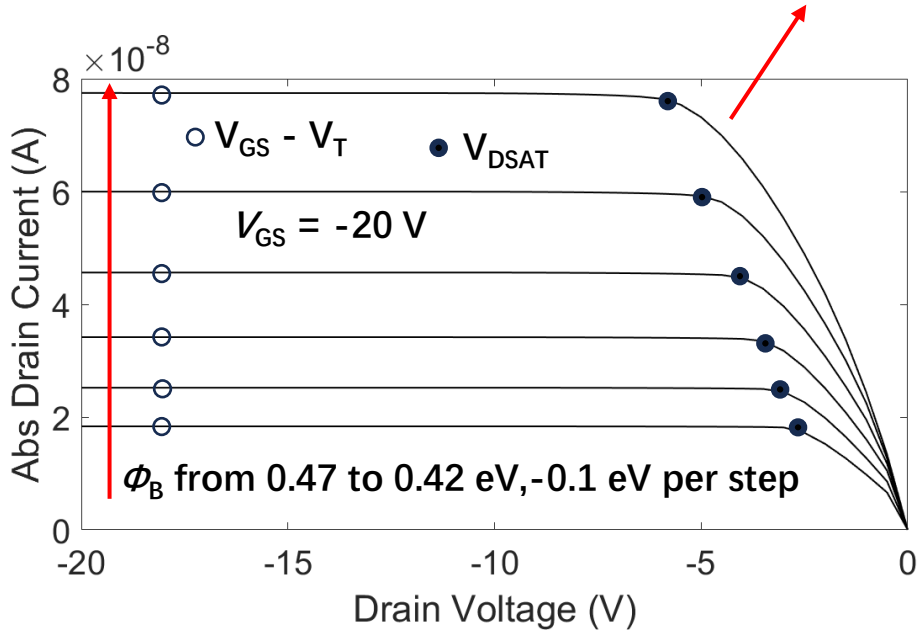
Same V_{DSAT}

Higher I_{DSAT}

➢ Simulations of structure parameters on V_{DSAT} and I_{DSAT}



Loss of SGT characteristic!



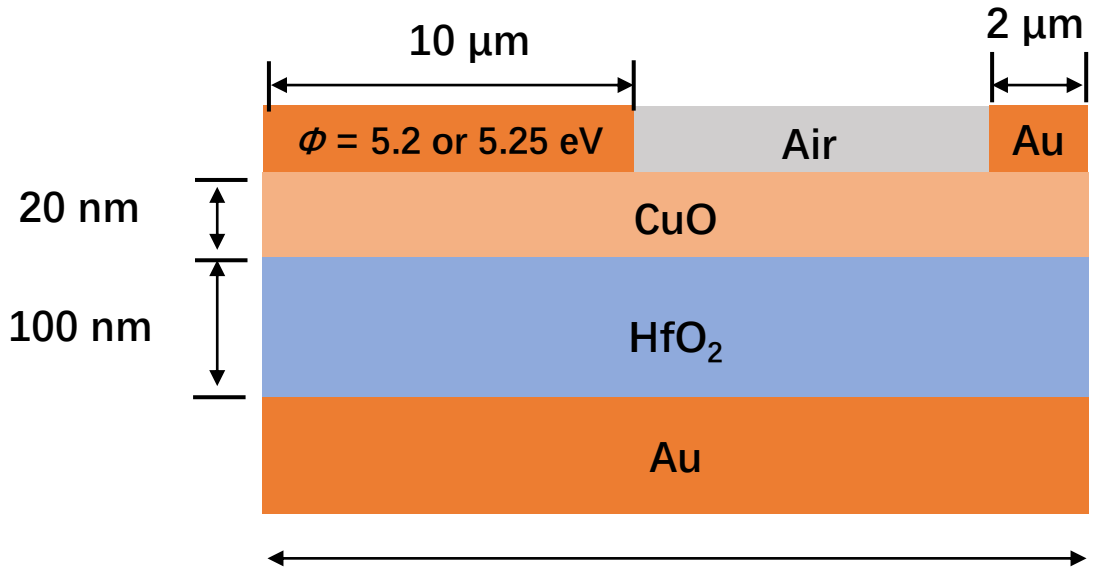
Reduce barrier height

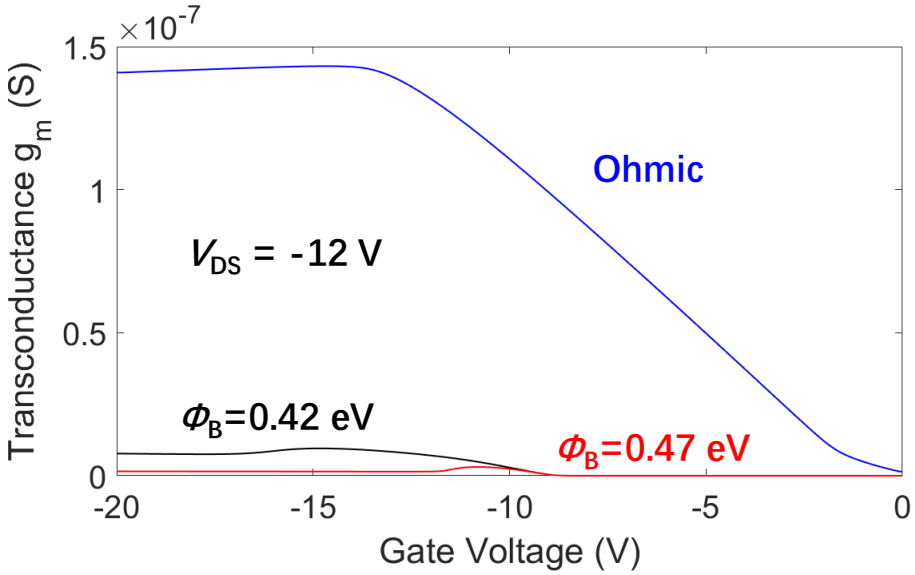
$$W_D = \sqrt{\frac{2\epsilon_0 \epsilon_s}{qN_D}\left(\phi_{bi} - V - \frac{k_B T}{q}\right)}$$

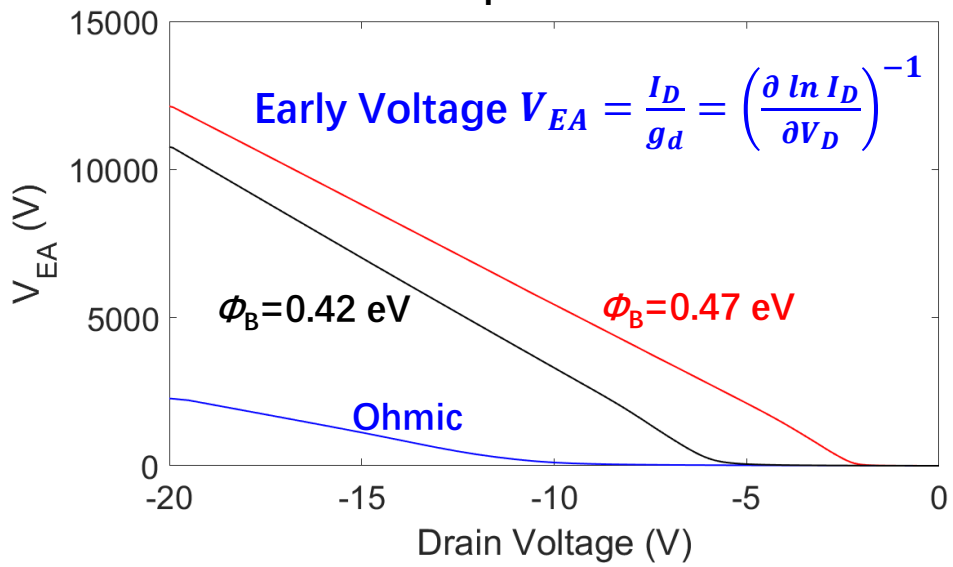
Φ_B = 0.47 eV *Lower I_{DSAT}* *Smaller V_{DSAT}*

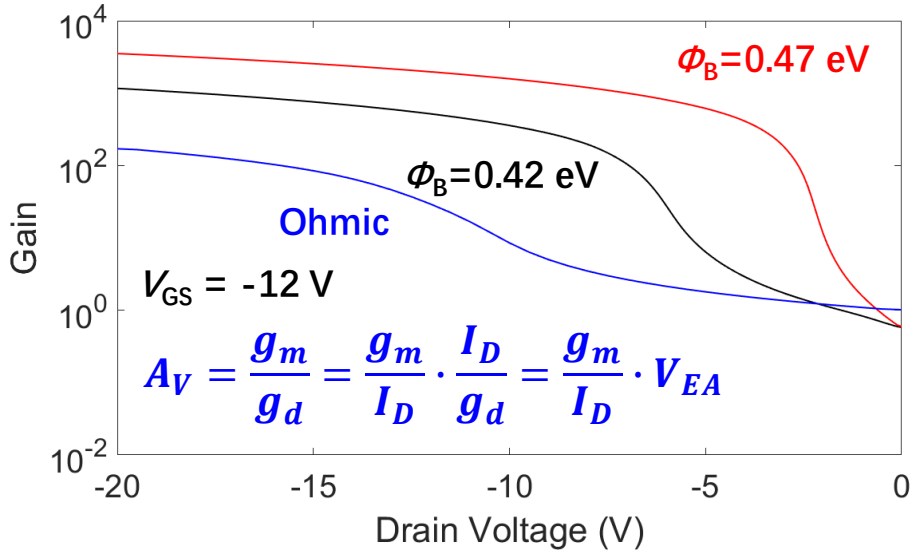
Φ_B = 0.42 eV *Higher I_{DSAT}* *Larger V_{DSAT}*

➢ Analog performance

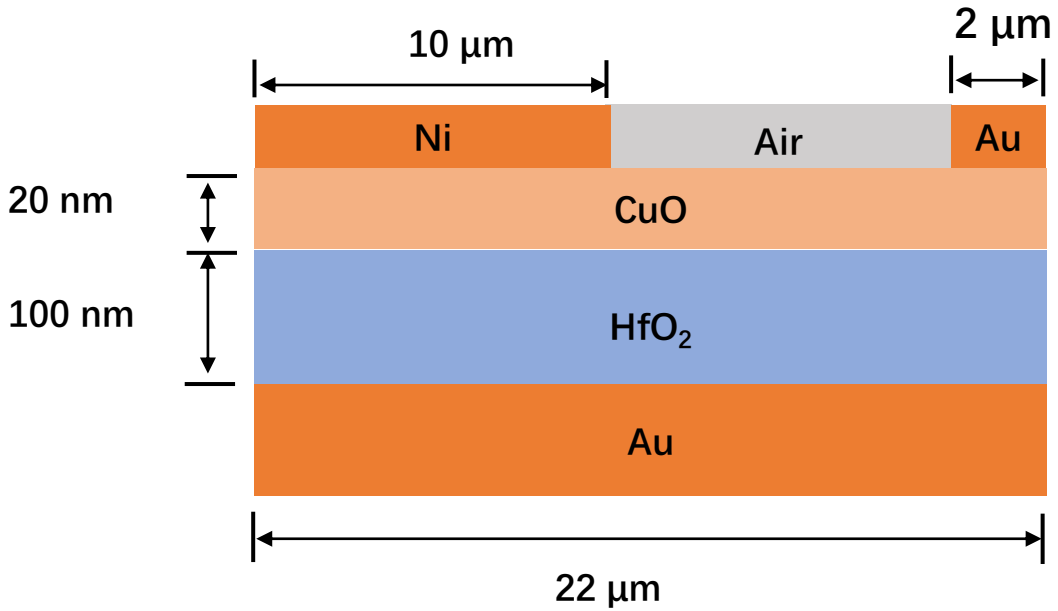


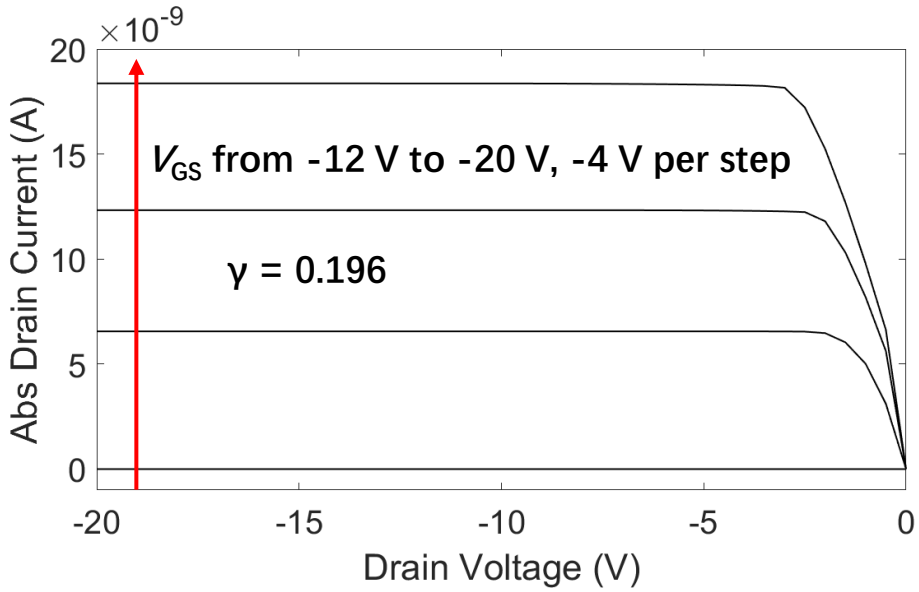






➢ Conclusion





Performance comparison at V_{GS} = -12 V:

	V_{DSAT}	I_{DSAT}	A_V
Ohmic contact	-10.8 V	8×10^{-7} A	~100
Schottky contact (Φ_B = 0.47 eV)	-2.8 V	7×10^{-9} A	~5000