Solid-State Electronics 217 (2024) 108946

Contents lists available at ScienceDirect

Solid State Electronics

journal homepage: www.elsevier.com/locate/sse

Analysis of anomalous C-V behavior for extracting the traps density in the undoped polysilicon with a double-BOX structure

Yang Huang [a,*], Yiyi Yan [b], Massinissa Nabet [b], Fanyu Liu [a,*], Bo Li [a,*], Binhong Li [a], Zhengsheng Han [a], Sorin Cristoloveanu [c], Jean-Pierre Raskin [b,*]

[a] Institute of Microelectronics and Key Laboratory of Science and Technology on Silicon Devices, CAS, and University of Chinese Academy of Sciences, China
[b] ICTEAM, Université Catholique de Louvain (UCLouvain), Belgium
[c] IMEP - INP Grenoble MINATEC, France

ARTICLE INFO

The review of this paper was arranged by Prof. Alex Zaslavsky

Keywords:
Radio Frequency
High resistivity Silicon-on-Insulator substrate
Polysilicon
Trap density
TCAD simulation
Small signal equivalent circuit model

ABSTRACT

A new Double-BOX structure is introduced to reveal the electrical properties of undoped polysilicon used to enhance the performance of radio frequency SOI substrates. A plateau is clearly observed in the capacitance–voltage (C-V) characteristics, which is due to the influence of the potential barrier formed at the grain boundary. A tangential approximation method based on a three-element circuit model is proposed for correcting the measured C-V curve. With the corrected C-V curve, the effective trap density distribution in polysilicon is determined for each frequency.

1. Introduction

High resistivity Silicon-on-Insulator (HR-SOI) substrate is widely used for radio frequency (RF) integrated circuits and mixed signal applications due to its low cost and low loss. The problem is the well-known parasitic surface conduction (PSC) effect caused by the fixed charges in the buried oxide layer (BOX) [1,2,3]. The PSC effect leads to resistivity degradation near the BOX/Substrate interface, and thus increases the substrate loss. To solve this problem, a trap-rich layer with high resistivity is introduced underneath the BOX [1,4]. This layer is commonly achieved with polycrystalline or amorphous silicon. The electrical properties of polysilicon are strongly affected by the large density of traps [5]. The more traps in it, the better the RF performance will be. Therefore, the trap density of polysilicon near the interface is an important parameter that governs the RF quality of the substrate. However, it is difficult to extract the trap density directly with C-V method on traditional trap-rich SOI wafers, due to the impact of the depletion layer in the silicon substrate. We propose a new structure with double BOX (D-BOX) layers to overcome this issue, as shown in Fig. 1. The presence of the BOX2 eliminates the impact of the bulk depletion layer on C-V performance, simplifying the analysis and making the characterization of trap density in the trap-rich layer come true.

In this paper, we characterize the trap density in the trap-rich layer with C-V method on D-BOX structure. The equivalent RC circuits at different gate biases are developed according to the analysis of TCAD simulation. Then, a three-element circuit model is used to correct the capacitance and conductance measurements. Finally, the effective trap density of the polysilicon is calculated directly from the corrected C-V curve.

2. Device fabrication and experimental setup

The D-BOX (metal/oxide/polysilicon/oxide/silicon) structure (Fig. 1) was fabricated at UClouvain. The fabrication process is as follows: firstly, a silicon dioxide (BOX2) layer was thermally grown at 900°C on top of the silicon substrate. Then, a polysilicon layer was deposited by low-pressure chemical-vapor deposition (LPCVD) at 625°C. The capacitive structure is composed of a silicon dioxide layer (BOX1)

* Corresponding authors.
E-mail addresses: yang.huang@uclouvain.be (Y. Huang), yiyi.yan@uclouvain.be (Y. Yan), massinissa.nabet@uclouvain.be (M. Nabet), liufanyu@ime.ac.cn (F. Liu), libo3@ime.ac.cn (B. Li), libinhong@ime.ac.cn (B. Li), zshan@ime.ac.cn (Z. Han), sorin.cristoloveanu@grenoble-inp.fr (S. Cristoloveanu), jean-pierre.raskin@uclouvain.be (J.-P. Raskin).

https://doi.org/10.1016/j.sse.2024.108946

Available online 26 April 2024

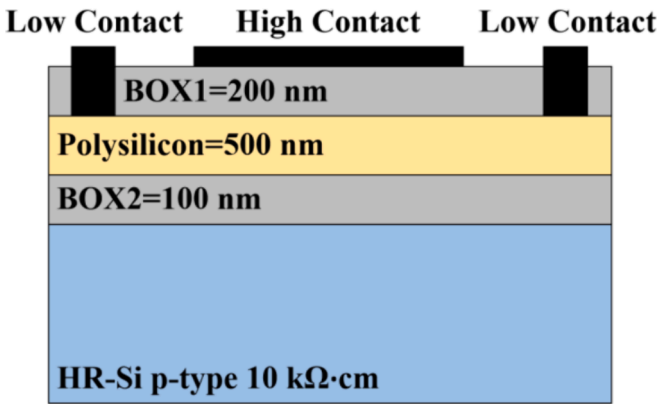

Fig. 1. Cross-section of the D-BOX structure with trap-rich layer.

deposited on top of the polysilicon film by plasma-enhanced chemical-vapor deposition (PECVD). Finally, an aluminum layer was deposited on top of BOX1 and in contact with the polysilicon film. The polysilicon film is undoped, while the silicon substrate is lightly p-doped with a resistivity of 10 kΩ•cm. The area of the metal gate on top of BOX1 layer is 8.76×10^{-6} m^2. Other information related to the structure are given in Fig. 1.

C-V and G-V measurements were performed using a Keysight B1500A semiconductor parameter analyzer from 1 kHz to 100 kHz under dark at room temperature. The High and Low electrodes are connected to the front gate and polysilicon, respectively. To obtain accurate and reliable results, the hold time and delay time are set to 30 s and 1 s, respectively.

3. Experimental results and discussion

Fig. 2 shows the measured C-V characteristics of the polysilicon MOS structure for frequencies from 1 kHz to 100 kHz. A large frequency dispersion is observed. This dispersion arises from the large value of series resistance and the time-constant dispersion of the traps in polysilicon. The depletion regime occurs at the minimum capacitance value, which aligns with the flat band voltage (V_{FB}). The curves are shifted to negative gate voltage, due to the positive fixed charges in the oxide (V_{FB} = -6 V). Moreover, a plateau is clearly observed in the electron accumulation region near flatband ($V_{FB} < V_G < 4$ V). This phenomenon appears for all the measured samples. Hereafter, we simulate the structure with a TCAD tool (Atlas from Silvaco) to explore and understand this specific behavior.

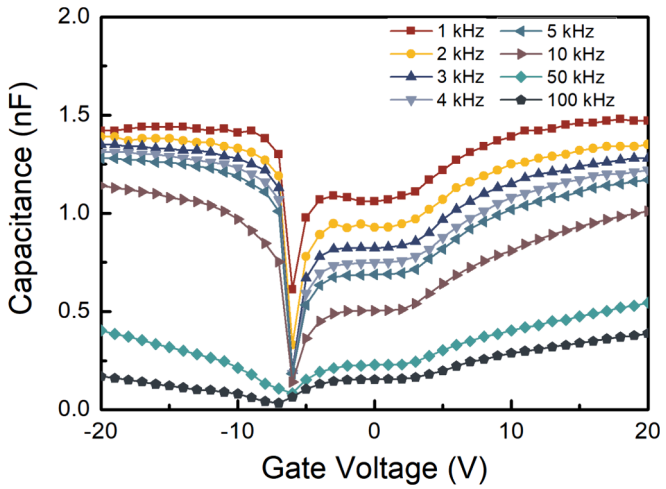

Fig. 2. Measured C-V curves of the polysilicon MOS structure for a frequency range from 1 kHz to 100 kHz.

Under the deposition conditions used in this work, the polysilicon is composed of a large number of columnar grains. According to previous research [6], there are few trap states in grains, whereas a high density of traps exists at oxide interfaces and grain boundaries. Therefore, the polysilicon layer can be described with the structure shown in Fig. 3 (a) where traps are only located at the front/back interfaces and along the grain boundaries. The bulk of the grain is treated as intrinsic monocrystalline silicon. A similar structure of polysilicon film has been proposed in the literature [6]. To simplify the simulation, we developed a model with only half of this structure, as shown in Fig. 3 (b). Here, only grain boundaries are considered. The distribution of trap states at the ground boundary shown in the literature [7,8] was used in the simulation. This distribution contains both exponentially decaying band tail states and Gaussian distributions of mid-gap states. The simulated curve shown in Fig. 4 (a) agrees quite well with the experimental results. Without a positive oxide charge V_{FB} is shifted to 0 V.

In our device, the gate controls the carrier density in the grains under the "High Contact", resulting in the modulation of the grain boundary barrier height. With the help of TCAD simulation, we obtain the energy band diagrams and the equivalent RC circuits of the polysilicon at different gate biases, as shown in Fig. 4 (b)-(f).

- At V_G = -15 V (Fig. 4 (b)), the holes are accumulated under the "High Contact". Since the polysilicon also has a p-type behavior at the grain boundary [6], the region near the grain boundary is in accumulation or weak depletion mode that can be neglected. The total capacitance equals to C_{ox} in series with C_{it}.
- At V_G = 0 V (Fig. 4 (c)), which is the flat band voltage, the polysilicon under the "High Contact" is fully depleted. The depletion capacitance (C_{dep}) in series with C_{ox} leads to the decrease of the total capacitance to its minimum value.
- At V_G = 1 V (Fig. 4 (d)), the electrons start to accumulate under the "High Contact". Because of the p-type behavior of the grain boundary, a depletion region is formed at the grain boundary. Due to the existence of C_{gb}, the total capacitance is smaller than that for hole accumulation (V_G = -15 V). Thus, a plateau appears on the C-V curve.
- At V_G = 4 V (Fig. 4 (e)), the electron concentration under the "High Contact" increases with the gate voltage, leading to a decrease of the width of the depletion region at the grain boundary. The values of C_{gb} and total capacitance should have increased, but a decreased or constant value of the total capacitance is observed in both experiments and simulations. This can be explained by the expansion of the inversion layer: another depletion region (C') is formed near the edge of "High Contact" and increases the depletion width.
- At V_G = 15 V (Fig. 4 (f)), the depletion width decreases further with V_G, resulting in a higher total capacitance. When the depletion width at the grain boundary is small enough, the value of C_{gb} can be neglected and the equivalent RC circuit can be simplified.

4. Trap extraction method and results

To obtain more reliable capacitance and conductance characteristics of the device, the series resistance R_S caused by the high resistivity polysilicon between the two contacts need to be de-embedded from the measurement data. Here, we use a three-element circuit model to correct the C-V curve, as shown in Fig. 5. Fig. 5(a) gives the two-element parallel circuit model serving for typical admittance characterization, where C_m is the measured capacitance and G_m is the measured conductance. Fig. 5 (b) presents the three-element circuit model with C_c being the corrected capacitance and G_c the corrected conductance. By equating the real part of the total impedance in Fig. 5(a) and (b), we obtain:

$$\frac{G_m}{G_m^2 + (\omega C_m)^2} = \frac{G_C}{G_C^2 + (\omega C_C)^2} + R_S \quad (1)$$

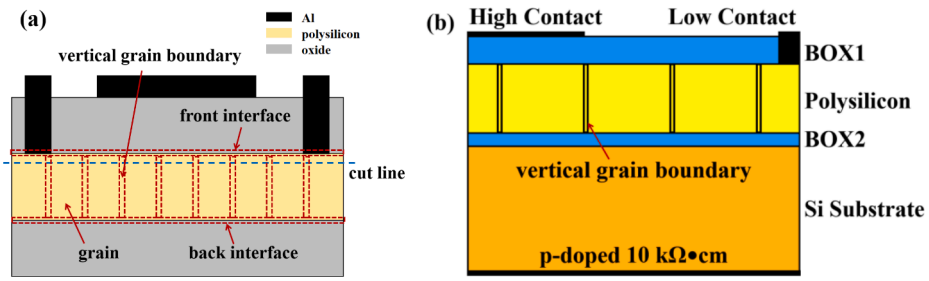

Fig. 3. (a) Structure of the polysilicon film with oxide interfaces and grain boundaries; (b) Cross-section of the simplified structure used in TCAD simulation.

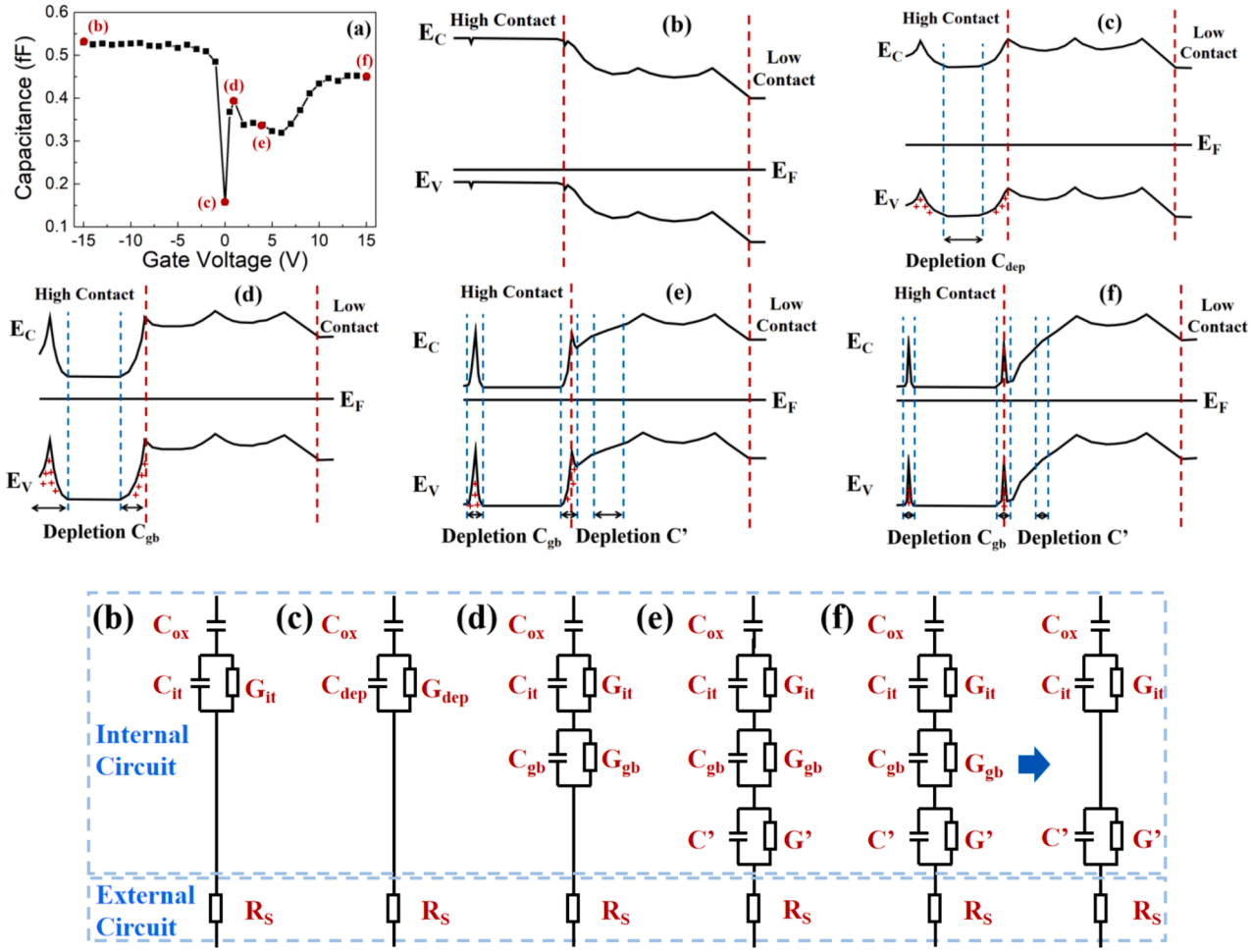

Fig. 4. (a) Simulated C-V curve at 1 kHz. Energy band diagrams and equivalent RC circuits of the polysilicon with (b) V_G = -15 V, (c) 0 V, (d) 1 V, (e) 4 V, and (f) 15 V. C_{ox} is the capacitance of BOX1. C_{it} and G_{it} are the capacitance and conductance of the interface traps, respectively. R_S is the series resistance. C_{dep} and G_{dep} are the total capacitance and conductance of the depletion region in polysilicon under the "High Contact", respectively. C_{gb} and G_{gb} are the total capacitance and conductance of the depletion region formed at the grain boundary. C' and G' are the capacitance and conductance of the additional depletion region near the edge of "High Contact".

where ω is the angular frequency. With $D = G/\omega$, Equation (1) can be rewritten as:

$$\frac{D_m}{\omega(D_m^2 + C_m^2)} = \frac{D_C}{D_C^2 + C_C^2} \times \left(\frac{1}{\omega}\right) + R_s \tag{2}$$

The intercept of $D_m/[\omega(D_m^2 + C_m^2)]$ vs $1/\omega$ with the Y-axis gives the value of R_S, as shown in Fig. 6. However, due the potential barrier formed at the grain boundary under the "High Contact", the value of R_S changes with gate bias and frequency. In hole accumulation region, no or very low potential barrier is formed at the grain boundary. The plot in Fig. 6(a) is linear as a function of $1/\omega$, which means that the value of R_S is independent on frequency and can be extracted directly from the intercept with the Y-axis. In electron accumulation region, the potential barrier is high at the grain boundary. Due to the non-negligible effect of the barrier region on the total R_S, the plot in Fig. 6(b) is no longer a linear function of $1/\omega$. The value of R_S depends on frequency and should be determined by the intercept of the tangent line with the Y-axis.

The extracted R_S as a function of gate bias at 1 kHz is plotted in Fig. 7. In strong hole accumulation region, R_S is nearly constant with a value of 4 kΩ. The peak value appears when the barrier has a maximum width at the grain boundary. With the increase of gate bias, the width of the barrier region decreases and so does the value of R_S. The shape of this

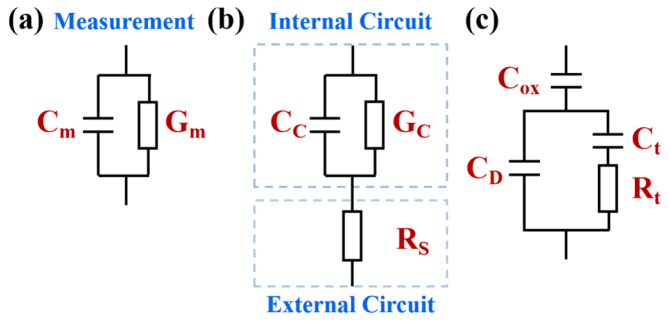

Fig. 5. Small signal equivalent circuit models of MOS capacitors: (a) parallel circuit model, (b) three-element circuit model, and (c) series RC model.

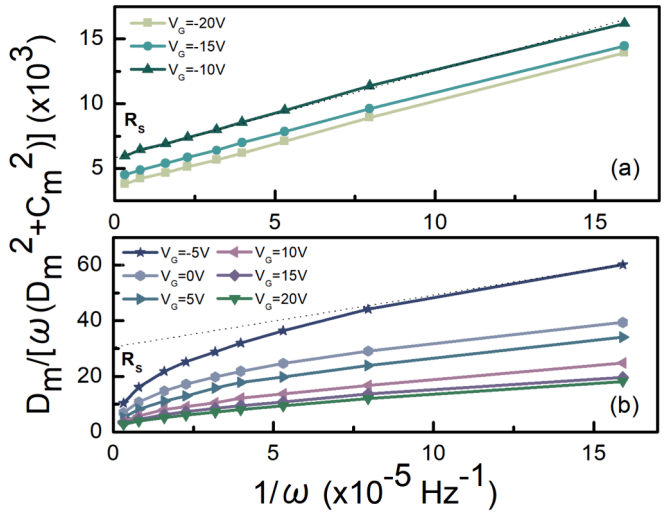

Fig. 6. Calculated $D_m/[\omega(D_m^2 + C_m^2)]$ as a function of $1/\omega$ to extract the value of R_S.

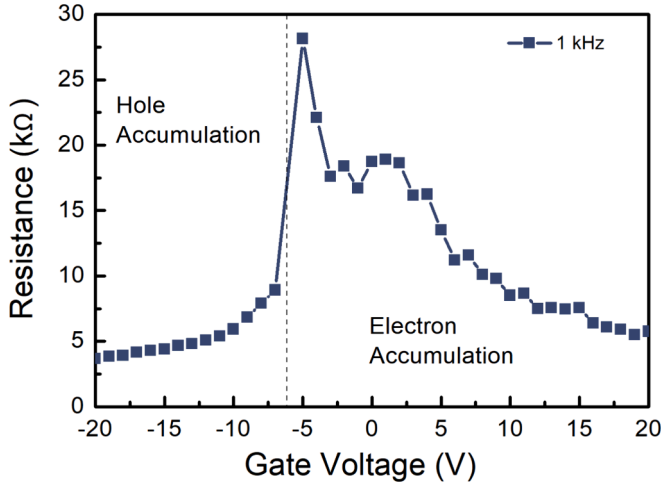

Fig. 7. Calculated R_S as a function of gate bias at 1 kHz.

curve corresponds well with the extracted effective resistivity of the trap-rich substrate in [4].

After withdrawing the effect of R_S, the corrected capacitance C_C and conductance G_C curves are obtained. Then, the equivalent circuit for the MOS capacitor proposed in [9,10] is used to calculate the effective trap density in polysilicon, as shown in Fig. 5 (c). Here, C_D is the depletion layer capacitance. C_t and R_t form the series RC network of the effective trap states in polysilicon, which includes the effects of both interface traps and grain boundary traps. Since the oxide capacitance C_{ox} is determined from the geometric parameters of the device and C_D can be ignored in hole/electron accumulation region, the numerical values for C_t and R_t can be calculated. The trap capacitance is converted to trap density by dividing by the electronic charge and the area of the capacitor. The calculated effective trap densities in polysilicon as a function of gate bias for a frequency range from 1 kHz to 5 kHz are shown in Fig. 8. It is found that the defect states in polysilicon have a U-shaped distribution with shallow exponential tail states near the conduction/valence band and deep states in the form of narrow peak near the mid-gap. Similar behavior in the defect states distribution of polysilicon was found in [7] and [11]. In addition, a frequency dispersion is observed over the whole range of gate bias, which indicates the wide distribution of time constant at the Fermi level in polysilicon. In other words, the trap states at a given surface potential have more than one time constant. Therefore, the trap density calculated by the single RC series circuit represent the average effect of all the states with their various time constants. It is worth noting that the calculated trap density at a specific frequency only represents those trap states capable of following the ac signal. To ensure all trap states respond to the ac signal, lower frequency measurements are needed.

5. Conclusions

We proposed a new D-BOX structure to characterize the trap density in the trap-rich layer with C-V method. A plateau is observed in the C-V characteristics of the undoped polysilicon MOS structure. To analyze this phenomenon, the energy band diagrams of the polysilicon at different gate biases were computed. It is the potential barrier at the vertical polysilicon grain boundaries that causes the anomalous C-V behavior. A three-element circuit model was developed to correct the capacitance and conductance measurements by considering the large value of series resistance caused by the high-resistivity polysilicon. This correction is able to recover the real electrical properties of the measured C-V curve and deliver the distribution of the effective trap density. The D-BOX structure used in this paper provides a simple evaluation method to determine the quality of trap-rich layer at wafer level without complex device fabrication process.

CRediT authorship contribution statement

Yang Huang: Methodology, Writing – original draft, Writing – review & editing, Data curation, Formal analysis, Visualization. **Yiyi Yan:** Investigation. **Massinissa Nabet:** Software. **Fanyu Liu:** Validation. **Bo**

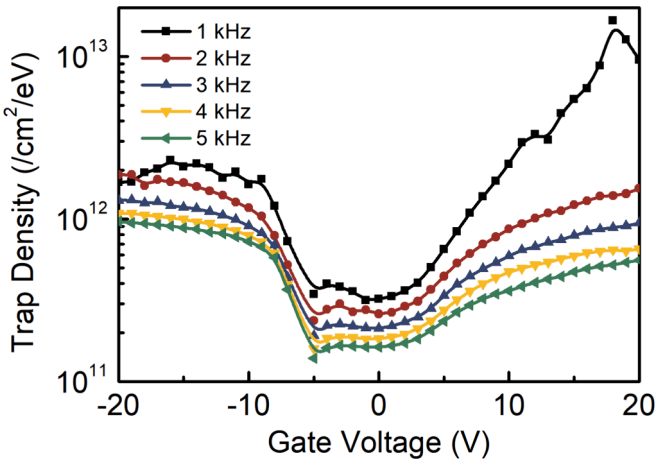

Fig. 8. Effective trap densities in polysilicon as a function of gate bias for a frequency range from 1 kHz to 5 kHz.

Li: Validation. **Binhong Li:** Validation. **Zhengsheng Han:** Supervision, Writing – review & editing. **Sorin Cristoloveanu:** Supervision, Writing – review & editing, Methodology. **Jean-Pierre Raskin:** Conceptualization, Project administration, Supervision, Writing – review & editing.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

Data will be made available on request.

Acknowledgements

We thank the Wallonia Infrastructure for nano fabrication (WINFAB) and the Wallonia electronics and communications measurements (WELCOME) platforms for the access to the experimental facilities. We also thank the University of Chinese Academy of Sciences (UCAS) Research Program for the support.

References

[1] Lederer D, Raskin J-P. RF performance of a commercial SOI technology transferred onto a passivated HR silicon substrate. IEEE Trans Electron Devices July 2008;55 (7):1664–71. https://doi.org/10.1109/TED.2008.923564.

[2] Lederer D, Raskin J-P. Effective resistivity of fully-processed SOI substrates. Solid State Electron 2005;49(3):491–6. https://doi.org/10.1016/j.sse.2004.12.003.

[3] Lederer D, Raskin J-P. New substrate passivation method dedicated to HR SOI wafer fabrication with increased substrate resistivity. IEEE Electron Device Lett 2005;26(11):805–7. https://doi.org/10.1109/LED.2005.857730.

[4] Roda Neve C, Raskin J-P. RF harmonic distortion of CPW lines on HR-Si and trap-rich HR-Si substrates. IEEE Trans Electron Devices 2012;59(4):924–32. https://doi.org/10.1109/TED.2012.2183598.

[5] Oodate Y, Tanimoto Y, Tanoue H, Kikuchihara H, Mattausch HJ, Miura-Mattausch M. Compact modeling of the transient carrier trap/detrap characteristics in polysilicon TFTs. IEEE Trans Electron Devices 2015;62(3):862–8. https://doi.org/10.1109/TED.2015.2388799.

[6] Kimura M, Yoshino T, Harada K. Complete extraction of trap densities in poly-si thin-film transistors. IEEE *Transactions on Electron Devices* 2010;57(12):3426–33. https://doi.org/10.1109/TED.2010.2073711.

[7] Dimitriadis CA, et al. Determination of bulk states and interface states distributions in polycrystalline silicon thin-film transistors. J Appl Phys 1993;74(4):2919–24. https://doi.org/10.1063/1.354648.

[8] Jackson WB, Johnson NM, Biegelsen DK. Density of gap states of silicon grain boundaries determined by optical absorption. Appl Phys Lett 1983;43(2):195–7. https://doi.org/10.1063/1.94278.

[9] Terman LM. An investigation of surface states at a silicon/silicon oxide interface employing metal-oxide-silicon diodes. Solid State Electron 1962;5(5):285–99. https://doi.org/10.1016/0038-1101(62)90111-9.

[10] Nicollian EH, Goetzberger A. "The si-sio, interface – electrical properties as determined by the metal-insulator-silicon conductance technique", in The. Bell Syst Tech J 1967;46(6):1055. https://doi.org/10.1002/j.1538-7305.1967.tb01727.x.

[11] Hirae S, Hirose M, Osaka Y. Energy distribution of trapping states in polycrystalline silicon. J Appl Phys 1980;51(2):1043–7. https://doi.org/10.1063/1.327709.