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Surface Passivation of CIGS Solar Cells Using Gallium Oxide

*Siddhartha Garud, Nikhil Gampa, Thomas G. Allen, Ratan Kotipalli, Denis Flandre, Maria Batuk, Joke Hadermann, Marc Meuris, Jef Poortmans, Arno Smets, and Bart Vermang**

This work proposes gallium oxide grown by plasma-enhanced atomic layer deposition, as a surface passivation material at the CdS buffer interface of $Cu(In,Ga)Se_2$ (CIGS) solar cells. In preliminary experiments, a metal-insulator-semiconductor (MIS) structure is used to compare aluminium oxide, gallium oxide, and hafnium oxide as passivation layers at the CIGS-CdS interface. The findings suggest that gallium oxide on CIGS may show a density of positive charges and qualitatively, the least interface trap density. Subsequent solar cell results with an estimated 0.5 nm passivation layer show an substantial absolute improvement of 56 mV in open-circuit voltage (V_{OC}), 1 mA cm^{-2} in short-circuit current density (J_{SC}), and 2.6% in overall efficiency as compared to a reference (with the reference showing 8.5% under AM 1.5G).

1. Introduction

$Cu(In,Ga)(S,Se)_2$ solar cells of the chalcopyrite crystal structure have been one of the champions of thin-film technologies, with record laboratory efficiencies reaching 22.6%.[1] High power conversion efficiencies in crystalline silicon solar cells have been achieved through the invention of complex cell architectures such as PERC (passivated emitter and rear cell). Passivation of the top and rear surfaces and the formation of low resistance contacts cutting through these passivation layers, have been key aspects of high-efficiency silicon solar cell architectures. The 22.6% record efficiency in CIGS solar cells required a treatment of the top absorber surface with Rubidium fluoride (RbF). Positive effects have also been observed with sodium, potassium, and rubidium.[1,2] Collectively, they provide new evidence for the role of the CIGS/CdS interface as a limiting factor for high efficiencies. The goal of the work presented in this publication was to introduce a passivation layer between CIGS and CdS and to reduce recombination at this interface in a reproducible manner. An analysis has been presented for the potential of gallium oxide deposited by plasma-enhanced atomic

S. Garud
Helmholtz Zentrum Berlin
12489 Berlin, Germany

S. Garud, N. Gampa, Prof. J. Poortmans
Imec – Partner in Solliance
3000 Leuven, Belgium

S. Garud, Prof. A. Smets
Delft University of Technology
2628 CD, Delft, The Netherlands

Dr. T. G. Allen
Australian National University
Canberra ACT 0200, Australia

KAUST Solar Center
King Abdullah University of Science and Technology
Thuwal 23955-6900, Saudi Arabia

Dr. R. Kotipalli, Prof. D. Flandre
Université catholique de Louvain
ICTEAM Institute
1348 Louvain-la-Neuve, Belgium

Dr. M. Batuk, Prof. J. Hadermann
University of Antwerp
Groenenborger Groenenborgerlaan 171
2020 Antwerp, Belgium

Prof. J. Poortmans
Department of Electrical Engineering (ESAT)
KU Leuven
3001 Leuven, Belgium

Dr. M. Meuris, Prof. B. Vermang
Imec Division IMOMEC – Partner in Solliance
3590 Hasselt, Belgium
E-mail: bart.vermang@uhasselt.be

Dr. M, Meurius
Institute for Material Research (IMO) Hasselt University
3590 Hasselt, Belgium

Prof. B. Vermang
Faculty of Engineering Technology
Hasselt University
3590 Hasselt, Belgium

The ORCID identification number(s) for the author(s) of this article can be found under https://doi.org/10.1002/pssa.201700826.

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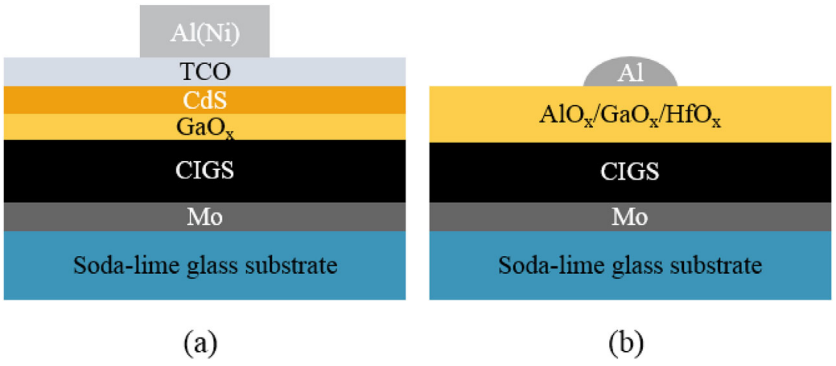


Figure 1. Schematics of the solar cell architecture with the gallium oxide passivation layer shown between CIGS and CdS (a) and Metal-insulator-semiconductor structure used for capacitance-voltage measurements (b) (not to scale).

layer deposition, as a passivation layer at the CIGS-CdS interface. A schematic of the cell architecture is shown in **Figure 1**a.

Passivation layers can reduce recombination at a surface and lead to an improvement in open-circuit voltage (V_{OC}) as well as better charge collection (visible in *EQE* and J_{SC}).[3–5] This can be due to a "chemical passivation" which reduces dangling bonds and active interface defects. It may also be due to a "field-effect passivation" which can, based on the polarity of charges in the region, either repel minority charge carriers and reduce recombination or repel majority carriers sufficiently to cause an inversion at the surface.[6,7]

Al_2O_3 passivation layers have been recently demonstrated on CIGS solar cells between the CIGS-Mo back contact interface.[8,9] At the front interface, CIGS solar cells have often featured buffer layers between the TCO and CIGS absorber. CdS is most commonly used for the band-alignment at this interface. Another layer such as i-ZnO is used on top of CdS to reduce shunts and maintain electrical homogeneity. However, CdS creates parasitic absorption below 550 nm wavelength of irradiation and Cd is well-known for its toxicity. Koida et al., have recently investigated a-$In_{2-2x}Ga_{2x}O_3$ as suitable buffer layers with $x = 0.9$ and $x = 1$ giving the most promising results.[10] The V_{OC} values obtained were comparable to the reference V_{OC} with a i-ZnO/CdS buffer layer, but the FF values were lower. These effects were primarily attributed to a positive conduction band offset which also led to the formation of a secondary barrier and reducing charge collection in forward bias voltages. The height of such a barrier can be reduced by decreasing the thickness of the buffer layer or by increasing the n-type doping in it. Hence, a-GaO_x with thicknesses from 80 to 10 nm were attempted with RF sputtering, but incomplete coverage lead to decreased shunt resistance. More recently, Heinemann et al., tested 10 to 5 nm layers of a-GaO_x with pulsed laser deposition on CIGS absorbers in superstrate configuration.[11]

In this aspect, Atomic Layer Deposition (ALD) can provide a unique step forward as it has been proven to be a highly conformal, soft method of deposition for ultra-thin layers.[12] This is also important due to the rough layer of CIGSe in this work. Furthermore, ultra-thin layers of oxides are required for limiting their contribution to series resistance. Typically, relatively high temperatures are required for ALD growth, such as 150 °C for aluminium oxide and 250 °C for hafnium oxide used in this study. They can introduce unintentional thermal annealing of CIGS absorbers. In this regard, plasma-enhanced atomic layer deposition (PE-ALD) is a particularly advantageous technique since it enables a low deposition temperature (75 °C in this work).[13]

2. Experimental Section

Copper, gallium, and indium were co-evaporated on soda lime glass/molybdenum substrates with temperatures of around 1350, 1040, and 1000 °C, respectively, with the substrates heated to 550 °C. The CIGS layer was verified by X-ray fluorescence (XRF) to be 1.7 μm thick. No gallium grading was used and the ratio of copper to gallium and indium (*CGI*) was approximately 80% and the ratio of gallium to gallium and indium (*GGI*) was 30%. All samples were deposited in the same co-evaporation run with very good uniformity.

The substrates were then heated in an annealing step for 15 min at 460 °C with 200 sccm of 10% H_2Se gas diluted in N_2 to create Cu(In,Ga)Se_2. In order to ensure that the CIGS surface was oxide free for the ALD deposition, all substrates (including the reference) were subjected to an etch by 30% KCN solution for 1 min. The samples were then sealed in vacuum until the ALD stage.

GaO_x was deposited via plasma-enhanced ALD at a low temperature of 75 °C and growth rate of 0.07 nm/cycle with trimethylgallium (TMGa) and oxygen plasma as precursors. Its optical bandgap is expected to be ≈4.6 eV as observed by ellipsometry in a previous work.[13] This is much higher than the CdS bandgap of 2.4–2.5 eV which causes parasitic absorption.[14] A metal-insulator-semiconductor (MIS) structure such as in Figure 1b was created with a gallium oxide layer from 256 cycles of ALD. This created approximately 20 nm of gallium oxide as evidenced in transmission electron microscopy (TEM) (Figure S1, Supporting Information). Completed solar cells were created from ultra-thin layers with namely 4, 8, 32, and 64 cycles leading to estimated maximum thicknesses of 0.3, 0.6, 2.3, and 4.5 nm of gallium oxide. All the plasma-enhanced atomic layer depositions were carried out at the Australian National University in Canberra. In other test samples, aluminium oxide was deposited via thermal ALD with trimethylaluminium (TMA) (pulse time: 0.016 ms, purge time: 40 s) and water (pulse time: 0.03 ms, purge time: 20 s) as precursors at a temperature of 150 °C. A linear growth rate of 0.12 nm/cycle was achieved. Hafnium oxide was similarly deposited via thermal ALD with Tetrakis(ethylmethylamino)hafnium (TEMAH) (pulse time: 0.1 ms, purge time: 35 s) and water (pulse time: 0.01 ms, purge time: 30 s) as precursors at a temperature of 250 °C leading to a linear growth rate of 0.11 nm/cycle.

The substrates were then subjected to chemical-bath deposition of CdS (≈50 nm), sputtering of 100 nm intrinsic ZnO and 400 nm Al-doped ZnO (total sheet resistance of 50 ohm) and e-beam deposition of Ni/Al/Ni front grids. Two to five cells of 0.5 cm^2 area were mechanically scribed on each substrate.

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2.1. Capacitance-Voltage Measurements

An MIS structure was first created to assess aluminium oxide (29 nm), gallium oxide (20 nm), and hafnium oxide (20 nm) as passivation layers grown by ALD. A schematic of the structure is shown in Figure 1b. Capacitance-voltage measurements were made in order to study the density of charges in the oxide layers and the interface trap density. The former was calculated from the flat-band condition. In order to maintain voltage stability of measurements, un-analyzed devices were measured in a single sweep under the same temperature and dark conditions. This would exclude any voltage dependent-hysteresis. The normalized capacitance voltage measurements of the three devices at 100 kHz are shown in **Figure 2**. They indicate flat-band voltages as summarized in **Table 1**.

The flat-band voltages can be attributed to a density of charges present in the oxide, which can be calculated with the following equation:[15]

$$Q_{eff} = C_{\mathrm{ox}} \frac{\Phi_{\mathrm{ms}} - V_{\mathrm{fb}}}{e} \tag{1}$$

Here Q_{eff} is the effective charge density in cm^{-2}, C_{ox} is the oxide capacitance in $\mathrm{F\,cm}^{-2}$, e is elementary charge in coulombs and ϕ_{ms} is the work-function difference between the Al metal contact and the CIGS semiconductor. C_{ox} was calculated using the oxide thicknesses mentioned earlier (verified with TEM in the case of GaO_x) and estimated dielectric constants of 7.6 for AlO_x,[16] 9.2 for GaO_x,[17] and 18.7 for HfO_x.[18] It can be noted here that while the dielectric constant of these oxides can slightly vary based on the substrate layer and deposition process, they would not change the order of magnitude of the effective charge density (Q_{eff}). The work function difference (ϕ_{ms}) was calculated using the following equations:[15]

$$\Phi_{\mathrm{ms}} = \Phi_{\mathrm{m}} - \left(\chi + \frac{E_g}{2} + \Phi_{\mathrm{fp}}\right) \tag{2}$$

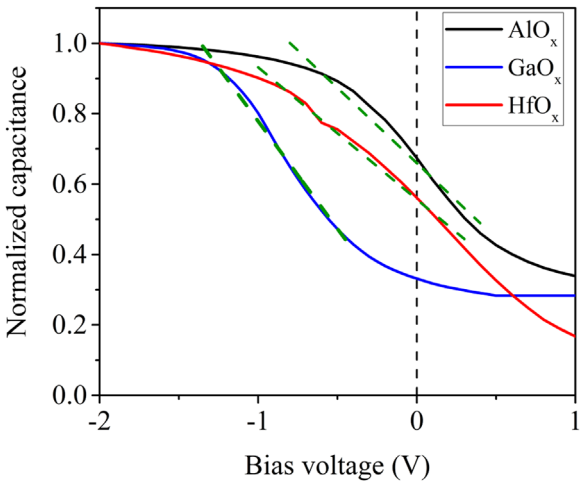


Figure 2. Normalized capacitance-voltage curves at 100 kHz for MIS structures with AlO_x, GaO_x, and HfO_x.

Table 1. Flat-band voltage calculated from *C-V* measurement.

Oxide layer	Flat-band voltage (V_{fb}) (V)	Oxide capacitance (C_{ox}) ($\mathrm{F\,cm}^{-2}$)	Charge density (Q_{eff}) (cm^{-2}) with $\chi_{CIGS} = 3.9$ eV	Charge density (Q_{eff}) (cm^{-2}) with $\chi_{CIGS} = 4.2$ eV	Charge density (Q_{eff}) (cm^{-2}) with $\chi_{CIGS} = 4.5$ eV
AlO_x	−0.5	2.7×10^{-7}	-2.0×10^{11}	-6.4×10^{11}	-1.1×10^{12}
GaO_x	−1.2	4.1×10^{-7}	1.4×10^{12}	5.8×10^{11}	-1.8×10^{11}
HfO_x	−1	8.3×10^{-7}	1.3×10^{12}	-2.1×10^{11}	-1.76×10^{12}

$$\Phi_{\mathrm{fp}} = V_t \ln \frac{N_a}{n_i} \tag{3}$$

$$n_i = \sqrt{N_C N_V e^{-E_g/\mathrm{kT}}} \tag{4}$$

Here, ϕ_m is the work-function of metal aluminium with an average of 4.17 eV.[19] E_g is the bandgap of CIGS (1.15 eV), and χ is electron affinity which was taken to be in the range of 3.9–4.5 eV.[20] ϕ_{fp} was calculated for an acceptor concentration of $N_a = 5 \times 10^{15}\,\mathrm{cm}^{-3}$ and intrinsic carrier concentration (n_i) of $7 \times 10^8\,\mathrm{cm}^{-3}$. n_i was calculated from conduction-band density of states ($N_C = 7 \times 10^{17}\,\mathrm{cm}^{-3}$) and valence-band density of states ($N_V = 1.5 \times 10^{19}\,\mathrm{cm}^{-3}$) and k being the Boltzmann constant.[7,20]

For the range of CIGS electron affinity (χ) of 3.9–4.5 eV, charge densities (Q_{eff}) were calculated as shown in Table 1. In the case of GaO_x, Q_{eff} is positive with a values in the range of $1.4 \times 10^{12}\,\mathrm{cm}^{-2}$ to $5.8 \times 10^{11}\,\mathrm{cm}^{-2}$ in case of $\chi = 3.9$–4.4 eV or weakly negative if CIGS is assumed to have a higher electron affinity. Since the doping levels in CIGSe material of these experiments are comparatively low ($10^{15}\,\mathrm{cm}^{-3}$), an oxide with positive charge could form a depletion layer and improve charge collection at the front CIGS-CdS interface. This effect has been theoretically studied by Sozzi et al.[6] and Bercegol et al.[7] In contrast, AlO_x shows high negative charge densities between -2×10^{11} to -1×10^{12} which is consistent with previous observations.[9]

A quantitative assessment of the D_{it} at the oxide-semiconductor interface has not been yet achieved due to the difficulty in conductance measurements at room temperature on these devices. (i.e., no parallel conductance peaks were detected). Nevertheless, we assume that low temperature measurements on these devices could provide more insights on the defect-state densities and distributions within the bandgap, such as in a previous work with AlO_x.[9]

In order to provide at least a qualitative assessment of D_{it}, the slope of the graphs in Figure 2 have been highlighted as dashed lines. According to the Terman method, *C-V* curves of a MIS capacitor can be interpreted as surface potential (ϕ_s) vs gate voltage curves, which contain information on the interface trap density. Surface potential fluctuations due to presence of interface states will therefore induce a spread in the *C-V* curves (especially in the depletion regime) as noticed in Figure 2. Gallium oxide clearly shows the most negative slope or in other words, the least D_{it} among these three samples.

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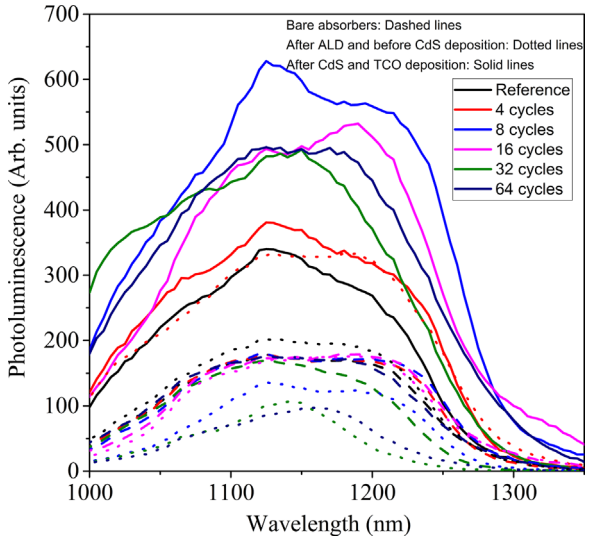


Figure 3. Photoluminescence measurements show the similarity between as-deposited absorbers (dashed lines) and differences in the completed cells (solid lines) possibly arising from GaO_x deposition.

With these encouraging results, solar cells were processed with varying thicknesses of gallium oxide deposited by the low temperature (75 °C) plasma-enhanced ALD on the CIGSe layer. The actual thickness of the gallium oxide layers on CIGSe after deposition and after CdS chemical bath deposition, are as yet, not verifiable as thicknesses less than 1 nm on such a rough CIGS surface were difficult to detect even with TEM. Nevertheless, all the solar cells were processed together in a stable process line and some differences in photoluminescence and electrical characterization are clearly visible and discussed in the following sections. Minimum temperatures of 127–300 °C are typically required to observe significant thermal annealing effects and hence, we expect 75 °C to not have any such impact.[21–24]

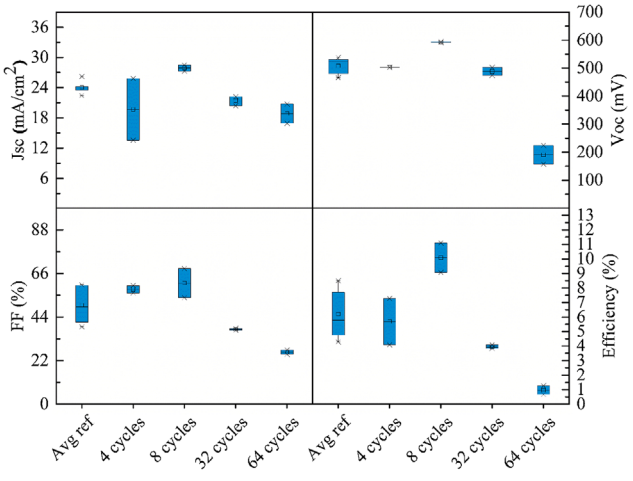


Figure 5. Electrical parameters of completed solar cells (2–5 cells in each case) show optimal values with 8 cycles of ALD.

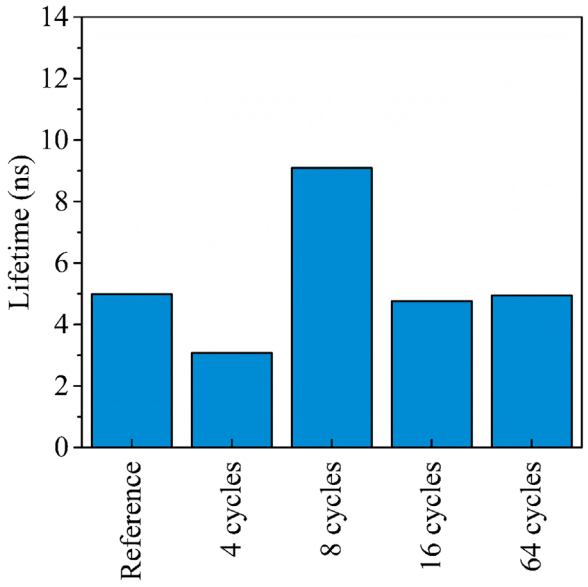


Figure 4. Higher charge carrier lifetime was observed with 8 cycles of ALD as compared to the reference and other samples.

2.2. Photoluminescence

The passivation layers have a significant effect on photoluminescence (*PL*) and carrier lifetime. In **Figure 3**, *PL* measurements show that all cells were equivalent when the absorber layers were created (dashed lines). In the stage after a KCN etch, after the deposition of gallium oxide and before CdS deposition, no significant differences are visible except for the sample with 4 cycles of ALD (dotted lines). The formation of a p-n junction by the deposition of CdS and TCO seems to be necessary to see a higher photoluminescence response and differences between cells (solid lines). This is visible in the reference cell. However, a further increase in response was

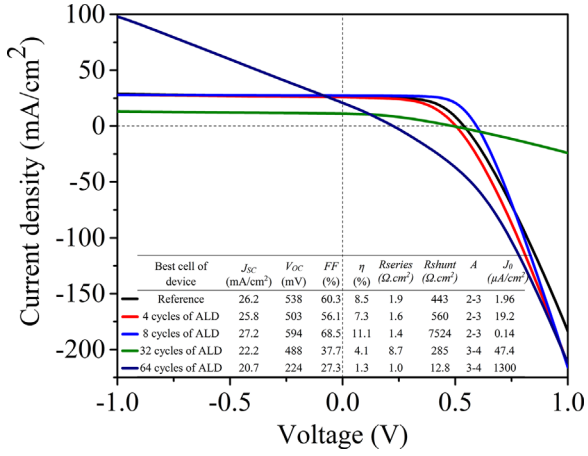


Figure 6. *J-V* curves of the best cells from each device show the reduction in recombination and increased shunt resistance with 8 cycles of ALD as compared to the reference. An increase in series resistance is visible with 32 cycles of ALD. A one-diode model was used for analysis according to the methods by Hegedus et al.[21]

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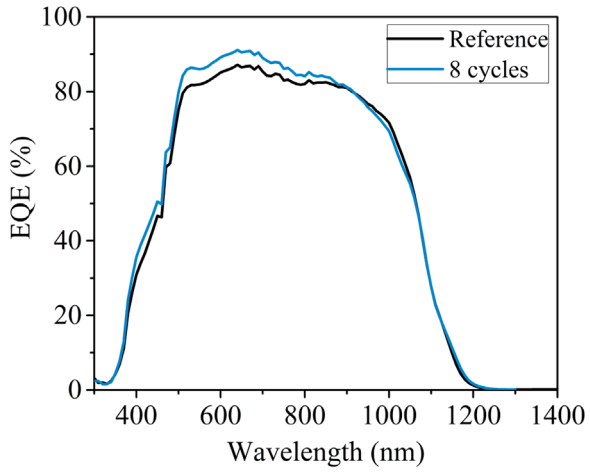


Figure 7. *EQE* of the cell with 8 cycles of ALD was observed to be better than that of the reference cell at the shorter wavelengths (500–800 nm).

recorded for the cells with passivation layers starting from 4 cycles to 64 cycles. The highest response was recorded for the cell with 8 cycles of ALD.

An increase in carrier lifetime was also observed with 8 ALD cycles; up to 9 ns as compared to 3 ns in the reference and other samples (**Figure 4**). A 2nd order exponential fitting was used for the time-resolved photoluminescence (TRPL) with the equation $I_{PL}(t) = C_1 e^{-t/\tau 1} + C_2\, e^{-t/\tau 2}$ (Figure S2 and Table S1, Supporting Information). The value of τ_2 has been used as an indication of charge carrier lifetime.

These improvements indicate that the GaO_x layers are able to passivate charge carrier traps on the top surface which otherwise act as recombination centers.

2.3. Electrical Performance Parameters

Next, the electrical parameters were characterized. The reduction in recombination is visible in V_{OC} as shown in **Figure 5**. It shows a clear increasing trend up to an optimum 8 cycles of ALD. The box plots were created with values from 2 to 5 cells in each case. *J-V* curves of the best cells from each device are shown in **Figure 6**. A one-diode model was used for analysis based on the methods by Hegedus et al., and the results are shown in the inset of Figure 6.[25] The calculated dark saturation current (J_0) correlates well with the V_{OC}, which are indicators of the total recombination in the cells. In the case of the cell with 8 cycles of ALD, good shunt resistance is also observed as a contributor to V_{OC}. The series resistance was higher when 32 cycles of ALD were used. In the sample with 64 cycles of ALD, shunting was observed which may have been caused due to unavoidable physical damage to the sample. This data is nevertheless, included for completeness as its behavior in forward bias is similar to those of the other cells (Figure 6). With all these factors combined, an increasing trend in cell efficiency is observed with up to 8 cycles of ALD (Figure 5) with an absolute increase of 2.6% in efficiency, 1.04 mA cm^{-2} in J_{SC}, 56.3 mV in V_{OC} and 8.22% in *FF* as compared to the reference. One reason for the improved J_{SC} was observed in the *EQE* (**Figure 7**) wherein better response was observed primarily at shorter wavelengths (500–800 nm).

3. Conclusion

An effective passivation layer can significantly reduce surface recombination and also increase reproducibility in solar cells via a reliable processing step. In addition, plasma-enhanced ALD has showcased a low-temperature of deposition (75 °C) which avoids undesirable annealing effects. ALD growth is currently the most suitable choice for thin-layers of conformal growth on even rough surfaces of photovoltaic materials.

This work presents gallium oxide deposited via Plasma-enhanced ALD as a potential passivation layer for CIGSe. Capacitance-voltage measurements on MIS structures have shown gallium oxide to likely have positive charge densities around 1.4×10^{12} to 5.8×10^{11} cm^{-2} and low D_{it} as compared to aluminium oxide and hafnium oxide. Improved photoluminescence response was observed with the inclusion of gallium oxide in the cell architecture.

In the case of preliminary solar cell results, it is as yet unclear if ultra-thin layers (<2 nm) can survive the chemical bath deposition of CdS. Nevertheless, since gallium oxide showcased passivation effects in the *C-V* and photoluminescence studies, solar cells were fabricated along with a reference in a stable process line. The electrical characterization of these cells did indeed show an absolute increase of 2.6% in efficiency originating from a substantial increase of 56.3 mV in V_{OC}, 1.04 mA cm^{-2} in J_{SC}, and 8.22% in *FF* with a gallium oxide layer as compared to the reference. Therefore as an outlook, future experiments can focus on alternative buffer layers or deposition techniques, point contact openings through thick gallium oxide layers (such as those simulated by Sozzi et al.[6] and Bercegol et al.,[7]) and also low-temperature conductance measurements on MIS structures to quantify D_{it}.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

CIGS solar cells, gallium oxide, plasma-enhanced atomic layer deposition, surface passivation

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