2023 Symposium on Design, Test, Integration & Packaging of MEMS and MOEMS

Effect of Silicon Substrate Resistivity on Large-Area High-Voltage Spiral Inductor Performance

Najeh Zeidi
SMALL Research Group, ICTEAM Institute, Université catholique de Louvain, Belgium
SI2E Laboratory, École nationnale d'ingénieurs de Sfax, Université de Sfax, Tunisia
najeh.zeidi@uclouvain.be

Martin Rack
ICTEAM Institute, Université catholique de Louvain, Belgium
martin.rack@uclouvain.be

Nicolas André
SMALL Research Group, ICTEAM Institute, Université catholique de Louvain, Belgium
nicolas.andre@uclouvain.be

Fares Tounsi
SMALL Research Group, ICTEAM Institute, Université catholique de Louvain, Belgium
SI2E Laboratory, École nationnale d'ingénieurs de Sfax, Université de Sfax, Tunisia
fares.tounsi@uclouvain.be

Jean-Pierre Raskin
ICTEAM Institute, Université catholique de Louvain, Belgium
jean-pierre.raskin@uclouvain.be

Denis Flandre
SMALL Research Group, ICTEAM Institute, Université catholique de Louvain, Belgium
denis.flandre@uclouvain.be

2023 Symposium on Design, Test, Integration & Packaging of MEMS/MOEMS (DTIP) | 979-8-3503-4131-7/23/$31.00 ©2023 IEEE | DOI: 10.1109/DTIP58682.2023.10267935

***Abstract*—In this work, we compare the performance of a large square spiral inductor with an area of 1.08×1.08 mm^2 and an operating frequency of a few hundred MHz, integrated atop four different types of silicon substrates. Measured and simulated results show that the high-resistivity (HR) substrate with a trap-rich (TR) layer yields significantly better performance in terms of quality factor, resonant frequency, self-inductance, and substrate capacitance than the HR or standard Si ones. These results approach those simulated for the same structure suspended on a MEMS membrane. Moreover, the inductor characteristics exhibit good stability under a back-contact voltage varying between -100 V and +100 V in the HR-TR case.**

Keywords—planar spiral inductor, high resistivity silicon substrate, trap-rich, high voltage, MEMS suspended inductor.

I. Introduction

Inductors are key elements in many electronic circuits and systems, especially in power electronics, digital isolators, RF-MEMS, bio-MEMS, or sensors [1]. Many approaches have been studied to increase the performance of integrated inductors, notably the quality factor and resonant frequency, such as optimizing the inductor dimensions or topology (shunted metal layers, multilevel, tapered, or symmetric inductors), using glass substrates, or suspending the inductor on a MEMS membrane [2][3]. Silicon (Si) substrate losses do indeed adversely affect inductor performance. They can be reduced using a metal-patterned ground shield (PGS) or high-resistivity (HR) Si substrates (i.e., with a resistivity $\rho > 1$ kΩ cm). The latter have become attractive for RF-integrated active and passive components as planar inductors due to their affordable cost, CMOS compatibility, and high performance compared to standard-resistivity (Std) Si substrates (i.e., $\rho \approx 10$–20 Ω cm) [4]. However, a parasitic surface conduction (PSC) effect definitely occurs at the interface between the Si dioxide insulating layer and the HR Si substrate due to oxide and interface defects created during the microfabrication process or the application of a large DC bias between the top components and the back substrate contact [5]. Either can attract free carriers at the HR-Si/oxide interface, thereby reducing the substrate's effective resistivity and leading to a highly conductive layer beneath the passive component. The PSC has an adverse impact on device performances, including RF losses, substrate crosstalk, and nonlinearities [6]. One technique to eliminate the PSC is to introduce a very thin material layer, typically polysilicon, rich in defects (i.e., electrically active traps) between the oxide layer and the HR substrate. Trap-rich (TR) substrates with a resistivity of up to 10 kΩ cm will be assessed in this work to fabricate a large-area integrated spiral inductor for the first time to our knowledge. Measured performances on the three different substrates (Std-Si, HR-Si, and HR-Si+TR) are compared with a simulated identical MEMS suspended structure used as a reference to assess the effect of the substrate on the performance. Compared with previous works, mostly focused on RF inductors of a few nH with areas of about 0.1 mm^2 or less, having operation frequencies above GHz [3][4], we investigate here the case of a large-area inductor of about 90 nH, targeting MEMS sensors or integrated power electronics, operating at a few hundreds of MHz and a DC back bias of up to ± 100 V.

II. Layout and Fabrication Process

The geometric parameters characterizing the assessed square spiral inductor are the number of turns N, the track width *w*, the spacing between turns *s*, the inner diameter *d*, the outer diameter *D*, and the track thickness *t*, whose values are given in Table I. The structure is fabricated on three different 380 µm-thick Si substrates (Fig. 1): *(i)* a Std-Si with ρ equal to 15 Ω cm, *(ii)* an HR-Si with ρ = 4 kΩ cm, and *(iii)* an HR-Si with an additional polysilicon trap-rich layer. In the two former cases, the Si dioxide layer has been thermally grown in a wet atmosphere at 1000°C. In the latter, a 500-nm-thick undoped polysilicon layer has been sandwiched between the HR substrate and the insulating 400 nm PECVD SiO_2 layer.

In the microfabrication process, a total of four photolithography steps are used. Firstly, an 800 nm-thick Al metal layer ($\rho = 3.2\ 10^{-8}$ Ω m) is sputtered by e-beam at 250°C and then patterned as an underpass. Next, a 500 nm-thick PECVD SiO_2 ($\varepsilon_r = 3.9$) is deposited as a dielectric between the underpass and the spiral and patterned using BHF (buffered hydrofluoric acid) to create the vias. Thirdly, the spiral shape, RF access pads, and surrounding ground planes are realized with the same metal deposition as the underpass. Finally, a top tensile 500 nm-thick PECVD Si_3N_4 is deposited to balance the SiO_2 layer compressive stress and passivate the chip, and is patterned to open the RF access pads.

TABLE II. THE EVALUATED SQUARE SPIRAL INDUCTOR DIMENSIONS.

Parameter	*N*	*w (µm)*	*s (µm)*	*d (µm)*	*D (µm)*	*t (µm)*
Value	10.5	23	12	335	1080	0.8

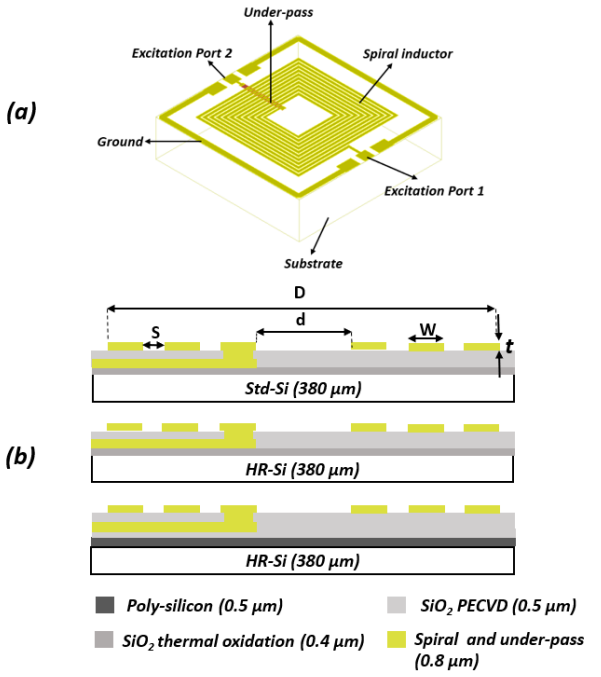

Fig. 1. The large spiral inductor: (a) simulated structure in ADS, and (b) cross-section view atop the three different Si substrates.

III. RESULTS AND DISCUSSION

The inductor was characterized on-wafer using a pair of ground-signal-ground (GSG) probes and an N5242B Keysight 26.5 GHz PNA-X vector network analyzer at room temperature. First of all, a short-open-load-thru (SOLT) calibration is performed to define the measurement reference planes at the probe tips over the frequency range 10 MHz–10 GHz. The measured S-parameters are converted into Y-parameters, and the pad surrounding parasitics are removed through an open-short de-embedding method [7].

A. Extraction methodology

Std-Si on-chip spiral inductors can be described by a lumped-element model thanks to their small dimensions relative to the wavelengths of interest. These elements are approximately derivable from basic physics, which allows us to better describe the involved phenomena. In the high-frequency range, a π-equivalent electrical model composed of three complex admittances, Y_a, Y_b, and Y_c, is fairly accurate (Fig. 2). The relations between these admittances and the measured Y-parameters of the π-network are expressed as:

$$[Y] = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} = \begin{bmatrix} Y_a + Y_b & -Y_b \\ -Y_b & Y_b + Y_c \end{bmatrix} \quad (1)$$

Hence, the equations used to extract all model lumped elements could be given by the detailed equations in Fig. 2 [8]. To extract the parasitic elements of the Y_c branch modeling the substrate losses (i.e., C_{ox2}, C_{si2}, and R_{si2}), we need to substitute $(Y_{11} + Y_{12})$ by $(Y_{22} + Y_{21})$ in the equations of Fig. 2. The inductor was also simulated using the ADS (Advanced Design System) software on the three considered substrates, and the results are compared with the measurements.

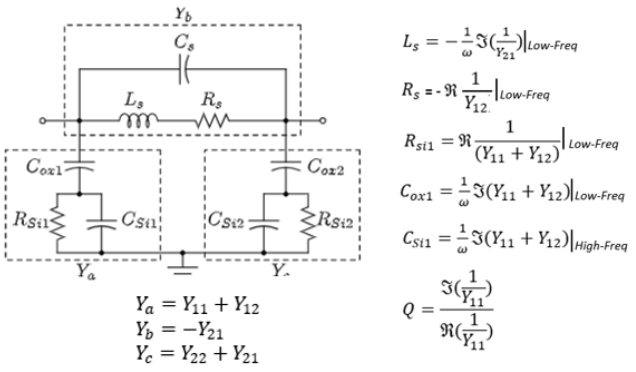

Fig. 2. Lumped-element equivalent electrical circuit of the Std-Si on-chip integrated inductor (left) and extraction equations (right) [8].

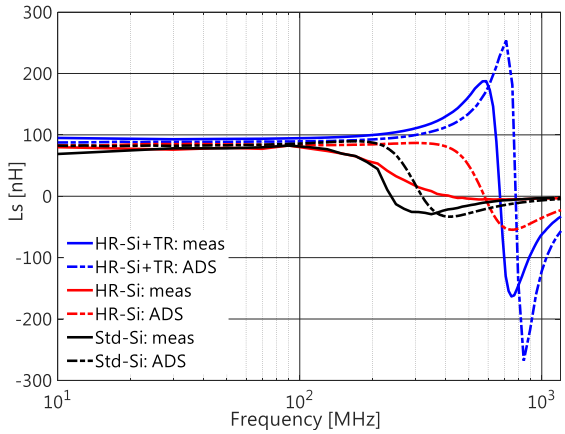

Fig. 3. Self-inductance simulated and measured results versus frequency for the 3 substrate cases.

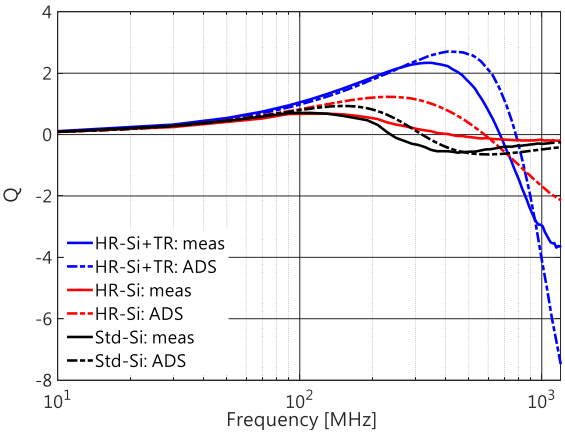

Fig. 4. Quality-factor simulated and measured results versus frequency for the 3 substrate cases.

B. Analysis of the inductor performances

Measured and simulated results confirm that the inductor DC resistance remains constant (~54.18 Ω) and independent of the substrate resistivity. The self-inductance (L_s) is defined as the ratio between the magnetic flux generated by the coil and the current passing through it. When the magnetic flux induced by the coil penetrates a conductive substrate, an eddy current, opposite in direction to the current in the winding above, can be generated inside the substrate [9]. This generates counter-active magnetic flux, reducing the original flux in the coil and thus causing the inductor to degrade. The lower the resistivity of the substrate, the easier

TABLE II. MEASURED AND SIMULATED PERFORMANCES OF THE INDUCTANCE ON THE 3 TYPES OF SUBSTRATE COMPARED TO THE SIMULATED REFERENCE MEMS SUSPENDED ONE.

	L_s (nH)		f_{res} (MHz)		Q-factor		C_{Ya} @800 MHz (pF)	
	Meas	*Simu*	*Meas*	*Simu*	*Meas*	*Simu*	*Meas*	*Simu*
Standard	80.9	82.4	230	310	0.68 @ 140 MHz	0.92 @ 160 MHz	0.83	0.98
HR	79.8	82.87	450	570	0.70 @ 180 MHz	1.22 @ 330 MHz	0.44	0.44
HR + TR	94.5	87.6	670	780	2.35 @ 350 MHz	2.67 @ 452 MHz	0.24	0.22
Suspended	-	94.9	-	1030	-	3.92 @ 650 MHz	-	

the image current can flow, leading to more unwanted power dissipation and degrading the performance. Moreover, larger inductors have magnetic fields that penetrate deeper into the substrate and suffer from higher substrate losses. Using HR substrates or a post-process micromachining step to etch the substrate underneath the inductor substantially minimizes these effects. As we will discuss later, resistive coupling in the substrate can then dominate the substrate losses. As a result, the inductance value decreases proportionally to the substrate resistivity and related losses.

Accordingly, the HR-Si+TR substrate gives the highest L_s of about ~87 nH (@10 MHz), as shown in Fig. 3 for simulations and measurements in Table II. From the results of Table II, it can be argued that the most prominent result of a large-side and multi-turn on-chip inductor is an increase in the self-inductance with a decrease in the resonant frequency compared to more usual smaller structures. That is a drawback for RF high-frequency applications but could be advantageous in lower frequency MEMS applications [10].

Energy losses from induced currents in the semi-conducting substrate were also found to be significant, along with the series trace resistance of the thin metal layer. Hence, to rate the substrate effect losses on the inductor performance, we studied the parasitic substrate capacitance of the branch Y_a (i.e., that combining C_{si1} and C_{ox1}) by measurements and simulations. The results shown in Fig. 5 were extracted before and after the inductors resonance (i.e., between 10 and 1100 MHz). At low measuring frequencies, the equivalent capacitance of the substrate is the greatest in the case of standard and HR silicon substrates. Nevertheless, by increasing the substrate resistivity, i.e., reducing the doping or introducing the TR layer to eliminate the PSC effect, the substrate parasitic capacitance significantly decreases at 800 MHz from ~0.83 pF for the Std-Si substrate to ~0.44 pF for the HR-Si substrate and ~0.24 pF for the HR-Si+TR substrate, which makes it possible to increase the resonant frequency of the inductance and to improve its quality factor. Indeed, the PSC effect, resulting from the attraction of electrons by the fixed positive charges trapped in the buried oxide (BOX), which are generated during microfabrication, induces a highly conductive thin layer at the silicon–BOX interface. When the signal propagates through the inductor, a leakage current through the PSC layer is produced, so an additional resistor R_{psc} should be introduced to account for the PSC effect in the HR substrates (Fig. 6), resulting in additional transmission losses in the form of harmonic distortion and crosstalk [11]. Although the PSC reduces the effective resistivity of the bulk HR substrate by more than an order of magnitude compared to its nominal value, it still gives slightly better inductor performance than that of the Std-Si. The PSC effect is temperature-, process- and voltage-dependent and significantly reduces the expected RF performance of HR substrates.

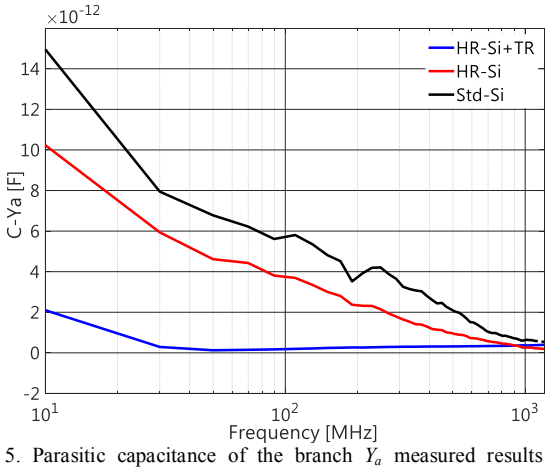

Fig. 5. Parasitic capacitance of the branch Y_a measured results versus frequency for the 3 substrate cases.

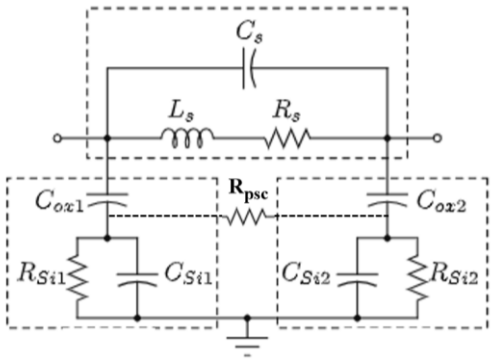

Fig. 6. Lumped-element equivalent electrical circuit of the HR-Si and HR-Si+TR on-chip inductor.

It has been proven that adding an undoped polysilicon layer, known as a trap-rich (TR) layer rich in defects, underneath the oxide layer can inhibit the PSC effect. The TR layer effectively pins free carriers, making the substrate virtually lossless. Consequently, with a sufficiently high resistivity layer, the nominal resistivity of the HR substrate is recovered, and crosstalk due to currents conducted through R_{psc} can be diminished to negligible values, increasing the overall inductor Q-factor. This is evidenced by the decay of C_{Ya} towards the low frequencies as shown in Fig. 5.

The quality factor (Q) of the inductor is defined as $2\pi f$ times the ratio between the peak stored and dissipated/lost energies per oscillation cycle. On-chip spiral inductors made on Std-Si substrates suffer from poor quality factors due to ohmic and substrate losses limiting the circuit's performance. In fact, with rising frequency, the metallic layer's resistance increases due to skin and proximity effects, while the substrate's losses rise as a result of induced currents and dielectric losses. By reducing both induced eddy currents in the substrate and dielectric losses, through HR substrates,

measured and simulated results confirm that the HR-Si+TR substrate provides a significantly higher Q-factor compared to HR-Si and Std-Si substrates in the range from 200 to 500 MHz (Fig. 4, Table II). The self-resonant frequency of the large inductor on Std-Si substrate is expressed as:

$$f_{res} = \frac{1}{2\pi}\sqrt{\frac{1}{L_S C_S} - \frac{R_S^2}{L_S^2}} \quad (2)$$

As observed, f_{res} is mainly a function of the series inductance and capacitance which both strongly depend on their environment, especially the used substrate. The HR-Si+TR substrate provides the highest resonance frequency, about 1.5 and 3 times higher than on HR-Si and Std-Si substrates, as their losses and parasitic coupling limit the maximum Q value and shift the resonant frequency to a lower value. It's worth noting that above the resonance frequency, where the Q (or L_s) curve crosses zero, the inductor behaves like a capacitor.

Next, the HR-Si+TR results are benchmarked by ADS simulation against the intrinsic performance of an identical inductor structure suspended on an oxide-based MEMS membrane, eliminating parasitic coupling and losses related to the substrate. That results in a further improvement in terms of quality factor and resonant frequency (Fig. 7). The maximum Q-factor of the suspended inductor is higher (3.92 at 650 MHz) than that of the HR-Si+TR substrate (2.67 at 452 MHz), while the resonant frequency increases from 784 MHz on Si-HR+TR to 1.03 GHz for the suspended structure. That represents a loss of performance of about 32% for the inductor on HR-Si+TR compared with an ideal suspended structure (with identical R_s), which can be attributed to silicon's higher relative permittivity (11.7) as compared to air (1.0), which impacts the overall value of C_s. As a conclusion, we can confirm that HR-Si + TR represent a good alternative to MEMS inductors considering the process cost and the microfabrication complication.

Finally, the inductor characteristics are analyzed when varying the back-contact voltage from -100 V to +100 V. This range is chosen to prevent the breakdown of the silicon dioxide, whose theoretical value is about 500 V/µm. The measured results show that the quality factor, the self-inductance, and the resonant frequency are rather insensitive over this range, validating that the inductor performance remains stable on the HR-Si+TR substrate and acceptable for high-voltage applications, contrary to the other substrate cases.

IV. Conclusion

In this work, the performance of a large-area integrated spiral inductor is studied as a function of the Si substrate resistivity, including losses and coupling in the substrate. Measured and simulated results demonstrate that the high-resistivity substrate with surface passivation by a trap-rich layer is the best choice, significantly over conventional standard-resistivity Si or non-passivated high-resistivity Si, in terms of self-inductance, quality factor, resonance frequency, and parasitic capacitance. Performances remain stable over a range of +/- 100 V applied between the top inductor and back contact and approach the simulated results of an ideally suspended MEMS structure by approximately 30%, at a potentially lower processing cost and better CMOS compatibility.

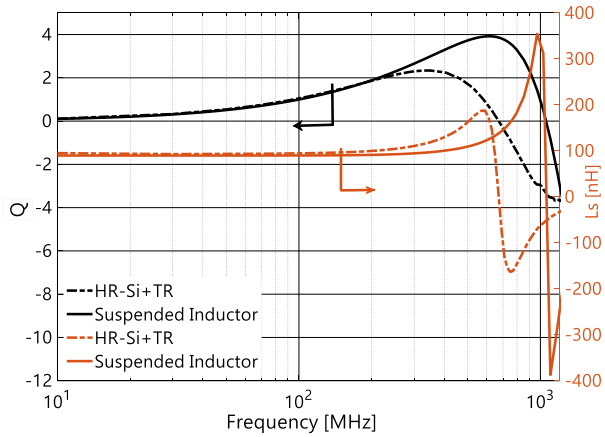

Fig. 7. L_s and Q vs frequency simulations of identical suspended MEMS inductor and integrated inductor on HR-Si+TR substrate.

References

[1] N. Zeidi, S. Kaziz, M. H. Said, L. Rufer, A. Cavallini, and F. Tounsi, 'Partial discharge detection with on-chip spiral inductor as a loop antenna', *Review of Scientific Instruments*, vol. 92, no. 9, p. 094701, Sep. 2021.

[2] Y.-S. Choi and J.-B. Yoon, 'Experimental analysis of the effect of metal thickness on the quality factor in integrated spiral inductors for RF ICs', *IEEE Electron Device Letters*, vol. 25, no. 2, pp. 76–79, Feb. 2004.

[3] H. Sun, Z. Liu, J. Zhao, L. Wang, and J. Zhu, 'The Enhancement of Q-Factor of Planar Spiral Inductor With Low-Temperature Annealing', *IEEE Transactions on Electron Devices*, vol. 55, no. 3, pp. 931–936, Mar. 2008.

[4] S. Liu, L. Zhu, F. Allibert, I. Radu, X. Zhu, and Y. Lu, 'Physical Models of Planar Spiral Inductor Integrated on the High-Resistivity and Trap-Rich Silicon-on-Insulator Substrates', *IEEE Transactions on Electron Devices*, vol. 64, no. 7, pp. 2775–2781, Jul. 2017.

[5] K. B. Ali, C. R. Neve, Y. Shim, M. Rais-Zadeh, and J.-P. Raskin, 'Non-linear characteristics of passive elements on trap-rich high-resistivity Si substrates', in *2014 IEEE 14th Topical Meeting on Silicon Monolithic Integrated Circuits in Rf Systems*, pp. 4–6, Jan. 2014.

[6] C. Roda Neve and J.-P. Raskin, 'RF Harmonic Distortion of CPW Lines on HR-Si and Trap-Rich HR-Si Substrates', *IEEE Transactions on Electron Devices*, vol. 59, no. 4, pp. 924–932, Apr. 2012.

[7] T. Yammouch, K. Okada, and K. Masu, 'Physical Modeling of MEMS Variable Inductor', *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 55, no. 5, pp. 419–422, May 2008.

[8] M. El Kaamouchi, P. Delatte, M. Si Moussa, J.-P. Raskin, and D. Vanhoenacker-Janvier, 'Temperature behavior of spiral inductors on high resistivity substrate in SOI CMOS technology', *Solid-State Electronics*, vol. 52, no. 12, pp. 1915–1923, Dec. 2008.

[9] T. Yammouch, K. Okada, and K. Masu, 'Physical Modeling of MEMS Variable Inductor', *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 55, no. 5, pp. 419–422, May 2008.

[10] F. Tounsi, L. Rufer, B. Mezghani, M. Masmoudi, and S. Mir, 'Highly flexible membrane systems for micromachined microphones - modeling and simulation', in *2009 3rd International Conference on Signals, Circuits and Systems (SCS)*, pp. 1–6, Nov. 2009.

[11] S. Liu, L. Zhu, F. Allibert, I. Radu, X. Zhu, and Y. Lu, 'Physical Models of Planar Spiral Inductor Integrated on the High-Resistivity and Trap-Rich Silicon-on-Insulator Substrates', *IEEE Transactions on Electron Devices*, vol. 64, no. 7, pp. 2775–2781, Jul. 2017.

FUNDING ACKNOWLEDGEMENT

This work was carried out with support received from the European Union's Horizon 2020 research and innovation program under the Marie Skłodowska-Curie individual fellowship agreement No. 101030887.

CITATION AND KEYWORDS

N. Zeidi, M. Rack, N. André, J. -P. Raskin, F. Tounsi and D. Flandre, "Effect of Silicon Substrate Resistivity on Large-Area High Voltage Spiral Inductor Performance," 2023 Symposium on Design, Test, Integration & Packaging of MEMS/MOEMS (DTIP), Valetta, Malta, 2023, pp. 1-4, doi: 10.1109/DTIP58682.2023.10267935.

Keywords: {Planar spiral inductor, High resistivity silicon substrate, Trap-rich, High voltage, MEMS suspended inductor},