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Design of SOI CMOS Circuits Robust to Combined Effects of Process Corners Variation, High Temperature and Radiations

El Hafed Boufouss

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Dissertation committee:

Prof. **Denis Flandre** (UCL, Belgium), adviser

Prof. **Danielle Vanhoenacker-Janvier** (UCL, Belgium), President

Prof. **Laurent Francis** (UCL, Belgium)

Prof. **Zouhair Guennoun** (EMI, Morocco)

Dr. **Vincent Dessard** (Senior Analog Design Consultant, Belgium)

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*To my mother, to my father,
to the whole family,
and to my wife.*

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Abstract

THE design of integrated circuits robust to harsh environments is one of the most challenging issues to modern electronic systems. In the past, the radiation damaging effects were only considered for space applications, nuclear power and military needs. Today, radiation impacts concern a large field of applications, such as medical equipments, biomedical and aeronautic electronics. Furthermore, due to the space weather variability, the radiation disturbs more and more the higher performance digital electronics, even at sea level.

Another challenge facing electronic circuits is the increase in temperature requirements up to 175 °C in automotive, which will be increased in the future to over 200 °C such as for aerospace and oil exploration. However, the increase in temperature seriously degrades the functionality of electronic circuits.

The main objective of this thesis is to design electronic circuits which can sustain simultaneous radiation and high temperature effects in advanced CMOS technologies. Therefore, process variations also have to be taken into account simultaneously.

The first part of the thesis studies the combined effects of radiation and temperature on electronic devices and circuits developed in partially-depleted Silicon-on-Insulator (PD SOI) technologies. The choice of SOI is motivated by its attractive features: extended range of operating temperatures, lower sensitivity to transient radiation effects (SEE) compared to other technologies and high robustness to total ionizing dose (TID) effects when a thin gate/buried oxide is used.

The second part of the thesis proposes new mitigation techniques against process variations, radiation and temperature effects on analog circuits. These mitigation techniques are based on the negative feedback and the body biasing techniques.

List of Acronyms

AC	Alternating Current
ADC	Analog-to-Digital Converter
ASET	Analog Single-Event Transient
ASIC	Application Specific Integrated Circuit
AMU	Atomic Mass Units
BiCMOS	Bipolar-CMOS technology
CME	Coronal Mass Ejection
CMOS	Complementary Metal Oxide Semiconductor
DARE	Design Against Radiation Effects
DC	Direct Current
DMS	Defense Meteorological Satellite
DRAM	Dynamic Random-Access Memory
DRC	Design Rule checking
DUT	Device Under Test
EEPROM	Electrically Erasable Programmable Read-Only Memory
ELT	Enclosed Layout Transistor
ESA	European Space Agency
ESD	Electrostatic Discharge
eV	Electron-Volt
FD	Fully depleted
GCR	Galactic Cosmic Rays
GEO	Geostationary Earth Orbit (35,786 km above the Earth's equator)
GPS	Global Positioning Satellite
Gy	Gray unit
I/O	Input/Output

IC	Integrated Circuit
LabVIEW	Laboratory Virtual Instrument Engineering Workbench
LEO	Low Earth Orbit (2000 km)
LET	Linear Energy Transfer
LET_{th}	Linear Energy Transfer threshold
MBU	Multiple-Bit Upset
MCU	Multiple-Cell Upset
MEO	Medium Earth Orbit (between 2,000 km and 35,786 km)
MOS	Metal Oxide Semiconductor
MOSFET	Metal-Oxide Semiconductor Field-Effect Transistor
NMOS	N-channel Metal-Oxide Semiconductor
NPN	NPN Bipolar transistor
OPA	Operational Amplifier
OTA	Operational Trans-conductance Amplifier
pC	Pico-Coulombs
PD	Partially Depleted
PLL	Phase-Locked Loop
PMOS	P-channel Metal-Oxide Semiconductor
PNP	PNP Bipolar transistor
PNPN	PNPN thyristor
SEB	Single Event Burnout
SEE	Single Event Effect
SEFI	Single Event Functional Interrupt
SEGR	Single Event Gate Rupture
SEL	Single Event Latch-up
SET	Single Event Transient

SEU	Single Event Upset
SiC	Silicon Carbide
SOI	Silicon On Insulator
SRAM	Static Random-Access Memory
SPICE	Simulation Program with Integrated Circuit Emphasis
STI	Shallow Trench Isolation
Sv	Sievert unit
TCAD	Technology Computer Aided Design
TID	Total Ionizing Dose
TMR	Triple Modular Redundancy
TNID	Total Non Ionizing Dose
VCO	Voltage Controlled Oscillator
V_{DS}	Drain to source voltage
V_{GS}	Gate to source voltage
V_{th}	Threshold voltage
WL	Write Line
ZTC	Zero Temperature Coefficient

Author's Publication List

Journal papers

1. **E. Boufouss**, L. A. Francis, V. Kilchytska, P. Gérard, P. Simon and D. Flandre, "Ultra-low Power High Temperature and Radiation Hard CMOS SOI Voltage Reference", *Sensors Journal*, Dec 2013, pp. 17265-17280.
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CHAPTER 1

Introduction

NOWADAYS, one of the most challenging issues for modern electronic systems lies in the failures induced by radiation. In the past, these damaging effects appeared just for space applications, nuclear power and military needs. Today radiation impacts concern a large field of applications, such as medical equipments, biomedical and aeronautic electronics. For example, the radiation dose for a commercial airline flight can reach about $500 \mu\text{radSi}/\text{hour}$ [1]. Furthermore, due to the space weather variability, the radiation disturbs more and more the higher performance digital electronics, even at sea level [2, 3].

Thanks to the strong shielding used in aerospace applications, the maximum total ionizing dose (TID) requirements for electronic circuits is 300 krad(Si) . However, due to the weight limitation (for cost reduction) and the increase in components number in future spacecraft generations, the shielding will be reduced. Thereby, the required total ionized dose for electronic circuits will reach much higher doses (up to Mrad(Si)) [4, 5].

Another challenge facing electronic circuits is the increase in temperature requirements. Indeed, up to five years ago, the major electronic industry had required circuits robust up to merely 125°C . Today, the temperature needs reach 175°C due to the automotive market, and will increase in the future up to more than 200°C [6].

Furthermore, some electronic systems have to operate under the combined effect of high temperature and hard radiation doses, such as the robotic spacecraft used in space exploration missions (on Mars, or Venus), and also in nuclear power plants.

This thesis was launched in this context of increased demand for harsh environment electronics, robust up to a high total radiation dose and a high temperature. Therefore, the first objective of this work is to study the effects of radiation combined with temperature on electronic devices and circuits developed in a partially depleted Silicon-on-Insulator (PD SOI) technology. The choice of a SOI technology is motivated by its attractive features: extended range of operating temperatures (up to 250°C) [7], reduced parasitic effects, low-power, high speed [8], lower sensitivity to transient radiation effects (SEE) compared to other technologies, and its high robustness to TID effects when a

thin gate/buried oxide is used [9].

A Second objective of this thesis, is to propose new mitigation techniques at design level against harsh environments (radiation and high temperature) effects and process corners variation for analog circuits.

To achieve these objectives, an investigation of radiation and temperature impacts on electronic devices has been performed in the first part of this thesis. Chapter 2 gives an overview of harsh environments, and their effects on semi-conductors technologies. Chapter 3 exposes transient effects of radiation and temperature. Thus, the simulation of single event effects (SEE) for a single PD SOI MOSFET and at circuit level (i.e. SRAM cells) are then performed using the 2D-TCAD Synopsys software. Afterwards, to overcome the complexity of such simulations and their huge time duration, a modeling of SEE effects was proposed based on a compact model developed using Verilog-A [10–12]. The SPICE integration of this compact model, and the validation check at different temperatures, have been a contribution of this thesis [13].

Another contribution of this work is the simulation of the combined effect of SEE effects and a temperature from 150 K to 500 K for a single MOSFET transistor and a standard 6T-SRAM cell designed in two different PD SOI technologies. Beside simulation and modeling of radiation effects, measurements of single event effects (SEE) for a standard 4-Nand flip-flop cell have been performed in the UCL Cyclotron facilities.

In chapter 4, the cumulative effects (TID) have been studied for two different PD SOI technologies. Total ionizing dose effects were measured for three ultra-low power analog circuits (Temperature sensor, Voltage reference, Comparator) designed in a PD SOI with 1 μm technology node [14]. These measurements have given a greater visibility on TID effects on analog circuits [15].

A new design of the previous voltage reference circuit was achieved in a more suitable PD SOI with a 130 nm process node. Robustness to radiation was simulated using custom model parameters including TID effects, such as mobilities and threshold voltages degradation [16]. Two layout implementations of the designed circuit were performed; one using Edgeless transistors, and another using standard transistors. Edgeless structures are known for their immunity against TID effects [17]. Unfortunately, in our case, the fabrication of these structures failed. Only the circuit with a standard transistors layout was functional, and still showed good results for the reference voltage up to 1.5 Mrad(Si) and 200 °C [16].

To understand the effects caused by the combination of a high total ionizing dose and a high temperature on such a PD SOI technology, the threshold voltages, the subthreshold slope and the mobilities of the MOSFETs were extracted under different conditions. The evolution of the threshold voltages, and the mobilities with temperature and radiation dose, can then be explained

in terms of the different balance between the fixed oxide charge N_{ox} and the interface states N_{it} build-up. [18].

The last chapter of this work, Chapter 5, proposes new mitigation techniques against process corners variation, radiation and temperature effects at design level for analog circuits. The state of the art of the existing mitigation techniques against radiation has first been exposed.

Secondly, the technique layout of Edgeless transistors and a design of rad hard current sources are presented.

Thirdly, the body biasing design technique is presented, and introduced as a new mitigation technique against the harsh environments effects, as well as the process corners variations on analog circuits.

Finally, designs of CMOS amplifiers robust to temperature variations (from -40°C to $+200^{\circ}\text{C}$), to higher TID effects (up to 200 mV negative shift of threshold voltages and up to 20 % of mobilities degradations), and resistant to all process corners variations, was presented.

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CHAPTER 2

Overview of harsh environments and their effects on electronics

FOR electronics, a harsh environment is a milieu characterized by extreme conditions such as a high or a low temperature, radiation, vibration, moisture, corrosion or pressure. More precisely a harsh environment is considered, if one or more of the following conditions are encountered [1]:

- Heat flux at atmospheric entry exceeding $1kW/cm^2$
- Hyper-velocity impact higher than 20 km/sec
- Temperature lower than $-55^{\circ}C$
- Temperature higher than $125^{\circ}C$
- Thermal cycling outside of the standard range of $-55^{\circ}C$ to $125^{\circ}C$
- High pressure exceeding 20 bars
- High radiation with total ionizing dose (TID) exceeding 100 kradSi

As an example of such as extreme environment, on the Venus planet, in addition to radiation, the temperature reaches $450^{\circ}C$ with a high pressure of 22 bars [1].

In this chapter, two extreme conditions for the electronics are studied, namely radiation and high temperature. Thus, the temperature effects on semiconductor devices are reviewed in the first section. Then an overview of radiation environments and their effects on electronic circuits are exposed in the last three sections.

2.1 High temperature effects

Electronic circuits suitable for temperatures beyond 125 °C are no longer a niche market thanks to several new applications related to automotive industry, avionics, space exploration, as well as in the oil industry. As shown in table 2.1, most of these new applications require a temperature lower than 300 °C. Therefore, the bulk and the Silicon-on-Insulator (SOI) technologies are usually used for these kind of electronic circuits.

Table 2.1: Example of high temperature applications [3].

applications	temperature range (°C)
automotive: engine/breaks	-40 to +250
Avionics: jet engine/intake	-40 to +320
Satellites	-150 to +200
Space exploration	-150 to +450
Oil exploration	-40 to +175
Geothermal exploration	-40 to +320

High temperature environments disturb electronic devices through various parameters, such as the mobility of carriers μ in the semiconductor, the leakage current of the devices, the threshold voltage V_{th} , the subthreshold slope parameter, the drain current, the On-to-Off current ratio (I_{ON}/I_{OFF}), the transconductance and the output conductance of the MOS transistors [2, 4]. These effects are detailed in the following paragraphs.

2.1.1 Effects on the threshold voltage V_{th}

The V_{th} variation with temperature depends on the used technology, the minimum channel length, the doping and, the gate oxide thickness of the transistors. For FD SOI, the threshold voltage depends only on the doping through the Fermi level (Eq.2.1). For PD SOI and Bulk, in addition to doping it depends on the gate oxide thickness [5, 6].

$$\frac{dV_{th}}{dT} = \frac{d\Phi_F}{dT} \quad (2.1)$$

$$\frac{dV_{th}}{dT} = \frac{d\Phi_F}{dT} + \frac{1}{C_{gox}} \cdot \frac{dQ_{depl}}{dT} \quad (2.2)$$

where Φ_F is the Fermi level, dQ_{depl} is the depletion charge and C_{gox} is the gate oxide capacitance. Fermi levels always decrease with temperature, as well as

the term " Q_{depl}/C_{gox} " for Bulk and PD SOI technologies [6]. Therefore, the threshold voltage of the MOS transistor always decrease with temperature.

The different previous works [2, 6] have shown a quasi linear variation of threshold voltage with temperature. For older technologies ($L_{min} \geq 1 \mu m$) the variation is about 3-5 mV/°C up to 250°C in Bulk, and 0.7-1 mV/°C for SOI up to more than 300°C (Fig.2.1-a). This variation of the V_{th} with temperature has been decreased in the newer technologies. As shown in Fig.2.1-b for a node technology of 130 nm, it is around 0.92 mV/°C for Bulk, 0.75 mV/°C for PD SOI and only 0.51 mV/°C for FD SOI up to 300°C.

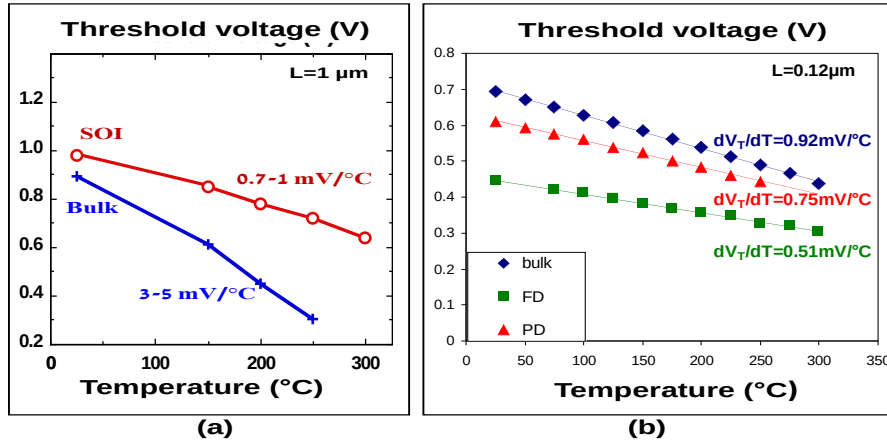


Figure 2.1: MOSFET threshold voltage versus temperature for different technologies (a) with $L_{min} = 1 \mu m$ [2], (b) for a $L_{min} = 130 nm$ [6].

2.1.2 Effects on the subthreshold slope parameter (SS)

Increasing the temperature of a MOSFET transistor leads to increase its subthreshold slope parameter SS. This increase versus temperature is expressed for Bulk and SOI technologies as [7]:

$$SS = \ln(10) \frac{kT}{q} n \quad (2.3)$$

where k is the Boltzmann constant, q the elementary charge, T the absolute temperature and n is the body factor. The latter is almost a constant for the Fully Depleted (FD) SOI ($n < 1$), while it has a strong temperature dependency ($1 \leq n \leq 2$) for the Bulk and PD SOI technologies [7].

2.1.3 Effects on the drain current and the I_{ON}/I_{OFF} ratio

For both Bulk and SOI technologies, the high temperature decreases the MOSFET drain current at high V_{GS} and lowers its on-to-off current ratio (I_{ON}/I_{OFF}) [4]. Figure 2.2 shows the I_{ON}/I_{OFF} ratio behavior with temperature for a 130 nm PD SOI nMOSFETs with different channel lengths (0.12, 0.2, 0.5, 1, 5, and 10 μm).

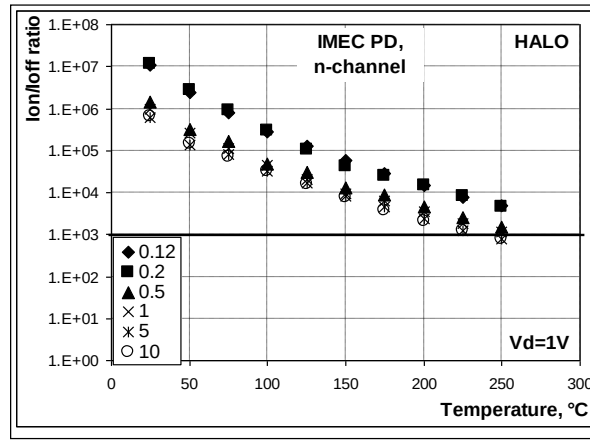


Figure 2.2: I_{ON}/I_{OFF} ratio in nMOSFETs with different channel lengths [4].

2.1.4 Effects on the leakage current

A high temperature leads to a huge increase of the leakage current of silicon devices. In the Bulk technology, the increase reaches up to 8 orders of magnitude between room temperature and 300 °C. For the SOI, the increase is only about 5 orders of magnitude [2]. This big difference between SOI and Bulk leakage has been explained in the reference [2] by two factors; first, the intrinsic concentration in the silicon n_i , secondly, by the junction area A_j in the transistors. In fact, the drain leakage current increases proportionally to the junction area A_j . Thanks to the buried oxide, the junction area of the SOI is about 100 times smaller than the Bulk. Furthermore in the Bulk and the PD SOI, the current leakage increases with temperature as the square of the intrinsic concentration (n_i^2), while for the FD SOI, it is only increased as n_i for long channel [2].

Figure 2.3 illustrates the drastic reduction in FD SOI MOS drain leakage current when compared to bulk at high temperature in a 1 μm process. For instance, at 300 °C, the leakage is about 1 nA/ μm of channel width for FD

SOI, while is $1 \mu\text{A}/\mu\text{m}$ in bulk [2]. For the PD technology, we have shown in Fig.2.2 that the leakage in 130 nm and $1 \mu\text{m}$ PD SOI remains 3 orders of magnitude lower than I_{ON} at a high temperature of 250°C .

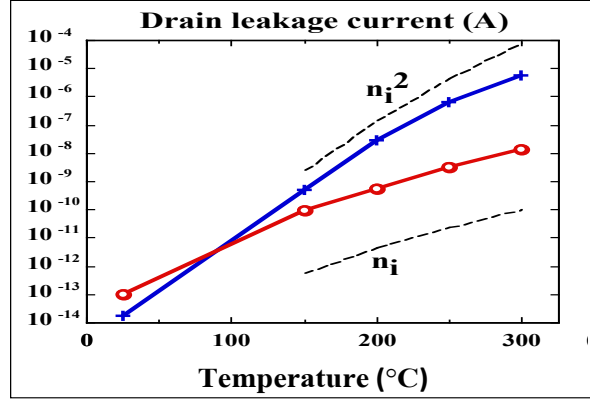


Figure 2.3: MOS drain leakage current versus temperature for Bulk and FD SOI ($L_{min}=1 \mu\text{m}$) [2].

2.1.5 Effects on the mobility μ

When the temperature of silicon increases, both the mobilities of electron and holes decrease. Their temperature dependence is given by [2]:

$$\mu(T) = \mu_0(T_0) \left(\frac{T_0}{T} \right)^\alpha \quad (2.4)$$

where μ_0 is the mobility at a temperature of $T_0=298 \text{ K}$, T is the temperature and α a factor with $1.5 \leq \alpha \leq 1.8$ for both Bulk and SOI technologies [2]. Thus, at high temperature (500 K) as shown in Fig.2.4 the mobility can be degraded by more than two times, compared to room temperature.

2.1.6 Effects on the transconductance g_m and the output conductance g_d of the transistors

Some of the most interesting MOSFET parameters for analogue applications, namely the transconductance g_m ($\delta I_{ds}/\delta V_{gs}$), and the output conductance g_d ($\delta I_{ds}/\delta V_{ds}$) are also degraded with temperature. As detailed in reference [2], g_m is related to the carrier mobility μ , and is decreased with temperature by a factor of 2.5 at 300°C for both Bulk and SOI technologies (Fig.2.5). Concerning g_d , it is degraded with temperature for the Bulk technology, and seems to be fairly stable for the SOI technology [2].

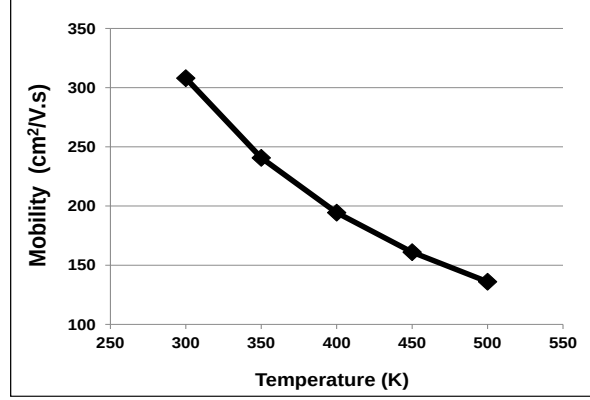


Figure 2.4: Example of mobility degradation with temperature for a factor $\alpha = 1.6$ and $\mu_0 = 305 \text{ cm}^2/\text{V.s}$.

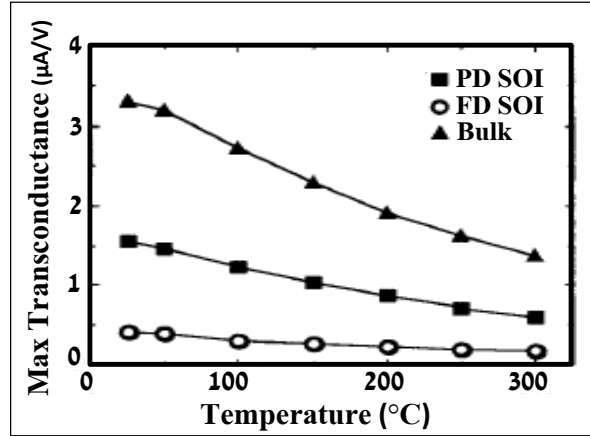


Figure 2.5: Maximum transconductance degradation with temperature for Bulk and SOI MOSFET [2].

As a conclusion, when temperature exceeds 125°C , it represents a real handicap for the Bulk technology, but fortunately the SOI technology is more robust, and represents a good choice for electronic applications up to 225°C for PD, and 300°C for FD [2, 5].

A comparison between the available technologies for high temperature electronics is shown in table 2.2. More comparison between different characteristics of these technologies are presented in the appendix A.

To be noted that the SiC technology [8] starts to interest the industry looking for robust and very high temperature circuits ($\geq 300^\circ\text{C}$). Low complexity

circuits have been already developed in this technology [9, 10].

Table 2.2: Existing technologies for high temperature applications [1].

Material of Device	Theoretical Max (°C)	Max for IC
Bulk Silicon	225+	125 °C
SOI	300+	250 °C
Gallium Arsenide-based	400+	
Gallium Nitride-based	600	
Silicon Carbide	600	350 °C
Diamond	800	
Vacuum Thermionic	1000	

2.1.7 Zero-temperature-coefficient (ZTC)

A standard way to minimize the temperature effects on the MOSFET parameters (drain current I_{DS} , transconductance g_m , current gain frequency cutoff f_T and maximum oscillation frequency f_{max}) is to bias the transistor at a specific supply voltage where both effects (mobilities and threshold voltage reduction) compensate one another, and these parameters remain constant as temperature varies (Fig.2.6). This bias condition is called the zero-temperature-coefficient (ZTC) [12].

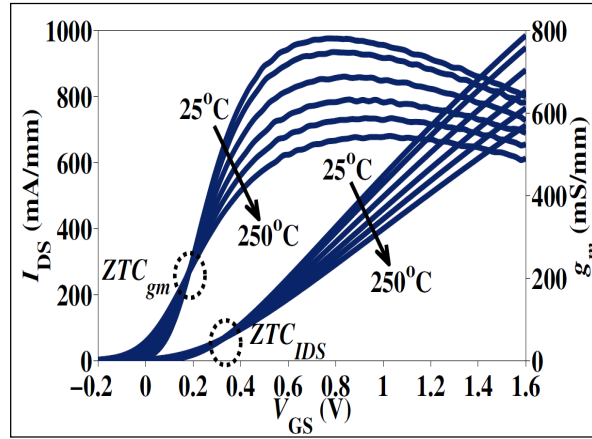


Figure 2.6: Zero-temperature-coefficient shown from $I_{DS}(V_{GS})$ and $g_m(V_{GS})$ characteristics for NMOS PD SOI ($L_{min} = 1 \mu m$) [13].

2.2 Overview of radiation

Multiple radiation sources are exposed in literature: some take their origin in the Sun (e.g. solar flares, coronal mass ejection and solar wind), or from the Earth (uranium mine, nuclear powers ...), others come from outside the solar system [14]. This section gives an overview of sources and environments radiation concerning electronic circuits.

2.2.1 Radiation sources

2.2.1.1 Solar flares

A solar flare is a sudden and quick release of magnetic energy that has built up in the solar atmosphere (Fig.2.7). This radiation phenomenon emits through the entire electromagnetic spectrum. Particles, including electrons, protons, and mainly heavy nuclei, are heated and accelerated in the solar atmosphere. Therefore, heavy ions should first be considered when analyzing the solar flare impact on the integrated circuit reliability [15].

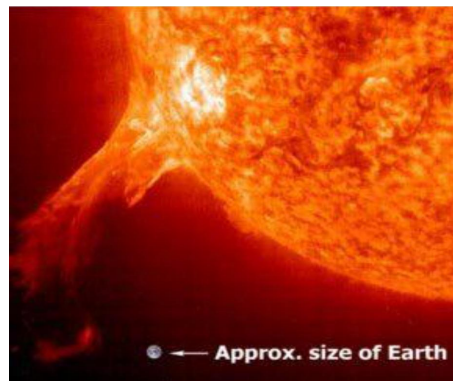


Figure 2.7: Solar flare [15].

2.2.1.2 Solar wind

Due to high temperature in the sun corona, electrons have sufficient energy to escape the gravity. As a reaction, protons and heavy ions are ejected in order to maintain the zero electrical charge of the sun. This ejection in all directions at a speed of about 400 km/s is called the solar wind [15].

2.2.1.3 Coronal mass ejections

A Coronal Mass Ejection (*CME*) is a huge plasma bubble ejected by the Sun (Fig.2.8) over several hours. The main particles generated by this phenomenon are high-energy protons [16].

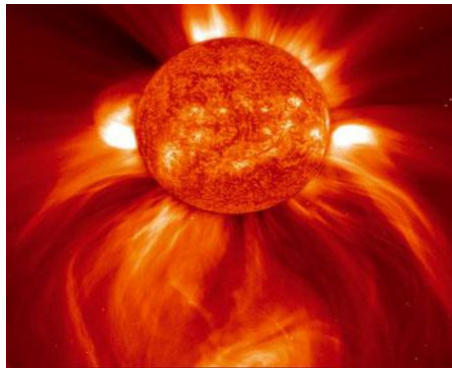


Figure 2.8: Coronal mass ejections [15].

2.2.1.4 Galactic cosmic rays

Galactic cosmic rays (*GCRs*) are high-energy charged particles (up to 1020 eV) coming from the outside of our solar system (usually from the *Milky Way*). They are composed of about 89% protons, 10% Helium nuclei, the remaining 1% consisting of heavier elements and electrons [16].

2.2.2 Radiation environments

2.2.2.1 Van Allen belts

In 1958 James Van Allen discovered two regions of the magnetosphere, where high-energy particles, mainly protons and electrons, are trapped by the Earth magnetic field (Fig.2.9). These particles are either issued from solar wind protons or from galactic cosmic ion collisions with the atmosphere. These zones were named Van Allen Belts (inner and outer belts).

The inner belt is mainly composed of high-energy protons (with energies up to some 100 MeV), extends from an altitude of about 100 km up to 12,500 km above the Earth surface [17].

The outer belt spreads from 20,000 km up to 40,000 km of the Earth surface [17]. Trapped particles are mostly high-energy electrons (with energies from 0.1 to 10 MeV).

Both belts present a potential risk for satellites, if their orbit spends a significant time in the radiation belts. Sensitive components are often shut off

or placed in "safe" mode using adequate shielding while passing through [15].

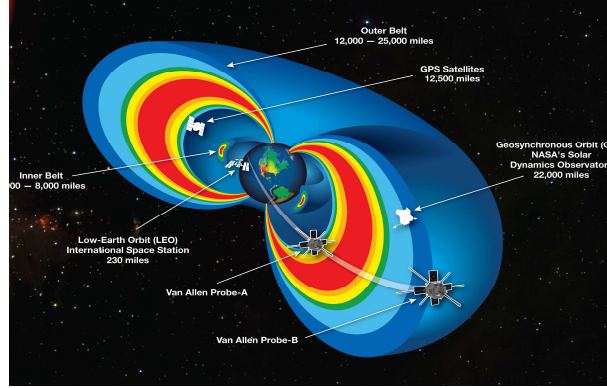


Figure 2.9: Van Allen radiation belts [17].

2.2.2.2 Atmospheric neutrons

High-energetic cosmic ray particles (mainly protons) can generate neutrons, secondary protons, muons and neutrinos by a spallation¹ reaction on atmospheric nuclei. The neutron peak flux can feature up to 10,000 particles/cm².hour ($E > 10$ MeV), and is located at an altitude of 18 km from the Earth surface. At ground level, the observed flux equals about 1/400 of the peak flux.

It is to be noted that the neutrons cannot cause errors in integrated circuits through direct ionization, as such is the case with protons and heavy ions, but they can generate soft errors resulting from recoils which may deposit enough charge in a small volume to trigger a transient event [15].

2.2.2.3 Terrestrial radiation sources

Different sources of radiation are present throughout the nature: in the soil, the water and the vegetation. The natural deposited dose is linked to several parameters such as the geographic location, the presence of uranium mine or decay products, such as thorium, radium, and radon, which are the major isotopes of concern for terrestrial radiations.

Sources of alpha impurities are also found in the micro-electronic fabrication, mainly in the wafer process, the packaging impurities, chip materials and solder. These alpha sources have a low energy (< 5 MeV), but are locally highly ionizing, and they may provoke dysfunction of electronic devices [15].

¹In nuclear physics, spallation is the process in which a heavy nucleus emits nucleons as a result of being hit by a high-energy particle, thus reducing its atomic weight.

2.3 Radiation interactions with electronics

Interactions between radiation environments and electronic devices depend on the particle type (photon, neutron, electron, proton, ion) and its energy. The following section indicates the existing interactions between electronics and radiation particles [19].

2.3.1 Interaction with photons

Photons are an electromagnetic radiation, electrically neutral, with zero mass, and have a speed of the light c . In most cases, they do not lose energy via ionization with atoms; except when they travel some significant distance. When photons cross the electronic devices, they induce electron-hole pairs in the matter (e.g. silicon and insulator) through a partial or total transfer of the photon energy to the electron. This transfer is observed via three kind of interactions [15]:

- The photoelectric Effect
This is the predominant mode of interaction for photons of low energy (less than 10 keV). The incident photon is completely absorbed by an atom which ejects a photo-electron. The interaction leaves an ionized atom with a vacancy that will quickly be filled through the capture of a free electron from the medium.
- Compton Scattering
Is mainly an interaction between a photon having a high energy (between 10 keV and several MeV) and an electron in the material. During the *Compton Scattering* mechanism, a fraction of the photon energy is transferred to the electron, which is then known as a recoil or a Compton electron.
- Pair Production
When a photon with a very high energy (more than 1,022 MeV) passes near to the nucleus of an atom, it is exposed to strong field effects from the nucleus. It may disappear as a photon and reappear as a positive (positron) and negative (electron) pair. This process called *pair production* becomes more likely with an increasing photon energy.

2.3.2 Interaction with neutrons

When passing through the matter, the neutron which has no charge mainly interacts with the nucleus of the atoms. However, the probability it might pass close enough to a silicon nucleus is low. If it happens, it causes two types of

interactions: scattering or absorption [20,21]. The speed and the direction of a neutron are changed when it is scattered by a nucleus, without impacting the composition of the latter (same number of protons and neutrons). But, due to recoil velocity the nucleus is left in an excited state that will emit possible radiation. In case a neutron is absorbed by a nucleus, either a wide range of radiation is generated, or a fission of the nucleus can be induced. For integrated circuits, three interactions can be considered [15]:

- Elastic Scattering
Is a mechanism where the neutron transfers a portion of its kinetic energy to the atom nucleus. When the transferred energy is sufficiently large, the nucleus can leave the crystalline silicon network (degradation of the silicon structure).
- Inelastic Scattering
Is an interaction similar to the "elastic scattering", except that the nucleus is subjected to an internal rearrangement into an excited state from which it releases a secondary particle. This radiation effect may create a number of electron-hole pairs able to perturb the transistor functionality.
- Absorption
Is the process where a neutron is absorbed by a nucleus, which leads to a mutation of the atom into an heavier element that interferes with the integrated circuit. In the CMOS technology, the neutron can be absorbed by the dopant (e.g. ^{10}B atom) and the reaction may produce an alpha particle and a ^7Li nuclei.

2.3.3 Interaction with charged particles

When a charged particle (proton, electron, alpha particle or heavier ion) crosses the matter, it creates several collisions with the electrons and the nuclei. The energy released by these interactions generates an ionization in the medium, and produces a number of electron-hole pairs, or generates an electromagnetic radiation.

For integrated circuits, alpha-particles and heavier ions always interact through direct ionization. This leads to generate single event effects. However, protons and electrons interact through indirect ionization provoked by the secondary particles for the older technologies (bigger than 90 nm), and by direct ionization for the newer technologies [15].

As a conclusion, the radiation interactions with electronics can either damage the atomic structures, or induce electron-hole pairs in the matter (insulator and semiconductor regions). In the CMOS technology, the created electron-hole pairs in the silicon induce single event effects. However, when created

in the oxide layers, the electron-hole pairs induce an alteration of the electrical characteristics of the devices. This is known as the cumulative effects of radiation (see following section).

2.4 Radiation effects on electronic devices

The radiation effects on the integrated circuits can be divided into two groups: effects due to a single particle, called Single Event Effects (*SEE*), and cumulative effects caused by a large number of particles. The following section exposes both effects, and defines some specific notions related to the radiation of integrated circuits.

2.4.1 Useful notions related to radiation

2.4.1.1 Linear Energy Transfer (LET)

When an ionized particle crosses the matter, it transfers its energy to the medium. The linear density of the energy lost by the particle is called the Linear Energy Transfer (LET), and is expressed in MeV/mg/cm² or pC/μm² and corresponds to [22]:

$$LET = \frac{1}{\rho} \cdot \frac{\Delta E}{\Delta x} \quad (2.5)$$

Where ρ is the material density, X the depth and ΔE is the deposited energy. This, is given by the equation 2.6, where θ is the ion incident angle (Fig.2.10):

$$\Delta E = \frac{dE}{dx} \cdot \frac{X}{\cos \theta} \quad (2.6)$$

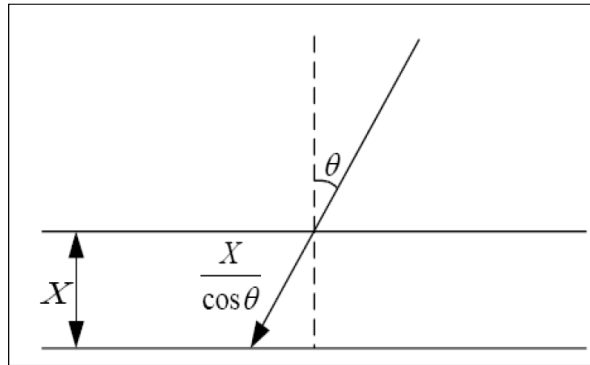


Figure 2.10: Deposited energy with a θ incident angle [15].

2.4.1.2 Linear Energy threshold (LETth)

When the deposited energy ΔE is higher than the critical energy E_c , a single event effect occurs in the components. The LET threshold LET_{th} is the minimum LET necessary for a charged particle to create a single event (e.g. to modify the state of a SRAM cell). Therefore, circuits having a high LET_{th} have a good immunity to single event effects.

2.4.1.3 Cross section σ

For a device under test, the cross section σ is defined by the ratio of the number of observed single events to the charged particles fluency (particles per cm^2). The cross section gives an idea of the probability that an ionized particle causes a single event, and is given by the following equation [15]:

$$\sigma = \frac{\text{number of observed events}}{\text{fluency}} \quad (cm^2) \quad (2.7)$$

2.4.1.4 Cross-section curve

The cross-section curve describes the sensitivity of an electronic component for a radiation effect. It is directly plotted from the measured cross-section versus the incident particle LET for heavy ions, or energy for protons. The x-axis of the curve is represented by the LET (or energy for protons), and the y-axis by the measured cross section. Two specific values characterize this curve: The first is the LET threshold, which is the lowest LET required to trigger a single event. The second is the saturation cross-section σ_{sat} , which indicates the maximal sensitivity of the device, and is thus an image of the total sensitive area of the device.

Figure 2.11 gives an example of the typical cross-section curve measured for heavy ions. It can be fit using a *Weibull* distribution with width W and shape S parameters. The curve shape equation is the following [15]:

$$\sigma = \sigma_{sat} \cdot \left[1 - \exp \left(\left(-\frac{LET - LET_{th}}{W} \right)^S \right) \right] \quad (2.8)$$

In the case of protons, another distribution called "*Bendel model*" is used with the threshold energy " E_{th} " instead of the LET_{th} [15]:

$$\sigma = \sigma_{sat} \cdot \left[1 - \exp \left(-0.18 \left(\sqrt{\frac{18}{E_{th}}} (E - E_{th}) \right)^{0.5} \right) \right]^4 \quad (2.9)$$

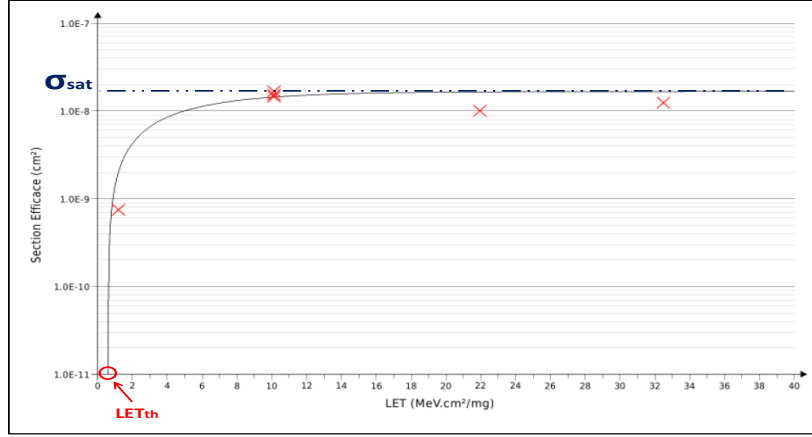


Figure 2.11: Example of an heavy ions cross-section curve [15].

2.4.2 Single Event Effects (SEE)

A single ionizing particle can produce two kinds of effects. The first one is temporary and can be recovered, such as Single-Event Transient (SET), Single-Event Upset (SEU) and Single-Event Functional Interrupt (SEFI). The second effect leads to a permanent damage on the device, such as Single-Event Latch-up (SEL) or Single-Event Gate Rupture (SEGR). It should be noted that single event effects can be produced either by direct ionization or by secondary particles from nuclear reactions [15].

2.4.2.1 Single-Event Transient (SET)

A single-event transient (SET) is a temporary disruption at the output of a device (transistor) or circuit caused by an ionizing particle passing through the device. Figure 2.12 gives an example of a SET induced in a standard 6T-SRAM cell.

2.4.2.2 Single-Event Upset (SEU)

Single-event upset (SEU) induces a state change in a digital cell (bit-flip). It occurs when critical charges are collected at sensitive nodes of storage elements such as SRAM cells, or when a SET is latched on a clock edge after propagating in a combinatorial logic (e.g. in a flipflop). Tolerance to SEU of an integrated circuit depends on several parameters such as technologies (e.g. SOI), transistors sizes, capacitors on the nodes, and supply voltage (Chapter 5 gives more details on this point).

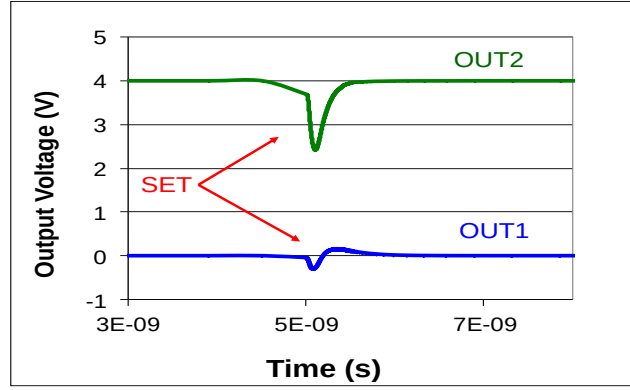


Figure 2.12: Example of a single-event transient.

2.4.2.3 Multiple-Bit Upset (MBU) and Multiple-Cell Upset (MCU)

Multiple upsets happen when several bit-flips are provoked by a single particle. If the change state occurs in the same memory word, it is called MBUs, whereas when several bit-flips occur in different memory words, it is known as MCUs. This can happen when a deposited charge is collected by several sensitive nodes of the circuit.

The newer technologies are more and more sensitive to the Multiple upsets phenomena, due to the small distances between the different transistors.

2.4.2.4 Single-Event Functional Interrupt (SEFI)

Single-event functional interrupts are an unexpected behavior in complex circuits such as micro-controllers caused by SEU. When a SEFI occurs, a reset of the application or a power switch off/on cycle is required to recover the full functionality of the circuit [23].

2.4.2.5 Single-Event Latch-up (SEL)

A single event latch-up occurs when a high-energy particle triggers the parasitic thyristor (PNPN structure) existing in CMOS and bipolar devices (Fig.2.13). The thyristor stays "shorted", and a huge current flows and increases the temperature of the transistor until its destruction. Thanks to its isolated substrate, the SOI technology is insensitive to this phenomenon.

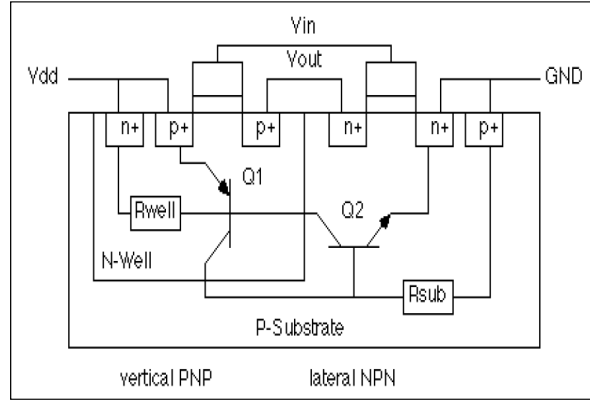


Figure 2.13: Cross section of the PNP parasitic structure in standard Bulk CMOS technology [15].

2.4.2.6 Single-Event Burnout (SEB)

The single-event burnout concerns mainly power MOSFETs. It occurs when the source gets forward-biased and the drain-source voltage becomes higher than the breakdown voltage of the parasitic structures. The resulting high current destroys the power transistor.

2.4.2.7 Single-Event Gate Rupture (SEGR)

The single event gate rupture occurs when a charged particle (heavy ion, proton) hits the gate oxide region while a high voltage is applied to the gate. A local damage happens then in the insulating layer of the silicon (also in buried oxide for SOI). Thus, the leakage current is increased and may also destroy the gate region. This phenomenon happens mainly in power MOSFETs or in high voltage EEPROM cells during the write or the erase phases.

More details about SEE effects are given in Appendix B.

2.4.3 Cumulative effects

When an electronic component is exposed to radiation during a period of time, some permanent parameters degradation and functional failures can appear in the device. These effects, called the cumulative effects, may be classified in two groups: Total Ionizing Dose (TID) and displacement damage effects, also called TNID (Total Non-Ionizing Dose) [15]. The following paragraphs give details on these two groups, and the units used for the radiation dose.

As a reminder, ionization is the process of removing electrons from atoms,

leaving two electrically charged particles behind, an electron and a positively charged ion.

2.4.3.1 Units of radiation dose

In the international system of units (SI system), "Gray" (Gy) and "Sievert" (Sv) are used for the radiation dose measurement. While in the United States, the used units are "rad", "rem" or "Roentgen" (R). In practice, the most used units are rad, Gy and Sv [24].

Gray :

One Gray is the absorption of one Joule of energy, in the form of ionizing radiation, per kilogram of matter, defined as:

$$1\text{Gy} = 1 \frac{\text{J}}{\text{kg}} = \frac{\text{m}^2}{\text{s}^2} \quad (2.10)$$

Sievert :

The Sievert unit is used to measure the biological effects of ionizing radiation, it is thus more used in medical fields.

$$1\text{Sv} = 1 \frac{\text{J}}{\text{kg}} \quad (2.11)$$

Rad :

The rad is the most used unit of the absorbed radiation dose, and is defined as $1 \text{ rad} = 0.01 \text{ Gy} = 0.01 \text{ J/kg}$.

ElectronVolt (eV) :

In physics, the electron volt eV is a unit of energy measurement. By definition, it is the amount of energy gained by the charge of a single electron moved across an electric potential difference of one Volt. Thus it is 1 Volt (1 Joule per Coulomb) multiplied by the elementary charge "e" (about $1.602176565 \cdot 10^{-19}$ C). Therefore, one electron volt is equal to $1.602176565 \cdot 10^{-19}$ J [25].

2.4.3.2 Displacement damage (TNID)

Better known as total non ionized dose (TNID) is mainly induced by the neutrons. The non-ionizing energy results in a displacement damage and defects in the semiconductor matter. This deposited energy: 1) displaces atoms of the crystal, 2) leads to a change in the minority carrier lifetimes of semiconductors, and 3) increases light absorption in optical materials. These effects provokes damage to the electrical characteristics of the semiconductors.

Neutrons cross the electronic devices without stop, thus induce a displacement damage through the total volume. Therefore, this effect impacts mostly optoelectronic devices and bipolar transistors. For MOSFET transistors, the channel constitutes the sensitive volume, which is very small compared to the bipolar transistors.

2.4.3.3 Total Ionizing Dose (TID)

The total ionizing dose effect is a permanent damage induced by photons or charged particles (heavy ions, electrons and protons). When these particles cross a semiconductor device, its insulating layers trap charges N_{ox} or produce interface charges N_{it} . This, impacts the electrical characteristics of the device. For the MOSFET transistors, TID effects provoke a shift in the threshold voltages and a mobilities degradation [26].

Table 2.3 gives an idea of the total dose accumulated per year for four different satellite orbits: Geosynchronous orbit (GEO), Global Positioning Satellite (GPS), Low Earth Orbit (LEO) and Defense Meteorological Satellite (DMS) [27].

Table 2.3: Estimated TID per year for four different satellite orbits [27].

Orbit name	GEO	GPS	LEO	DMS
Apogee (km)	35,796	20,189	1,600	946
Perigee (km)	35,795	20,172	1,600	824
Inclination (degrees)	0	55	60	99
Dose (rad(Si)/year)	6,600	59,000	17,300	1,260

2.5 Conclusion

High temperature environments disturb electronic devices through various parameters, such as the mobility of carriers μ in the semiconductor, the leakage current of the devices and the threshold voltage V_{th} of the MOS transistors. Although the SOI technology have demonstrated since several years a lower sensitivity to these temperature effects compared to Bulk. The Silicon Carbide (SiC) will be probably the future technology for very high temperature circuits ($> 300\text{ }^{\circ}\text{C}$).

There are several radiation sources that impact integrated circuits. Some of them are linked to the atmospheres (sun and stars) and mainly affect electronics used in space and aerospace applications. Other sources are linked to the human utilization such as in medical, military and nuclear centers.

Radiation sources generate two types of particles, charged particles like protons, electrons and heavy ions, and uncharged such as photons and neutrons. The first kind of particles interacts directly with the electronic devices by creating a number of electron-hole pairs in the silicon and insulators. While the second kind affects electronic components through secondary effects, and can induce electron-hole pairs or displacement damage in the lattice silicon atom.

The radiation impacts on the integrated circuits can be classified into two groups: first, the effects due to a single particle (SEE) and impacting directly the silicon matter. The second is the cumulative effects caused by either, a long time exposition to radiation like in space, or a very high ionizing energy such as in nuclear centers. These effects induces permanent failures in the devices due to charges buildup in the insulators layers (e.g. gate or buried oxides for SOI technology).

Table 2.4 provides relevant radiation effects on integrated circuits and, table 2.5 gives a summary of the radiation effects on different technologies: Bipolar, CMOS, BiCMOS and Silicon-on-Insulator SOI.

SOI CMOS clearly appears as the most promising for the objectives of this thesis, since it enables the realization of complex IC with lower sensitivity to temperature and radiation effects.

Table 2.4: Radiation effects on integrated circuits.

Particles type	Induced effects	effects on IC
Photons	Creation of electron-hole pairs in insulators	Total ionizing dose
	Creation of electron-hole pairs in silicon	Single event effects
Neutrons	Creation of electron-hole pairs in silicon	Single event effects
	Displacement of silicon atoms	Displacement damage (TNID)
Charged particles	Creation of electron-hole pairs in silicon	Single event effects
	Creation of electron-hole pairs in insulators	Total ionizing dose

Table 2.5: Radiation effects on different technologies [15].

Technology	Radiation effects
Power MOS	TID SEGR SEB
Bipolar	TID TNID SEU SET
Bulk CMOS	TID SEE
BiCMOS	TID TNID SEE
SOI CMOS	TID Low sensitivity to SEE insensitive to SEL

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CHAPTER 3

Single event effects combined with temperature in digital circuits

As discussed in the previous chapter 2, single event effects can affect the functionality of the electronic devices. Indeed, when an ionized particle crosses a transistor (Fig.3.1) it creates a number of electron-hole pairs. An electric field in the device is able to separate the pairs and allow the collection of an amount of charges. This may create a parasitic current between the drain and source of the transistor. To simulate this radiation impact on an electronic circuit, numerical simulators can be used. Thus, Sentaurus ISE-TCAD (Technology Computer-Aided Design) or Silvaco ATLAS are mostly used at transistor level simulations. But, due to their huge time burden, the modeling of radiation effects becomes absolutely necessary for SPICE simulation at circuit level.

As single event effects (SEE) concern mainly digital circuits, this chapter studies transient effects of radiation on: 1) a single MOS transistor, 2) two different SRAMs cells, and 3) a 4-Nand flip-flop.

We first show how to simulate single event effects using the Sentaurus TCAD software. Secondly, the combined effect of temperature and SEE is discussed. Thirdly, a compact model for modeling radiation effects at different temperatures is presented. In order to validate this compact model, comparisons between its results and Sentaurus TCAD were carried out. Fourthly, different types of SEE measurements and experimental results for a 4-Nand flip-flop are exposed. In the end, a comparison between simulated and measured LET_{th} for an UCL SRAM cell has been performed.

3.1 Simulation of SEE effects

Single event effects can be simulated by using a numerical software developed by Synopsys named Sentaurus ISE-TCAD [1]. It allows: 1) to create a physical

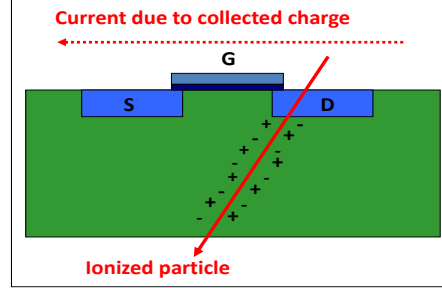


Figure 3.1: Ionized particle crosses a transistor.

structure description for the irradiated device, including all details on technological implementation. 2) To simulate this structure using all semiconductor physical equations. The following paragraphs give more details on the Sentaurus ISE-TCAD software, and the physical structure description of the studied transistors.

3.1.1 Sentaurus ISE-TCAD simulator

Sentaurus ISE-TCAD tool simulates several characteristics (electrical, thermal, optical ...) and effects (radiation, temperature, latch-up, ESD ...) of semiconductor devices. Simulations are launched on a 2D (2 dimensional) or a 3D physical structure description of the real device. This physical structure description is generated by the graphical user interface (GUI). Many technological and physical parameters have to be taken in account to create this structure, such as materials mobilities or doping concentration. Once built, the structure is checked and validated through electrical simulations. For instance, for a MOS transistor, the structure parameters can be fitted to the typical DC characteristics: $I_D(V_{GS})$ or/and $I_D(V_{DS})$.

Figure 3.2 shows a 2D structure for a NMOS transistor in a PD SOI CMOS process featuring a 25 nm thick gate oxide, a 250 nm thick silicon body, a 1 μm thick buried oxide with 1 μm channel length and a width of 6 μm . Figure 3.3 shows a fair agreement between measured and simulated (using the 2D structure Fig.3.2) curves at room temperature (300 K).

When the physical 2D structure description is checked and validated, the impact of radiation and temperature can be simulated using the Sentaurus device simulator.

In such simulation, many parameters depending on the radiation conditions have to be set; the type of particles, the direction (angle of incidence: vertical, horizontal or titled by some degrees), the location when the particle crosses the

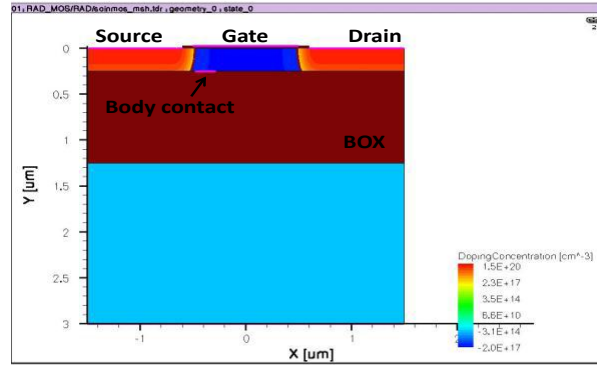


Figure 3.2: 2D structure of a PD SOI N-MOSFET from 1- μm technology.

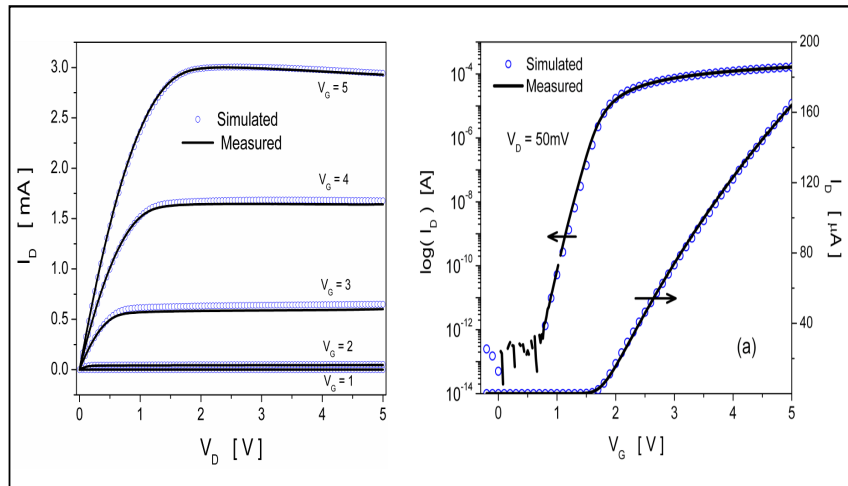


Figure 3.3: Comparison between simulated and measured $I_D(V_{DS})$ and $I_D(V_{GS})$ curves at low V_{DS} for the device of Fig.3.2, at 300 K [8].

device, the track radius of the particle and its energy. The electrical parameters of the devices also have to be set.

The following instructions show how to define a radiation setup in an ISE-TCAD netlist:

```
Physics{
Temperature=300          * temperature in K
AreaFactor=6             * transistor width in  $\mu\text{m}$ 
EffectiveIntrinsicDensity( OldSlotboom )
```

```

Mobility(
DopingDep
eHighFieldsaturation( GradQuasiFermi )
hHighFieldsaturation( GradQuasiFermi )
<Enormal)
Recombination( SRH(DopingDep) )
HeavyIon(                * type of particle
Direction=(0,1)          * vertical direction, (1,0) for horizontal direction
Location=(0,1)           * location of radiation is in the drain
Time=0.5e-6              * time when the particle hits the device
Length=1.25              * depth of the radiation
Wthi=0.1                * diameter of particle
LETf=0.64              * energy of the particles (in pC/μm2)
Gaussian                 * form of drain current  $I_D$ 
PicoCoulomb )           * unit of energy

```

A complete example of ISE-TCAD netlist is available in Appendix C.

3.1.2 Simulation of single event effects

3.1.2.1 Simulation of a single PD SOI NMOS transistor

The simulation of single event effects on a NMOS transistor has endless possibilities, depending on the position where the particle crosses the transistor, its incidence angle, its track radius, its energy and the voltages of the transistor nodes.

The SEE simulation we considered here, is performed on the 2D structure of Fig.3.4 at time $t=5\text{ns}$, with a particle featuring an energy LET of 20 MeV/mg/cm^2 and at worst case. This corresponds to the OFF state of transistor ($V_{GS} = 0$ and $|V_{DS}| > 0$) and the particle hits at the drain with a vertical angle of incidence [2].

Induced drain current by radiation I_{RAD} is plotted in Fig.3.5, it shows a very fast current pulse (some ps) with a peak about 4 mA, starting at the moment of radiation ($t=5\text{ns}$).

3.1.2.2 2D-TCAD mixed-mode simulation

Simulation of a complete (analog/digital) circuit using the physical devices simulators, needs a complex 2D structure representing the circuit. It also requires a very long time to be performed. To avoid these issues another technique is used to simulate the SEE on the complete circuit. Called mixed-mode simulation [3], this technique consists in limiting the use of the device simulator to the

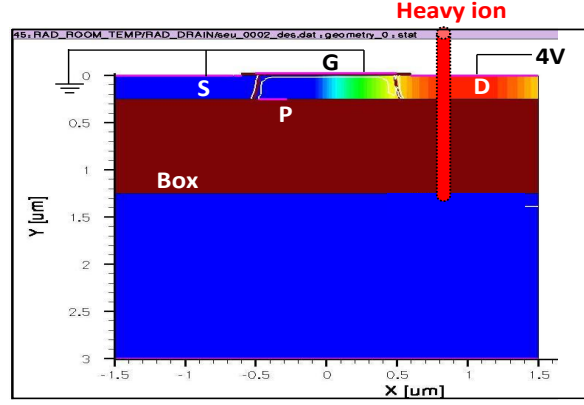


Figure 3.4: Simulation of heavy ion crossing the drain of transistor of Fig.3.2 with a normal incidence.

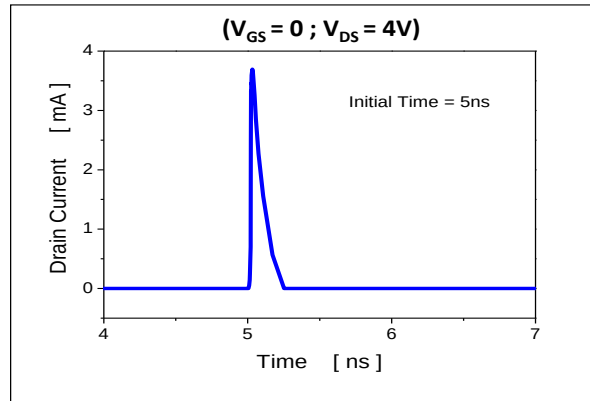


Figure 3.5: Induced current pulse by particle in the drain of the transistor under condition of Fig.3.4

struck transistor while the rest of design is represented by SPICE elements. For instance, Fig.3.6 shows the mixed-mode simulation schematic for a 6T SRAM cell, considering N1 as the struck transistor.

3.1.2.3 LET_{th} extraction for a PD SOI CMOS 6T-SRAM cell

The simulated PD SOI CMOS 6T-SRAM cell (Fig.3.7) has $6\ \mu\text{m}$ and $12\ \mu\text{m}$ channel widths respectively for NMOS and PMOS transistors, with $1\ \mu\text{m}$ channel length. Simulations are performed using a 2D-TCAD mixed mode for a SRAM cell in memory state (no write, no read). The bit and word lines are

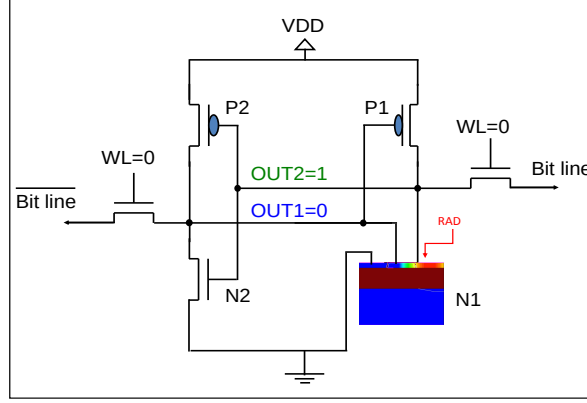


Figure 3.6: A mixed-mode simulation schematic for a 6T-SRAM cell.

pre-charged to VSS (0 V) and the supply voltage VDD is 4 V (the used technology is dedicated for a power supply from 3 V to 5 V). Choosing time of the SEE radiation is $t = 5$ ns at a temperature of 300 K.

The structure of the 6T-SRAM is symmetric and the NMOS transistor is more sensitive to SEE effects than the PMOS [4]. Thus, the worst case simulation corresponds to a particle that hits one NMOS transistor in off state (N1 in Fig.3.7 for example). This worst case simulation gives the threshold LET (LET_{th}) for such a 6T-SRAM.

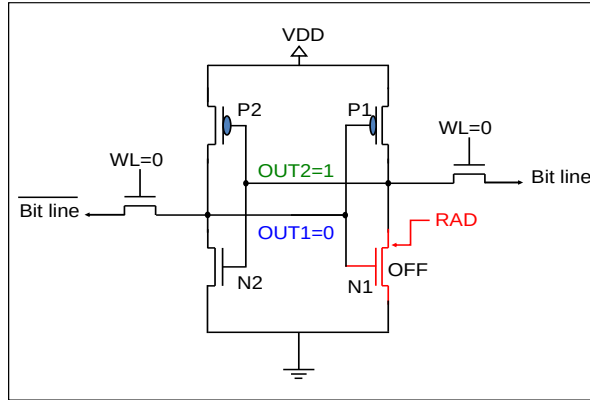


Figure 3.7: Standard 6T-SRAM cell.

As shown in Fig.3.8, for a simulation with an energy LET lower than 30 MeV/mg/cm², a single event transient (SET) occurs in the SRAM cell. The initial logic state is first altered and is recovered after about 0.5 ns. When the

particle energy reaches a $LET = 30 \text{ MeV/mg/cm}^2$, a single even upset happens (Fig.3.9), OUT1 shifts from "0" logic to "1" (4 V). Therefore at a temperature of 300 K the LET_{th} of such a 6T-SRAM cell is 30 MeV/mg/cm^2 .

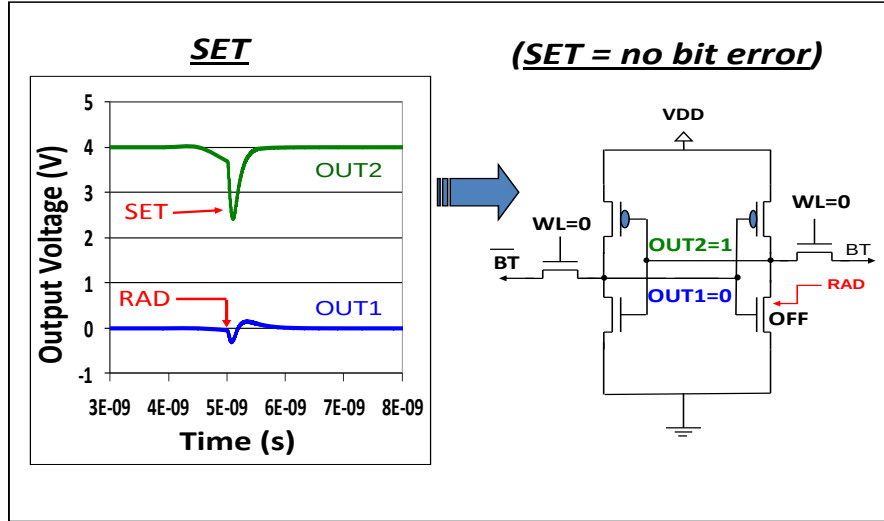


Figure 3.8: SET for a 6T-SRAM cell ($LET = 20 \text{ MeV/mg/cm}^2$).

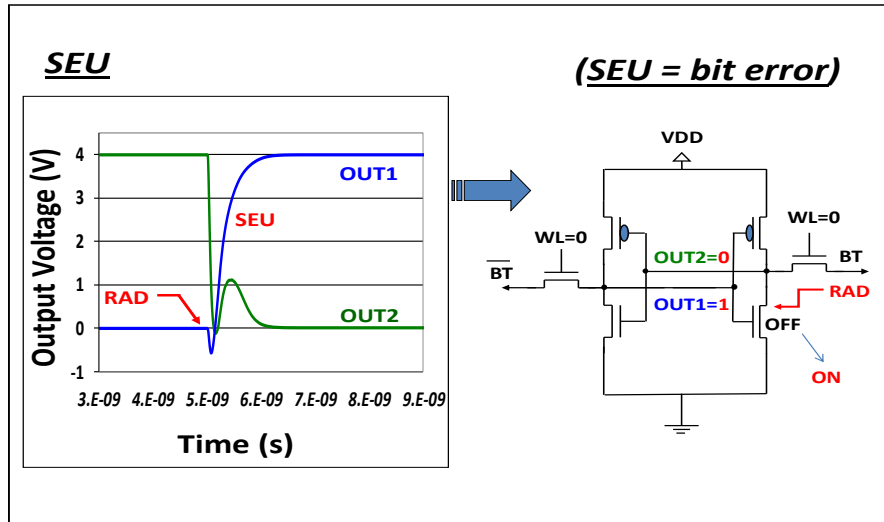


Figure 3.9: SEU for a 6T-SRAM cell ($LET = 30 \text{ MeV/mg/cm}^2$).

3.2 Modeling of radiation effects

3.2.1 Compact model

Beside the creation and the check of the 2D structure, the TCAD simulation takes a large time for one simulation; i.e. about two hours for 10 ns of transient simulation of the 6T-SRAM, on a workstation with 1.6 GHz clock frequency and a 4 GB RAM. In case of 3D TCAD simulations, several days are needed. Furthermore, numerous simulations are needed before finding the right LET_{th} .

Due to this intricate approach, it is essential to develop a simple model of the single event effects (SEE) which can be simulated directly with SPICE. Many works to model the SEE in SPICE are presented in the literature [5–7]. These works are based on the introduction of a current source between drain and source to model the radiation induced current in the transistor (Fig.3.10).

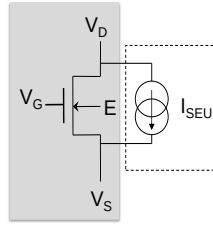


Figure 3.10: SEU model from literature.

The developed compact model¹ considers more physical aspects. It is based on the concept of connecting a current source I_{SEU} controlled by different voltages on the terminals of the BSIMSOI model (Fig.3.12). The current source I_{SEU} is defined by the equations of the generation of electron-hole pairs by a heavy ion strike through the channel, used in [8] as:

$$I_{SEU} = \pi \cdot r^2 \cdot (J_n + J_p) \quad (3.1)$$

$$J_n = qD_n \nabla \rho_n(LET, r, t_{si}, t) + q\rho_n(LET)\mu_n E \quad (3.2)$$

$$J_p = qD_p \nabla \rho_p(LET, r, t_{si}, t) + q[N_A + \rho_p(LET)]\mu_p E \quad (3.3)$$

where J_n and J_p are the electrons and holes current densities for the *NMOSFET* and *PMOSFET* case respectively, r is the track radius, D_n and D_p the diffusion coefficients of electrons and holes, $\mu_n = \mu_{eff}$ and $\mu_p = \mu_n/2.7$ the

¹By Dr. J. Alvarado using Verilog-A language

mobilities of electrons and holes, N_A the doping concentration, $\rho(LET) = LET \cdot (Z_\rho/w)$ is the electron-hole pairs generated by the ion track, LET is the linear energy transfer given in $eV/mg/cm^2$, Z_ρ is the density of the target material (i.e. for silicon $2.33 g/cm^3$), w is the energy necessary to produce one electron-hole pair (i.e. for silicon $3.6 eV/e-h$) and $\nabla\rho_n$ and $\nabla\rho_p$ the gradients of electrons and holes generated by the ion track, t_{si} is the thick silicon body.

The current injected in the body I_{SEU} constitutes the base current of the NPN parasitic bipolar transistor which induces a collector current I_C from the drain to the source of the irradiated N-MOSFET (Fig.3.11).

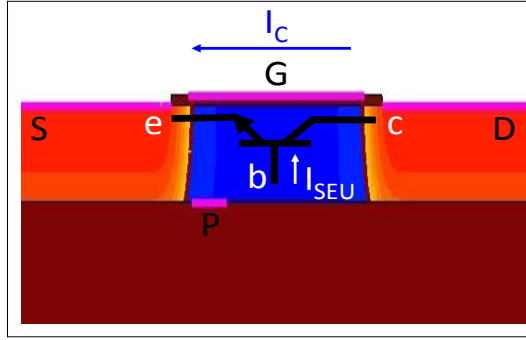


Figure 3.11: Top view of a SOI NMOSFET showing the parasitic bipolar.

The compact model connections for irradiated SOI N-MOSFET are presented in Fig.3.12. The Verilog-A module provides the single event current I_{SEU} to the NMOS body contact (P).

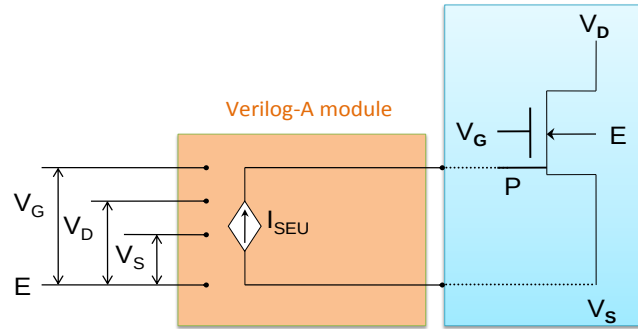


Figure 3.12: Schematic of the proposed compact model connection.

3.2.2 Simulation using the compact model

The compact model allows to simulate radiation effects using merely ELDO software [9]. For a PD SOI N-MOSFET transistor with a length of $1\ \mu\text{m}$, a width of $6\ \mu\text{m}$, at OFF state ($V_{GS} = 0$, $V_{DS} = 4\text{V}$), a LET of $30\ \text{MeV}/\text{mg}/\text{cm}^2$ and three temperatures of 300 K (room temperature), 400 K (125°C) and 500 K (225°C) the compact model gives an induced drain currents as presented in Fig.3.13. It can also be used to simulate the SEE in a complete circuit. For instance, for a 6T-SRAM cell, the compact model can be connected to the struck transistor (Fig.3.14).

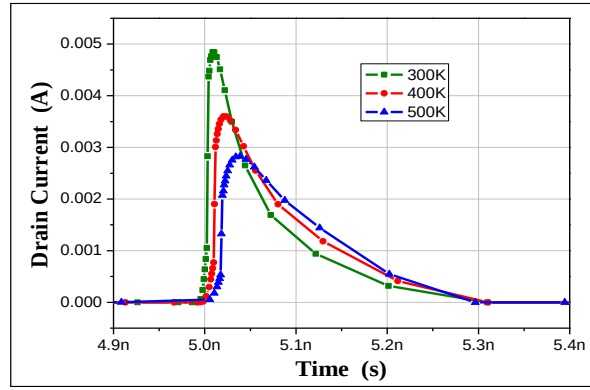


Figure 3.13: Compact model simulation of drain current at $\text{LET}=30\ \text{MeV}/\text{mg}/\text{cm}^2$.

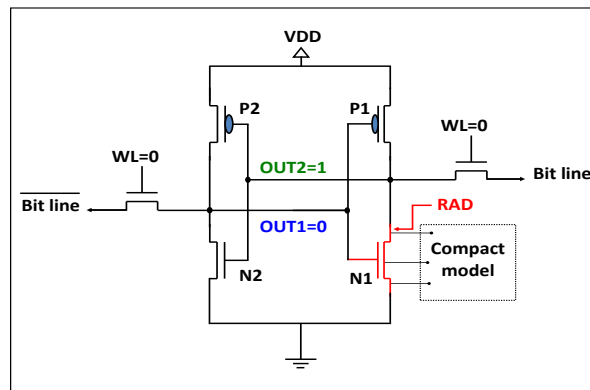


Figure 3.14: 6T-SRAM cell simulation using the compact model.

3.2.3 Comparison between compact model and 2D-TCAD simulations

In order to validate the compact model, its results have been compared to the 2D-TCAD results. Thus, the induced current in a single NMOS transistor and the extracted LET_{th} for a 6T-SRAM have been compared.

3.2.3.1 For single PD SOI N-MOSFET transistor

Figure 3.15 shows a comparison between 2D-TCAD and the compact model results for the induced current by radiation in a PD SOI NMOS transistor ($W=6\text{ }\mu\text{m}$, $L=1\text{ }\mu\text{m}$, $V_{GS} = 0$ and $V_{DS} = 4\text{V}$) at a room temperature (300 K) and a LET of 30 MeV/mg/cm^2 .

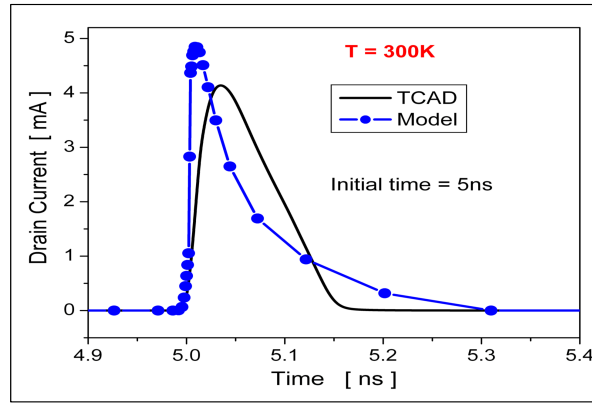


Figure 3.15: Comparison of 2D-TCAD and compact model results at 300 K.

The model does not exactly reproduce the induced current extracted from the 2D-TCAD simulations, but it reproduces the same behavior of induced current. More important, the induced charge² in the transistor is very close for both simulations (Table 3.1).

Table 3.1: Comparison between 2D-TCAD and compact model at 300 K.

Simulator	Max Peak (mA)	Delay at 10% of Max Peak (ps)	Charge (fC)
2D-TCAD	4.14	140	359
Compact model	4.84	180	358

²Equal to the integration of the radiation induced current

Now, by changing the temperature in the simulations, the behavior of the induced current remains the same for both simulators versus temperature (Fig.3.16). Also, as detailed in Table 3.2, the induced charge remains identical versus temperature. This charge is obviously the main factor responsible for the single event upset on the digital circuits. In fact, a SEU occurs when the critical charge value Q_{CRIT} is reached on a sensitive node of the circuit [10]. Thus, the compact model gives the same charge as 2D-TCAD simulations at different temperatures, which allows for reproducing the same threshold LET for different digital circuits.

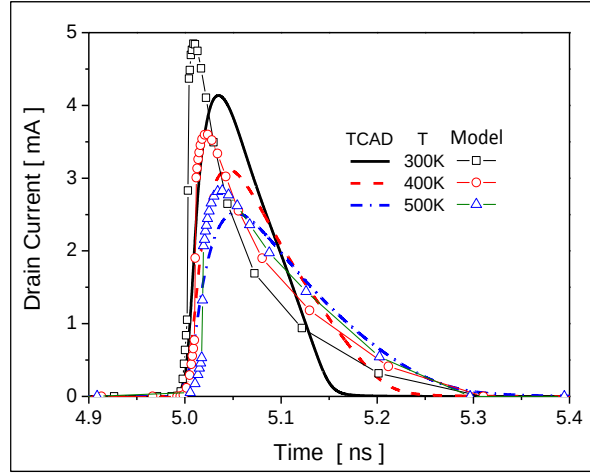


Figure 3.16: Comparison of 2D-TCAD and compact model results at different temperatures [8].

Table 3.2: Comparison of extracted parameters between 2D-TCAD and compact model at different temperatures.

Temp	Max Peak (mA)		Delay at 10% of Max Peak (ps)		Charge (fC)	
	TCAD	Model	TCAD	Model	TCAD	Model
300 K	4.14	4.84	140	180	359	358
400 K	3.10	3.59	200	210	360	364
500 K	2.53	2.81	250	240	361	350

3.2.3.2 For PD SOI CMOS 6T-SRAM cell

The use of the compact model to simulate the radiation effects at different temperatures on a PD SOI 6T-SRAM cell takes less than 1min per SPICE simulation and, yields results very comparable to 2D-TCAD which takes 1 hour per simulation. Table 3.3 shows a fair agreement between LET_{th} versus temperature obtained from both simulators.

In conclusion, the comparison between mixed-mode 2D-TCAD and SPICE simulations for a single PD SOI NMOS transistor and a 6T-SRAM under different temperature conditions shows a good agreement for the proposed compact model. This model is less complicated and requires a smaller simulation time by comparison to the mixed mode 2D-TCAD.

Furthermore, this model could easily be extended to other circuits simulations. This result is of interest to allow for extensive circuit design studies, which cannot be carried out with TCAD physical simulations.

Table 3.3: Comparison of extracted LET_{th} (MeV/mg/cm²) between 2D-TCAD and compact model at different temperatures.

Temperature	LET_{th} extracted by 2D-TCAD	LET_{th} extracted by Compact model
300 K	34	34.5
350 K	33	32.8
400 K	28.5	29
450 K	28	28.2
500 K	26.5	26.8

3.3 Combined effect of temperature and SEE on PD SOI of 1 μm and 130 nm technologies

This section presents and compares the combined effect of temperature and SEE for two PD SOI technologies. The first one has 25 nm thick gate oxide, a 250 nm thick silicon body, a 1 μm thick buried oxide with a 1 μm as minimum channel length and a power supply from 3.3 V to 5 V. The second has a L_{min} of 130 nm, featuring a 5 nm thick gate oxide, a 150 nm thick silicon body, a 400 nm thick buried oxide and a power supply of 2.5 V.

3.3.1 The effect on a single MOSFET transistor

Using the 2D-TCAD simulator, single event effects simulations were performed at different temperatures for both different technologies. Simulations consider a heavy ion as a particle with a radius of 0.1 μm , a deposited energy (LET) of 30 MeV/mg/cm² and a vertical incidence at the drain (Fig.3.17). The drain-to-source voltage $V_{DS} = 4$ V for transistor from older technology, and only 2.5 V for newer transistor ($L_{min} = 130$ nm).

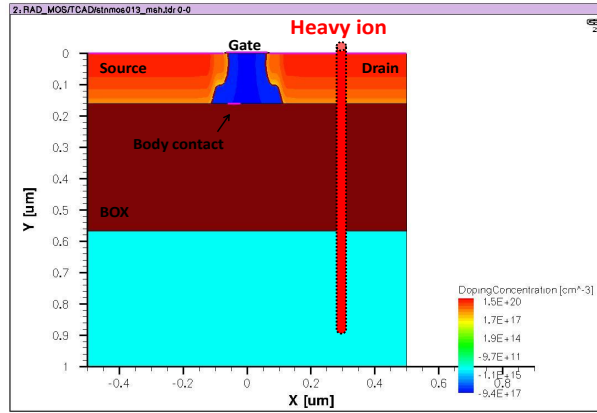


Figure 3.17: Heavy ion crossing the drain with a normal incidence ($W = 1\mu\text{m}$, $L_{min} = 130$ nm).

Figure 3.18 shows the current induced by radiation in a NMOS transistor from the older technology, at a temperature from 300 K (room temperature) up to 500 K (225 °C). Whereas Fig.3.19 shows the same current, for a NMOS transistor from the newer technology, for a temperature range from 150 K (-125 °C) up to 500 K.

For both PD SOI technologies the pulse amplitude of the current induced by SEE I_{SEE} decreases when the temperature increases, while its time delay

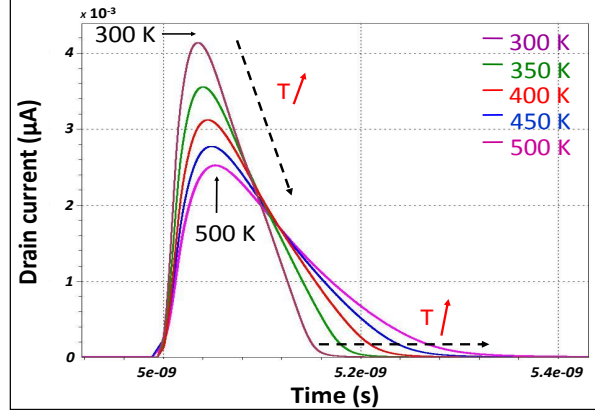


Figure 3.18: Induced current vs time from 300 K up to 500 K ($W = 1\mu\text{m}$, $L_{\min} = 1\mu\text{m}$).

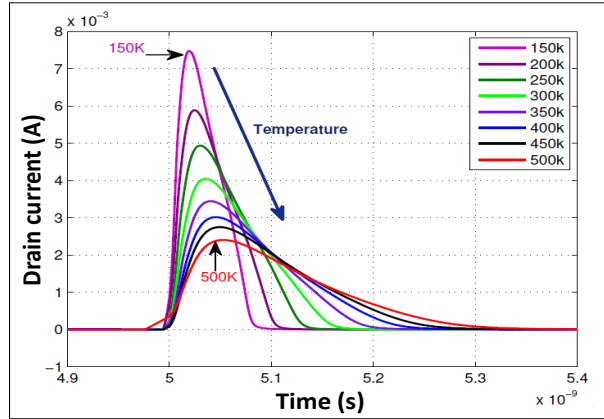


Figure 3.19: Induced current vs time from 150 K up to 500 K ($W = 1\mu\text{m}$, $L_{\min} = 130\text{ nm}$).

defined at 10% of the maximum increases. Similar results have been found in the literature for Bulk technology at temperature up to 418 K (145 °C) [11,12].

Figure 3.20 shows the dependency of the pulse amplitude and the time delay with temperature for the technology with $L_{\min} = 1\mu\text{m}$. This behavior could be explained as follows:

For the maximum current amplitude I_{SEE} , by the average of the electron mobility μ [13]:

$$I_{SEE} = \langle \mu * E_{Field} \rangle * LET \quad (3.4)$$

where E_{Field} is the electric field and LET the energy of the ionized par-

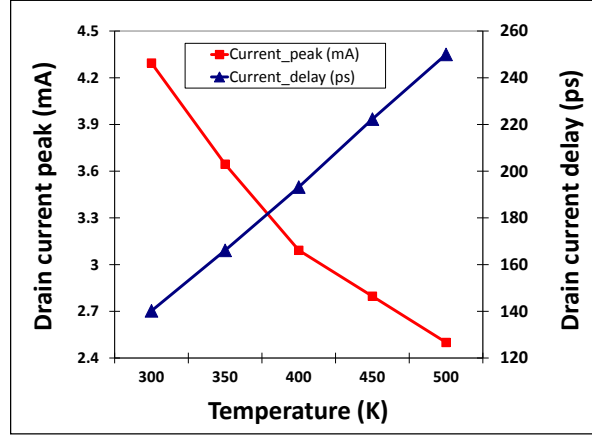


Figure 3.20: Pulse amplitude and delay time versus temperature for a LET of 30 MeV/mg/cm² ($L_{min} = 1 \mu m$).

ticles. The mobility μ decreases with temperature (following $\alpha \propto T^{-\alpha}$ with $1.2 \leq \alpha \leq 1.8$). Figure 3.21 confirms this hypothesis when the pulse amplitude is compared to a curve with an α of 1.3.

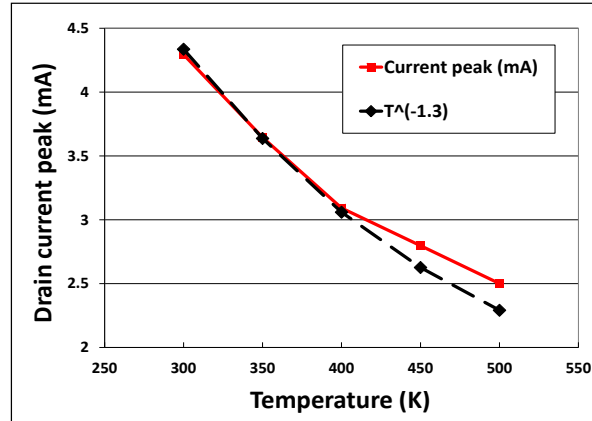


Figure 3.21: Comparison between the pulse amplitude curve for a LET of 30 MeV/mg/cm² and a curve of $T^{-1.3}$ versus temperature ($L_{min} = 1 \mu m$).

For the delay, a first approach used in the literature, is to consider the diffusion current, which depends on the diffusion coefficient D . The later is

related to temperature T and mobility μ by the Einstein relationship [14]:

$$D = \frac{\mu \cdot k \cdot T}{q} \propto T^{\alpha-1} \propto T^{0.3} \quad (\text{for } \alpha = 1.3) \quad (3.5)$$

where q is the electron charge and k the Boltzmann constant. However, as shown in Fig.3.22, this supposition is not sufficient to explain the simulated linear variation of delay as a function of temperature.

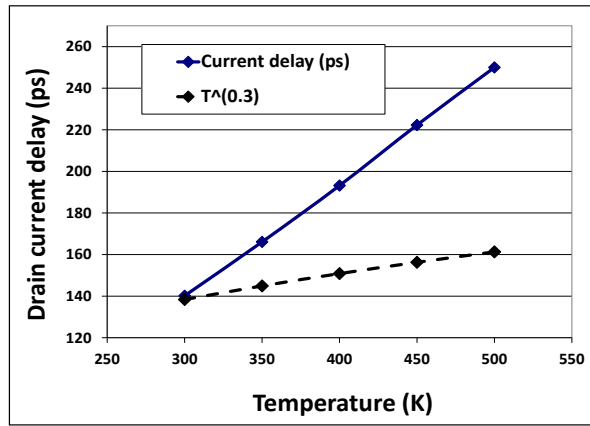


Figure 3.22: Comparison between the delay time curve for a LET of 30 MeV/mg/cm² and a curve of $T^{0.3}$ versus temperature ($L_{min} = 1 \mu m$).

The linear variation of delay as a function of temperature, could be explained by the SOI internal parasitic bipolar, in which the time constant for the return to equilibrium following an on-to-off transient depends on the bipolar gain β . The later parameter increases indeed linearly with temperature. Next paragraph (3.3.1.2) gives more details about parasitic bipolar created during the single event effect in a PD SOI NMOS transistor.

3.3.1.1 Comparison of the two PD SOI technologies versus temperature and SEE

A comparison of the combined effect of the temperature and SEE on both PD SOI technologies is presented in Fig.3.23. The pulse amplitude is always higher in the older technology due: to the bigger electrical field in the transistor ($V_{DS} = 4$ V instead of 2.5 V in new technology), and to the greater sensitive volume in the older technology (250 nm instead of 150 nm thick silicon body). In fact, a bigger sensitive volume means a large number of created electron-hole pairs in the silicon body, which increases both peak and delay of current in the older technology.

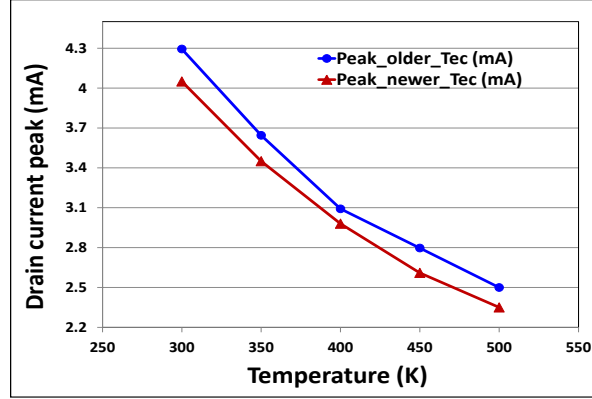


Figure 3.23: Comparison between the pulse amplitude curves of older and newer technologies for a LET of 30 MeV/mg/cm^2 versus temperature.

3.3.1.2 Creation of a parasitic NPN transistor during SEE

When a single PD SOI MOS transistor ($L = 1 \mu\text{m}$) is crossed by a particle, a parasitic bipolar between drain and source with the body contact as base is created (Fig.3.24). To confirm this, the Fermi levels in the transistor have been extracted by simulation. Indeed, the Fermi levels (Fermi(electrons) - Fermi(holes)) of the transistor terminals (body and source) remains unchangeable before and after radiation. But increases by 1 V during the radiation time (Fig.3.25). This extracted Fermi level corresponds to the body-to-source voltage V_{BS} , which also corresponds to the base-to-emitter voltage V_{be} of the parasitic transistor.

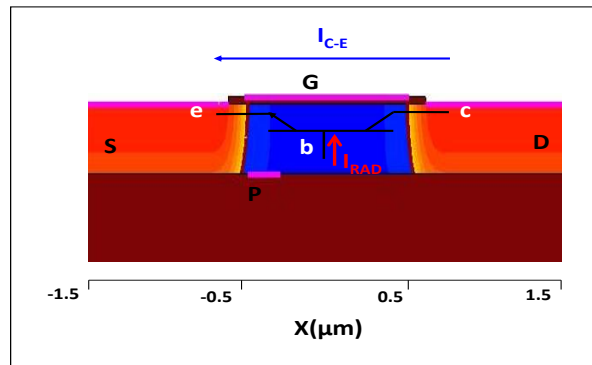


Figure 3.24: SOI N-MOSFET structure showing the parasitic bipolar transistor.

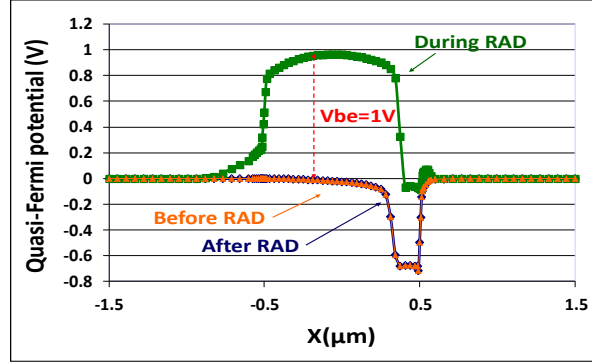


Figure 3.25: Quasi Fermi potential of irradiated transistor ($L_{min} = 1 \mu m$).

Thus, using the Fermi level of the transistor terminals, the creation of the parasitic bipolar during radiation has been proved for this older PD SOI technology. However, to confirm this creation of parasitic bipolar in different PD SOI technologies, the same simulations and extraction of Fermi levels were performed for the newer PD SOI technology ($L_{min} = 130 \text{ nm}$). Finally, as shown in extracted Fermi levels (Fig.3.26), the creation of parasitic bipolar was again confirmed for this newer technology.

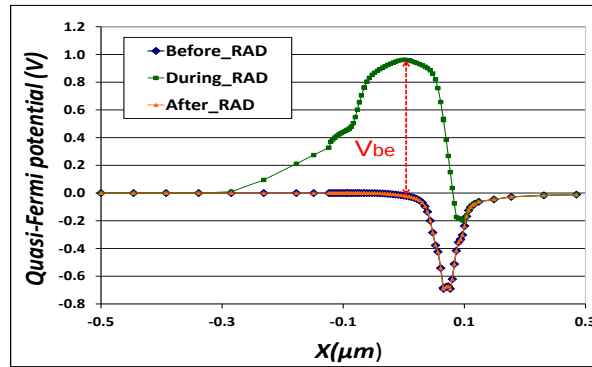


Figure 3.26: Quasi Fermi potential of irradiated transistor ($L_{min} = 130 \text{ nm}$).

Additional simulations to confirm these effects were stopped when we found papers from the literature confirming the parasitic bipolar creation during the radiation [15, 16].

3.3.1.3 Induced charge by the radiation versus temperature

The charge induced by SEE in a PD SOI NMOS transistor corresponds to the integral of induced current ($\int_{SEE}$). This charge versus temperature have been extracted using 2D-TCAD simulations (Fig.3.27). The induced charge increases slightly with the temperature, even if the LET remains unchanged (30 MeV/mg/cm²). This could be explained by the parasitic bipolar transistor, which induced more current with temperature.

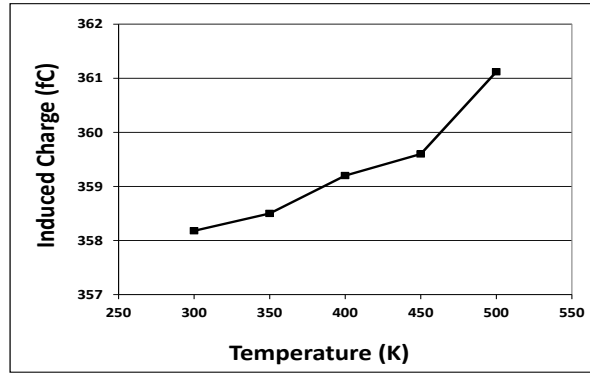


Figure 3.27: Induced charge for a LET of 30 MeV/mg/cm² ($L_{min} = 1 \mu m$).

3.3.2 The effect on a standard CMOS 6T-SRAM cell

To evaluate the combined effect of temperature and SEE on a digital circuit, a PD SOI 6T-SRAM cell from the older technology has been considered. It has 6 μm and 12 μm channel widths for NMOS and PMOS transistors respectively, and 1 μm channel length, with a power supply of $V_{DD} = 4$ V. 2D-TCAD Mixed mode simulations are used to extract the LET_{th} versus temperature (Fig.3.28-a).

As a conclusion, when the temperature increases, the LET_{th} is directly decreased. Therefore, the SEU sensitivity of the 6T-SRAM is increased with the temperature. This, can partly be explained, as cited in a previous work [11], by the decrease of the threshold voltage value V_{th} with temperature, and partly by the increase of the collected charge as discussed above (due to parasitic bipolar).

The same mixed mode simulations are performed for a similar 6T-SRAM cell, designed in the newer technology (L_{min} of 130 nm), with a power supply of only $V_{DD} = 2.5$ V. Figure ??-b shows the same impacts on the SRAM cell as the previous technology (L_{min} of 1 μm). When the temperature increases, the LET_{th} decreases from 29 MeV/mg/cm² at 150 K up to 22 MeV/mg/cm²

at 500 K. As a result, the SEU sensitivity of the 6T-SRAM also increases with temperature.

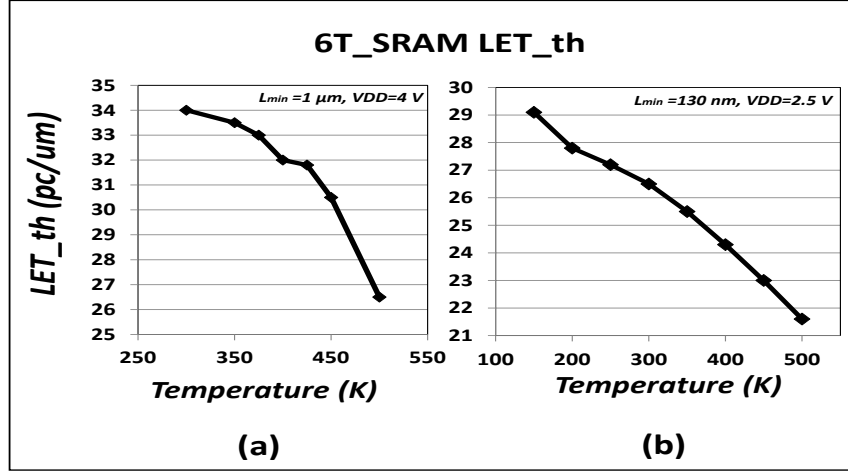


Figure 3.28: Extracted LET_{th} for a 6T-SRAM cell versus temperature (a) with $L_{min} = 1 \mu m$ and $VDD = 4 V$, (b) with $VDD = 2.5 V$ and for $L_{min} = 130 nm$.

By comparing both PD SOI technologies, we conclude that, the 6T-SRAM cell from the older technology is more robust to SEE at different temperatures. In fact, as shown in Table 3.4, the LET_{th} is always lower in the newer technology. This can be explained by the higher power supply and higher nodes capacitance in the older technology. As shown in Chapter 5, these two features are used as mitigation techniques against SEE on the integrated circuits.

Table 3.4: Comparison of the LET_{th} in " $MeV/mg/cm^2$ " between older and newer technologies at different temperatures.

Temp	LET_{th} for older technology ($L_{min}=1 \mu m$)	LET_{th} for newer technology ($L_{min}=130 nm$)
300 K	34	26.6
350 K	33.5	25.6
400 K	32	24.3
450 K	30.5	23
500 K	26.5	21.7

As a conclusion of this section, the combined effect of temperature and SEE always increase the sensitivity of PD SOI digital circuits to transient radiation effects.

3.4 Measurements of SEE effects

The single event effects measurement can be performed using the beam lines of the UCL cyclotron, Louvain-la-Neuve, Belgium. Five beam lines are available; Light Ion (Protons) Irradiation Facility (LIF), Laser Facility, Gamma Irradiation Facility (GIF), Heavy Ion Irradiation Facility (HIF), and Neutron (monoenergetic neutrons) Irradiation Facility (NIF) [17]. During this thesis, the last three facilities were used for our measurements.

3.4.0.1 Heavy-ions tests using HIF

The heavy-ions tests are performed in a vacuum chamber (Fig.3.29). The covered energy range is between 0.6 MeV/AMU and 27.5 MeV/AMU (Atomic Mass Units). There are two types of heavy-ions, one type with a high LET energy, and the other one with a high penetration. Tables 3.5, 3.6 show the existing particles for this beam line [17].



Figure 3.29: HIF measurements chamber.

In our case, a high LET energy has been used to check transient radiation effects for 1 μm PD SOI CMOS 4-Nand flip-flop (3.30). The tests were performed at room temperature in steady state condition, inducing a high level output value (3.3, 4 or 5V) via the asynchronous inputs, whereas the synchronous inputs were preserved at low level. A LabView [18] program has been developed to control the oscilloscope, in order to catch every transient effect on the flip-flop output. However due to the small sensitive area of the 4-Nand flip-flop ($< 0.1 \mu\text{m}^2$) and to the limited number of particles available in this beam (a max of 10^4 part/s.cm² [17]) no SEE was detected during the tests. In

Table 3.5: HIF particles with high LET energy [17].

M/Q=5	DUT energy [MeV]	Range [$\mu\text{m Si}$] (penetration)	LET [Mev/mg/cm ²]
¹²⁴ Xe ²⁵⁺	420	37	67.7
⁸⁴ Kr ¹⁷⁺	305	39	40.4
⁸³ Kr ²⁵⁺	756	92	32.6
⁴⁰ Ar ⁸⁺	151	40	15.9

Table 3.6: HIF particles with high penetration [17].

M/Q=5	DUT energy [MeV]	Range [$\mu\text{m Si}$] (penetration)	LET [Mev/mg/cm ²]
¹³ C ⁴⁺	131	292	1.1
²²⁴ Ne ⁷⁺	235	216	3
⁴⁰ Ar ¹²⁺	372	117	10.2
⁵⁸ Ni ¹⁸⁺	567	100	20.4

fact, with a small sensitive area less than $0.1 \mu\text{m}^2$, the 4-Nand flip-flop needs at least a time of exposition higher than 10^5s (13.9 hours) to be crossed by one particle and induces an SEE.

To overcome this issue, new measurements have been performed in the Neutron Irradiation Facility, which has a higher fluence. Next paragraph gives the obtained results.

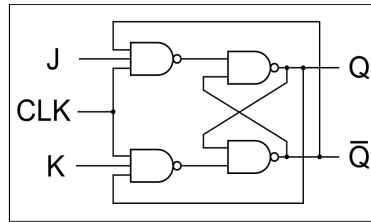


Figure 3.30: 4-Nand flip-flop circuit.

3.4.0.2 Proton-Neutrons tests using NIF

The neutron irradiation has been performed at the Neutron Irradiation Facility (NIF) with similar conditions than the HIF tests. Using the previous LabView program, single event transients (SET) were detected in the 4-Nand flip-flop at

different power supplies $V_{dd}=3.3$ V, 4 V and 5 V (Fig.3.31 for 5 V). Whereas single event upsets (SEU) were detected only at 3.3V as is shown in Fig.3.32.

The low power supply appears to be more sensitive to the single event effects, this is in agreement with modeling/simulations results which predict a lower threshold LET for a lower power supply case [19].

This increment in the probability to hit the sensitive nodes is due to two reasons; first, to the higher number of particles available in the neutron beam (2.10^{13} n/s.cm² [17]) than in the heavy ion beam (10^4 part/s.cm²), with which we were not able to detect any SET or SEU in the 4-Nand flip-flop. Secondly, to the secondary particles created by the high number of neutrons, which have a greater possibility to pass through the small sensitive area and induce a SET or SEU depending on the bias condition.

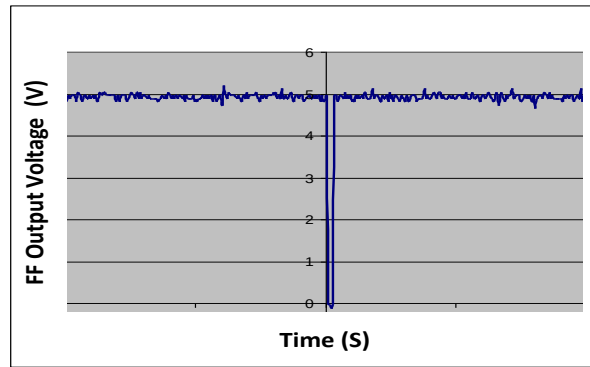


Figure 3.31: SET on the output of the 4-Nand flip-flop $V_{dd}=5$ V.

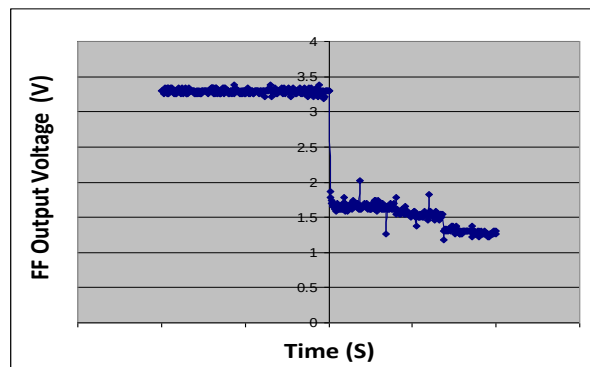


Figure 3.32: SEU on the output of the 4-Nand flip-flop at $V_{dd}=3.3$ V.

3.5 Comparison between experimental and simulated results

Figure 3.33 shows the experimental results of a UCL SRAM cell (Fig.3.34) used in the UCL 80C51 micro-controller [20]. For a power supply of 2.4 V, the $LET_{th} = 60 \text{ MeV/mg/cm}^2$. This value have been compared to simulated LET_{th} from 2D-TCAD and the compact model.

During the measurement, the 80C51 has an internal addressing space of 256 bytes, on hold state (WR=RD=0, IN=0, VDD=2.4 V), 50% of the memory cells are at "1" logic (OUT=1) and the other 50% are at "0". Thus, in order to simulate the 80C51 SRAM cell, and to match simulations with the measurements, both cases of memory (OUT=0 and OUT=1) have been studied:

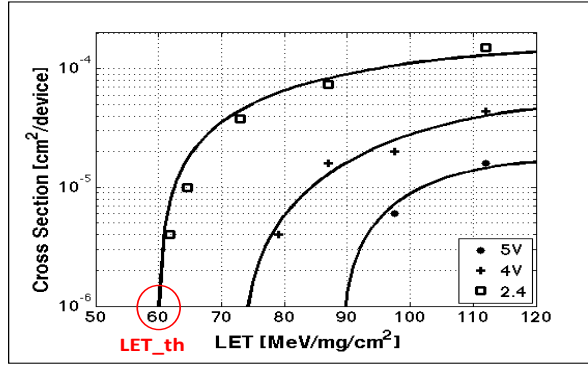


Figure 3.33: Cross section of the 8051 SRAM versus LET [20].

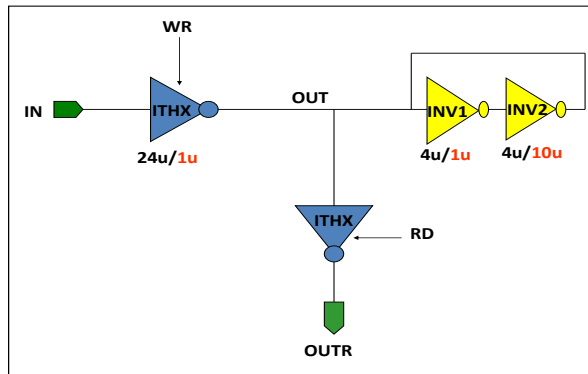


Figure 3.34: Schematic of 80C51 SRAM cell.

Case of $OUT=0$:

In this case, as shown in Fig.3.35, two upset scenarios can happen, one from the first inverter INV1 and one from the tristate inverter ITHX (Fig.3.36). The LET_{th} in this case can be calculated by the minimum of both scenarios:

$$LET_{th}(OUT = 0) = \min[LET_{th}(\text{scenario1}), LET_{th}(\text{scenario2})] \quad (3.6)$$

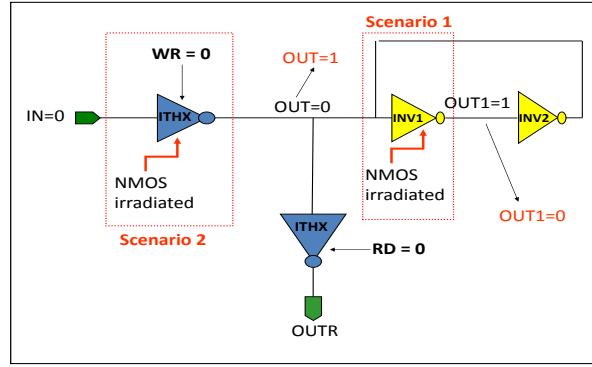


Figure 3.35: SEU scenarios for the case $OUT=0$.

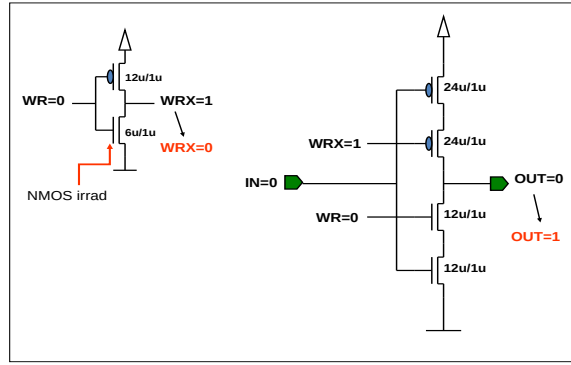


Figure 3.36: SEU 2nd scenario with ITHX strike.

Case of $OUT=1$:

In this case, just one upset scenario can happen, which corresponds to the second inverter INV2 being struck (Fig.3.37). Therefore, the LET_{th} of the 80C51 SRAM cell can be calculated as the minimum of both cases ($OUT=0$ and $OUT=1$):

$$LET_{th}(SRAM_{80C51}) = \min[LET_{th}(OUT = 0), LET_{th}(OUT = 1)] \quad (3.7)$$

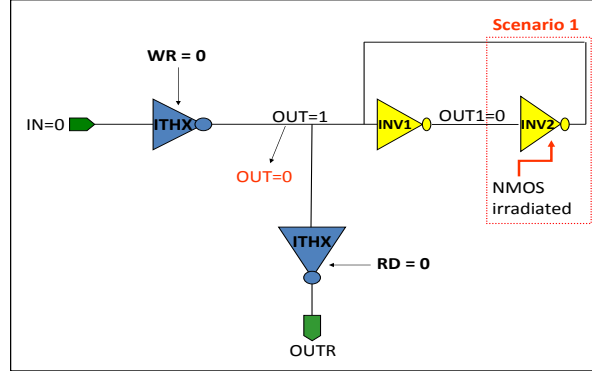


Figure 3.37: SEU scenario for the case $OUT=1$.

The following table shows a comparison between simulated and measured LET_{th} for the 80C51 SRAM at room temperature (25°C) :

Table 3.7: Comparison between simulated and measured LET_{th} for the 80C51 SRAM.

Case ($V_{dd} = 2.4 \text{ V}$)	LET_{th} ($\text{MeV}/\text{mg}/\text{cm}^2$)
Case1 ($OUT=0$)	95
Case2 ($OUT=1$)	> 300
Min (Case1, case2)	95
Measurements	60

The first simulation results at room temperature using the typical 2D-TCAD (Table 3.7) have shown a higher LET_{th} versus the measurements. To understand this difference, and in order to match simulated and measured LET_{th} , several hypotheses have been investigated:

- The measured chips were either in fast or slow process corner.
- During the test, the temperature of the transistors junction can reach more than 25°C due to the chip operation and radiation environment and particles, for instance, 35°C .

- The position and direction of the particles hit during measurements are different from our simulations.
- During the measurements, more than one particle can hit the transistor and create an Upset with less energy.
- Conditions of measurement. For example, a damage of oxide/silicon due to particles.

Checking the first hypothesis requires a new 2D-TCAD structure for each simulated corner, and takes a lot of time. Therefore, the compact model is used to simulate the radiation on the 80C51 SRAM cell at different process corners at a temperature of 35 °C. Thereby, in the fast corner case (low V_{th}), a LET_{th} closer to the experiments has been obtained (Table 3.8).

Table 3.8: Comparison between simulated and measured LET_{th} for the 80C51 SRAM under different process conditions.

Case (Vdd = 2.4 V)	LET_{th} (MeV/mg/cm ²)
2D-TCAD typical corner simulation at 25 °C	95
Compact model fast corner simulation at 35 °C	64
Measurements	60

As shown in the previous comparisons, several hypotheses and scenarios have to be studied and simulated before being able to find a match between the results from measurements and simulations. Using the compact model gives a fast way to find the correct LET_{th} of the digital circuits.

3.6 Conclusion

Simulations of single event effects using the Sentaurus 2D-TCAD simulator have been detailed in the first part of this chapter.

Secondly, a compact model which allows to easily simulate SEE compared to 2D-TCAD is presented. A good matching has been shown between results from this compact model and Sentaurus 2D-TCAD at different temperatures.

Thirdly, the combined effect of temperature and SEE is discussed for two different PD SOI technologies featuring minimum channel lengths of 1 μm and 130 nm. For a single MOSFET transistor, SEE simulations have shown a decrease of the pulse amplitude of the induced current I_{SEE} , and an increase of its time delay. This leads to a slight increase in the induced charge in the simulated transistor.

The 6T-SRAM cell has shown to be more sensitive to radiation when the temperature increased. This, can be explained by: 1) the increase in the collected charge in the devices, 2) the reduction of the threshold voltages of transistors with temperature, 3) the parasitic bipolar transistor created by radiation in such PD SOI technologies, which also increases the induced current in the transistor. Based on these results, we can conclude that PD SOI digital circuits become more sensitive to single event effects (SEE) when the temperature increases.

Fourthly, different types of SEE measurements and experimental results for a standard 4-Nand flip-flop were exposed. By the end, a good matching has been demonstrated between measured and simulated LET_{th} for an UCL SRAM used in the UCL 80C51 micro-controller.

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CHAPTER 4

Combined effect of total ionizing dose and high temperature in analog IC

SINGLE event effects at different temperatures have been simulated and detailed in the previous chapter for digital CMOS circuits, designed in two different PD SOI technologies (with $L_{min}=1\text{ }\mu\text{m}$ and $L_{min}=130\text{ nm}$). Using the same technologies, this chapter studies experimentally the combined effect of total ionizing dose (TID) and high temperature for analog CMOS circuits.

The first part of this chapter shows how to simulate the TID effects on MOS transistors. The second part shows the measured impact of TID for a microsystem composed of three ultra low-power circuits: a voltage reference, a temperature sensor, and a comparator designed in the older PD SOI technology with $L_{min}=1\text{ }\mu\text{m}$. The last part studies the combined effect of TID and temperature for a designed ultra low power voltage reference, and for single MOSFET transistors available in the 130 nm PD SOI technology.

4.1 Simulations of TID effects

TID effects of radiation could be simulated by using Sentaurus ISE-TCAD, as used in SEE effects. However, as the impacts of TID effects on semiconductor devices are mainly the degradations of mobilities and the shift of threshold voltages, these effects could be included directly in the BSIM model parameters of transistors. Thereby, the SPICE simulator could be used to simulate TID effects, which is very helpful and less time consuming than using the Sentaurus ISE-TCAD. The following instructions show how to introduce a shift δV_{th} in the threshold voltage and a degradation of the mobility $\delta\mu_{mob}$ in the BSIM model parameters of a NMOS transistor in PD SOI technology.

```
param vth0eff = 'vth -  $\delta V_{th}$ '  
param u0eff = 'mobility* $\delta\mu_{mob}$ '
```

If a dependency between voltage threshold shift and mobility degradation has to be included, the expression becomes :

param vth0eff = 'vth - δV_{th} '

param u0eff = 'mobility*(1 - δV_{th})'

An example of TID simulation on a 130 nm PD SOI transistors is shown in Fig.4.1 and 4.2. The typical DC $I_D(V_{GS})$ and $\log(I_D(V_{GS}))$ characteristics are simulated at 25 °C with (squares) and without (circles) TID effects. In this case, a shift of $\delta V_{th}=250$ mV and a mobility degradation of $\delta\mu_{mob}=25\%$ are considered. The checked MOSFET transistors (N and P) have a channel width and length of $W=2.5\text{ }\mu\text{m}$, $L=0.5\text{ }\mu\text{m}$ respectively, and a drain to source voltage (V_{DS} , V_{SD}) of 50 mV. Curves $\log(I_D(V_{GS}))$ show the included shift of the threshold voltage V_{th} , whereas $I_D(V_{GS})$ curves show the mobilities degradation of MOSFET transistors. This technique has been used in the following sections to simulate the TID effects in the different circuits.

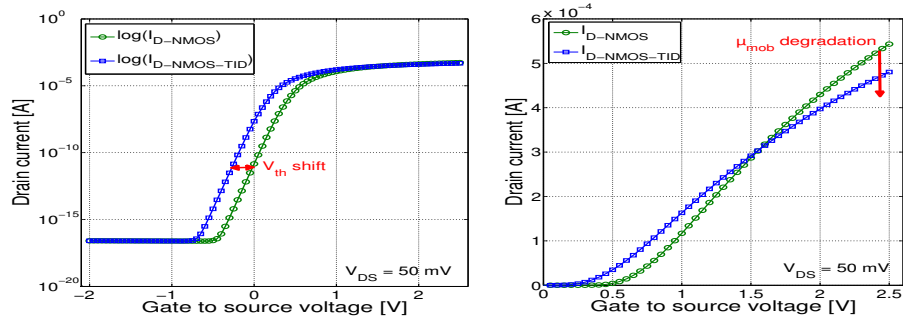


Figure 4.1: Simulated $I_D(V_{GS})$ curves of NMOS ($W=2.5\text{ }\mu\text{m}$, $L=0.5\text{ }\mu\text{m}$), with ($\delta V_{th}=250$ mV, $\delta\mu_{mob}=25\%$) and without TID effects at 25 °C.

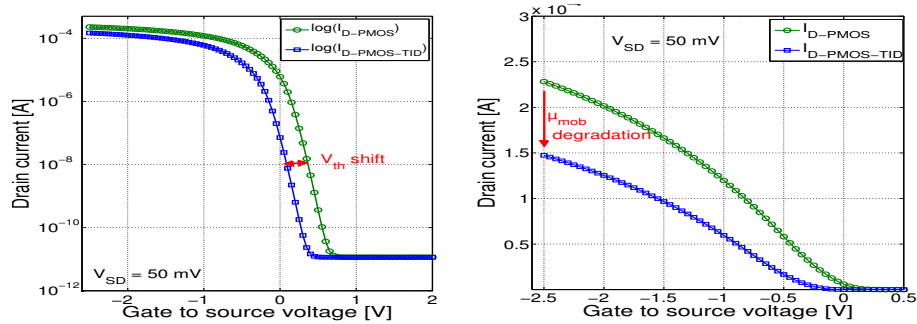


Figure 4.2: Simulated $I_D(V_{GS})$ curves of PMOS ($W=2.5\text{ }\mu\text{m}$, $L=0.5\text{ }\mu\text{m}$), with ($\delta V_{th}=250$ mV, $\delta\mu_{mob}=25\%$) and without TID effects at 25 °C.

4.2 Measurements of TID effects on 1 μm PD SOI technology

Measurement of TID effects is usually performed in the Gamma Irradiation Facility (GIF) of the UCL cyclotron [1]. Three sources, Cobalt ^{60}Co and Caesium ^{137}Cs are used to generate Gamma rays (Fig.4.3). The maximum dose rate for this facility is about 10 krad (Si)/hour [2]. When higher doses were required, irradiation tests have been performed in the "Institut National des Radioéléments" (IRE) [3], Fleurus, Belgium. The next paragraphs show measurement results of an ultra low-power microsystem used for biomedical applications. Irradiated at the IRE facility up to a dose of 30 kGy (3 Mrad(Si)).

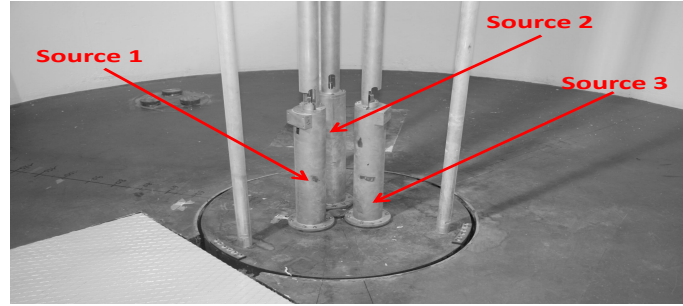


Figure 4.3: UCL Gamma Irradiation Facility [2].

4.2.0.3 ULP Microsystem tests

An ultra-low-power, harsh environment microsystem (ULP-MST) designed¹ using the 1 μm PD SOI technology [4], is tested before and after the TID effects. This microsystem has three main functions: firstly it detects a user-defined temperature threshold T_0 , secondly it generates wake-up signal turns on a data-acquisition microprocessor, and thirdly it operates as a temperature sensor in a harsh environment. Figure 4.4 shows the analog part of this microsystem, which is composed of three ultra low-power CMOS circuits: a voltage reference, a temperature sensor, and a comparator. These circuits have been optimized to operate in the subthreshold regime of the transistors in order to achieve an ultra low-power dissipation (less than 100 μW) at high temperature (up to 250 $^{\circ}\text{C}$). The first part of this paragraph presents the designs and the simulation results of the three circuits. The second part shows the measurements results of the three circuits before and after a 10 to 30 kGy irradiation dose. The last part discusses the annealing effect on the circuits and draws conclusions.

¹By Dr. M. Assaad, UCL

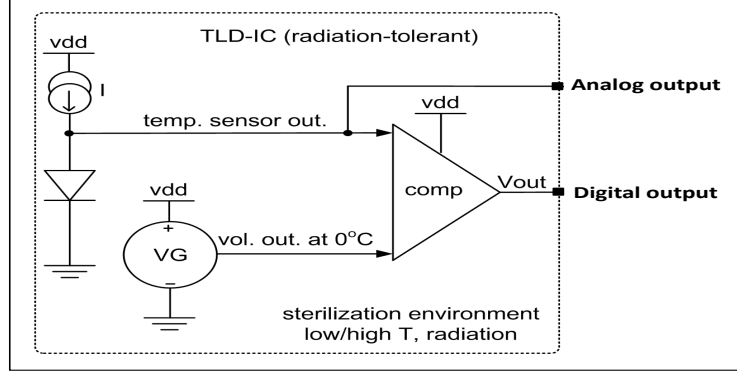


Figure 4.4: ULP-MST block diagram.

A) Circuits design and simulations results The design of blocks used in this microsystem have been developed in a $1\ \mu\text{m}$ partially-depleted (PD) SOI CMOS technology for a supply voltage of 5 V, and a temperature range of $-50\ ^\circ\text{C}$ to $250\ ^\circ\text{C}$.

A1- Voltage reference circuit: The voltage reference circuit (Fig.4.5) used in this microsystem is a CMOS design circuit based on a gate-to-source voltage difference between a pair of PMOS and NMOS transistors [5]. On the contrary to this previous work, in our case, the transistors are optimized to work in subthreshold regime. To be noted that the resistor R_B is an external resistor for tuning capability .

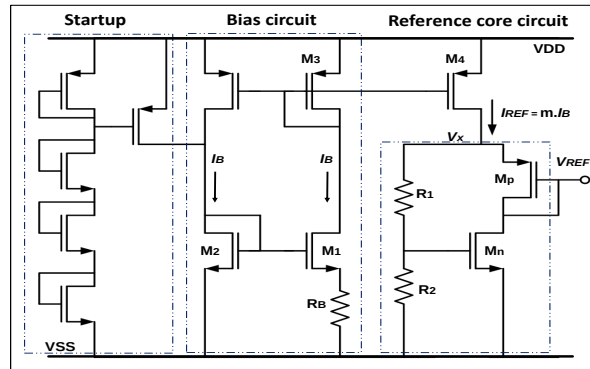


Figure 4.5: Voltage reference circuit.

From the Fig.4.5, the voltage reference value V_{REF} can be expressed directly

as :

$$V_{REF} = \left(1 + \frac{R_1}{R_2}\right) \cdot V_{GSn} - V_{GSp} \quad (4.1)$$

In this design, one of the main specifications is the temperature dependency of the voltage reference V_{REF} which has to be as low as possible, particularly at the temperature threshold T_0 of the application. The aforesaid dependence is expressed by evaluating the temperature coefficient (TC), and it is defined at T_0 by the following expression:

$$TC_{T_0} = \left(\frac{1}{V_{REF}}\right) \cdot \left[\frac{dV_{REF}}{dT}\right] \quad (4.2)$$

The simulation results of V_{REF} give an average voltage of about 2 V (Fig.4.6), with a temperature coefficient lower than 55 ppm/°C for the temperature range of -25 °C to 50 °C which is the initially required application range (Fig.4.7). The simulation shows a TC lower than 1000 ppm/°C (i.e. 1 mV/°C) for the total temperature range from -40 °C to +300 °C. The current consumption is about 3.05 μ A at 100 °C, and the power dissipation is lower than 40 μ W at the highest temperature of 300 °C (Fig.4.12).

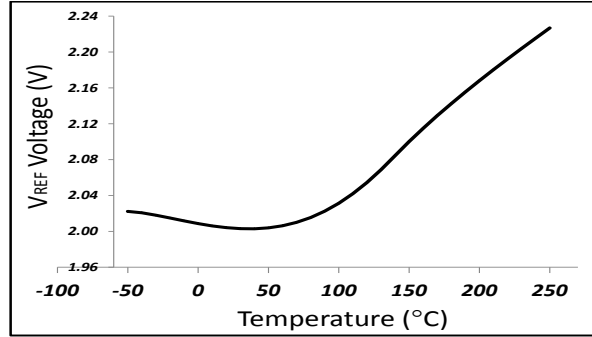


Figure 4.6: Simulated voltage reference V_{REF} vs temperature.

A2- Temperature sensor circuit: The second proposed circuit (Fig.4.8) is a diode-based temperature sensor composed of a current source driving a contact current on three series diodes. The current source is similar to that used in the previous voltage generator circuit, with transistors optimized to operate in subthreshold regime. The simulation of the diode used in this technology shows a voltage slope versus temperature of 2 mV/°C. Thus, the three series diodes give a quasi linear characteristic versus temperature with a slope of 6 mV/°C (Fig.4.9). The current consumption of this circuit is of about 0.4 μ A at room temperature, and the power dissipation remains lower than 20 μ W at high temperature (250 °C) with a power supply of 5 V (Fig.4.12).

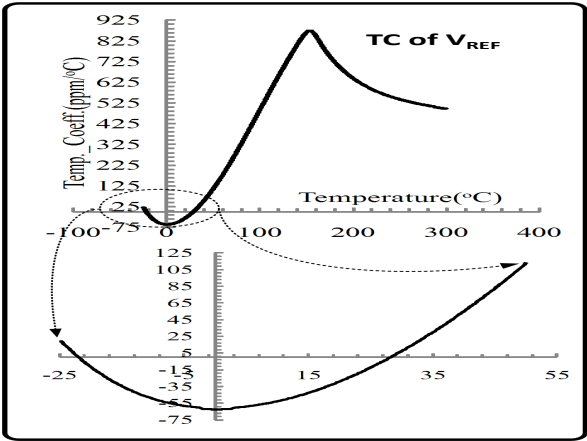


Figure 4.7: Simulated temperature coefficient vs temperature [4].

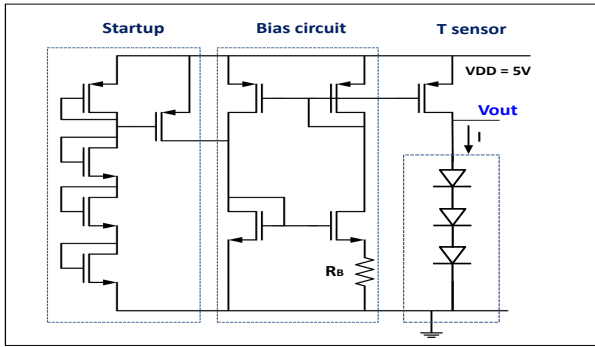


Figure 4.8: Temperature sensor circuit.

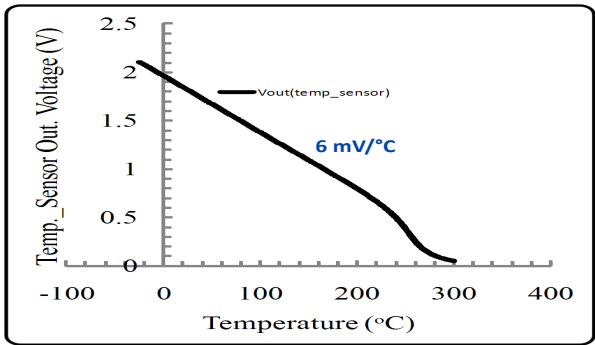


Figure 4.9: Simulated temperature sensor output voltage vs temperature [4].

A3- Comparator circuit: The comparator circuit (Fig.4.10) is a traditional 2-stages based comparator [6]. The comparator design uses the same bias current circuit as both previous circuits, always with transistors optimized to operate in subthreshold regime. This leads to a biasing current of about $2.11 \mu\text{A}$ at room temperature and lower than $40 \mu\text{W}$ at $+300^\circ\text{C}$ at a 5 V power supply (Fig.4.12). As illustrated in Fig.4.11, the comparator generates a wake-up signal when the sensor output voltage passes below the V_{REF} at the threshold level of temperature T_0 (corresponding to 0°C); this turns on a power switch and hence the remote microprocessor.

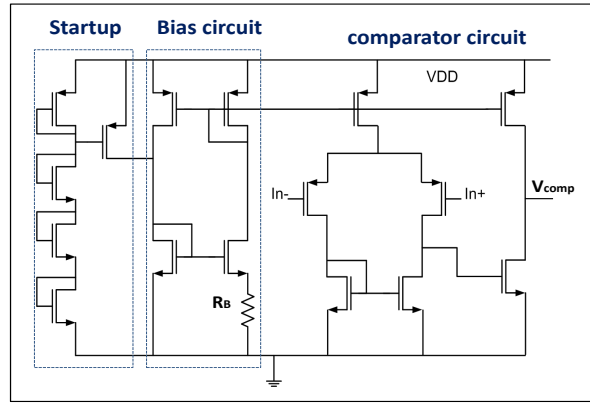


Figure 4.10: Comparator circuit.

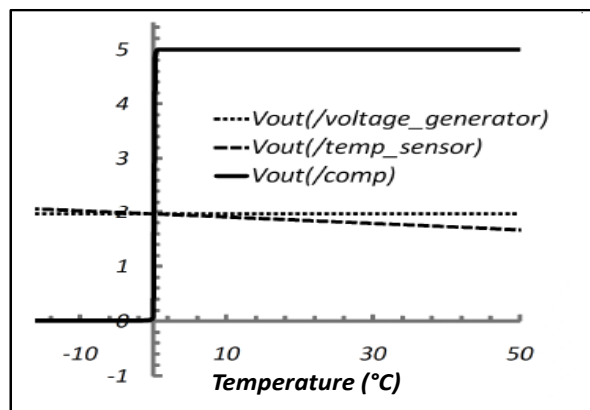


Figure 4.11: Simulated output voltages of the microsystem [4].

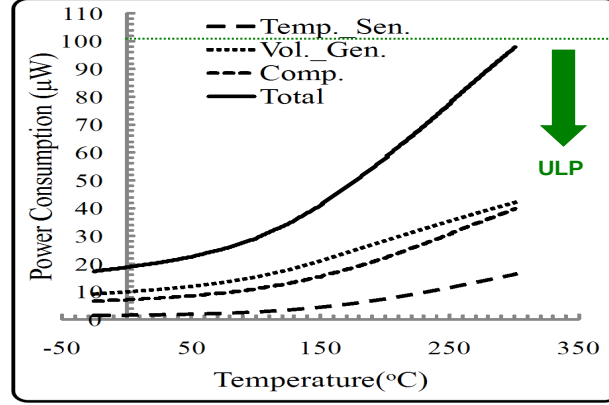


Figure 4.12: Simulated power consumption versus temperature [4].

B) Measurement results and Annealing effects on the circuits The main application of the microsystem is to operate under harsh environments such as high ranges of temperature and radiations. To validate this feature, the simulation results were first confirmed by measuring the microsystem outputs in a large range of temperatures from -40°C to $+300^{\circ}\text{C}$. After that, some chips of the microsystem were exposed to radiation up to total doses of 10 kGy (i.e. 1 Mrad(Si)), 20 kGy and 30 kGy, and were tested again at a temperature range of -40°C to $+125^{\circ}\text{C}$.

B1- Measurements before radiation: Figure 4.13 presents the measurements of the microsystem outputs versus temperature. As expected, the comparator shifts from 0 to 5 V at the temperature threshold $T_0 = 0^{\circ}\text{C}$, and the temperature sensor has a quasi-linear characteristic versus temperature with a slope of $5.4 \text{ mV}/^{\circ}\text{C}$ for the temperature range of -40°C to $+250^{\circ}\text{C}$. But, for the initially required temperature range (-25°C to $+50^{\circ}\text{C}$), the slope is closer to the theoretical value of $6 \text{ mV}/^{\circ}\text{C}$. The total current consumption of the microsystem versus temperature remains lower than $20 \mu\text{A}$ (i.e. $100 \mu\text{W}$ for a 5 V power supply) at $+250^{\circ}\text{C}$ (Fig.4.14). Thus, the microsystem corresponds to an ultra low power application up to $+250^{\circ}\text{C}$. The measured chips were exposed to radiation at the IRE facility and re-measured. The next paragraph shows the measurement results after radiation.

B2- Measurements after radiation: As a result of irradiation, the output voltage values for the temperature sensor and the voltage reference V_{REF} were shifted down (Fig.4.15,4.16). Fortunately, the output characteristic of the temperature sensor remained quasi linear versus temperature with the

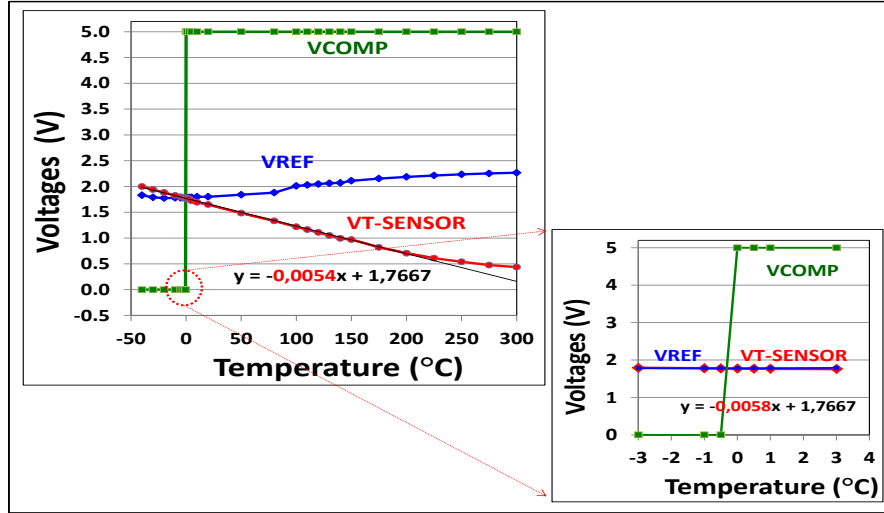


Figure 4.13: Measured output voltages of the microsystem.

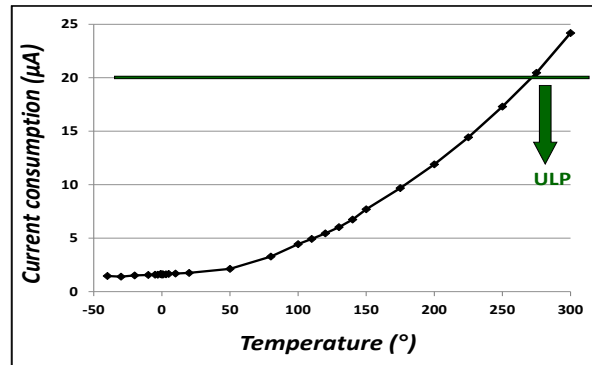


Figure 4.14: Measured current consumption vs temperature of the microsystem.

same slope as before the irradiation (Fig.4.15). However, these voltages shift down led to a change of the temperature detection level from $T_0 = 0^\circ\text{C}$ to 60°C (Fig.4.17), which disturbed the microsystem detection functionality. The measured current consumption for 6 different chips at three irradiation doses of 10, 20 and 30 kGy (3 MRad(Si)) at room temperature, was increased by more than six times (Fig.4.18), but it remains lower than $20\ \mu\text{A}$, measured at the high temperature of 275°C and $25\ \mu\text{A}$ at 300°C .

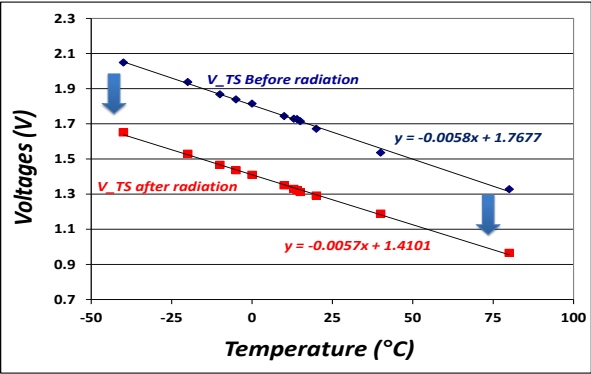


Figure 4.15: Measured temperature sensor output before and after 30 kGy TID.

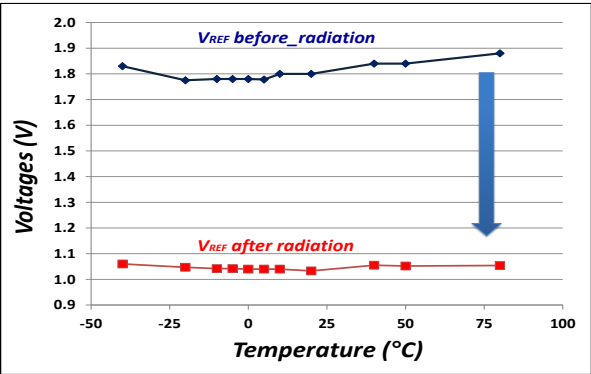


Figure 4.16: Measured voltage reference before and after 30 kGy TID.

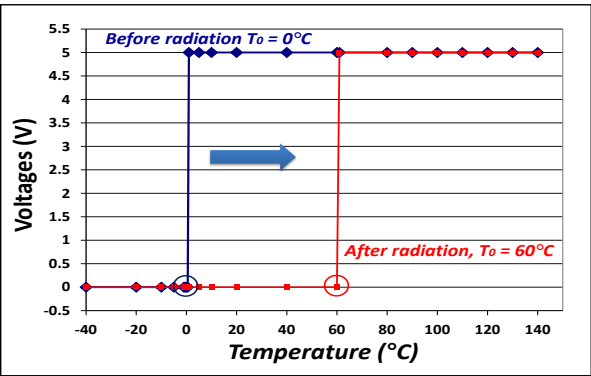


Figure 4.17: Shift of level detection from 0 to 60°C after 30 kGy TID.

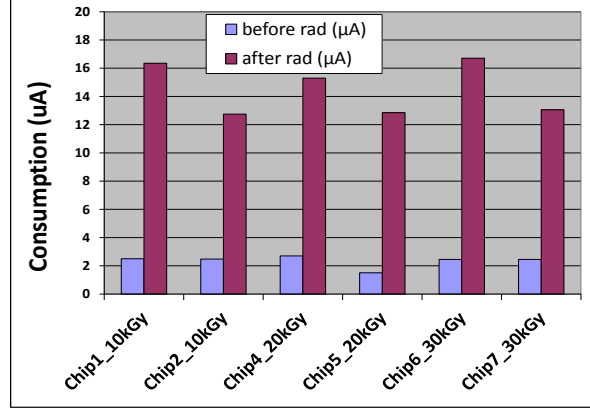


Figure 4.18: Measured microsystem consumption before and after TID at 25°C.

B3- Measurements discussion: After exposition to radiation, the current consumption of the circuits is increased, however instead to be increased the output voltage values are lowered. The designed schematics have been analyzed, and the increase of the current can be explained by the startup and bias circuits present in the schematics of the microsystem (Fig.4.19). In fact, after radiation the voltage threshold of the NMOS transistors V_{th_n} is lowered, this decreases the gate voltage ($V_{st}=3*V_{th_n}$) of the PMOS transistor M_{st} . This leads to increase its drain current I_{st} . Thus, the bias currents (I_B and I_{REF}) are increased after TID and increases the the microsystem current consumption.

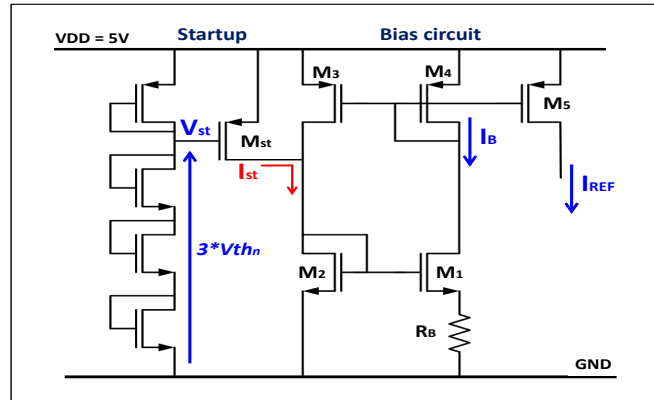


Figure 4.19: Startup and bias circuit used in design of microsystem circuits.

In the voltage reference (Fig.4.5), both reference current I_{REF} and threshold

voltage absolute value $|V_{th_p}|$ of the PMOS transistor M_p increase with TID. In order to compensate these increases, the source-to-gate voltage ($V_{SG} = V_X - V_{REF}$) of M_p is increased through a decrease of the reference voltage V_{REF} .

TID simulations have been performed to confirm this hypothesis. Figure 4.20 shows the simulated current consumption and V_{REF} value versus TID effects. As expected, the current consumption increased, while the reference voltage V_{REF} decreased.

It has to be noted that, at 300 mV shift of V_{th} , a good matching on the reference voltage value ($V_{REF} = 1.06$ V) is obtained between simulated and measured reference voltage after 30 kGy TID (Fig.4.16).

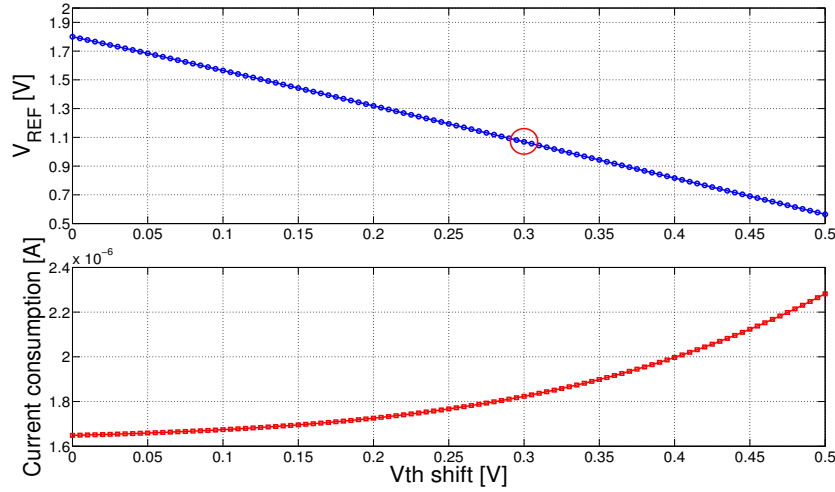


Figure 4.20: Simulated V_{REF} and current consumption of the voltage reference circuit vs TID at 25°C.

B4- Proposed solutions: To readjust the temperature detection level of the microsystem at $T_0 = 0^\circ\text{C}$, the output value of the voltage reference can be shifted up by tuning the value of the external resistor R_B . Figure 4.21 shows the readjustment of T_0 from 60°C to 0°C . For example, this tuning can be done automatically by a calibration process using a connected microprocessor and its embedded ADC.

For the current consumption, the annealing effects [7] help the partial recovery of the device operation at high temperature. Figure 4.22 shows the current consumption after one temperature cycle for a chip irradiated at a dose of 30 kGy. Thus at a temperature of 0°C , the consumption was reduced from $11\ \mu\text{A}$ to $5\ \mu\text{A}$ with just one cycle and a high temperature of 120°C . Even

more, if the temperature increases up to 300 °C the current consumption will be reduced even more, and also after several temperature cycles.

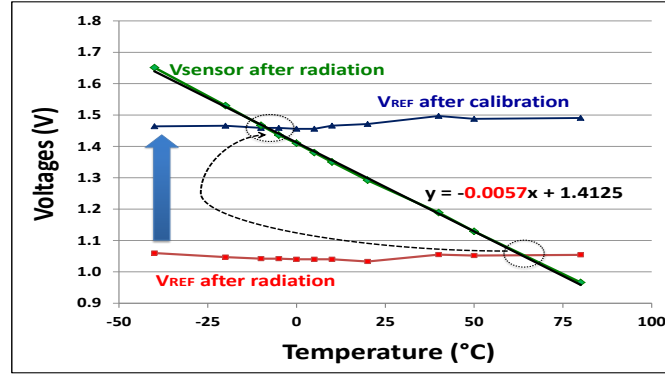


Figure 4.21: Adjustment of T_0 value by tuning the value of the resistor R_B .

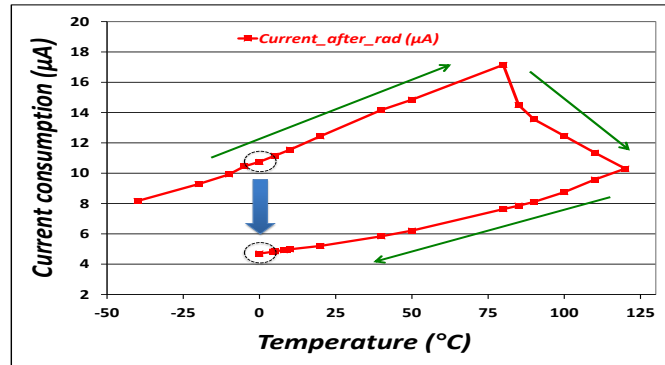


Figure 4.22: Current consumption of the microsystem after one cycle of annealing at 120 °C.

C) Conclusion As a conclusion, the measurement results of an ultra-low-power CMOS circuit were presented: a temperature sensor, a voltage reference and a comparator. These circuits were demonstrated to be functional up to 300 °C and consume, before radiation, less than 20 μA at +250°. After total dose radiation, the used startup circuit causes an increase of the current consumption in the microsystem and a shift down of the output voltage values. This shift disturbs the functionality of the microsystem. We have also shown that the impact of the radiation up to 3 Mrad(Si) in the current consumption of the microsystem remains lower than the influence of the high temperature.

4.3 Combined effect of total ionized dose and temperature on 130 nm PD SOI

In this part we study experimentally the combined effect of the total ionized dose and the temperature on the 130 nm PD SOI technology, firstly on available MOSFET transistors, and secondly on a designed ultra low power voltage reference circuit.

4.3.1 Effect on PD SOI MOSFET transistors

In order to understand the effect of the combination of TID and high temperature on SOI MOS transistors, their threshold voltages $V_{th_{n,p}}$, the subthreshold slope parameter SS and their mobilities μ were extracted. Thereby, the typical DC $I_D(V_{GS})$ characteristic of three NMOS and three PMOS transistors featuring a width of $2.5 \mu\text{m}$ and a length of $0.5 \mu\text{m}$ were performed. Measurements have been performed during irradiation at room temperature, 100°C and 200°C , using a small ceramic heater resistor placed under the transistors. The irradiation was performed at the Cyclotron facility of UCL with Gamma-rays, using a Cobalt source (^{60}Co).

The gamma-rays radiation is known to result in oxide and interface charges build-up (N_{ox} and N_{it}). Due to the weak electric field at small V_{GS} , only oxide charges N_{ox} are created in the transistors. While, at high $V_{GS} \approx V_{th}$ both oxide and interface charges (N_{ox} and N_{it}) are present and impact the transistors [8].

The extracted $I_D(V_{GS})$ curves (at low drain-to-source voltage of 25 mV) for NMOSs in the Fig.4.23, 4.24, 4.25 and for PMOSs in the Fig.4.26, 4.27, 4.28 show the oxide and interface charges build-up (N_{ox} and N_{it}) at different temperature.

4.3.1.1 Effect on the MOSFET threshold voltages

The oxide and interface charges build-up (N_{ox} and N_{it}) shifts the threshold voltages in MOS transistors as ($V_{th_n} \propto (N_{it} - N_{ox})$ and $|V_{th_p}| \propto (N_{it} + N_{ox})$) [9]. Thus, for PMOS as shown in Fig.4.29, the absolute $|V_{th_p}|$ value increases with radiation and temperature. This is due to the increase of both N_{ox} and N_{it} charges with radiation.

For an NMOS transistor, the voltage threshold depends on the temperature (Fig.4.30). At room temperature, induced N_{ox} charges are dominant (versus N_{it}) and, therefore the V_{th_n} value decreases slightly. At 100°C , a balance between N_{ox} and N_{it} occurs and keeps a relatively stable value for V_{th_n} versus

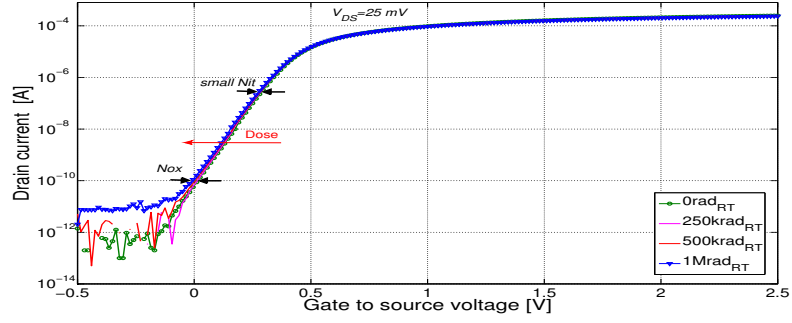


Figure 4.23: Measured I_D versus V_{GS} curves of NMOS transistor ($W/L = 2.5/0.5$ in μm) at room temperature for different radiation doses

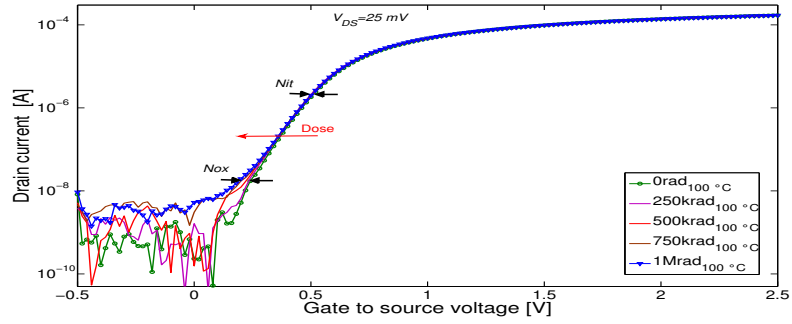


Figure 4.24: Measured I_D versus V_{GS} curves of NMOS transistor ($W/L = 2.5/0.5$ in μm) at 100°C for different radiation doses.

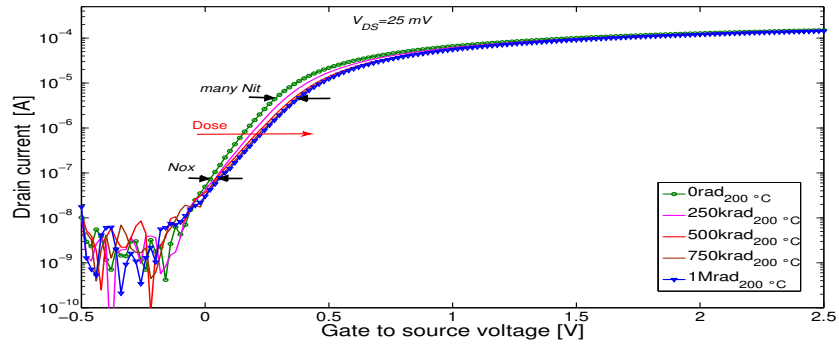


Figure 4.25: Measured I_D versus V_{GS} curves of NMOS transistor ($W/L = 2.5/0.5$ in μm) at 200°C for different radiation doses.

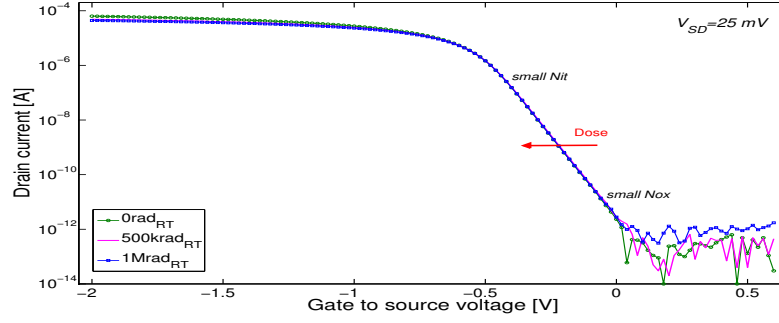


Figure 4.26: Measured I_D versus V_{GS} curves of PMOS transistor ($W/L = 2.5/0.5$ in μm) at room temperature for different radiation doses.

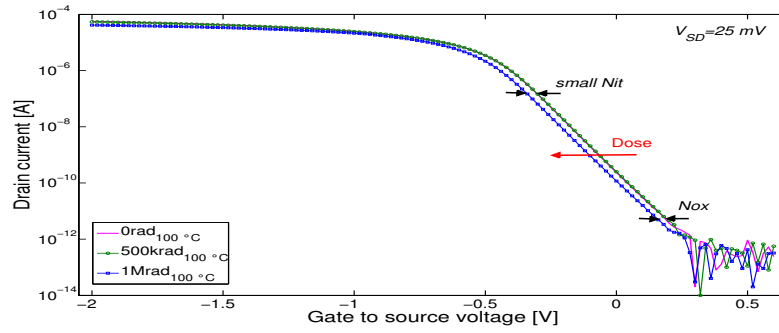


Figure 4.27: Measured I_D versus V_{GS} curves of PMOS transistor ($W/L = 2.5/0.5$ in μm) at 100 °C for different radiation doses.

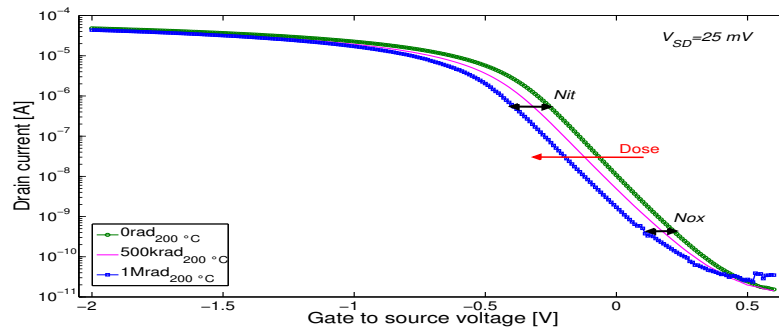


Figure 4.28: Measured I_D versus V_{GS} curves of PMOS transistor ($W/L = 2.5/0.5$ in μm) at 200 °C for different radiation doses.

radiation dose. Both N_{it} and N_{ox} charges increase at 200 °C and leads to an increase of the NMOS threshold voltage with the dose.

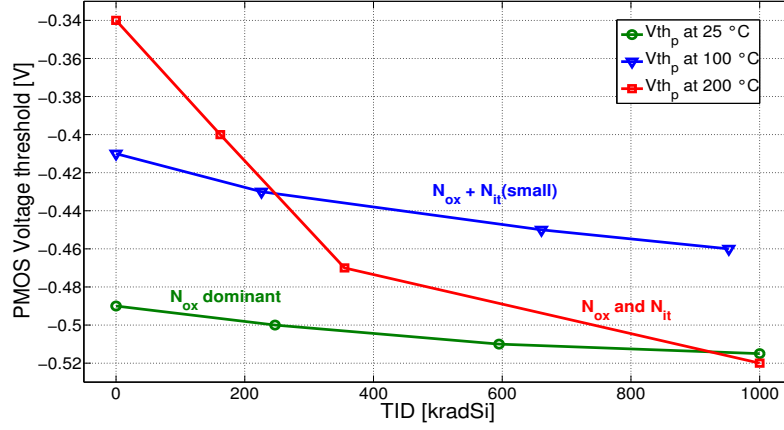


Figure 4.29: Measured PMOS V_{thp} vs TID at different temperatures.

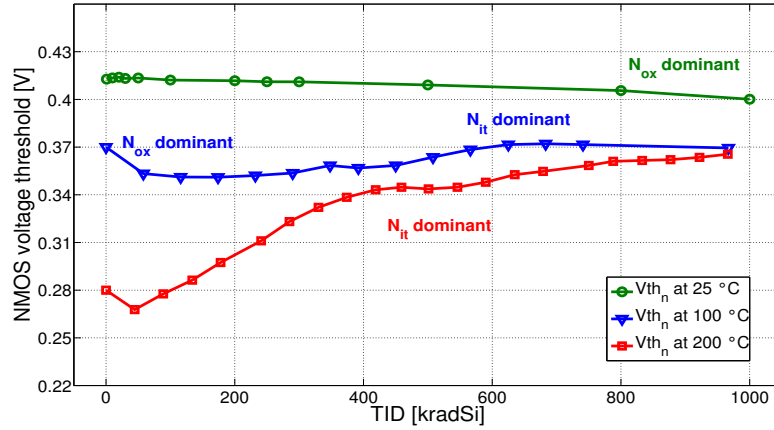


Figure 4.30: Measured NMOS V_{thn} vs TID at different temperatures.

4.3.1.2 Effect on the subthreshold parameter SS

For the subthreshold parameter SS , the curves g_m over I_D versus drain current I_{Dsat} have been extracted. The maximum values of g_m/I_D curves are known to be inversely proportional to the subthreshold parameter SS [10]. The g_m/I_D parameters were extracted using the following equation:

$$g_m/I_d = \frac{\delta(I_D)}{\delta(V_{GS})} \cdot \frac{1}{I_D} = \frac{\delta(\ln(I_D))}{\delta(V_{GS})} \quad (4.3)$$

The extracted curves of g_m/I_D versus $I_{D_{sat}}$ before radiation and after 1 Mrad(Si) total dose radiation, show an increase of the subthreshold parameter SS under TID effects at all measured temperature (Fig.4.31, 4.32, 4.33). It has to be noted that, the same behavior of subthreshold parameter under temperature and TID has been reported in the literature in the reference [11].

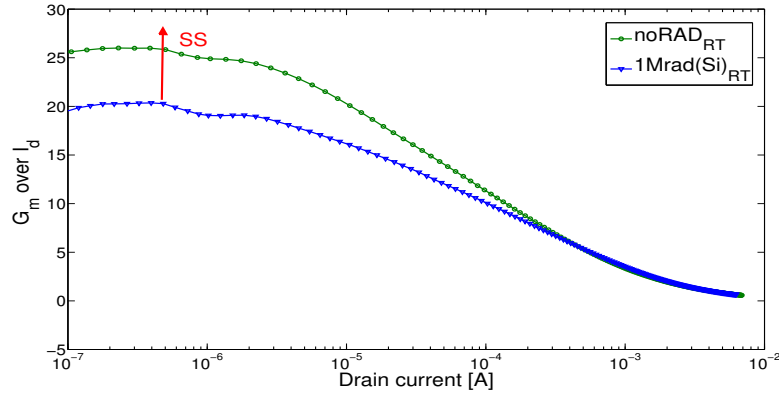


Figure 4.31: Extracted g_m/I_D curves vs v_{gs} at room temperatures.

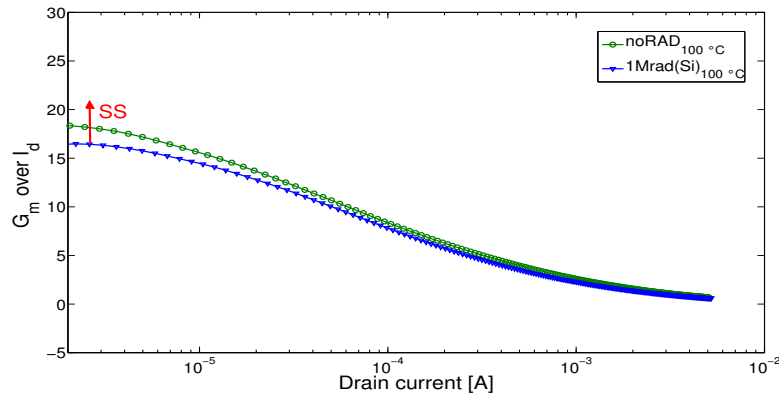


Figure 4.32: Extracted g_m/I_D curves vs v_{gs} at 100 °C.

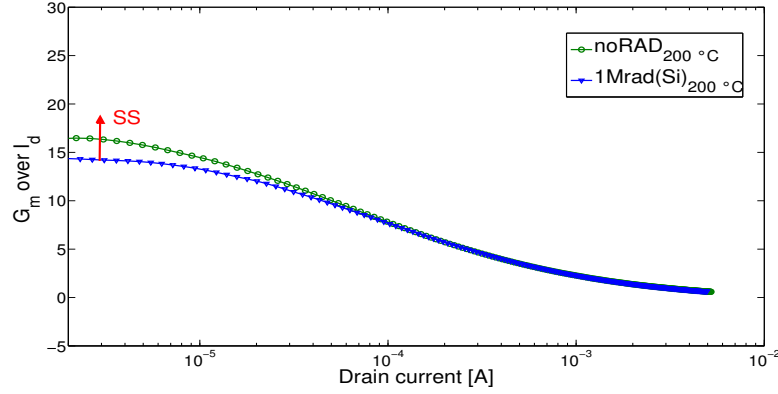


Figure 4.33: Extracted g_m/I_D curves vs v_{gs} at 200 °C.

4.3.1.3 Effect on the MOSFET carriers mobilities μ

The degradation of the carriers mobility under TID is well known and reported in several references [12–14]. It has been explained by the increase of the oxide and interface charges (N_{ox} and N_{it}) in the transistors during radiation. These charges are inversely proportional to the carriers mobility ($\mu \propto N_{it}^{-1} + N_{ox}^{-1}$) [9]. Furthermore, as shown in Chapter 2, the carriers mobilities are degraded by temperature.

Under both TID and temperature effects, the carriers mobility is also degraded as shown in the figures 4.34, 4.35, 4.36. Proportional to the carriers mobility μ , the transconductance maximum value gm_{MAX} is decreased under TID effects at different temperatures.

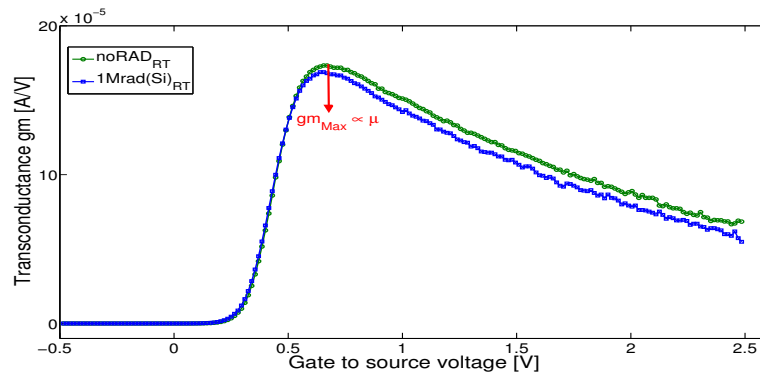


Figure 4.34: Extracted $gm(V_{GS})$ versus TID at room temperature.

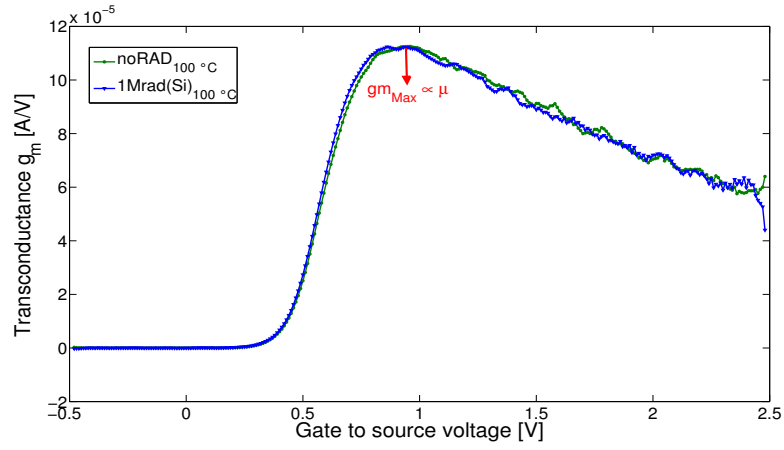


Figure 4.35: Extracted $g_m(V_{GS})$ versus TID at 100°C .

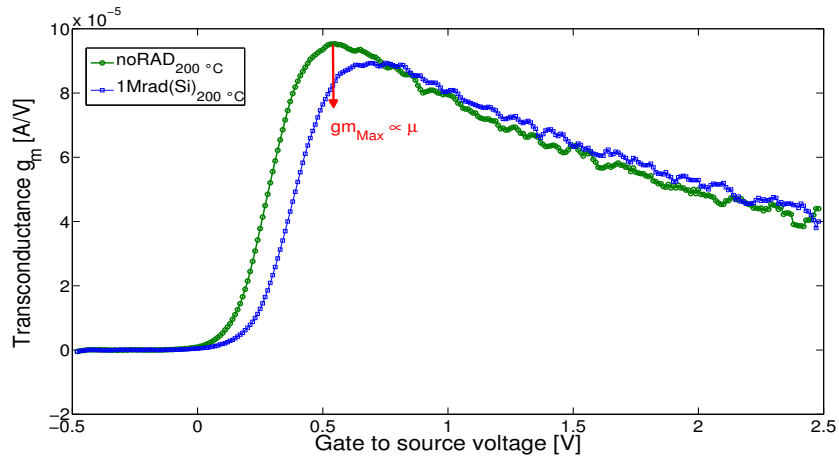


Figure 4.36: Extracted $g_m(V_{GS})$ versus TID at 200°C .

4.3.2 Effect on a ultra-low power voltage reference

Based on the previous microsystem circuit, an ultra-low power voltage reference circuit robust to extreme conditions has been designed in the suitable 130 nm PD SOI technology featuring a thin gate oxide of only 5 nm. The design simulations have been performed over a temperature range of $[-40, +200\text{ }^{\circ}\text{C}]$, and for different process corners. Robustness to radiation was simulated by using custom model parameters including TID effects, such as mobilities and threshold voltages degradation.

The proposed circuit has been tested up to a high total radiation dose, i.e. 1 Mrad (Si) performed at three different temperatures (room temperature, $100\text{ }^{\circ}\text{C}$ and $200\text{ }^{\circ}\text{C}$). The maximum drift of the reference voltage V_{REF} depends on the considered temperature and on the radiation dose, it remains however lower than 10% of the mean value of 1.5 V. The typical power dissipation at 2.5 V supply voltage is about $20\text{ }\mu\text{W}$ at room temperature, and only $75\text{ }\mu\text{W}$ at a high temperature of $200\text{ }^{\circ}\text{C}$. The total occupied area including pad-ring is less than 0.09 mm^2 .

4.3.2.1 Basic concepts

A- Voltage reference circuit description :

The voltage reference is a CMOS circuit (Fig.4.37) based on the gate-source voltage difference between a pair of P-type MOS (PMOS) and N-type (NMOS) transistors (M_p and M_n) biased by a proportional to absolute temperature (PTAT) current I_{REF} (Eq.4.11). Differently to the initial work described in [16], our design was: 1) improved by introducing a cascode bias stage for enhanced stability, and a new start-up design to avoid start deficiency at extreme temperature and process corners (resulting in high V_{th}); 2) extended to operate in a large temperature range from -40 to $+200\text{ }^{\circ}\text{C}$; 3) conceived to limit the power dissipation in harsh environments, using transistors optimized to operate in subthreshold regime.

In the next paragraph, the operation of the previous circuit [17] is reviewed, and in the next sections, an improved architecture is proposed.

B- Design principles :

From the analysis of the circuit described in Fig.4.37, the voltage reference value V_{REF} and the bias current I_B are obtained as:

$$V_{REF} = \left(1 + \frac{R_1}{R_2}\right) \cdot V_{GSn} - |V_{GSp}|, \quad (4.4)$$

$$I_B = \frac{V_{GS2} - V_{GS1}}{R_B}, \quad (4.5)$$

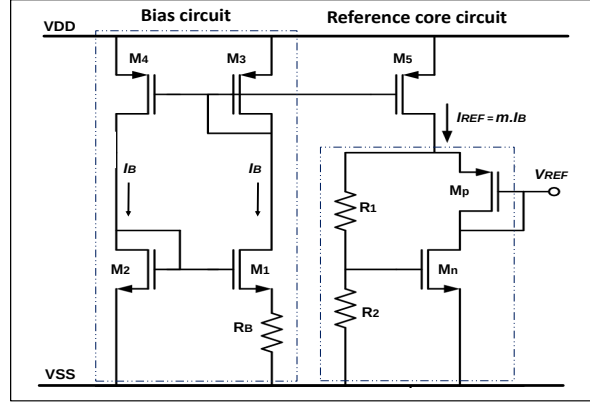


Figure 4.37: Voltage reference circuit [17].

where V_{GSn} , V_{GSp} , V_{GS1} and V_{GS2} are the gate-source voltages for transistors M_n , M_p , M_1 and M_2 , respectively. For NMOS and PMOS transistors operating in the subthreshold regime, the $I - V$ characteristics can be expressed by [18]:

$$I_{Dn} = \beta_n \cdot U_T^2 \cdot \exp\left(\frac{V_{GS} - V_{thn}}{n \cdot U_T}\right) \cdot \left[1 - \exp\left(\frac{V_{DS}}{U_T}\right)\right], \quad (4.6)$$

$$I_{Dp} = \beta_p \cdot U_T^2 \cdot \exp\left(\frac{V_{SG} - |V_{thp}|}{n \cdot U_T}\right) \cdot \left[1 - \exp\left(\frac{V_{SD}}{U_T}\right)\right], \quad (4.7)$$

where $\beta_n = \mu_n \cdot C_{ox} \cdot (W_n/L_n)$ and $\beta_p = \mu_p \cdot C_{ox} \cdot (W_p/L_p)$, $\mu_{n,p}$ is the electron and holes mobilities in the channel, C_{ox} is the oxide capacitance per unit area, V_{thn} and V_{thp} are the threshold voltages of NMOS and PMOS respectively, W_n (W_p) and L_n (L_p) are the channel width and length for NMOS (PMOS) respectively. $U_T = k_B \cdot T/q$ is the thermal voltage (k_B is the Boltzmann constant, q the elementary charge and T the absolute temperature), n is the body factor ($\propto$ the subthreshold slope SS), V_{GS} and V_{DS} (V_{SG} and V_{SD}) are the gate-to-source and drain-to-source voltages respectively for the NMOS (PMOS) transistor.

For $|V_{DS}| > 4U_T$, the drain current I_D becomes almost independent of the drain-to-source voltage [19], so that from Eqs. (4.6) and (4.7) we can extract :

$$V_{GSn} = n \cdot U_T \cdot \ln\left(\frac{I_{Dn}}{\beta_n \cdot U_T^2}\right) + V_{thn}, \quad (4.8)$$

$$|V_{GSp}| = n \cdot U_T \cdot \ln\left(\frac{I_{Dp}}{\beta_p \cdot U_T^2}\right) + |V_{thp}|. \quad (4.9)$$

In figure 4.37, if k is the size ratio ($W_1 \cdot L_2 / (L_1 \cdot W_2)$) of transistors M_1 and M_2 , m the current copy ratio in the output stage ($I_{REF} = m \cdot I_B$) and using

Equations (4.5) and (4.8), the bias current I_B is given by:

$$I_B = n \cdot U_T \cdot \left(\frac{\ln(k)}{R_B} \right). \quad (4.10)$$

$$I_{REF} = m \cdot n \cdot U_T \cdot \left(\frac{\ln(k)}{R_B} \right). \quad (4.11)$$

Assuming that the current through the resistances R_1 and R_2 is negligible and using Eqs.(4.4), (4.8) and (4.9), we obtain the following expression of V_{REF} :

$$V_{REF} = n \cdot U_T \cdot \left[\ln \left(\frac{\beta_{Mp}}{\beta_{Mn}} \right) + M_r \cdot \ln \left(\frac{n \cdot m \cdot \ln(k)}{R_B \cdot \beta_{Mn} \cdot U_T} \right) \right] + (1 + M_r)V_{thn} - |V_{thp}| \quad (4.12)$$

with $\beta_{M_n(p)} = \mu_{n(p)} \cdot C_{ox} \cdot (W/L)_{n(p)}$ for the output transistors M_n and M_p respectively (Fig.4.37). These β parameters ($\propto T^{-\alpha}$ with $\alpha \geq 1.5$), together with parameter n and the threshold voltages V_{thn} and V_{thp} , have a temperature dependency [20]- [21]. M_r is the resistors ratio (R_1/R_2). R_B is a non-silicided polysilicon resistance, showing an almost negligible temperature dependency in the simulations.

4.3.2.2 Circuit realization

A new design of the voltage reference (Fig.4.38) was developed with a cascoded current source, to reduce the V_{REF} variations due to the process corners, supply voltage variation and mainly the radiation effects caused by single ionized particles [22]. As it is based on the same principle as the previous design [17], the voltage reference expression V_{REF} remains unchanged (Eq.(4.12)).

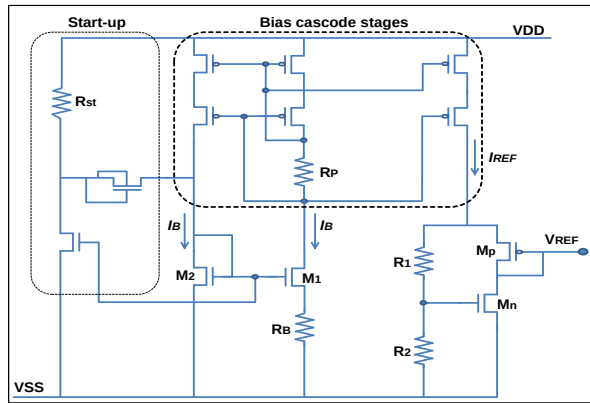


Figure 4.38: Proposed voltage reference circuit.

A- Technology characterization at high temperature :

The voltage reference circuit was developed based on the analog MOSFETs of an industrial 130 nm PD SOI CMOS featuring a 5 nm gate oxide thickness and a 280 nm minimum length. The SPICE (BSIM3SOI) models available for this technology are commercially validated up to 150 °C. We checked the models validity up to 200 °C, by comparing the typical DC $I_D(V_{GS})$ characteristic of a MOSFET transistor extracted by simulations and from measurements for different temperatures (25, 150, 175 and 200 °C). Figures 4.39 and 4.40 show two examples of the good agreement between simulated and measured curves, for NMOS and PMOS transistors at 25 °C and 200 °C, in the subthreshold region of interest. The slight discrepancies for the PMOS transistor can be neglected since the circuit design has to cope with much larger variations due to process, temperature and radiations.

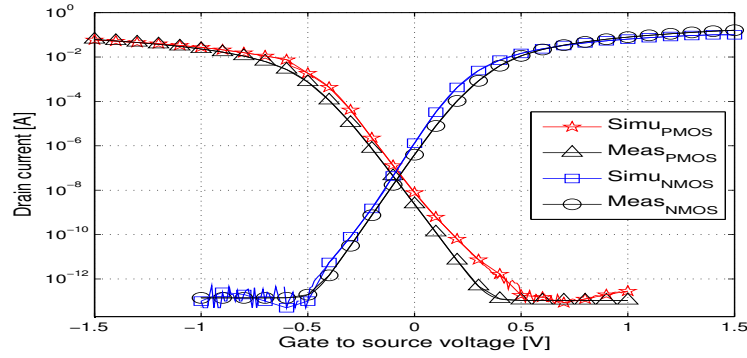


Figure 4.39: Measured and simulated I_D versus V_{GS} curves at 25 °C, $V_{DS} = 1.5$ V, $W = 1$ μm , $L = 0.28$ μm .

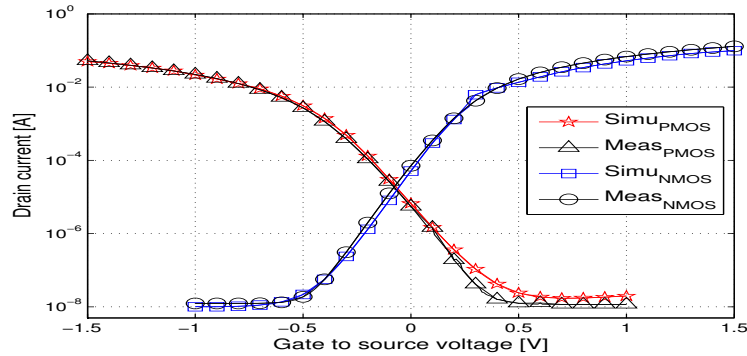


Figure 4.40: Measured and simulated I_D versus V_{GS} curves at 200 °C, $V_{DS} = 1.5$ V, $W = 1$ μm , $L = 0.28$ μm .

B- Design optimization :

The design optimization consists in determining the current bias I_B and the transistor and resistor sizes (in Fig.4.38) to minimize the V_{REF} variation with the device physical parameters as given by the previous equations and process corners. The temperature dependence of the voltage reference has to be as low as possible. The aforesaid dependence is expressed by evaluating the temperature coefficient (TC) defined by the following expression:

$$[TC] = \frac{1}{V_{REF}} \times \left[\frac{dV_{REF}}{dT} \right]. \quad (4.13)$$

In order to minimize the TC coefficient for our design, we have extracted the temperature dependencies of the physical parameters, computed Eq.(4.13) and searched the best design parameters (W_1 , W_2 , L_n , m , M_r , W_n , W_p and R_B). However, this first guess does not take the process corners into account. Next, extensive ELDO (Mentor Graphics) simulations have been performed for the different process corners in a temperature range of -40 up to +200 °C.

C- Design robustness against radiation effects :

To take into account the variations due to radiation effects, additional constraints were considered as follows:

- The designed circuit was checked with custom model parameters of transistors including TID effects on transistors [9] (worst case : up to 20% mobilities degradation and negative voltage threshold shifts of 200 mV).
- Using transistors with a body contact to limit the effect of the parasitic bipolar possibly created by radiation [22].
- Choosing a relatively long transistor to ensure a lower leakage current and a lower threshold voltages shift, which may appear as a result of TID and high-temperature effects [8, 10, 23].
- The circuit layout is further carried out by paying attention to critical components; all matched device pairs were realized by a centroid implementation, including the necessary dummies (Fig.4.41).

Table 4.1 gives the bias setting, and the different dimensions of transistors and resistors used in the proposed voltage reference circuit.

D- Simulations results :

Simulations are performed for five different process corners and a custom model parameters of transistors including TID effects, namely:

- Typ: typical corner (typical $|V_{th}|$ values)

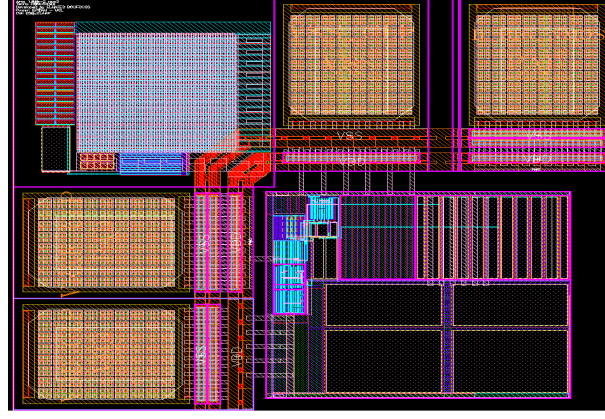


Figure 4.41: Final layout of the voltage reference.

Table 4.1: Voltage references bias setting and devices dimensions.

Parameter	Description	Value
VDD	Power supply	2.5 V
I_B	Bias current@25 °C	2.5 μ A
$(W/L)_1$	Size of NMOS M_1	40 μ m/0.5 μ m
$(W/L)_2$	Size of NMOS M_2	10 μ m/0.5 μ m
$(W/L)_{3-6}$	Size of PMOS M_3, M_4, M_5 and M_6	10 μ m /0.5 μ m
$(W/L)_{7-8}$	Size of PMOS M_7 and M_8	25 μ m/0.5 μ m
$(W/L)_p$	Size of PMOS M_p	200 μ m/0.5 μ m
$(W/L)_n$	Size of NMOS M_n	20 μ m/1 μ m
$(W/L)_9$	Size of NMOS M_9	5 μ m/0.5 μ m
$(W/L)_{st}$	Size of NMOS M_{st}	5 μ m/1 μ m
R_B	R_B resistor value	25 k Ω
R_1/R_2	R_1/R_2 resistors values	500/200 k Ω
R_{st}	R_{st} resistor value	1.5 M Ω

- FFA: Fast PMOS and NMOS (min $|V_{th}|$ values) with minimum resistance values
- SSA: Slow PMOS and NMOS (max $|V_{th}|$ with maximum resistance values
- FSA and SFA: are the crossed cases (fast and slow)
- RAD: Custom model parameters of transistors including TID effects (20% degradation of the mobility and a threshold voltage shift of 200 mV).

As shown in Fig.4.42, the reference voltage V_{REF} versus a temperature range of -40 to $+200$ °C gives an average voltage of 1.5 V for the typical corner, with a variation of $\pm 8\%$ over all process corners and temperature/radiation conditions. More specifically, lower $|V_{th}|$ values lead to a lower V_{REF} at a given temperature according to Equation (4.12), whereas the temperature dependence depends on the exact balance between the n and U_T terms which increase and tend to increase V_{REF} when temperature increase, and the V_{th} terms which increase and tend to increase V_{REF} when temperature decreases. The power consumption increased with temperature as shown in the Fig.4.43.

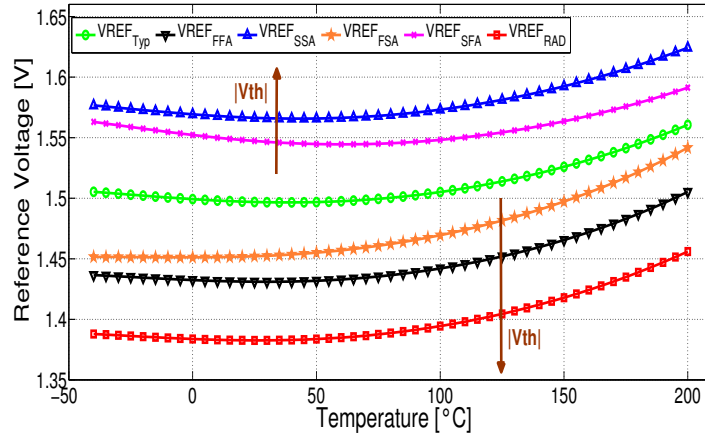


Figure 4.42: Simulated reference voltage vs temperature and process corners.

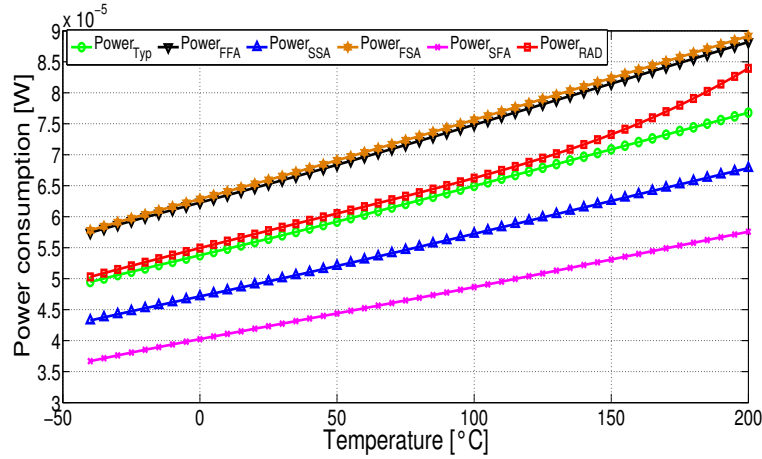


Figure 4.43: Simulated power consumption vs temperature and process corners.

4.3.2.3 Experimental results

The main purpose of our voltage reference is to be used under harsh biomedical sterilization conditions. To validate this feature, the voltage reference circuit has first been measured in a large range of temperatures from -40 up to $+200$ °C using two different equipments. Firstly, from -40 to $+90$ °C, a climatic chamber with a good accuracy (± 0.5 °C), and secondly, with a small ceramic heater resistor for the range of 90 to 200 °C. Other chips have been tested during irradiation at different temperatures, using the small ceramic heater resistor placed under the chips. The irradiation was performed at the Cyclotron facility of UCL with Gamma-rays, using a Cobalt source (^{60}Co). The next sections present the results measured for a power supply of 2.5 V.

A- Temperature measurements :

As shown in Fig.4.44, the experimental voltage reference generates a mean reference voltage of about 1.5 V (Fig.4.44) with a variation of about 1% , for the temperature range of -40 – 90 °C with a temperature coefficient less than 133 ppm/°C. This increases to 470 ppm/°C for the larger tested temperature range of -40 – 200 °C with a maximum variation of 10% . The maximum power dissipation is less than 42 μW at the lower temperature of -40 °C, about 50 μW at room temperature, and only 75 μW at a high temperature of 200 °C (Fig.4.45).

The 10% increase in the reference voltage value V_{REF} versus temperature can be explained by the increase in the subthreshold current and parameters n , U_T and $(1/\beta_{Mn})$ shown in the Eq. (4.12). The decrease in the absolute values of the threshold voltages of transistors V_{thn} and $|V_{thp}|$ with temperature [20] helps (but not sufficiently) to limit the increase in the V_{REF} value versus temperature. To first order, the power dissipation of the circuit is equal to " $V_{DD} \cdot (m+2) \cdot I_B$ " and according to Eq. (4.11) it is proportional to the term $n \cdot U_T$ ($\propto n \cdot T$). This explains the linear variation with temperature of the power dissipation of the reference voltage (Fig.4.45).

B- Measurements under combined high temperature and radiation exposure :

Six chips were exposed to gamma-rays radiation during one week with a dose rate of 10 krad/h, and regularly measured. Two chips were kept at room temperature, two heated at 100 °C during radiation, and the last two chips at 200 °C. The voltage reference value remains about the expected voltage of 1.5 V with a maximum increase of $\pm 5\%$ shift for room temperature and 200 °C. At 100 °C the voltage reference value increases with the total dose up to 400 krad (Si), and starts to decrease at a higher dose (Fig.4.46). The power consumption

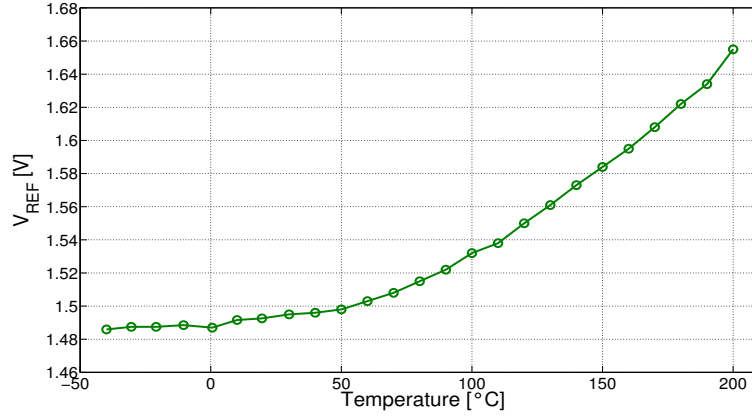


Figure 4.44: Measured voltage reference V_{REF} versus temperature.

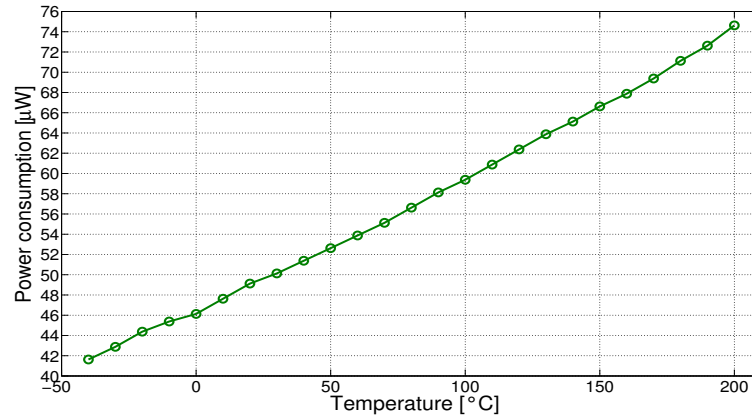


Figure 4.45: Measured current consumption versus temperature.

of the voltage reference increases with radiation and temperature, except for the highest heating temperature during radiation, for which the power remains stable at about $75 \mu\text{W}$ upon radiation (Fig.4.47). Similar trends were observed for all measured chips.

Similarly to the temperature case, we can express the radiation dependencies of the voltage reference circuit. This is about 25 ppm/krad for room temperature up to 1 Mrad (Si).

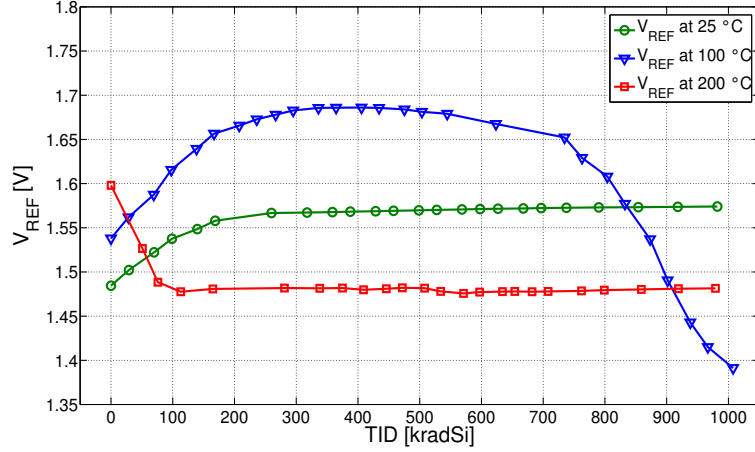


Figure 4.46: Measured voltage reference V_{REF} vs TID at different temperatures.

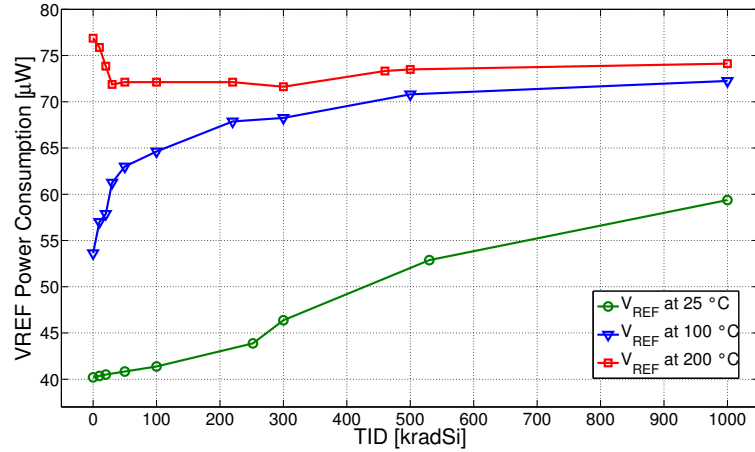


Figure 4.47: Measured voltage reference power consumption at 2.5V power supply, in the same conditions as in Fig.4.46.

D- Discussion of the measurement results :

Based on the previous expression of V_{REF} (Eq. (4.12)) and knowing from previous measurements (Fig.4.31,4.32 and 4.33) that the parameter n ($\propto$ sub-threshold slope SS) is increased and the carrier mobilities $\mu_{n(p)}$ are both degraded by radiation (Fig.4.34, 4.35 and 4.36) and temperature [9, 24], we can explain the combined effect of radiation and temperature on the circuit (Figures 4.46 and 4.47) as follows.

- At room temperature: As the shift of the threshold voltages of PMOS

and NMOS seems to be small, the increase in V_{REF} and the power dissipation can be explained by the increase in parameter n and the decrease in mobility μ_n ($\propto$ to $1/\beta_{Mn}$) under radiation.

- At 100 °C: At a small dose (less than 400 krad) the same effects as for room temperature occur. For a higher dose, the absolute value of the threshold voltage of PMOS increases, while the NMOS one remains quasi stable, leading thus to the decrease of the voltage value in V_{REF} and the stabilization of the power dissipation.

- At 200 °C: After an initial decrease in V_{thn} and an increase in $|V_{thp}|$ which is reflected in a decrease in V_{REF} value and the power dissipation, both absolute values of V_{thn} and V_{thp} increase under radiation. Thus, they compensate each other in the Equation (4.12) leading to a stable value of V_{REF} and power consumption.

4.3.2.4 Comparison with the state of the art

Table 4.3.2.4 summarizes the performance of the proposed voltage reference circuit, and compares it with the results of the literature. When compared to our previous work [17], the new circuit is twice less sensitive to a temperature variation and, the sensitivity to radiation is divided by more than one order of magnitude thanks to: (1) the suitable SOI technology featuring a reduced oxide thickness (5 nm in this work versus 25 nm in the previous work) which limits the oxide charge build-up and, hence the TID degradation; (2) the new design circuit performed with a reasonable margin for the current consumption.

When compared to the literature ([16], [25] and [26]), the proposed circuit operates in a wider range of temperature -40 to $+200$ °C and radiation (up to 1 Mrad (Si)) than other solutions. Our circuit proposes a high reference voltage value of 1.5 V with a small current consumption (less than 20 μ A at room temperature), and achieves a low temperature coefficient for a similar range of temperatures. Similar to our design, the voltage reference in [27] has been designed in the sub-threshold regime of transistors. However, the layout has been performed using enclosed gate transistors using the 130 nm Bulk technology, this allows a high robustness against TID effects (up to 44 Mrad(Si) but limits the temperature range of this voltage reference (only 0 to 80 °C) with a TC of 200 ppm/°C.

Table 4.2: Performance comparison with similar voltage references described in the literature.

Parameter	This Work	Previous work [17]	Leung [16]	Malcovati [25]	Ivanovic [26]	Gromov [27]
Technology	0.13 μm SOI	1 μm SOI	0.6 μm Bulk	0.35 μm BiCMOS	–	0.13 μm Bulk
Supply voltage	2.5 V	5 V	1.4 to 3 V	1 V	–	1.4 V
Reference voltage (V)	1.5	1.8	0.333	0.54	1.6	0.405
Temperature range (°C)	–40–200	–40–300	0–100	0–80	–40–120	0–80
TC (ppm/°C)	133 [–40, 90 °C]	375 [–40, 90 °C]	94	212	90	200
	470 [–40, 200 °C]	825 [–40, 200 °C]				
Consumption @ 25 °C	20 μA	2 μA	9.7 μA	92 μA	-	-
V_{REF} shift due to radiation (ppm/krad)	25	426	–	–	140	0.68
Irradiation particles	Gamma-rays	Gamma-rays	–	–	Neutron	X-rays
Max V_{REF} shift due to combined effect of temperature and radiation	+10%	–	–	–	–	–
Dose Mrad (Si)	1	1	–	–	1	44

4.4 Conclusions

In this chapter, simulations of cumulative effects were presented in this first part. Secondly, measurement results of ultra-low-power 1 μm PD SOI circuits (a temperature sensor, a voltage reference and a comparator) before and after TID effects were presented and discussed.

Thirdly, the combined effect of TID and temperature has been measured on single 130 nm PD SOI MOSFET transistors and for a voltage reference circuit. The carriers mobility μ , the subthreshold parameter n and the threshold voltages $V_{th_{n,p}}$, for transistors have been extracted under radiation. Under this combined effects (TID + temperature), the subthreshold parameter n increases while the mobility μ decreases. A significant increase is shown in the absolute value of the PMOS threshold voltage with radiation at high temperature, while for NMOS, the threshold voltage value V_{th_n} decreases slightly at room temperature, keeps a relatively stable value versus radiation dose at 100 °C, and increases at a higher temperature of 200 °C, depending on the balance between N_{ox} and N_{it} buildup.

In the end, an ultra-low power voltage reference circuit to be used in a harsh environment was presented. This circuit has been simulated up to 200 °C using our extended MOS models, and was shown to consume about 75 μW at a higher temperature. The design was proved to be robust against radiation effects (using custom model parameters), and the voltage reference value very fairly stable over a large range of process corners and temperature variations. To enhance immunity to total dose effects, the layout has been implemented using specific guidelines and a suitable SOI CMOS technology with thin gate and buried oxides.

Measurements have shown a fairly correct operation of such an ultra-low power circuit for a large temperature range (from -40 °C up to $+200$ °C) and under the combination of a total ionizing dose (up to 1 Mrad (Si)) and a high temperature. The threshold voltages $V_{th_{n,p}}$, mobilities and subthreshold slope for the used SOI transistors extracted under radiation and temperature, fairly support the observed V_{REF} and power consumption dependences on temperature and total dose radiation.

Furthermore, we have observed the the separate effects of process corners, temperature and radiation influence V_{REF} and power consumption with a similar orders of magnitude. This justifies our strategy to take them all into account in the design phase.

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CHAPTER 5

Mitigation techniques against radiation effects for analog circuits

MITIGATION techniques against SEE and TID effects for analog circuits are presented in this chapter. Firstly, the state of the art of existing SEE and TID mitigation techniques is presented.

Secondly, TID mitigation techniques at design level are proposed in the 130 nm PD SOI technology. Thus, a design of hard current sources are detailed. Afterwards, the body biasing technique is presented and introduced as a new TID mitigation in analog circuits. By the end, hard amplifiers robust against the effects of TID, temperature and the process corners variations are presented.

5.1 State of the art of SEE mitigation

As discussed in Chapter 2, a single particle can induce a single-event upset in digital circuits. However in the analog and mixed-signal (A/MS) systems, a single particle may induce a transient signal (SET) that can perturb the signals propagating through the circuit. In some cases it can induce permanent failures such as SEL, SEB and SEGR. Several mitigation techniques against these effects have been developed. These can be implemented at different levels; technology, device, layout/design circuit and system. Following paragraphs detail these techniques.

5.1.1 Mitigation techniques at technology, device and layout level

Analog Single-Event Transients (ASET) mitigation are typically based on the increase of the critical charge Q_{crit} , or reducing the collected charge Q_{col} required to generate this single event. Known as the "brute force" methodology [1], it uses one or more of the following propositions.

The critical charge is increased (Q_{crit}) by increasing:

- The drive currents and the supply voltage [1].
- The transistor sizes [2, 3].
- The capacitance at nodes vulnerable to single-events [4].

The reduction of the collected charge (Q_{col}) goes through:

- Using Silicon On Insulator (SOI) technology, which is latchup free and SEE hardened, as the charge collection volume is at least 10 times less than bulk silicon [5–7]. As shown in the Fig.5.1 the energy disposition volume for bulk is always higher than the SOI.

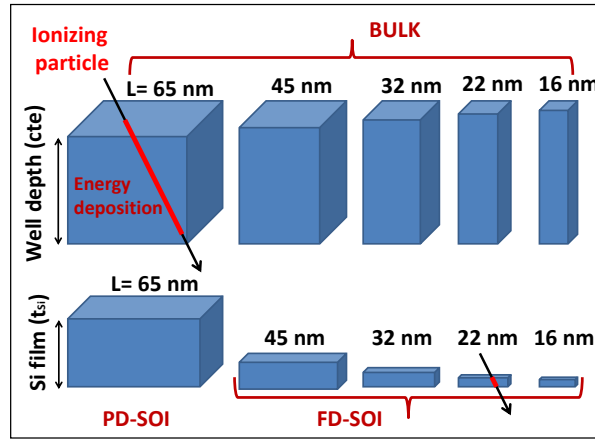


Figure 5.1: Energy deposition volumes traversed by ionizing particle for Bulk and SOI technologies (adapted from [7]).

- Using very thin epitaxial silicon layer (Fig.5.2) to reduce the risk of latchup [8].
- Using buried layer (Fig.5.3) which consists in a highly doped zone buried inside the well, in order to collect charge deposited by particles [9].
- Using triple-well structures (Fig.5.4) to decrease SEU and SEL sensitivity [10].
- Addition of dummies for charge collection [11].
- Reducing substrate and well impedances by increasing number of contacts [12–15].

- Using guard rings around MOS devices [16–19].
- Using nodal separation [20] to reduce "shared charge" between sensitive nodes.
- Placing the less sensitive transistors between pairs of sensitive devices [21].
- Placing layout of matched transistors in a differential data path, in order to exploit the charge-sharing phenomenon (Fig.5.5, 5.6). Therefore rejecting any common-mode perturbation [22].

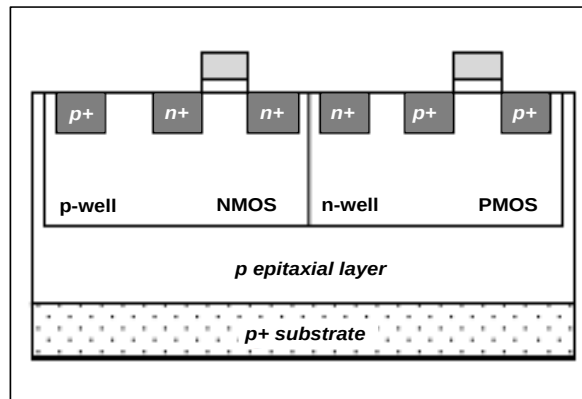


Figure 5.2: Example of epitaxial layer in CMOS technology [8].

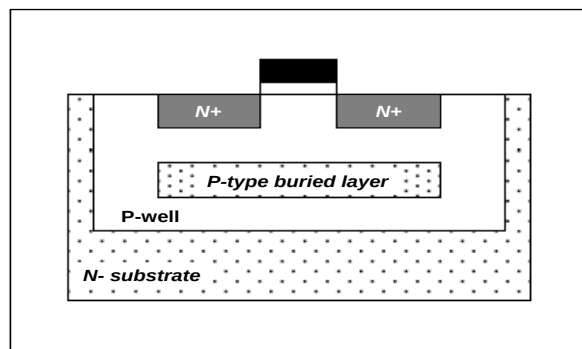


Figure 5.3: View of a P-type buried layer in a P-well [9].

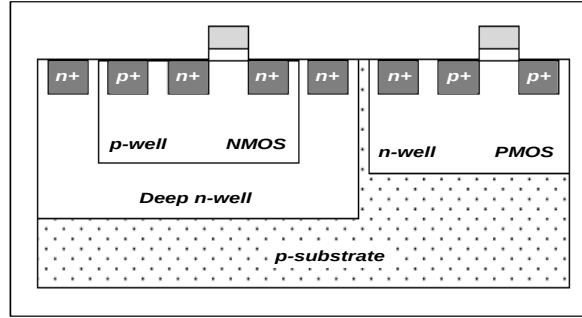


Figure 5.4: Triple-well technology implementing [10].

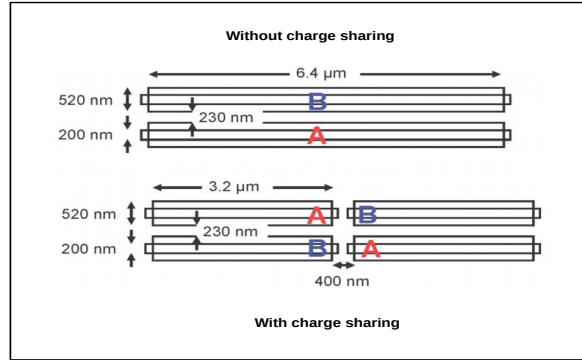


Figure 5.5: Layout without and with maximizing charge sharing [22].

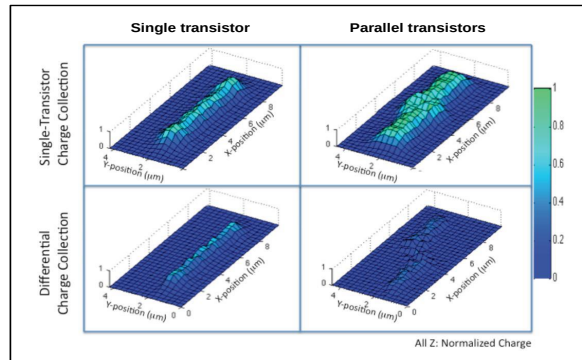


Figure 5.6: Charge collected by a single transistor (left) and parallel (right) in differential (bottom) and single (top) charge collection [22].

5.1.2 Mitigation techniques at design and system-level

ASET mitigation can also be implemented through the design of circuits and systems. Next paragraphs present a variety of mitigation techniques for A/MS circuits.

5.1.2.1 Triple Modular Redundancy TMR

TMR though more common in digital circuits, has been also used in mixed-signal circuits, such as in a pipelined ADC [23], a Voltage-controlled oscillator (VCO) [24] or a voltage comparator [25]. For example, for the voltage comparator, the standard single comparator was replaced by three parallel comparators driving a CMOS majority-voting circuit. This latter was hardened by over sizing the transistors [3].

5.1.2.2 Resistive Decoupling

The resistive decoupling is used for hardening memory cells by introducing series resistors. These increase the time constant seen by the storage nodes and limit the maximum change in voltage during a SET [27]. This technique is also used in A/MS circuits [28], to filter high-frequency transients by decoupling sensitive nodes and introducing a time constant through a series resistor.

5.1.2.3 Filtering

Filtering consists in introducing a low-pass or bandpass filter to critical nodes in order to reduce the amplitude and duration of ASETs [30]. This SET mitigation was used either in A/MS [28,31] and in advanced CMOS memory circuits [32].

5.1.2.4 Analog Redundancy (Averaging)

Analog averaging is a hardware redundancy which allows for reducing transient perturbation by parallelizing a circuit N times. Figure 5.7 shows how to reduce a perturbation ΔV on an analog voltage to $\Delta V/N$ using N parallel resistors [26].

5.1.2.5 Differential Design and Dual Path Hardening

A way to limit the effect of SET in Analog design is to use fully-differential design circuits, which has better noise rejection over their single-ended counterparts [36]. Dual path hardening is a technique that can improve immunity to SET. It consists in splitting the input nodes into separate parallel signal paths. It has been used in differential switched capacitor circuits [37] and comparators (Fig.5.8) [38].

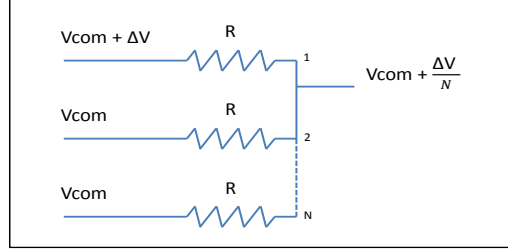


Figure 5.7: Analog averaging through the use of N identical resistors.

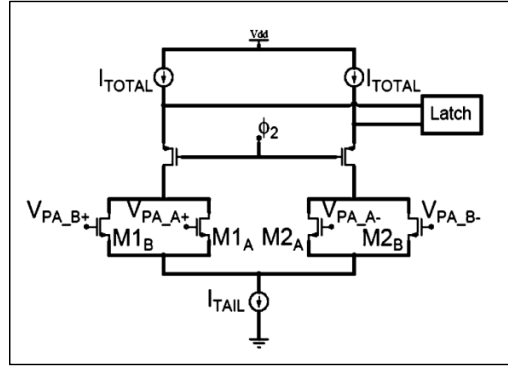


Figure 5.8: Dual Path Hardening used for a comparator [38].

5.1.2.6 Modifications in analog performances: Bandwidth, Gain, Current Drive

One way to improve ASET sensitivity of A/MS circuits is to reduce the bandwidth to the minimum specification, thus all transients outside of the frequency band will be eliminated.

References [34,35] show a way to reduce the SET sensitivity of Operational Amplifiers (mostly used in analog circuit), by reducing their gains (open and closed loop). This limits the amplitude and the duration of the SET event.

When it is possible, it is recommended to increasing the bias current which improves the ability to dissipate the energy deposited by charged particles [4].

As a conclusion, to decrease SET sensitivity using analog performances of circuits it is recommended to:

- Reduce the bandwidth as much as possible.
- Minimize the open and closed-loop gains.
- Increase the bias current.

5.2 The existing TID mitigation techniques

Electronic circuits exposed to radiation show permanent failures caused by Total Ionization Dose (TID). These effects are due to an accumulation of trapped charge N_{ox} in the gate (and buried for SOI) oxides and of interface states N_{it} during irradiation. Many studies in the literature such as in references [39–41] have demonstrated that the TID effect decreases when the oxide thickness scales down. The existing TID Hardening techniques have been mainly done at process and layout level, using the following techniques.

5.2.1 Dry thermal oxidation

The dry thermal oxidation consists in increasing the overall quality of oxides and to reduce hole trapping [42], thereby reducing the trapped charge caused by TID. This technique is achieved during process fabrication of silicon by modifying several parameters (growth/deposition rates and times, temperatures, gas, etc).

5.2.2 Implantation into oxides

This technique is based on the implantation of elements, such as Al, Si, P, Fl and As, into the oxides. This has been shown to improve the TID hardness by increasing electron trapping [43–45]. Figure 5.9 shows the results of this hardening process on both thicker and thinner SOI process [46].

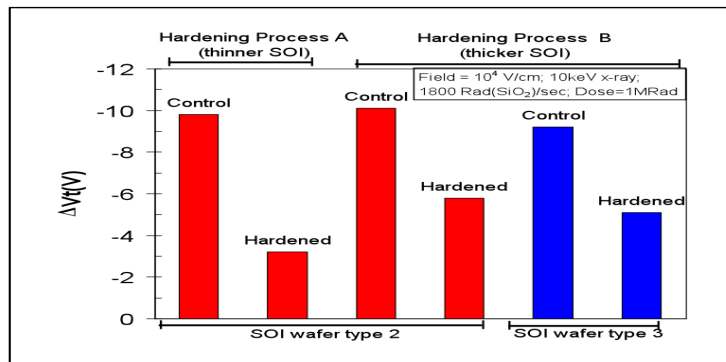


Figure 5.9: Threshold voltage shifts for different SOI layer thicknesses with and without hardening process [46].

5.2.3 Enclosed Layout Transistor (ELT)

The enclosed Layout Transistor, also called Edge-Less or square gate transistors [47], is a NMOS transistor with a layout avoiding contact between the STI (Shallow Trench Isolation) oxide, and any p-doped channel region. The layout is carried out by surrounding the n+ diffusion (source or drain) by the thin gate oxide (Fig.5.10). As shown in Fig.5.11, conventional CMOS transistor has two bird's beak regions [48]. These regions, trap positive charges during TID radiation and invert the p-type substrate, which creates parasitic channels between the drain and the source. This bird's beak effect can be considered as two parasitic transistors in parallel to the CMOS transistor [48]. Using enclosed Layout Transistor eliminates the bird's beak effect, which reduces the current leakage and the threshold voltages decrease, caused by trapped charge in the transistor [48].

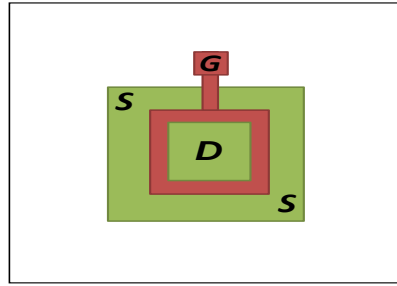


Figure 5.10: Layouts of: ELT (a), Ringed-Source (b) and Dual-Drain Ringed-Source (c) transistors (adapted from [49]).

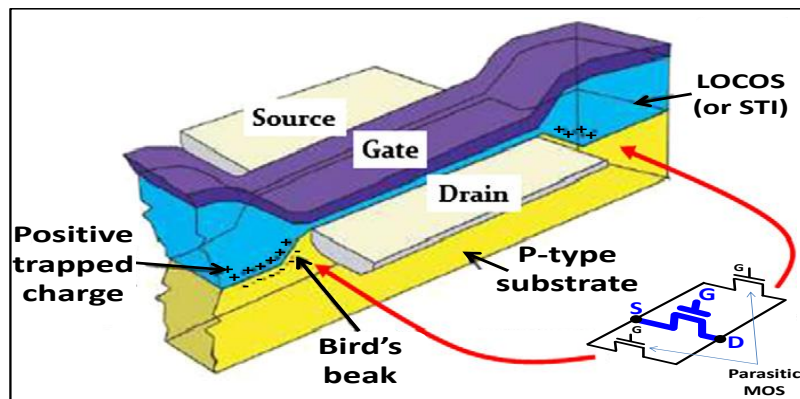


Figure 5.11: MOSFET with Bird's beak effects (adapted from [50]).

Other enclosed-geometry transistors such as Ringed-Source (Fig.5.12-a) and Dual-Drain Ringed-Source (Fig.5.12-b) have demonstrated to reduce radiation induced leakage current between source and drain, with a compact layout transistor compared to ELT [49].

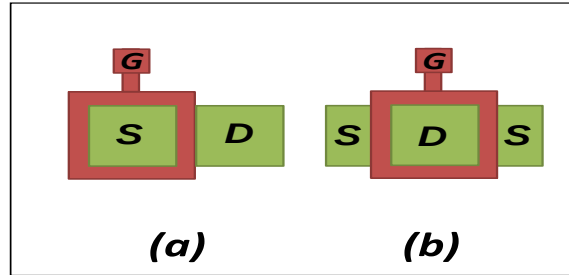


Figure 5.12: Layouts of: ELT (a), Ringed-Source (b) and Dual-Drain Ringed-Source (c) transistors (adapted from [49]).

5.2.4 Radiation-hardened libraries

Several commercial rad-hard libraries are available. These libraries have been achieved using previous listed hardening techniques in bulk CMOS technologies. Some of these libraries are listed as follows:

- ESA Design Against Radiation Effects library (DARE): Digital library with some I/O pads, developed in 180 nm CMOS bulk technology, with a hardness higher than 1 Mrad(Si) [51]- [52]
- CERN 0.24 μm radiation hardened library : Developed for the Large Hadron Collider (LHC), using a commercial 0.24 μm , 2.5 V bulk CMOS technology, with very high radiation tolerance (eg. up to 30 Mrad(Si) for a ring oscillator device [53]).
- BAE 0.15 μm radiation hardened library: Developed using a 150 nm standard cell ASIC library hard up to 3 Mrad(Si)
- Aeroflex 600, 250, 130 and 90 nm radiation hardened libraries: with a radiation tolerance from 100 krad(Si) greater to 1 Mrad(Si).
- Atmel MH1RT 0.35 μm and ATC18RHA 0.18 μm CMOS radiation hardened libraries: with TID tolerance higher than 100 krad(Si).
- ST Microelectronics radiation hardened library: using 65 nm commercial library cells with TID tolerance up to 100 krad(Si).

5.3 Proposed TID mitigation at layout level

5.3.1 PMOS and NMOS edgeless transistors

As mentioned previously, edgeless transistors have demonstrated better total-dose radiation immunity compared to standard transistors with lateral isolation [48], [50]. When this technique is used for both PMOS and NMOS transistors, only charges induced in the oxides (gate and box) impact the threshold voltages of NMOS and PMOS transistors. The threshold voltages Vth_{TID} of NMOS and PMOS after TID can be expressed respectively as [54]:

$$Vthn_{TID} = Vth_n - \frac{q \cdot N_{ox}}{C_{ox}} + \frac{q \cdot N_{it}}{C_{ox}} \quad (5.1)$$

$$|Vthp_{TID}| = |Vth_p| + \frac{q \cdot N_{ox}}{C_{ox}} + \frac{q \cdot N_{it}}{C_{ox}} \quad (5.2)$$

where $Vth_{n,p}$ are the threshold voltages before radiation, q is the electron charge, C_{ox} is the oxide capacitance per unit area N_{ox} and N_{it} are the oxide and interface charges build-up respectively.

In the case where the impact of the oxide charges N_{ox} is more important than interface charges N_{it} , the ΔN_{it} can be neglected in front of ΔN_{ox} . Therefore, the threshold voltages shifts of NMOS and PMOS transistors becomes:

$$\Delta(Vthn)_{TID} = \Delta(Vthp)_{TID} = -q \cdot \Delta(N_{ox}) \cdot C_{ox}^{-1} \quad (5.3)$$

As shown in next section, this characteristic can be used to mitigate TID effects at the design level.

5.3.2 Sizes calculation of edgeless square gate transistors

The sizes of edgeless transistors with square gate depend on some layout constraints such as the "design rules check" (DRC) and the dependency between the width W and the length L of a surrounding-gate topology. To determine the width W an accurate formula [55] can be used:

$$W = \left(\frac{2 \cdot \pi \cdot L}{\ln \left(\frac{W_D + \frac{L \cdot \pi}{2}}{W_D} \right)} \right) \quad (5.4)$$

where W_D is size of the internal active region, it has a minimum size of $W_{D_{min}} = 2 \cdot e + c$, where e is the minimum distance of contact on active (drain/source) to polysilicon (gate) and c is the contact size (Fig.5.13).

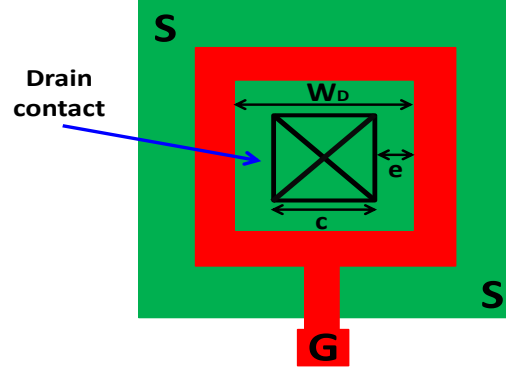


Figure 5.13: Layout of edgeless square gate transistor.

5.3.3 Fabrication of 130 nm PD SOI edgeless transistors

In this work, edgeless transistors with body contact connection, were implemented in the layout of the voltage reference circuit (Fig.4.38). Such layout of transistor requires square gate, which induces DRC errors. To overcome this issue, a derogation has been applied to the foundry and has been accepted. However, unfortunately in our case the fabrication of the edgeless structures failed due to the foundry issues. Figure 5.14 shows the carried out transistors layout in the technology PD SOI 130nm.

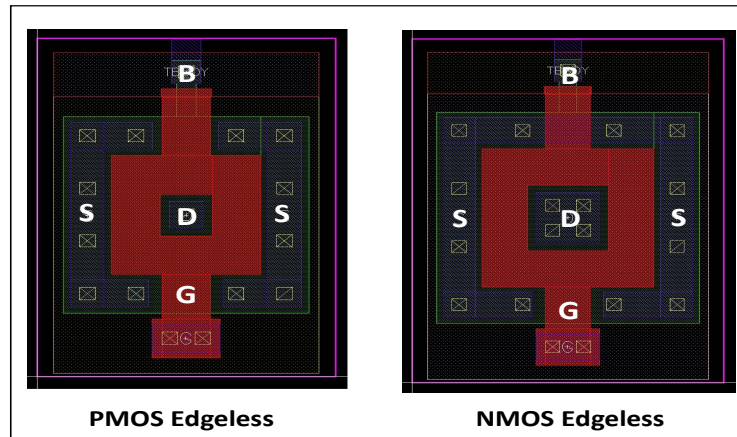


Figure 5.14: NMOS and PMOS edgeless layout in PD SOI 130nm.

5.4 Proposed TID mitigation techniques at design level for the 130 nm PD SOI

This section proposes new TID mitigation techniques at design level for analog circuits. Firstly, two current sources robust to TID effects in the 130 nm PD SOI technology are presented. The first current source, has a simple structure with only three transistors and a resistor, and has to be implemented using edgeless transistors. While the second current source is a more complete structure using an error amplifier. In addition to the TID effects, this current source is robust to temperature and process corners variations. Secondly, a new mitigation technique against TID for analog design circuits is proposed. It is based on the body biasing technique, which compensates the TID effects in critical and sensitive transistors in the analog circuits, such as the differential pair transistors of an OTA. Finally, the designs of rad-hard amplifiers in the 130 nm PD SOI technology using this body biasing technique are detailed.

5.4.1 Design of hardened current sources

In this part, a simple current source less sensitive to TID effects is presented. Afterward, the design of a more complete current source, robust to TID, temperature and process corners variations is detailed.

5.4.1.1 Current source with simple design

Figure 5.15 shows the schematic of a current source, composed of two diode-connected transistors (NMOS and PMOS) providing a fixed overdrive voltage V_{ov} ($V_{GS} - V_{th}$) versus TID effects, for a NMOS transistor M_{REF} and a degeneration resistor.

In order to limit the TID effects on such a current source, the transistors have to be implemented using an edgeless layout.

A- Design principle :

By using long channel transistors (negligible Early effect) in the strong inversion regime, the current I_{fs} of the first stage (Fig.5.16) and the common drain voltage V_{out} can be expressed as ($k_{n,p} = \mu_{n,p} \cdot C_{ox} \cdot (W_{n,p}/L_{n,p})/2$, $M = \sqrt{\frac{k_n}{k_p}}$):

$$I_{fs} = k_n * (V_{out} - V_{thn})^2 = k_p * (V_{DD} - V_{out} - |V_{thp}|)^2 \quad (5.5)$$

$$V_{out} = \frac{(V_{DD} - M \cdot V_{thn} - |V_{thp}|)}{1 + M} \quad (5.6)$$

After TID effects, in first order, the mobilities degradation of NMOS and

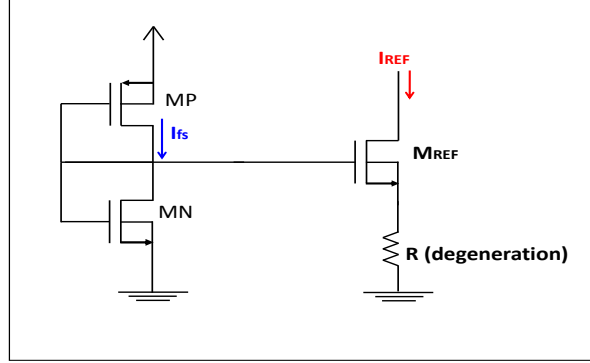


Figure 5.15: TID hardened current source.

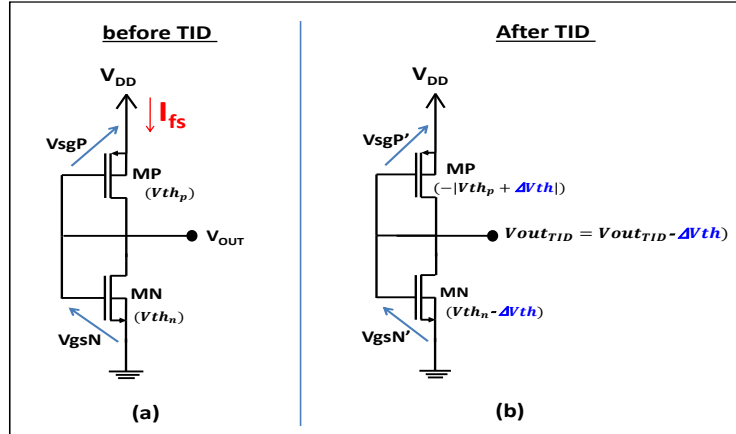


Figure 5.16: First stage of the TID hardened current source.

PMOS transistors are similar ($\Delta(\mu_n) \approx \Delta(\mu_p)$), then the factor $\sqrt{\frac{k_n}{k_p}}$ remains unchanged. Now, by substituting the threshold voltages by their values after TID for edgeless transistors ($V_{thn_{TID}} = V_{thn} - \Delta(V_{th})$ and $V_{thp_{TID}} = V_{thp} + \Delta(V_{th})$), the common drain voltage $V_{out_{TID}}$ after TID becomes: $V_{out_{TID}} = V_{out} - \Delta(V_{th})$. Using this common drain voltage as a gate-to-source voltage of a NMOS transistor M_{REF} (Fig.5.17), gives a drain current with an unchanged overdrive voltage V_{ov} versus TID. In fact, before TID, the overdrive voltage is $V_{ov} = V_{out} - V_{thn}$, and after TID the overdrive voltage becomes:

$$\begin{aligned}
V_{ov_{TID}} &= V_{out_{TID}} - V_{th_{n_{TID}}} \\
&= V_{out} - \Delta(V_{th}) - (V_{th_n} - \Delta(V_{th})) \\
&= V_{out} - V_{th_n} \\
&= V_{ov}
\end{aligned}$$

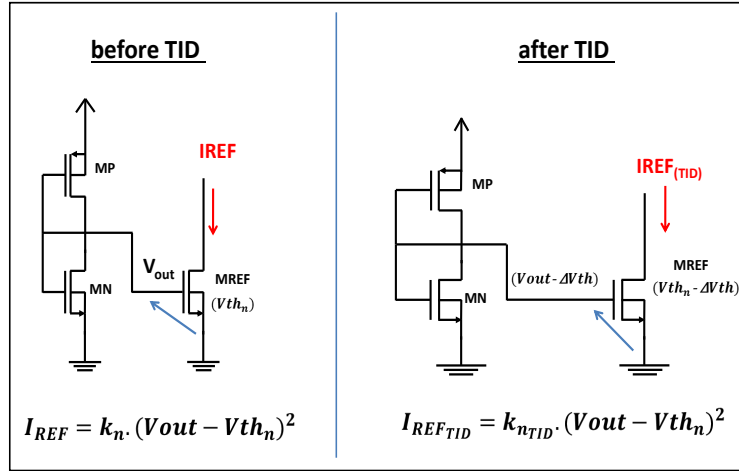


Figure 5.17: Current source insensitive to V_{th} shifts.

Thus, the transistor M_{REF} has an unchanged overdrive voltage V_{ov} . However, its drain current $I_{REF_{TID}} = k_{n_{TID}} \cdot V_{ov}$ varies linearly with the mobility μ_n . This is degraded with the TID effects and leads to decrease the current $I_{REF_{TID}}$. In order to limit this mobility degradation impact on the drain current $I_{REF_{TID}}$, a degeneration resistor can be added to the transistor M_{REF} . Indeed, as shown in Fig.5.18 when the current $I_{REF_{TID}}$ decreases, the gate-to-source $V_{GS} = V_{out_{TID}} - R \cdot I_{REF}$ of the transistor M_{REF} increases. This in turn results in an increase in $I_{REF_{TID}}$, a change that is opposite to that initially assumed. Thus the resistor R induces a negative feedback action and reduces TID effects on the transistor M_{REF} .

B- Simulation results :

The current source has been simulated at a temperature of 25 °C, using the sizes shown in Table 5.4. Figure 5.19 shows the simulated reference current with and without; 1) voltages threshold shift, 2) mobilities degradation. The current source gives a reference current $I_{REF} = 10 \mu A$ with a variation 1) lower than 1% with $V_{th_{n,p}}$ a negative shift of up to 250 mV, 2) lower than 5% when the mobilities degradation reaches up to 25%. Figure 5.20 shows the simulated reference with and without TID effects (both $V_{th_{n,p}}$ and mobilities).

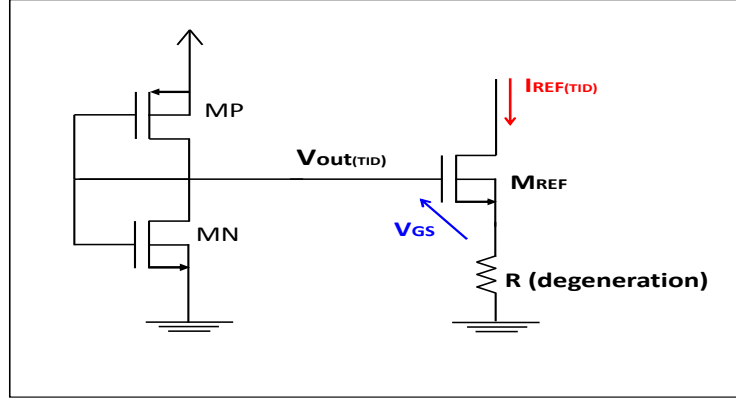
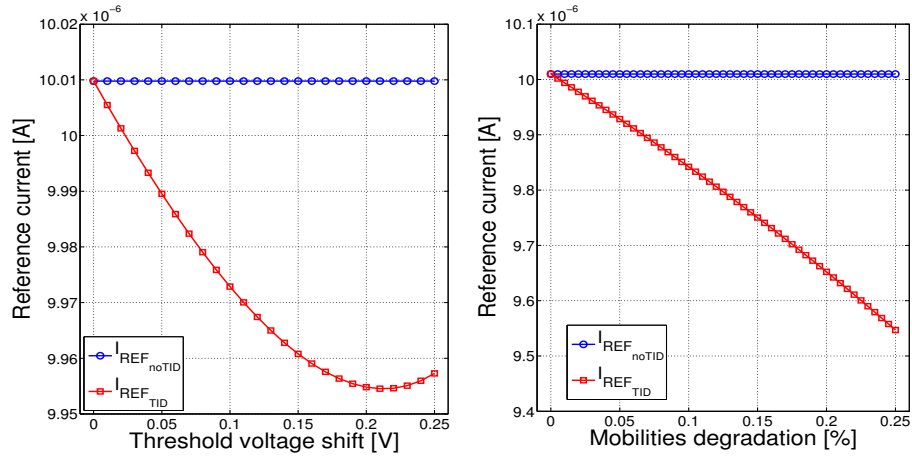


Figure 5.18: Degeneration resistor action in the current source.

Table 5.1: Current source devices dimensions.

Parameter	Description	Value
$(W/L)_{MP}$	Size of PMOS MP	$0.5 \mu\text{m}/10 \mu\text{m}$
$(W/L)_{MN}$	Size of NMOS MN	$0.5 \mu\text{m}/10 \mu\text{m}$
$(W/L)_{MREF}$	Size of NMOS M_{REF}	$7.5 \mu\text{m}/1 \mu\text{m}$
R	degeneration resistor value	$30 \text{ k}\Omega$


 Figure 5.19: I_{REF} with and without 1) voltages threshold shift 2) mobilities degradation at 25°C .

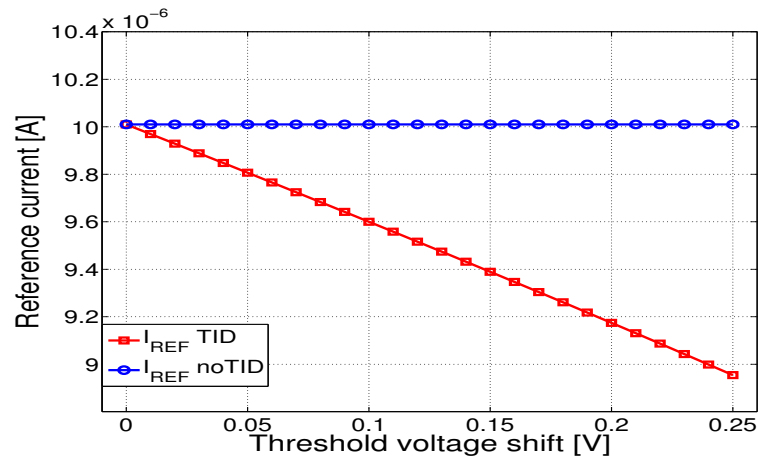


Figure 5.20: Reference current with and without TID effects at 25°C.

This technique can also be used for a source current with a PMOS transistor (Fig. 5.21).

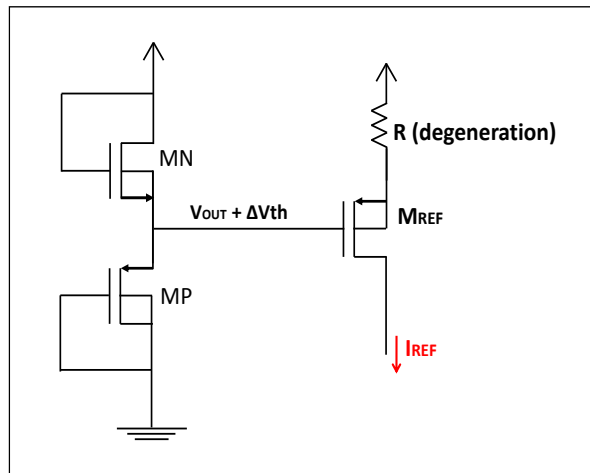


Figure 5.21: TID hardened current source with a PMOS transistor.

5.4.1.2 Hardened current source

Figure 5.22 shows the schematic of the proposed hardened current source. It is composed by an error amplifier regulating the gate-to-source voltage V_{GS} of a NMOS transistor (MN1A in Fig.5.22), in a way to fix its drain current (at $I_D = 1 \mu A$) versus temperature, TID and process corners variations. This unchanged drain current can be copied using a current mirror, and provides a reference current I_{REF} as shown in Fig.5.22. Next paragraphs show and explain the current source and the error amplifier designs.

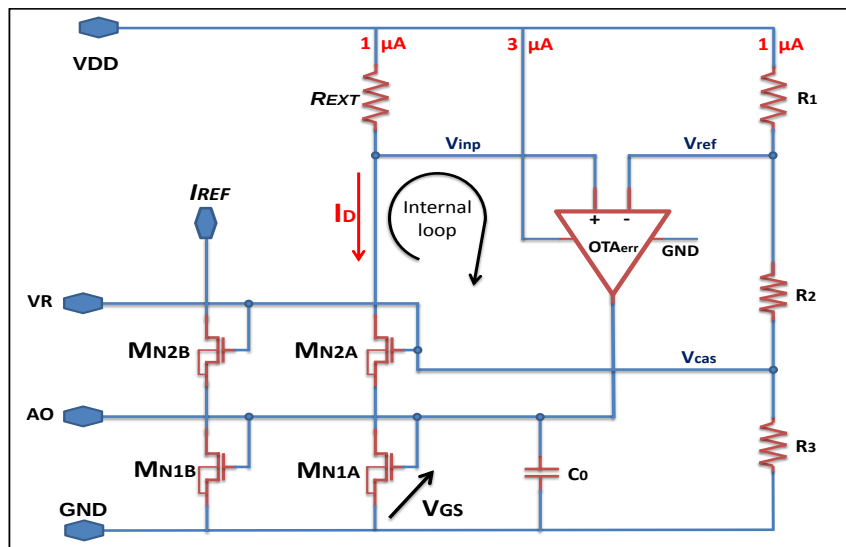


Figure 5.22: Hardened current source using NMOS biasing.

The following specifications have been considered for the design simulations:

- A fixed supply voltage $VDD = 2.5$ V
- A temperature range from -40 up to $+200$ °C
- TID effects, including a negative shift of threshold voltages $Vth_{n,p}$ up to 200 mV with carriers mobilities degradations up to 20%.
- All process corners of the transistors have been considered: 1) Typical case (Typ), 2) Fast NMOS and PMOS (FFA) which correspond to the case when the threshold voltages $Vth_{n,p}$ are low, and the carriers mobilities $\mu_{n,p}$ are high, 3) Slow NMOS and PMOS (SSA), in this case the $Vth_{n,p}$ are high and the carriers mobilities $\mu_{n,p}$ are low, 4) Fast NMOS and slow PMOS (FSA), 5) Slow NMOS and fast PMOS (SFA).

Tables 5.2 and 5.3 give the simulated threshold voltages $Vth_{n,p}$ and the carriers mobilities $\mu_{n,p}$ of MOSFETs at different temperatures and the process corners. In order to take into account the TID effects on MOSFETs, a negative shift of 200 mV has to be added to the $Vth_{n,p}$ values, as well as a degradation of 20% of the $\mu_{n,p}$ values.

Table 5.2: Simulated threshold voltages of the MOSFETs versus temperature and process corners.

Process corners	Temperature (°C)	Vth_n (mV)	Vth_p (mV)
Typical	-40	499	-584
	+25	440	-536
	+200	282	-406
FFA	-40	457	-543
	+25	399	-496
	+200	242	-367
FSA	-40	442	-636
	25	384	-588
	+200	226	-461
SFA	-40	555	-531
	+25	497	-483
	+200	338	-354
SSA	-40	541	-624
	+25	482	-576
	+200	323	-476

A comparison of these simulated values shows that the temperature, the process corners and the TID have a similar influence on the MOSFETs characteristics (up to 200 mV shifts on $Vth_{n,p}$, and more than 20% $\mu_{n,p}$ degradation). Thus, we have to take all process corners, the temperature and the radiation effects into account during the design phases.

A- Current source design :

The design of the current source is based on the introduction of a negative feedback between the error amplifier OTA_{err} and the transistor MN1A. This allows to keep a fixed drain current ($I_D = 1 \mu A$) in MN1A by adjusting its gate-to-source voltage V_{GS} . In fact, when the current I_D is lowered (by TID, temperature or process corners) the positive input of the OTA is increased

Table 5.3: Simulated carriers mobilities of the MOSFETs versus the temperature and the process corners.

Process corners	Temperature (°C)	μ_n (cm ² /V.s)	μ_p (cm ² /V.s)
Typical	-40	353	143
	+25	308	135
	+200	216	111
FFA	-40	382	164
	+25	336	151
	+200	240	126
FSA	-40	370	159
	25	323	145
	+200	228	118
SFA	-40	338	132
	+25	295	124
	+200	205	102
SSA	-40	324	128
	+25	282	118
	+200	195	97

($V_{inp} = VDD - R_{EXT} * I_D$), thereby the OTA_{err} output voltage (which is the V_{GS}) is increased, and leads to increase back the current I_D . The same compensation happens again when the current I_D is increased. Thus, copying I_D gives a reference current I_{REF} . Therefore, the following design constraints have to be considered:

- The transistor MN1A should be designed with a gate-to-source voltage $V_{GS} > 200$ mV, as this voltage would be reduced by the OTA_{err} in order to compensate the lowering of the threshold voltage caused by the process corners, the temperature and the TID effects (up to 200 mV decrease in V_{th}). Here, a $V_{GS} = 300$ mV has been chosen in order to keep some margin.
- The resistor R_{EXT} (Fig.5.22) connected to the positive input of the amplifier ($V_{inp} = VDD - R_{EXT} * I_D$) has to remain unchanged in order to compensate properly the variation in the drain current I_D of the transistor MN1A. However, in the used 130 nm PD SOI technology, the process variation of the resistors is high, about 30%¹. Therefore, an external resistor has to be used.

¹From the "design rules manual" of the used 130 nm PD SOI technology

- A minimum DC gain is required in the error amplifier OTA_{err} in order to perform a good regulation, and to obtain a small variation in the reference current I_{REF} . DC simulations of the current source have been performed using an ideal error amplifier. Figure 5.23 shows the simulated I_{REF} versus DC gain of the ideal error amplifier for the different process corners, temperatures and TID effects. Thus, for a variation of I_{REF} lower than 0.5%, the DC gain has to be higher than 55 (V/V) or 35 dB. Concerning the bandwidth of the error amplifier, as the regulation concerns the DC signals, a bandwidth of some kHz is sufficient.

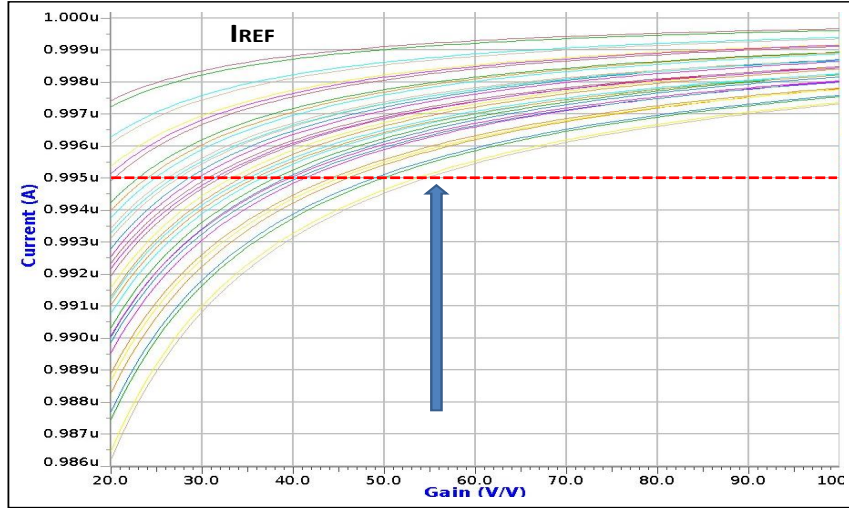


Figure 5.23: Simulated I_{REF} versus error amplifier DC gain, at different process corners, temperature and TID effects.

- The power supply is considered as fix ($V_{DD} = 2.5$ V), thus the negative input voltage V_{ref} of the OTA_{err} can be generated directly from a resistive divider (R_1 , R_2 and R_3). In the case when the power supply V_{DD} changes, a voltage reference has to be used to generate the voltage V_{ref} as shown in Fig.5.24.

The drain current of transistor MN1A has been chosen at $I_D = 1 \mu\text{A}$ to limit the sizes of the used resistors to a maximum value of $2.5 \text{ M}\Omega$ ($R_1 + R_2 + R_3$). This current I_D can be reduced by increasing the resistors (R_1 , R_2 and R_3) values, or by decreasing the power supply (V_{DD}).

For the internal loop stability of the current source, a capacitor $C_0 = 15 \text{ pF}$ has been added in the schematic of the current source. Finally, in order to improve the output impedance of this current source, a cascode stage has

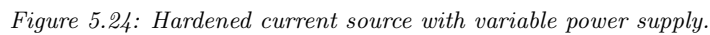


Table 5.4: Current source devices dimensions.

B- Error amplifier OTA_{err} :

A single stage OTA [56] has been used for the error amplifier OTA_{err} in the current source design (Fig.5.25). In order to ensure a low power and a high gain, the OTA_{err} has been designed with transistors in the subthreshold regime with a high $[g_m/I_d] = 20 \text{ V}^{-1}$. The maximum current consumption by branch is only 600 nA (at 200 °C with FFA corner process). The gain of such a single stage OTA is $A_V = [g_m/I_d] \cdot V_{ea}$, where V_{ea} is the Early voltage of the output transistor [56].

Figure 5.26 shows the simulated frequency response of the OTA gain (in the follower configuration) for different temperatures, TID effects and process corners variations. Tables 5.5 and 5.6 give the dimensions of the used devices and the OTA performance.

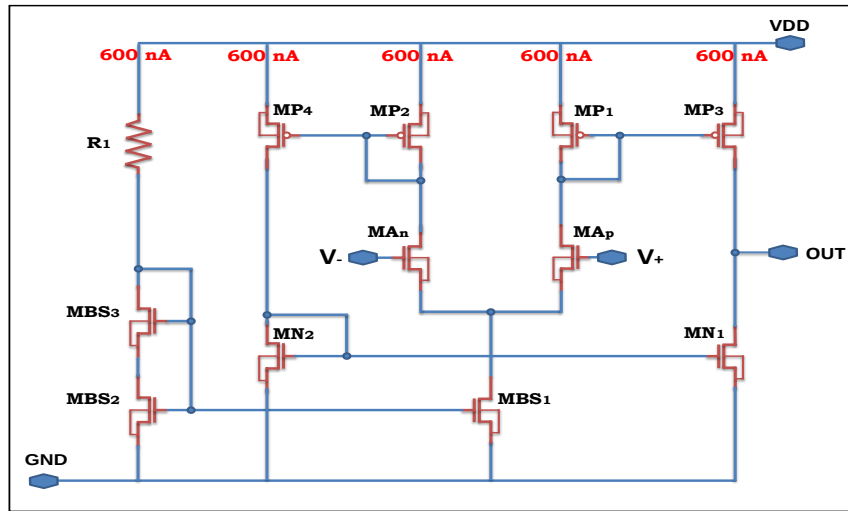


Figure 5.25: Error amplifier schematic.

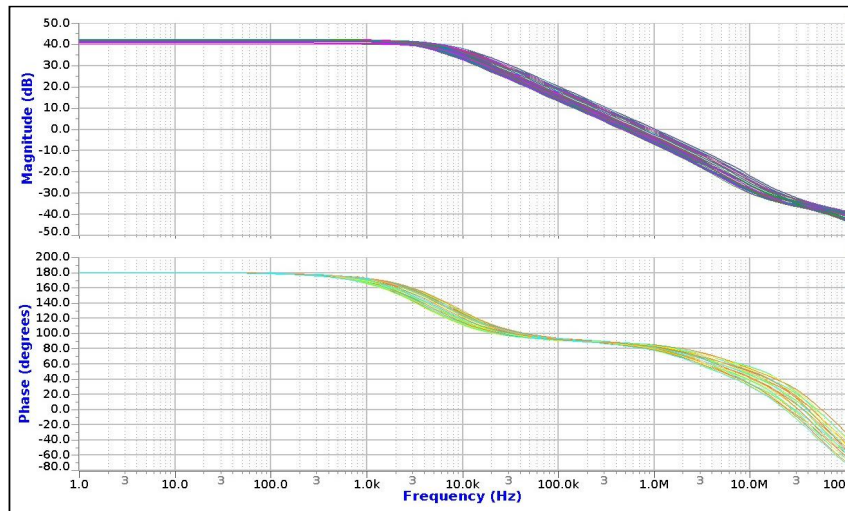


Figure 5.26: Simulated frequency response of the OTA, at different process corners, temperatures and TID effects.

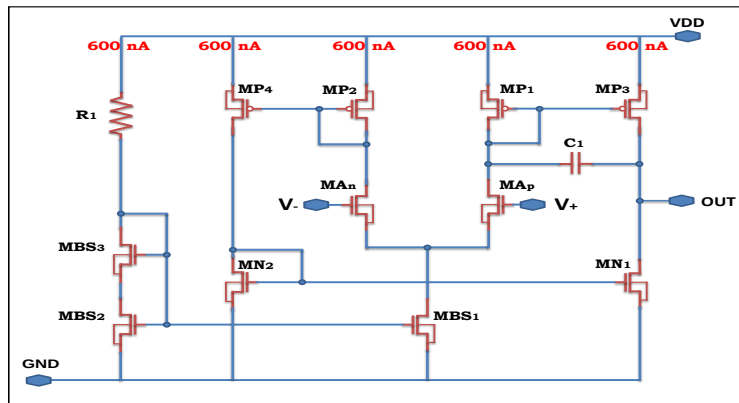
Table 5.5: OTA devices dimensions.

Parameter	Description	Value
$(W/L)_A$	Sizes of NMOS M_{An} , M_{Ap}	$2\text{ }\mu\text{m}/0.5\text{ }\mu\text{m}$
$(W/L)_{MP}$	Sizes of PMOS $M_{MP1,2,3,4}$	$5\text{ }\mu\text{m}/0.5\text{ }\mu\text{m}$
$(W/L)_{MN}$	Sizes of NMOS $M_{MN1,2}$	$5\text{ }\mu\text{m}/0.5\text{ }\mu\text{m}$
$(W/L)_{MBIAS}$	Sizes of NMOS $M_{MBS1,2,3}$	$1\text{ }\mu\text{m}/10\text{ }\mu\text{m}$
R_1	R_1 resistor value	$3.5\text{ M}\Omega$

Table 5.6: OTA performance summary.

Parameter	Description	Value
VDD	Power supply	2.5 V
I_{Diss}	Max current consumption @ 200°C	$3\text{ }\mu\text{A}$
A_{V0}	Min DC gain	40 dB
f_T	Min cutoff frequency	450 kHz
C_L	Load capacitance	1 pF
φ_M	Min Phase margin	84°

In order to reduce the large capacitor $C_0 = 15\text{ pF}$ to only 5 pF without impacting the stability of the system, a second capacitor $C_1 = 1\text{ pF}$ has been added in the schematic of the error amplifier, using the advantage of the Miller effect (Fig.5.27). This technique, is possible here as the transconductance gm_{MP_1} of the transistor MP_1 is very low (about 10^{-6}). Thus, the dominant pole generated by C_1 ($Z_p = gm_{MP_1}/C_1$) remains in low frequencies.

Figure 5.27: Error amplifier schematic with capacitor C_1 using the Miller effect.

C- Simulation results :

In order to check the stability of the system, AC simulations have been performed for the internal loop (Fig.5.22). Thus, the loop has been opened in the positive input of the error amplifier OTA_{err} . Figure 5.28 shows the simulations results, which confirm the stability of the system with a good phase margin higher than 60° .

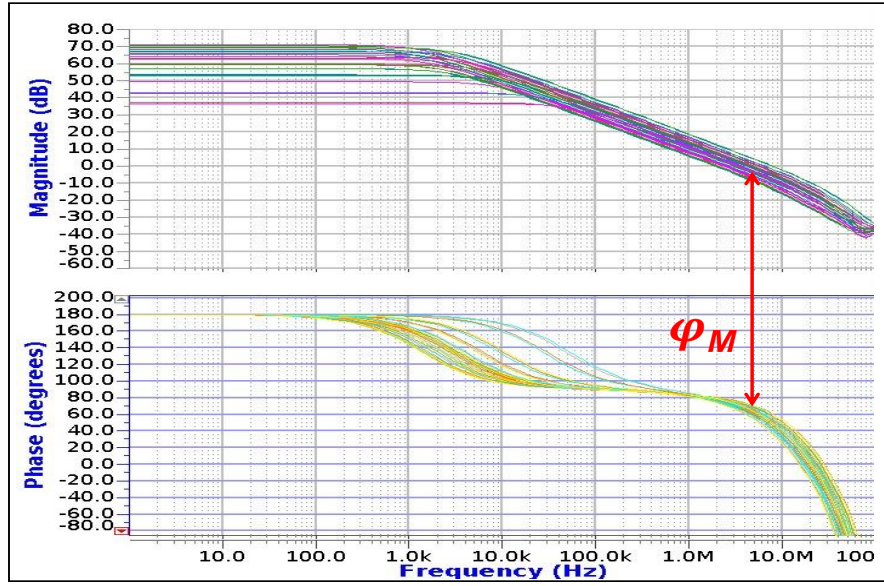


Figure 5.28: AC simulations results of the internal loop stability versus TID, temperatures and process corners variations.

The DC simulations were performed versus TID, temperatures and process corners variations. Figure 5.29 shows the simulated reference current I_{REF} . It is about $1\ \mu\text{A}$ with a variation lower than $0.6\%^2$. The total current consumption is $5\ \mu\text{A}$ including $3\ \mu\text{A}$ in the OTA_{err} . Table 5.7 summarizes the current source performance.

It has to be noted that a similar current source, based on PMOS monitoring, can be designed with the same principle as shown in Fig.5.30.

²This low variation is obtained for a fixed power supply ($V_{DD} = 2.5\ \text{V}$). When it is not the case (as in Fig.5.24), the variation will be similar to that of the generated reference voltage V_{ref} .

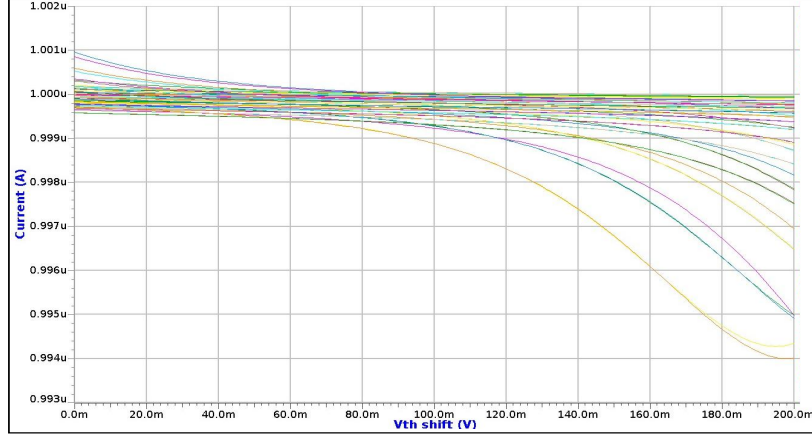


Figure 5.29: Simulated reference current I_{REF} versus TID modeled as $V_{th(n,p)}$ and $\mu_{n,p}$ degradations, at different temperatures and process corners.

Table 5.7: Current source performances.

Parameter	Description	Value
I_{REF}	Reference current	$1 \mu A$
$\Delta(I_{REF})$	Max variation	0.6 %
I_{Diss}	Max current consumption @ $200^\circ C$	$5 \mu A$
φ_M	Min phase margin of the internal loop	60°

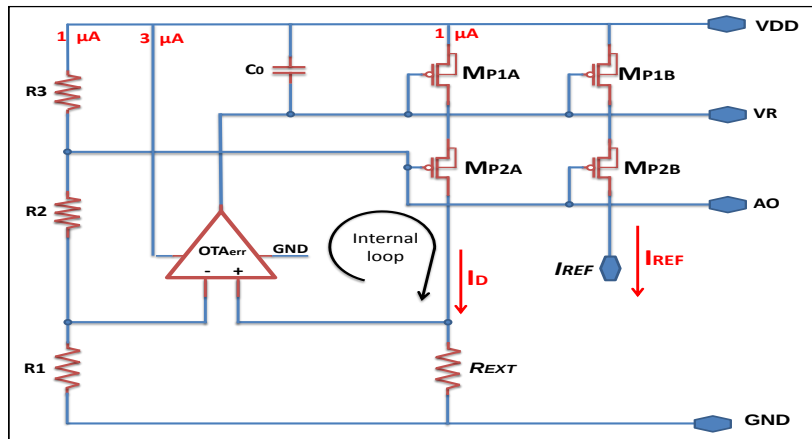


Figure 5.30: Harsh environment current source using PMOS biasing.

5.4.2 The body biasing technique

In digital circuits, the body biasing is a technique where the substrate or wells of CMOS transistors are biased to a voltage different from the ground and the power supply. This induces a voltage difference between the transistor source and body ($V_{bs} \neq 0$), allowing the control of the threshold voltage V_{th} as [57]:

$$V_{th} = V_{T0} + \gamma(\sqrt{2\phi_F - V_{bs}} - \sqrt{2\phi_F}) \quad (5.7)$$

where V_{T0} is the zero-bias threshold, ϕ_F is the Fermi potential, and γ is the body effect parameter.

For instance, applying a positive body-to-source voltage ($V_{bs} > 0$) leads to decrease the transistor threshold voltage V_{th} . However, the body-to-source voltage has to be limited to max 0.5 V in order to avoid the forward biasing of the parasitic bipolar (source/drain junctions) in the MOS transistor.

Two cases are defined for the body biasing technique; firstly, the "Reverse Body Bias" (RBB) [58], which involves applying a negative body-to-source voltage to the transistor. This is mainly used to reduce leakage and power consumption of digital circuits during standby mode. Secondly, the "Forward Body Bias" (FBB) [59] is considered when a positive body to source voltage is applied. It can be used to increase the speed of the logic gates.

For radiation effects, the body biasing has already been used to mitigate TID on logic gates [60,61]. Furthermore, as shown in reference [62], the RBB provides smaller transistors and a lower leakage up to 1 Mrad(Si) than edgeless transistors in a 130 nm bulk technology.

For analog circuits, the body biasing has been used to correct the process variations, as well as to reduce the temperature and aging effects in CMOS transistors [63,64]. It has also been used to optimize the low power and to improve the analog performances, such as gain and linearity [57], or to increase the R_{on}/R_{off} ratio of analog switches as shown in Fig.5.31.

The body biasing in digital design involves applying a fixed body bias for transistors. Whereas, in analog circuits, it is rather a dynamic body biasing, which gives an adaptive voltage depending on the variability of the transistor threshold voltage V_{th} .

Based on these previous uses and advantages of the body biasing technique in both digital and analog circuits, we have chosen to introduce and to develop the dynamic body biasing technique as a mitigation technique against TID and temperature effects, as well as process corners variations in analog circuits.

Next sections show how the body biasing technique can be implemented in two different ways. Firstly, by using the direct body biasing technique (DBB), secondly by using the body replica biasing technique (BRB) [57]. Both these techniques have been implemented for a standard single stage OTA amplifier,

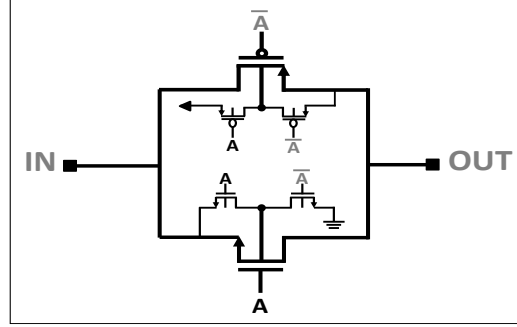


Figure 5.31: Transmission gate with adaptive body biasing [65].

and for a Folded cascode amplifier, both designed in the 130 nm PD SOI CMOS technology, and simulated in the follower configuration.

5.4.3 Effect of harsh environments and process corners variations on a single stage OTA amplifier

Figure 5.32 shows the schematic of a standard single stage OTA amplifier, designed with a $[g_m/I_d] = 20 \text{ V}^{-1}$, and biased with a fixed current ($I_{ref} = 2 \mu\text{A}$) from the hardened current source. Table 5.8 gives the transistors sizes.

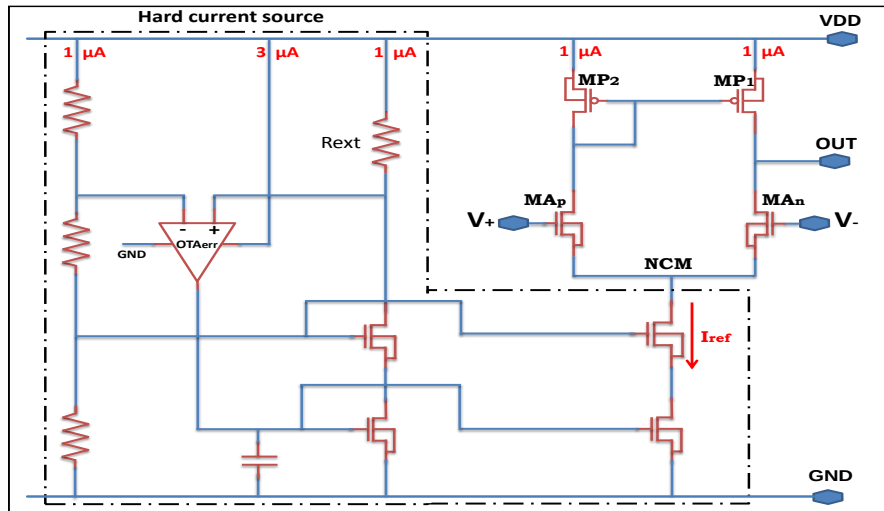


Figure 5.32: Simple single stage OTA using the hardened current source.

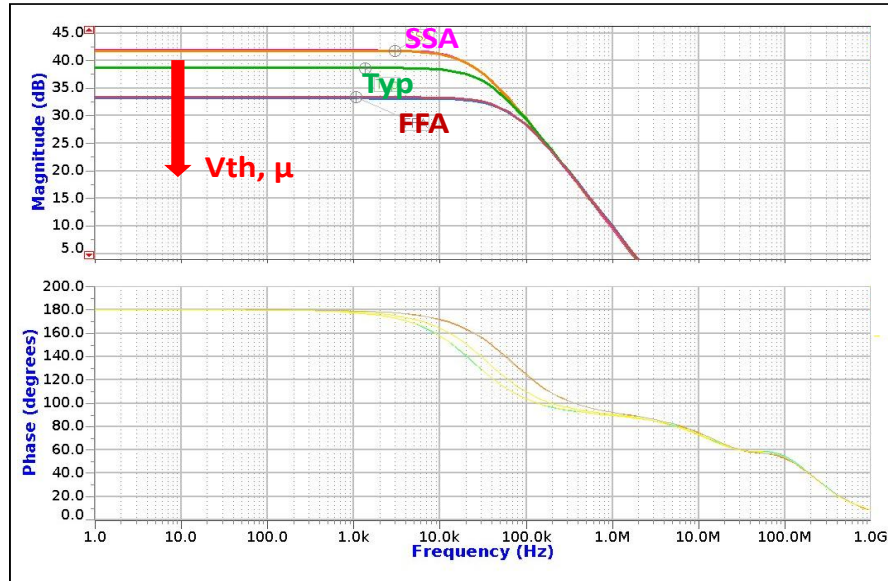
Table 5.8: Transistors dimensions of the single stage OTA.

Parameter	Description	Value
$(W/L)_A$	Size of NMOS M_{An} , M_{Ap} ,	$9.6 \mu\text{m}/1 \mu\text{m}$
$(W/L)_{MP}$	Size of PMOS M_{MP1} , M_{MP2}	$12.5 \mu\text{m}/1 \mu\text{m}$

5.4.3.1 Simulation of the OTA gain

This OTA amplifier has been simulated in the follower configuration, under the combined effect of temperature and radiation at different process corners, an input common mode of 1.5 V, and a load of $C_L=1$ pF.

Figures 5.33, 5.34 and 5.35 show the gain curves of three process corners (Typ, FFA, SSA) at three temperatures (-40 , $+25$ and $+200^\circ\text{C}$) with TID effects. A first conclusion of these figures is that the OTA gain is degraded when the threshold voltages and the mobilities of the transistors are lowered.

Figure 5.33: OTA simulated gain for three process corners at $+25^\circ\text{C}$ with TID effects.

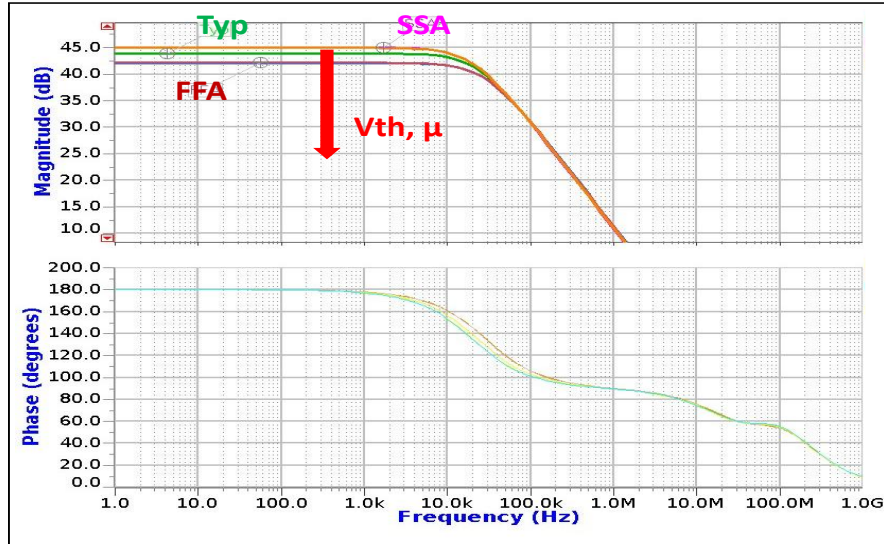


Figure 5.34: OTA simulated gain for three process corners at -40°C with TID effects.

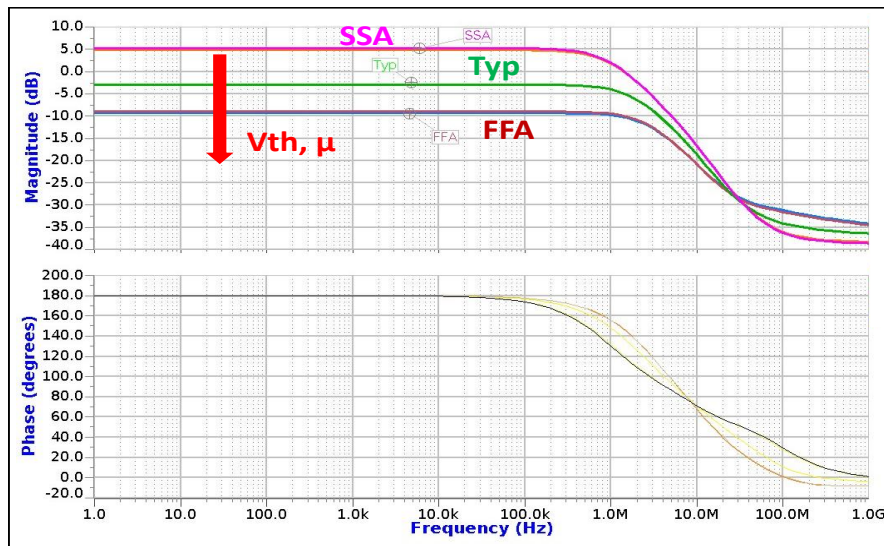


Figure 5.35: OTA simulated gain for three process corners at $+200^{\circ}\text{C}$ with TID effects.

Figures 5.36, 5.37 and 5.38 present the OTA gain curves versus TID effects at the three previous temperature for the typical case. Also in this case when the threshold voltages and the mobilities are reduced, the OTA gain is degraded.

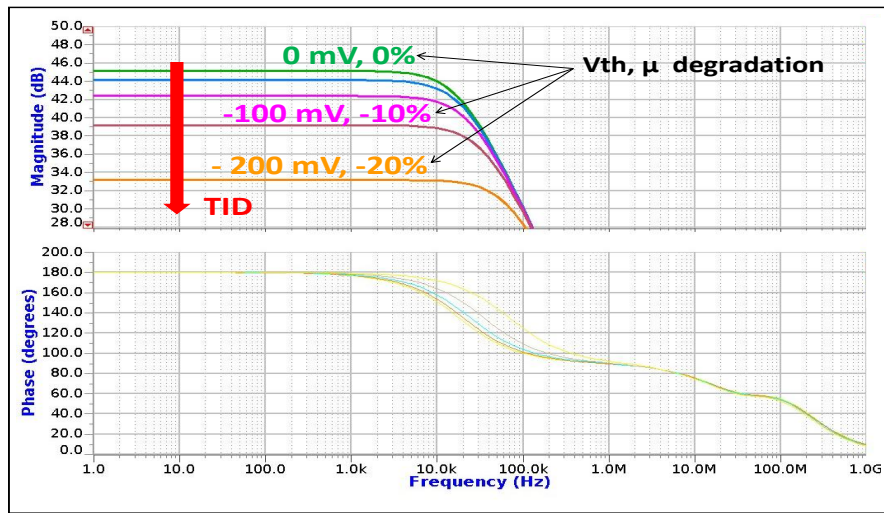


Figure 5.36: OTA simulated gain versus TID effects at $+25^{\circ}\text{C}$ in the typical corner.

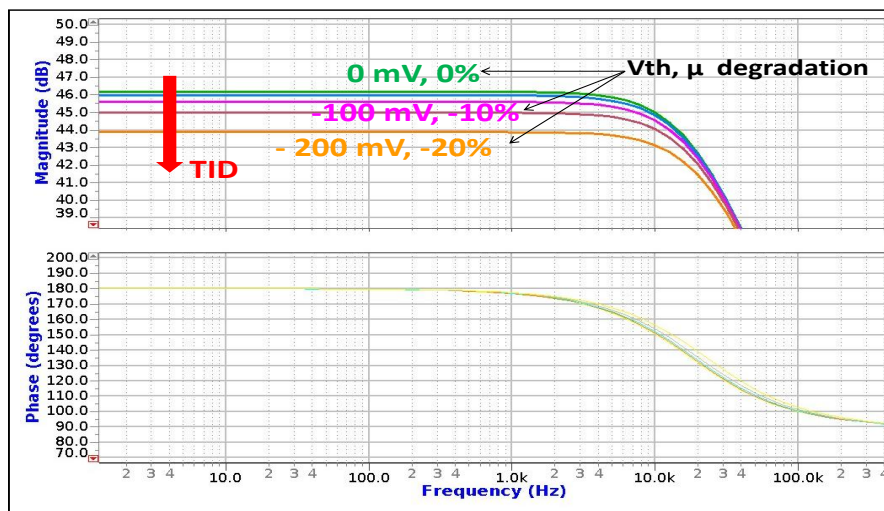


Figure 5.37: OTA simulated gain versus TID effects at -40°C in the typical corner.

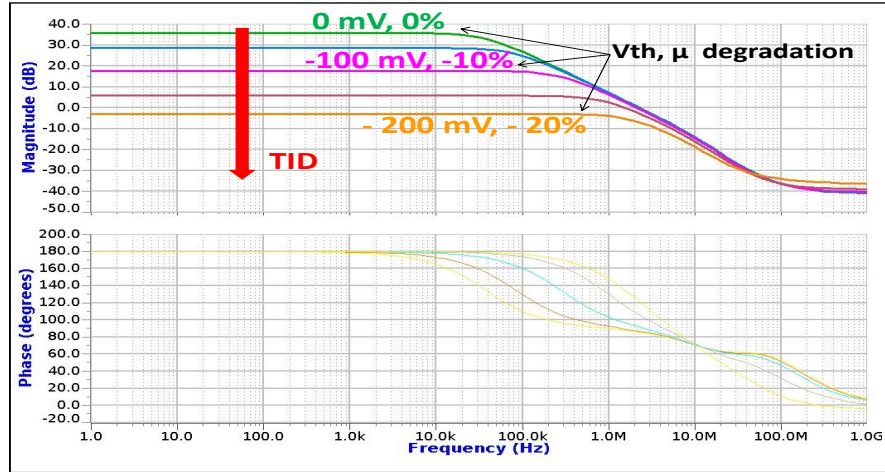


Figure 5.38: OTA simulated gain versus TID effects at $+200^{\circ}\text{C}$ in the typical corner.

The last figure Fig.5.39 shows simulated gain curves at the different process corners for a range of temperatures from -40 up to $+200^{\circ}\text{C}$ with the TID effects. The gain becomes very low and even lower than 1 in extreme cases of reduced V_{th} and μ . This is due to the desaturation of the differential pairs transistors in these extreme cases as explained below in 5.4.3.2.

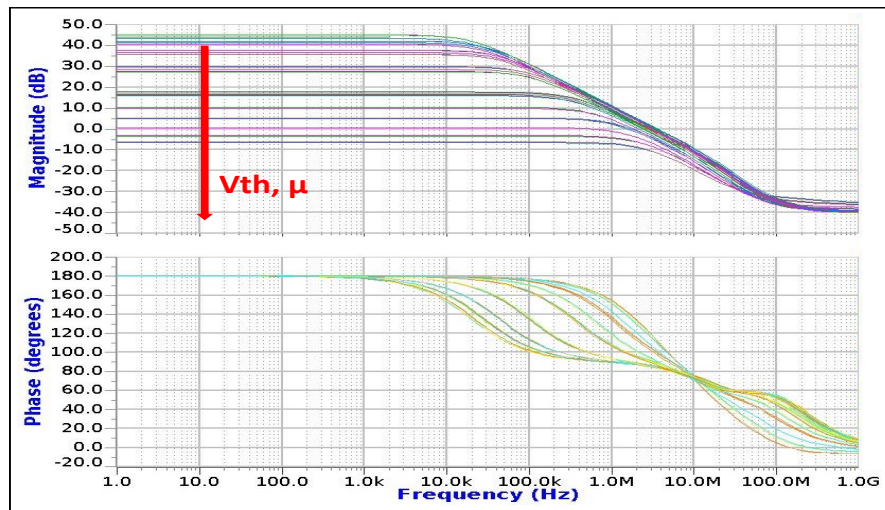


Figure 5.39: OTA simulated gain versus TID and temperature effects for different process corners.

5.4.3.2 Explanation of the gain degradation

The degradation of the OTA gain with the decrease in threshold voltages and mobilities can be explained as:

1- When the gain remains relatively high, the degradation can be explained through the OTA gain expression which is:

$$A_V = g_m \cdot (r_{on} // r_{op}) = \frac{2 \cdot V_{ea_n} \cdot V_{ea_p}}{(V_{ea_n} + V_{ea_p}) \cdot V_{ov_{pair}}} \quad (5.8)$$

where $g_m \cong I_{ref} / V_{ov_{pair}}$ is the transconductance and $V_{ov_{pair}} = (V_{GS_{pair}} - V_{th})^3$ of the differential pair transistor, $r_{on} = 2 \cdot V_{ea_n} / I_{ref}$ and $r_{op} = 2 \cdot V_{ea_p} / I_{ref}$ are the output resistances and $V_{ea_{n,p}}$ are the Early voltages of the NMOS and PMOS transistors respectively.

Under the effects of TID, temperature and process corners, the threshold voltage V_{th_n} of NMOS transistors is decreased and the mobility is degraded. Now, as the current $I_{ref}/2$ ($\propto \mu \cdot V_{ov_{pair}}$) in the differential pair transistor is unchanged, the voltage $V_{ov_{pair}}$ is increased firstly in order to compensate the mobility degradation, and secondly due to the decrease in the threshold voltage V_{th_n} . This lowers the gain A_V (Eq.5.8). The OTA tries to limit the $V_{ov_{pair}}$ rise by increasing the common source voltage "NCM". However, this reduces the drain-to-source voltage V_{DS} of the differential pair transistor, which reduces its Early voltage V_{ea_n} and leads to reduce again the OTA gain (Eq.5.8).

2- When the gain becomes very low in extreme cases of reduced V_{th} and μ , the transistor MA_n of the differential pair leaves the saturation region, and the OTA gain is totally degraded. For instance, a very low $V_{DS} = 10$ mV in the transistor MA_n is shown in the Fig.5.40. This, shows the DC nodes voltages for the worst case of simulation corresponding to the FFA process corner at a temperature of 200 °C, and with hard TID effects modeled as a negative shift of 200 mV in the threshold voltages, and 20% degradation in the mobilities.

In order to limit this gain degradation in this single stage OTA, the body biasing techniques (DBB and BRB) have been implemented in such a way as to reduce the threshold voltages shifts, and the increase in the common source voltage "NCM". Both biasing techniques, the direct body biasing (DBB) and the body replica biasing (BRB), are presented in the next paragraphs.

It has to be noted that the previous error amplifier OTA_{err} used in the current source, has been used as an error amplifier in the following rad-hard amplifiers structures with the same sizes, and an internal capacitor $C_1 = 1$ pF with Miller effect to meet AC stability in the internal loops created by this

³Called the overdrive voltage for transistor designed in strong inversion regime

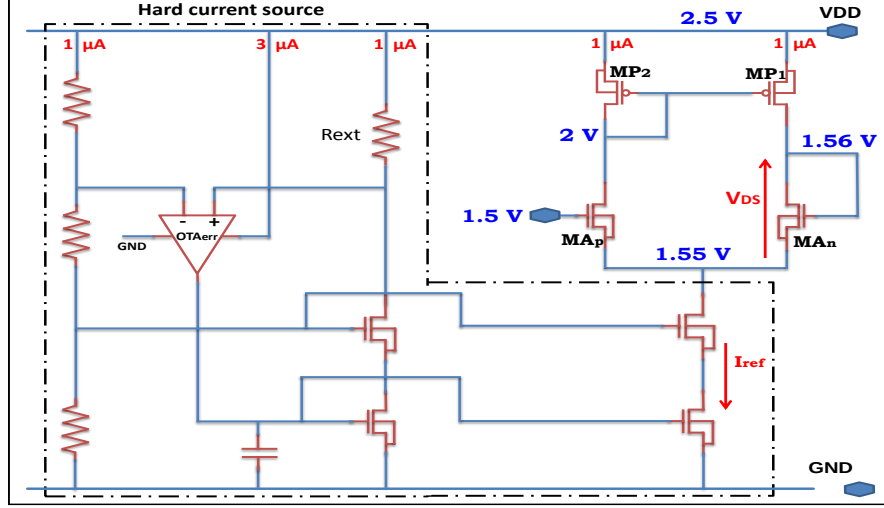


Figure 5.40: OTA DC nodes voltages at the worst case of simulation.

OTA_{err} . The same specifications as for the design of the current source have been considered, namely:

- A fixed supply voltage $VDD = 2.5 \text{ V}$
- A temperature range from -40 up to $+200^\circ\text{C}$
- TID effects, including a negative shift of the threshold voltages $Vth_{n,p}$ up to 200 mV with a mobilities degradation up to 20%
- All process corners have been considered

5.4.4 Design of hardened amplifiers using the direct body biasing (DBB)

When the single stage OTA has a fixed input common mode V_{CM} , the DBB technique can be used as shown in Fig.5.41.

A- Design principle :

The idea is to keep a fixed voltage $V_{ov_{pair}}$ for the differential pair transistors by introducing a negative feedback between their body V_B and their source NCM nodes. Thus, the error amplifier OTA_{err} keeps an unchanged voltage in the source node NCM by adjusting the voltage of the body node V_B (Fig.5.41). In fact, when the NMOS threshold voltage Vth_n decreases (due to process corners, TID or temperature), the voltage VGS_{pair} tends to decrease in order to keep a fixed current in the differential pair. This comes through the increase of the

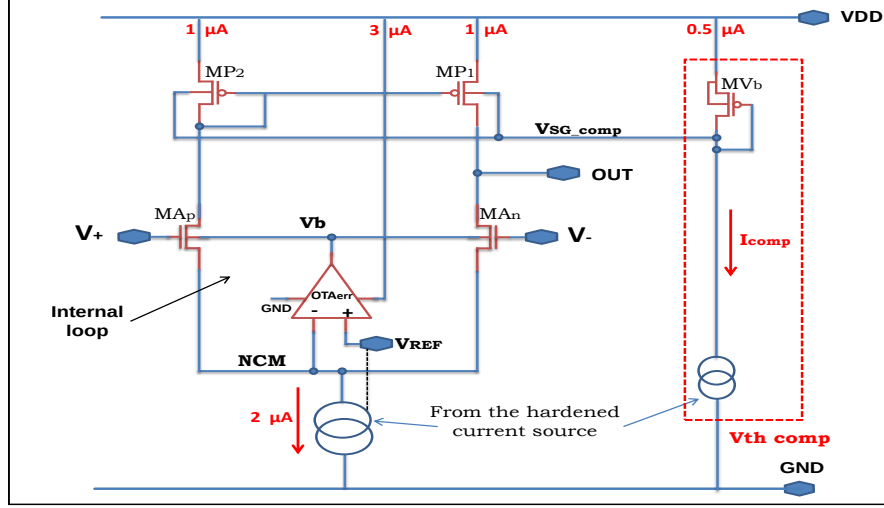


Figure 5.41: Schematic of a hardened amplifier using the DBB technique.

node NCM , which is also the negative input of the OTA_{err} . As a result, the voltage of V_B (output of the OTA_{err}) is decreased, and leads to increase back the threshold voltage V_{th_n} . Again, the same compensation happens when the V_{th_n} increases, mainly due to process corners variations in the NMOS transistors.

Another threshold voltage compensation of the PMOS active load transistors (MP_1 and MP_2 in Fig.5.41) can be added to the schematic. The branch "Vthp comp" is used to generate a voltage V_{SGcomp} used as a body bias of the PMOSs active load. This stage is composed by a diode connected PMOS (M_{Vb} in Fig.5.41) biased with a small fixed current ($I_{comp} = 500$ nA) from the current source. Under TID effects, the source-to-gate voltage ($VDD - V_{SGcomp}$) of transistor M_{Vb} increases exactly as the PMOS threshold voltage shift $\Delta(V_{th_p})$. This leads to decrease the body-to-source voltage of the PMOSs active load (MP_1 and MP_2), and to decrease their absolute threshold voltage value $|V_{th_p}|$, and hence to limit the TID, process corners and temperature effects on these PMOS active load.

It has to be noted that, the voltage V_{SGcomp} has to be no lower than 2 V to avoid the activation of the body-source diode of the PMOS active load transistors ($V_S = 2.5$ V). This can be done by choosing large sizes for the diode connected PMOS M_{Vb} ($W/L = 12.5/0.5$ in μm).

B- Simulation results :

Firstly, the stability simulations of the internal loop have been checked by

opening the loop at the negative input of the OTA_{err} . This gives a large margin phase with a minimum of 64° . Secondly, the AC simulations have been performed with the same previous input common mode of $V_{CM} = 1.5$ V in the follower configuration, and a voltage $V_{REF}=1$ V coming from the resistive divider of the used current source (Fig.5.22).

Figure 5.42 and Table 5.9 show the transfer function and the performances of the OTA using this body biasing technique, versus TID temperature and process corners variations. Which are much better and resolve the gains degradation issue shown in the same OTA without this DBB technique (Fig.5.39). The maximum current consumption is about $10.5 \mu\text{A}$ including $5 \mu\text{A}$ for the hardened current source.

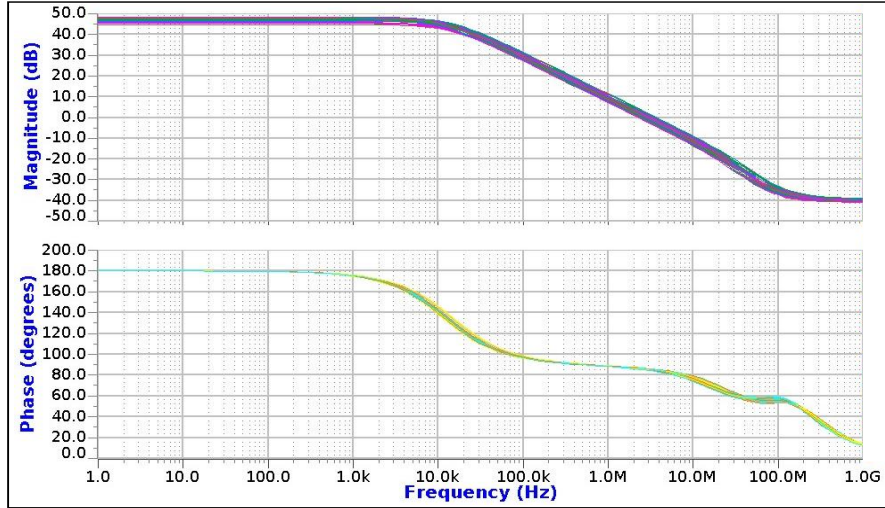


Figure 5.42: OTA simulated results using DBB for different process corners, TID and temperature effects.

Table 5.9: OTA performances using the DBB.

Parameter	Description	Value
A_{V0}	Min DC gain	44 dB
I_{Diss}	Max current consumption @ 200°C	$10.5 \mu\text{A}$
f_T	Min cutoff frequency	2.5 MHz
C_L	Load capacitance	1 pF
φ_M	Min phase margin of internal loop	64°

Figures 5.43 and 5.44 show the simulated DC gain at 200 °C, versus the input common mode at hard TID effects (a threshold voltages negative shift of 200 mV with a mobilities degradation of 20%) for the OTA with (Fig.5.41) and without (Fig.5.32) the body biasing technique. The maximum DC gain is only 6 dB for the OTA without DBB. However, it is higher than 40 dB for the hardened OTA with a large input range from 1 V to 2.1 V.



Figure 5.43: Simulated DC gain of the hardened OTA of Fig.5.41, for the different process and TID effects versus the input common mode, at $T=200^{\circ}\text{C}$.

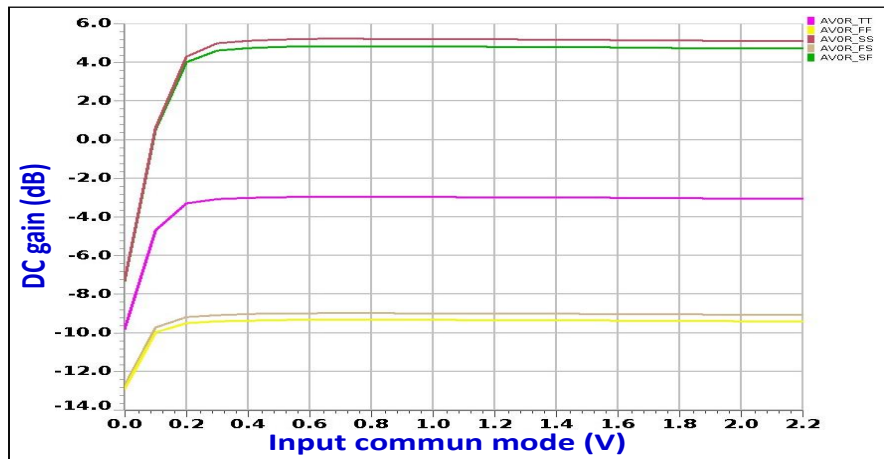


Figure 5.44: Simulated DC gain of the OTA of Fig.5.32, for the different process and TID effects versus the input common mode, at $T=200^{\circ}\text{C}$.

5.4.5 Design of hardened amplifiers using the body replica biasing (BRB)

In this part, the body replica biasing technique (BRB) has been implemented on a replica of the differential pair transistor of the amplifier. Design and simulation results are presented for the single stage OTA with a fixed and variable input common mode. AC simulations were performed with a load capacitance of $C_L = 1$ pF, and in the follower configuration for the OTA.

5.4.5.1 Hardened amplifier with fixed input common mode

A- Design principle :

In this case, a replica of a branch of the differential pair transistor is used to generate an appropriate body voltage able to compensate the variation in threshold voltage V_{th_n} of NMOS transistors. As shown in Fig.5.45, a replica of the differential pair transistor M_{Dup} is biased with a fixed current ($I_D = 1$ μ A) from the current source. Thanks to the resistive network (R_1 and R_2), the gate voltage of the M_{Dup} has the same common mode voltage V_{CM} as the differential pair transistors. The negative feedback has been introduced between the source and body voltages of this replica transistor using the error amplifier OTA_{err} . Its positive input is a fixed voltage V_{REF} which can be taken from the resistive network used in the current source. The value of V_{REF} depends on the input common mode, and on the required gate-to-source voltage in the differential pair transistors $V_{GS_{diff}} = V_{GS_{Mdup}} = V_{CM} - V_{REF}$. Table 5.10 gives the sizes of the transistor M_{Dup} and the R_1 and R_2 .

Table 5.10: Dimensions of the devices used in the OTA.

Parameter	Description	Value
(W/L)	Size of NMOS M_{Dup}	9.6 μ m/1 μ m
R_{CM}	R_1/R_2 resistors values	1 M Ω

The compensation in this case happens as follows, when the threshold voltage of the transistor M_{Dup} is lowered (increased), the source voltage (V_S in Fig.5.45) of the M_{Dup} is increased (decreased), in order to keep the current I_D constant. This increases (decreases) the negative input of the OTA_{err} , leading to decreases (increases) in the body voltage of transistor M_{Dup} (the OTA_{err} output). This compensates the threshold voltage V_{th_n} variation of the transistor M_{Dup} , as well as the differential pair transistors.

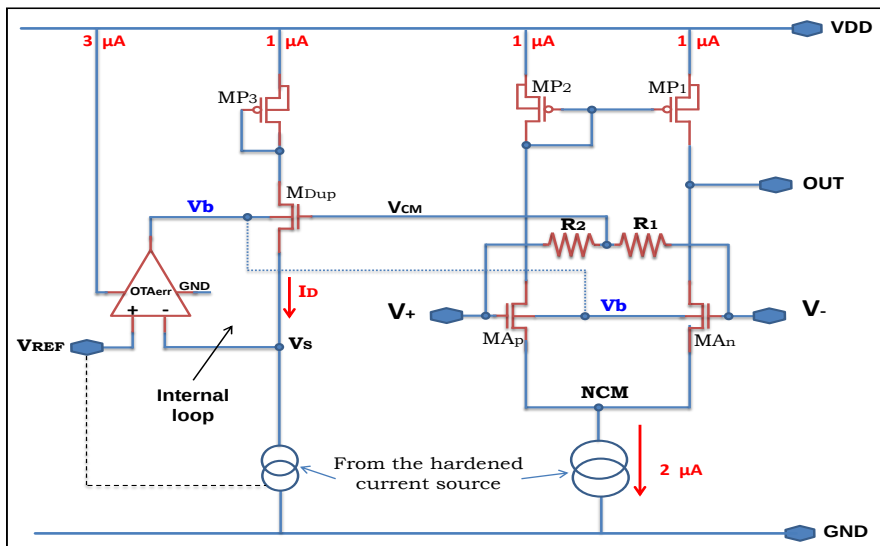


Figure 5.45: Schematic of a hardened amplifier using the BRB technique with a fixed input common mode.

B- Simulation results :

Beside the internal loop stability simulations which give a minimum margin phase of 60° (loop opened at the negative input of the OTA_{err}), the AC simulations have been performed versus TID for all process corners and temperatures from -40°C up to 200°C . Figures 5.46 and 5.47 show the obtained transfer functions, using this BRB technique with a $VGS_{diff} = 300\text{ mV}$ for the two input common mode limits $V_{CMmin} = 0.7\text{ V}$ and $V_{CMmax} = 2.3\text{ V}$. These V_{CM} limits have been extracted from AC simulations, and a limit is considered when the degradation of the gain is lower than 10% versus the typical case.

The lower input common mode $V_{CM_{min}}$ of this hardened amplifier is imposed by the input common mode of the OTA_{err} ($V_{CM_{min}} = V_{CM-OTA} + VGS_{Mdup}$), whereas the higher input common mode $V_{CM_{max}}$ is limited by the source-to-drain voltage of the transistor MP_1 .

Table 5.11 shows the OTA performances. A minimum DC gain of 37 dB and 44 dB is extracted for the input common mode limits. The max current consumption is 11 μ A including 5 μ A in the current source.

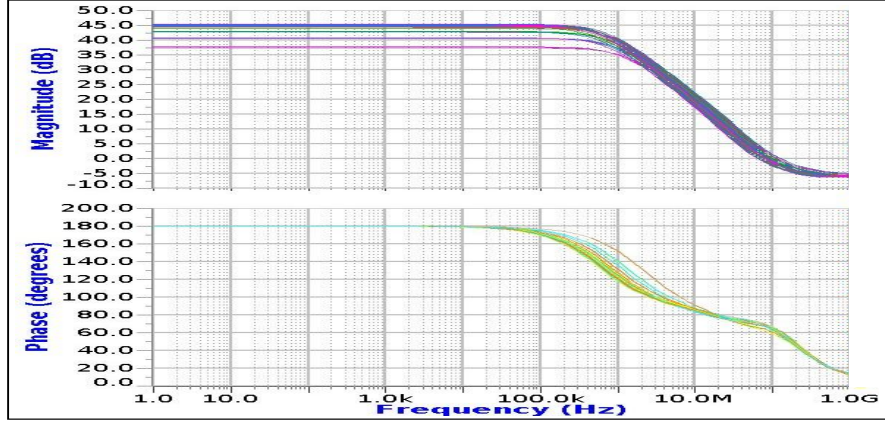


Figure 5.46: OTA simulated results using BRB for different process corners, TID and temperature effects at $V_{CM}=0.7$ V.

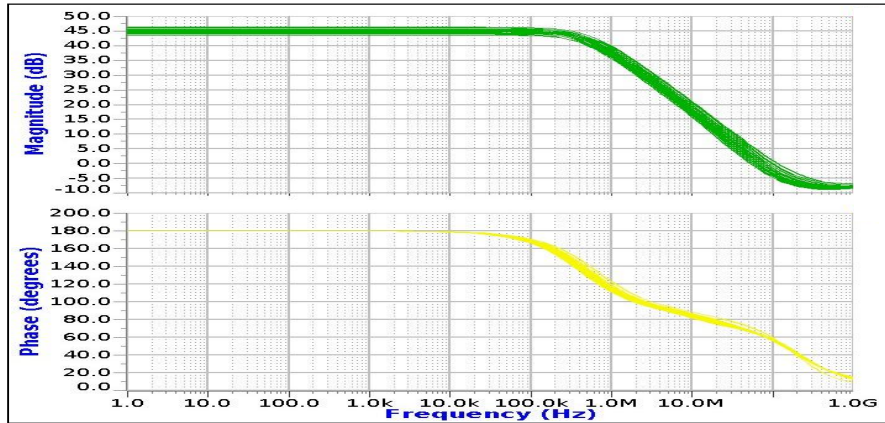


Figure 5.47: OTA simulated results using BRB for different process corners, TID and temperature effects at $V_{CM}=2.3$ V.

Table 5.11: OTA performances using the BRB.

Parameter	Description	Value
A_{V0}	Min DC gain @ $V_{CM} = 0.7/2.3$ V	37/44 dB
I_{Diss}	Max current consumption @ 200 °C	11 μ A
f_T ($C_L=1$ pF)	Min cutoff frequency	2.5 MHz
φ_M	Min φ_M of internal loop	60 °

5.4.5.2 Hardened amplifier with a variable input common mode

A- Design principle :

Figure 5.48 shows the schematic of the hardened OTA used with a variable input common mode.

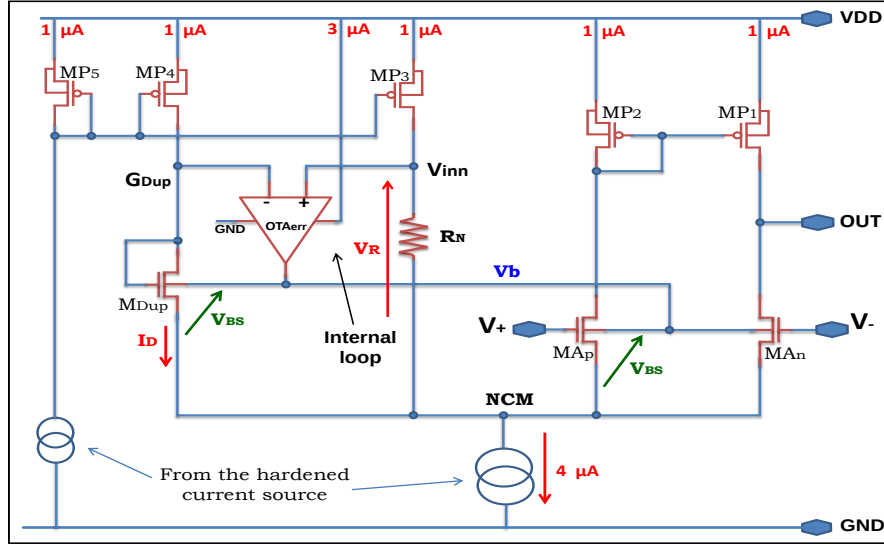


Figure 5.48: Body biasing using the duplicated transistor for a hardened amplifier with a varying input common mode.

Based on the same principle of the previous structure of the BRB technique, except for the replica which is composed in this case, of a diode-connected transistor M_{Dup} biased with a fixed current. The idea here is to generate an appropriate body-to-source voltage V_{BS} in order to compensate the variation in the threshold voltage of the replica, as well as the differential pair transistors. The negative input of the OTA_{err} is connected to a resistor R_N biased by a fixed current from the hardened current source. As the voltage drop ($V_R = V_{inn} - V_{NCM}$) of this resistor is unchanged, thus any variation of the common node NCM (between the replica transistor and the differential pair transistors) is reported to the node V_{inn} , the negative input of the OTA_{err} . This changes the body-to-source voltage V_{BS} in order to compensate the variation in threshold voltage. Table 5.12 gives the sizes of the used transistors and the R_N .

Indeed, when the threshold voltage V_{th_n} is decreased (increased) the voltage value of NCM (and V_S) is increased (decreased) in order to keep a constant $V_{OV} = V_{CM} - V_{th_n}$ in the NMOS transistors. This generates two effects; firstly, it decreases (increases) directly the body-to-source voltage ($V_{BS} = V_B -$

Table 5.12: Dimensions of the devices used in the hardened OTA.

Parameter	Description	Value
$(W/L)_{3-5}$	Size of PMOS MP_3 , MP_4 and MP_5	12.5 $\mu\text{m}/1 \mu\text{m}$
R_N	R_N resistor value	350 k Ω

NCM); secondly, the negative input of the OTA_{err} is increased (decreased), which decreases (increases) the OTA_{err} output voltage, and also leads to decrease (increase) the body-to-source voltage V_{BS} . Both generated effects lead to decrease (increase) the threshold voltage.

B- Simulation results :

Figures 5.49 and 5.50 show the frequency of the designed OTA, for both input common mode limits $V_{CM_{min}} = 0.8 \text{ V}$ and $V_{CM_{max}} = 2.3 \text{ V}$. Similar to the DBB, the BRB technique resolves the gains degradation issue shown in the single stage OTA.

Table 5.13 summarizes the OTA performances. Thus, a high gain is preserved at extreme conditions, and the current consumption is only 13 μA , including 5 μA dissipated in the hardened current source. The stability simulations have been performed by opening the internal loop at the positive input of the OTA_{err} .

Table 5.13: OTA performances using the BRB.

Parameter	Description	Value
A_{V0}	Min DC gain @ $V_{CM} = 0.8/2.3 \text{ V}$	36/44 dB
I_{Diss}	Max current consumption @ 200 $^{\circ}\text{C}$	13 μA
f_T	Min cutoff frequency	2.5 MHz
C_L	Load capacitance	1 pF
φ_M	Min phase margin of internal loop	84 $^{\circ}$

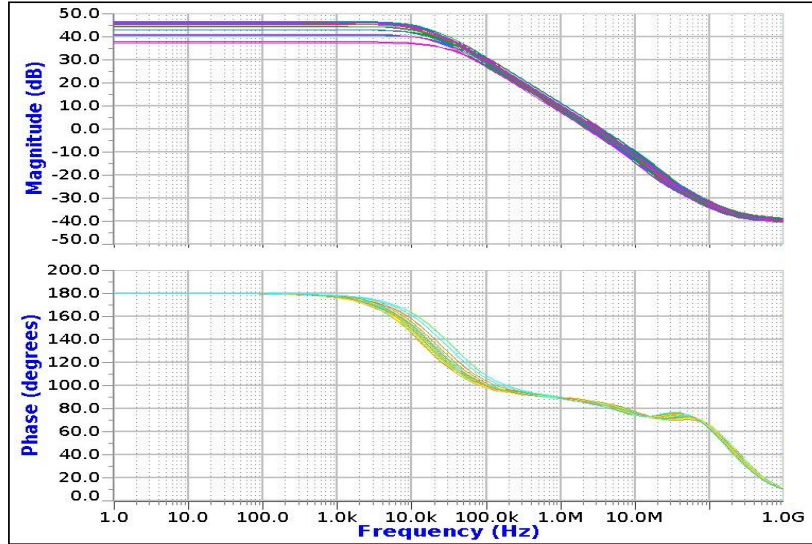


Figure 5.49: OTA simulated results using the BRB for different process corners, TID and temperature effects at $V_{CM}=0.8$ V.

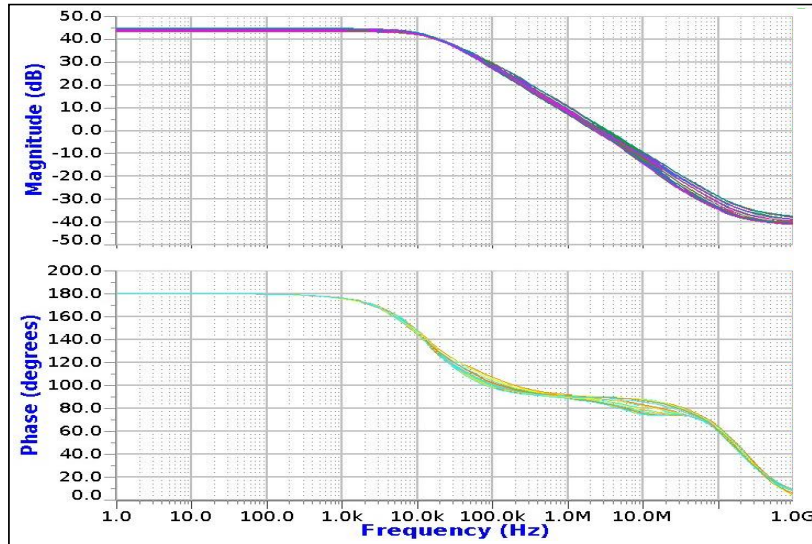


Figure 5.50: OTA simulated results using the BRB for different process corners, TID and temperature effects at $V_{CM}=2.3$ V.

5.4.5.3 Hardened folded cascode amplifier

A- Design principle :

A hardened folded cascode amplifier can be designed using the body replica biasing. As shown in Fig.5.51, the BRB can be used in the differential pair transistors as used in the previous single OTA. For the second PMOS stage

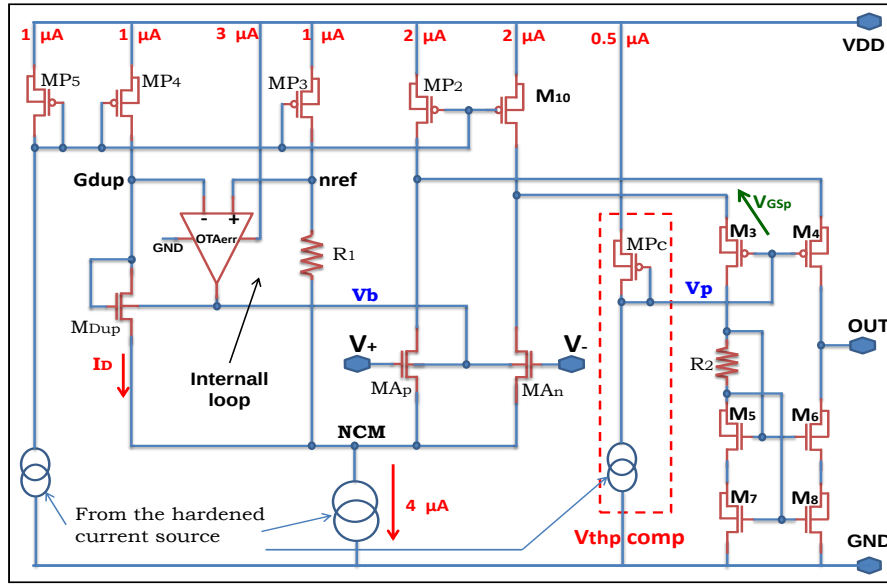


Figure 5.51: Hardened folded Cascode using BRB technique.

(M_4 and M_3) mounted in common gate stage, it can be biased by the branch "Vthp comp" used in the OTA with the DBB. This, ensures a fixed voltage $V_{ov} = V_{GS} - |V_{thp}|$ for the PMOS transistor M_4 and M_3 versus TID, and leads to keep a fixed transconductance g_{m4} in this PMOS second stage. Thus, as detailed in the expression below [67], keeping a fixed transconductance g_{m1} and g_{m4} versus different effects, leads to keep a higher DC gain in this folded cascode amplifier.

$$A_V = g_{m1} \cdot [(g_{m4} \cdot r_{o4} \cdot (r_{oAp} / r_{o10}))] / [g_{m6} \cdot r_{o6} \cdot r_{o8}] \quad (5.9)$$

Where g_{m1} , g_{m4} and g_{m6} are the transconductances of the differential pair transistor, the second PMOS stage and the NMOS transistor M_6 in Fig.5.51 respectively. r_{oAp} , r_{o4} , r_{o6} , r_{o8} and r_{o10} are the output resistances of the differential pair transistor, the second PMOS stage, NMOS transistor M_6 , M_8 and PMOS transistor M_{10} respectively.

B- Simulation results :

Figure 5.52 shows the AC simulations versus TID for all process corners and temperatures from -40°C up to 200°C for a common mode of 1.25 V.

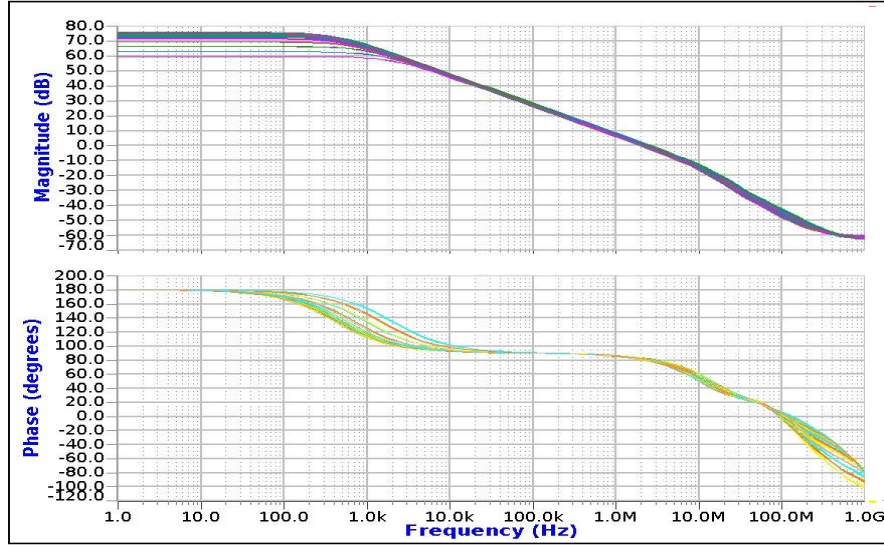


Figure 5.52: Folded cascoded simulated results using the BRB for different process corners, TID and temperature effects at $V_{CM}=1.25$ V.

Table 5.14 gives the folded cascode amplifier performances. The current consumption is about $15\text{ }\mu\text{A}$, including $5\text{ }\mu\text{A}$ in the current source.

Table 5.14: Folded cascode performances using the BRB.

Parameter	Description	Value
A_{V0}	Min DC gain @ $V_{CM} = 0.4$ V	57 dB
A_{V0}	Min DC gain @ $V_{CM} = 2.2$ V	50 dB
I_{Diss}	Max current consumption @ 200°C	$15\text{ }\mu\text{A}$
f_T	Min cutoff frequency	2.5 MHz
C_L	Load capacitance	1 pF
φ_M	Min phase margin of internal loop	81°

Figures 5.53 and 5.54 show the extracted DC gain at -40°C and 200°C respectively, versus the input common mode at hard TID effects (a negative shift of 200 mV in the threshold voltages with a mobilities degradation of 20%).

For an input common mode range of 0.4 V up to 2.2 V, the DC gain remains higher than 50 dB. The internal loop stability simulations have been performed by opening the loop at the positive input of the OTA_{err} and give a high phase margin of 81° .

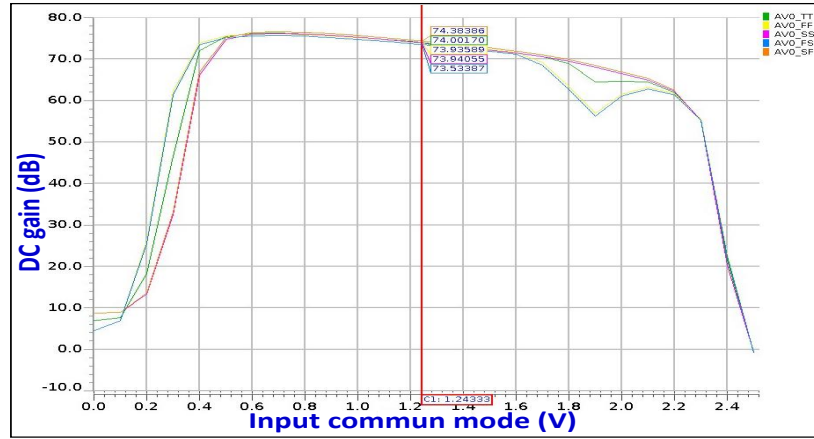


Figure 5.53: Folded cascode simulated DC gain for different process and hard TID effects versus the input common mode, at $T=-40^\circ C$.

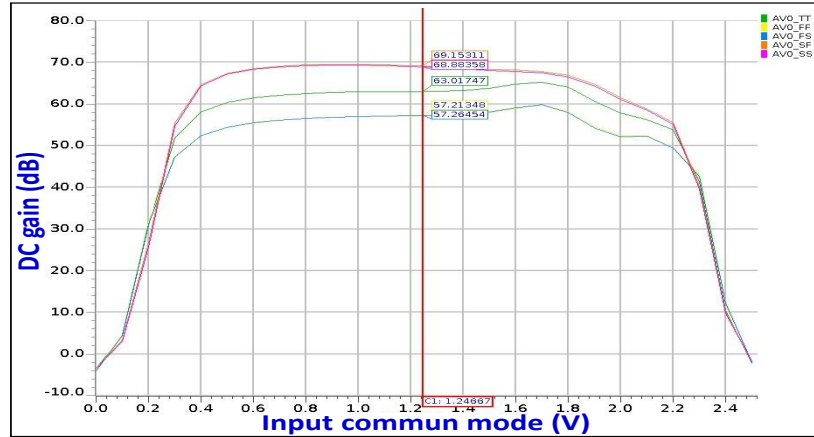


Figure 5.54: Folded cascode simulated DC gain for different process and hard TID effects versus the input common mode, at $T=200^\circ C$.

5.5 Conclusion

The first part of this chapter presents the state of the art of SEE and TID mitigation techniques for analog circuits. SEE mitigation has been implemented at different levels: technology, device, layout/design circuit and system. For TID mitigation techniques, it has been discussed in literature at only technology and layout levels.

Afterwards, TID mitigation techniques at design level for analog circuits have been proposed in the 130 nm PD SOI technology. Firstly, two hardened current sources have been presented. The first current source has a simple structure, and can be implemented in the case where the impact of the oxide charges N_{ox} is more important than the interface charges N_{it} . The second current source is a more complete structure, using an error amplifier regulating the gate-to-source voltage V_{GS} of a NMOS transistor in a way to generate a fixed current I_{REF} . When the used power supply is unchangeable ($VDD = 2.5$ V), the reference current I_{REF} has a very low variation of about 0.6% under extreme conditions of 1) a large range of temperature $[-40^{\circ}\text{C}, +200^{\circ}\text{C}]$, 2) hard TID effects with a negative shift of threshold voltages $V_{th_{n,p}}$ up to 200 mV and carriers mobilities degradations up to 20%, 3) for all process corners variations.

Secondly, a new mitigation technique against TID for analog design circuits is proposed. It is based on the body biasing technique, which compensates the process corners variations, TID and temperature effects in critical and sensitive transistors in the analog circuits (e.g. the differential pair transistors of an OTA).

This body biasing technique can be implemented in two different ways: firstly, by using the direct body biasing technique (DBB), secondly by using the body replica biasing technique (BRB).

These two techniques have been implemented for a standard single stage OTA amplifier and for a folded cascode amplifier, both designed in the 130 nm PD SOI technology. The use of these techniques allows to keep a fairly unchanged amplifier gain, cutoff frequency, and phase margin versus: 1) the hard TID effects 2) a large temperature range of -40 up to $+200^{\circ}\text{C}$, 3) all process corners (Typ, FFA, SSA, FSA, SFA, SSA), for a large range of the input common mode.

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CHAPTER 6

Conclusions

THE main objective of this thesis was first to study the effects of harsh environments on electronic circuits, mainly radiation and high temperature. The second objective was to propose mitigation techniques at design level against these effects. This has been achieved in four parts as follows.

First part (chapter 2) :

In the first part of this thesis, an overview of harsh environments and their effects on electronics has been performed. From this overview we can conclude that:

1) For integrated circuits, several harmful radiation sources exist. Some of them are linked to the atmospheres (sun and stars), and other sources are linked to the human utilization such as in medical, military and nuclear centers.

2) Radiation sources generate two types of particles; firstly, charged particles such as protons or heavy ions, which interact directly with the electronic devices by creating a number of electron-hole pairs in the silicon and insulators. Secondly, uncharged particles such as photons and neutrons, which affect electronic components through secondary effects, and can induce electron-hole pairs or displacement damage in the lattice silicon atom.

3) The radiation impacts on the integrated circuits can be classified into two groups: first, the effects due to a single particle (SEE), which mainly concern digital circuits. The second are the cumulative effects caused either by a long time exposition to radiation, or by a very high ionizing energy. These last effects concern more analog circuits as they introduce permanent shifts in the electrical characteristics of transistors.

4) High temperature environments also disturb electronic devices through various parameters, such as the mobility of carriers, the leakage current of the devices and the threshold voltage V_{th} of the MOS transistors.

5) The SOI technology has demonstrated since several years a lower sensitivity to temperature as well as to the SEE effects compared to Bulk, and also a low sensitivity to TID when a thin (gate and buried) oxide is used in PD. Therefore, SOI appears as the most promising technology for the objective of

this thesis.

Second part (chapter 3) :

The second part studies the single event effects (SEE) combined with temperature in digital circuits. 2D-TCAD simulations and modeling of SEE (using a compact model) have first been detailed. A good matching has been shown between results from this compact model and Sentaurus 2D-TCAD at different temperatures.

Secondly, the combined effect of temperature and SEE is discussed for two different PD SOI technologies featuring minimum channel lengths of 1 μm and 130 nm. For a single MOSFET transistor, SEE simulations have shown a decrease in the pulse amplitude of the induced current I_{SEE} , and an increase in its time delay.

The 6T-SRAM cell has shown to be more sensitive to radiation when the temperature is increased, due to : 1) the increase in the collected charge, 2) the reduction of the threshold voltages with temperature, 3) the parasitic bipolar transistor created by radiation in such PD SOI technologies, which increases the induced current in the transistors.

Thirdly, different types of SEE measurements and experimental results for a standard 4-Nand flip-flop were exposed.

By the end, a good matching has been demonstrated between measured and simulated LET_{th} for an UCL SRAM used in the UCL 80C51 micro-controller.

A major conclusion of this second part is that digital circuits become more sensitive to single event effects (SEE) when the temperature increases.

Third part :

Chapter 4 presents the combined effect of a total ionizing dose and a high temperature in analog integrated circuits. The simulations of cumulative effects were first presented. Secondly, measurement results before and after TID effects of an ultra-low-power 1 μm PD SOI circuits were presented and discussed. Thirdly, the combined effect of TID and temperature has been measured on single PD SOI MOSFET transistors and for a voltage reference circuit. The carriers mobilities μ , the subthreshold parameter n and the threshold voltages $V_{th_{n,p}}$, for transistors have been extracted. Under this combined effects, the subthreshold parameter n is increased and the mobilities μ are degraded. A significant increase is shown in the absolute value of the PMOS threshold voltage with radiation at high temperature, while for NMOS, the threshold voltage value V_{th_n} decreases slightly at room temperature, keeps a relatively stable

value versus radiation dose at 100 °C, and increases at a higher temperature of 200 °C, depending on the balance between N_{ox} and N_{it} buildup.

At the end of the chapter 4, an ultra-low power voltage reference designed in a suitable technology of 130 nm PD SOI was presented. This circuit has been simulated up to 200 °C using our extended MOS models, was proved to be robust against radiation effects (using custom model parameters). Simulated voltage reference has shown a very fairly stable value over a large range of process corners and temperature variations.

Measurements have shown a fairly correct operation of such an ultra-low power circuit for a large temperature range (from -40 °C up to +200 °C) and under the combination of a total ionizing dose (up to 1 Mrad (Si)) and a high temperature. The extracted parameters of transistors ($V_{th_{n,p}}$, n and μ) under radiation and temperature, fairly support the observed V_{REF} and power consumption dependencies on temperature and total dose radiation.

A major conclusion of this third part is that for the PD SOI technology under combined effects of TID and high temperature, the mobilities of transistors are degraded, the subthreshold parameter n is increased, the PMOS absolute threshold voltage is significantly increased and the NMOS threshold voltage is decreased at low temperature and increased at high temperature depending on the balance between N_{ox} and N_{it} buildup. These effects on the transistors mainly influence the analog performances of circuits.

Fourth part (chapter 5) :

The last chapter of this thesis, first presents the state of the art of SEE and TID mitigation techniques for analog circuits. Secondly, some TID mitigation techniques at design/layout levels for analog circuit have been proposed. Thus, an edgeless layout can be used to mitigate PD SOI transistors against TID effects. At design level two hard current sources designed in 130 nm PD SOI have been presented. Afterwards a new mitigation technique based on the body biasing technique is proposed. This technique compensates the TID effects in critical and sensitive transistors in analog circuits, such as the differential pair transistors of an OTA.

By the end, two different ways to use body biasing techniques (direct body biasing and body replica biasing) have been implemented for a standard single stage OTA amplifier and for a folded cascode amplifier, both designed in the 130 nm PD SOI technology. With these body biasing techniques the amplifiers keep a fairly unchanged gain, cutoff frequency and phase margin versus process corners variations, TID and temperature effects.

A main conclusion of this last part, is that edgeless transistors can be used to reduce TID effects on transistors. The body biasing can be used as a mitigation

technique against TID, temperature and process corners variation for analog circuits.

The whole thesis leads to conclude that the process corners variation, the temperature and the radiations, have a similar influence on the analog circuits. Thus, all of these effects have to take into account during the design phases.

The body biasing techniques represent an important degree of freedom in the design level, that can be used to readjust or to tune the characteristics of MOSFETs. This, allows to face the circuits issues induced by harsh environment and process corners effects

Overall Perspectives :

The body biasing techniques (DBB and RBB) have been implemented for the design of OTAs, as a mitigation technique against the process corners variation, the high temperature and radiation effects. In the PD SOI technology, the simulations show good results for the different OTA structures, against these effects. The next measurements of a designed OTA using the direct body biasing technique and a Hard current source, will confirm the robustness of the body biasing technique, against the harsh environments effects as well as the process corners variation.

The body biasing techniques can also be used in the design of the voltage reference detailed in chapter 4. In fact by keeping a fixed threshold voltages in the NMOS transistors (M_1 , M_2 and M_n) and the PMOS transistor M_p (Fig.4.38), the current $I_{REF}=[V_{GS2}-V_{GS1}/R_B]$ and the voltage reference $V_{REF}=[(1 + R_1/R_2).V_{GS_n} - V_{GS_p}]$ will remain fixe versus process corners, temperature and radiation effects. With this design compensation technique, the current consumption of the circuit can be reduced below 1 μA .

By the end, the body biasing techniques can used with different technologies having a body or back-gate access such as Bulk, SiC and mainly with the newest technologies such as UTBB FD planar SOI.

APPENDIX A

Technologies comparison

A.1 Comparison of characteristics for different technologies

Table A.1 shows a comparison between different characteristics, for four technologies; SOI, SiC, GaN and Vacuum devices.

Table A.1: Comparison of different characteristics for SOI, SiC, GaN and Vacuum devices [1].

Material	SOI	SiC	GaN	Vaccum Thermionics
Transistor normal normal state	off	on	on	on
Max Operating Voltage	3 V - 5 V	> 200 V	> 15 V	> 200 V
Demonstrated Max Temperature (°C)	300	500	300	500
Power Consumption	Low	High	Medium	High
Commercial integration	MSI	SSI	SSI	Discrete

SSI denotes small-state integration; MSI medium-state integration; discrete elements are not yet integrated.

A.2 Combination of extreme conditions

Following Table A.2 shows some examples of harsh environments. It has to be noted that, Europa is a moon of the planet Jupiter.

Table A.2: Extreme environments in the Solar System [1].

Target	Radiation (krad/day)	Pressure (bar)	Low Temperatures (°C)	High Temperatures (°C)	Chemical Corrosion	Physical Corrosion
High temperature and high radiation						
Venus	20	92		+482	Sulfuric acid clouds	
Jupiter	150	22		+230		
Low temperature and high radiation						
Europa orbit	40					
Europa surface	20		-180			
Europa sub-surface	0.3 at 10 cm		0 at 5 km			
Thermal cycling						
Moon			-230	+197		Dust
Mars		0.007	-143	+27		Dust

A.3 Silicon Carbide technology

A.3.1 Technology features [28]

Due to the higher; Band-gap, Thermal Conductivity and Breakdown field, the Silicon Carbide (SiC) is a powerful technology for use in extreme conditions, such as high-temperature, high-radiation and high-power. The atomic crystal of the SiC is composed of 50% carbon and atoms covalently bonded with 50% atoms. For electronic applications three atomic structures have been developed; 3C-SiC, 4H-SiC (Fig.A.1) and 6H-SiC. Most important semiconductor electrical properties of SiC have been compared in the Fig. A.2 to Silicon, GaAs and 2H-GaN technologies.

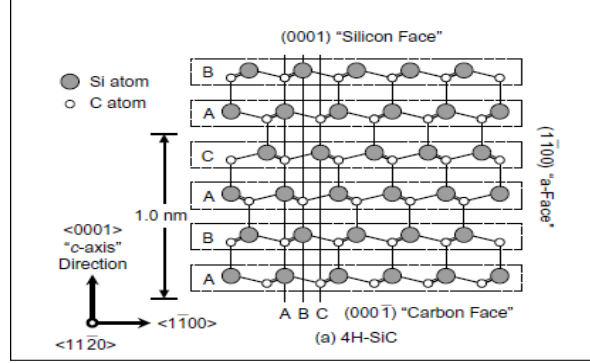


Figure A.1: Atomic crystal of 4H-SiC technology [28].

A.3.2 Electronic circuits using SiC technology [29]

The SiC technology has a small leakage current compared to SOI and bulk, thanks to the improved gate oxide process in SiC technology. For automotive applications, bulk technology reaches max 125°C with a big volume cooling system, while SiC technology reaches 250°C without any cooling system. Table A.3 gives an idea of the important parameters for a transistor in 4H-SiC technology, with p-type epi doped at $4 \cdot 10^{15} \text{cm}^{-3}$ at 25°C and 300°C .

Table A.3: Important parameters for a transistor in 4H-SiC [29].

Parameter	25°C	300°C
V_{th} (V)	-9V	-8.5
I_{dSAT} (mA)	30	10
G_m (mS)	4.6	1.7
R_{sheet} of resistor	11.5 k Ω /sq	41.8 k Ω /sq

For circuits, a common source amplifier developed with SiC technology [29] has shown a perfect behavior at 300°C with a loss of only 3 dB on the gain compared to room temperature (Tab.A.4).

Table A.4: Important parameters for a transistor in 4H-SiC [29].

Parameter	25°C	300°C
Common source open loop gain (dB)	60	57

Property	Silicon	GaAs	4H-SiC	6H-SiC	3C-SiC	2H-GaN
Bandgap (eV)	1.1	1.42	3.2	3.0	2.3	3.4
Relative dielectric constant	11.9	13.1	9.7	9.7	9.7	9.5
Breakdown field	0.6	0.6	//c-axis: 3.0 ⊥c-axis: 2.5	//c-axis: 3.2 ⊥c-axis: > 1	1.8	2-3
$N_D = 10^{17} \text{ cm}^{-3}$ (MVcm ⁻¹)			3-5	3-5	3-5	1.3
Thermal Conductivity (W/cm-K)	1.5	0.5				
Intrinsic carrier concentration (cm ⁻³)	10^{10}	1.8×10^6	$\sim 10^{-7}$	$\sim 10^{-5}$	~ 10	$\sim 10^{-10}$
Electron mobility at $N_D = 10^{16} \text{ cm}^{-3}$ (cm ² V ⁻¹ s ⁻¹)	1200	6500	//c-axis: 800 ⊥c-axis: 800	//c-axis: 60 ⊥c-axis: 400	750	900
Hole mobility at $N_A = 10^{16} \text{ cm}^{-3}$ (cm ² V ⁻¹ s ⁻¹)	420	320	115	90	40	200
Saturated electron velocity (10 ⁷ cms ⁻¹)	1.0	1.2	2	2	2.5	2.5
Donor dopants and shallowest ionization energy (meV)	P: 45 As: 54	Si: 5.8	N: 45 P: 80	N: 85 P: 80	N: 50	Si: 20
Acceptor dopants and shallowest ionization energy (meV)	B: 45	Be, Mg, C: 28	Al: 200 B: 300	Al: 200 B: 300	Al: 270	Mg: 140
2005 Commercial wafer diameter (cm)	30	15	7.6	7.6	15	None

Figure A.2: Comparison of important semiconductor electronic of SiC and other technologies [28].

APPENDIX B

Single event effects SEE

B.1 Mechanism for Single Event Effects

Figure B.1 shows the mechanism for single event effects, whilst Fig.B.2 shows the charge collection in the semiconductor device. This collection charge occurs in pn-junction, and is generated by drift and funneling effects for high field regions and by a diffusion mechanism for low field regions.

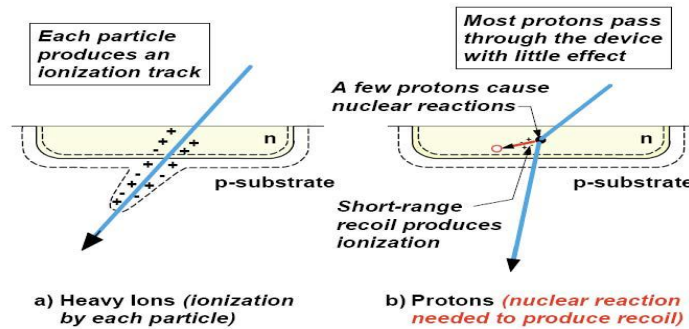


Figure B.1: Mechanism for Single Event Effects [30].

B.2 Single Event Upsets SEU

When SEU current I_{SEU} exceeds the restoring current from a cross-coupled inverter such that the node voltage drops below $V_{DD}/2$ for too long, an upset occurs Fig.B.3.

B.3 Single Event Transients SET

Single event transients (SET) always generate a transient pulse on an electric signal. For instance, Fig.B.4 shows an output signal of a comparator. it has to

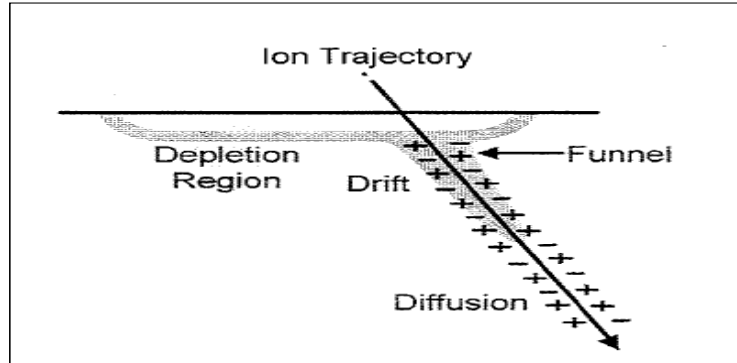


Figure B.2: Charge collection in a pn-junction [30].

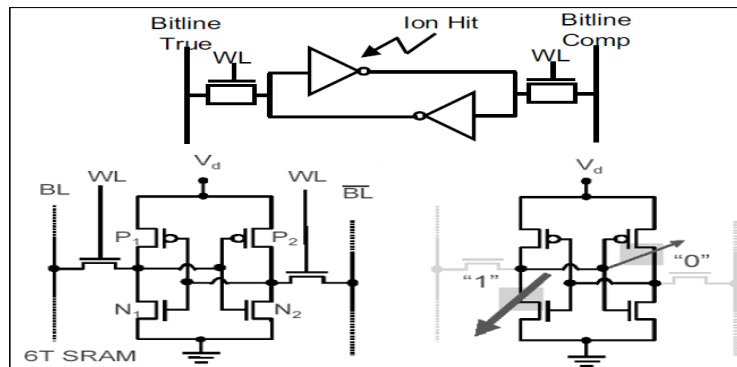


Figure B.3: 6T SRAM during a SEU [30].

be noted that, the SET effects depend strongly on the bias conditions.

B.4 Single Event Latch-up SEL

The single event Latch-up occurs when a parasitic thyristor (Fig.B.5) is created by a particle (heavy ions, protons or neutrons). SEL is temperature dependent and can cause a circuit lockup and/or a catastrophic device failure. SOI or insulated oxides technologies are totally immune against SEL.

B.5 Single Event Burnout SEB

The single event burnout is caused by a localized current in the body of the transistor induced by a particle (heavy ion, proton or neutron), which turns on

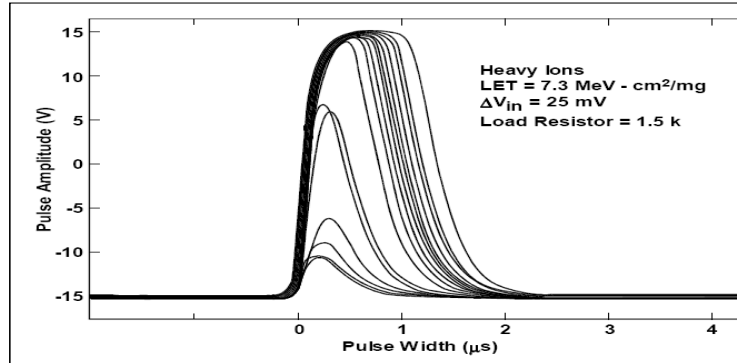


Figure B.4: Transients pluses caused by SET on a comparator [30].

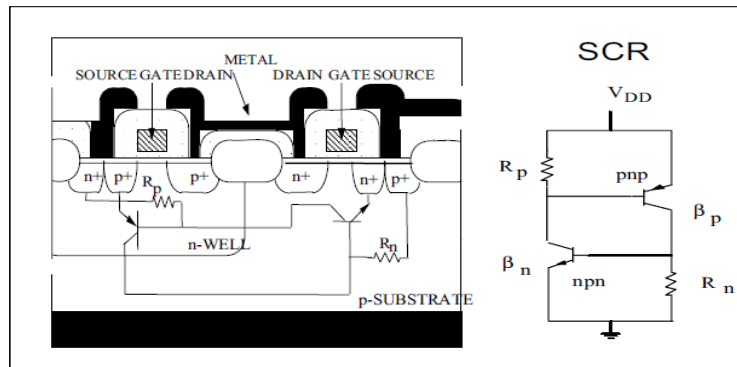


Figure B.5: latch-up structure [30].

a parasitic bipolar transistor, and creates a direct current path between drain and source (Fig.B.6). This effect is always destructive, and concerns mainly power transistors such as CMOS, BJT, FET and MOSFETs.

B.6 Single Event Gate Rupture SEGR

The single event gate rupture (Fig.B.7) is a destructive effect caused by heavy ions, it depends on the electric field in gate oxide and on the angle of incidence of particle. It mostly concerns power MOSFETs.

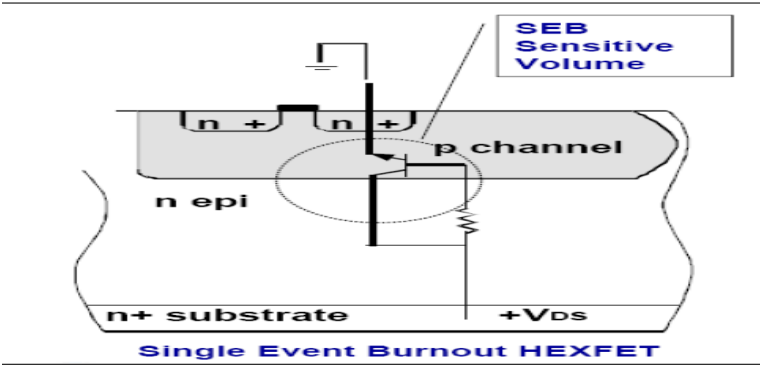


Figure B.6: Single Event Burnout [30].

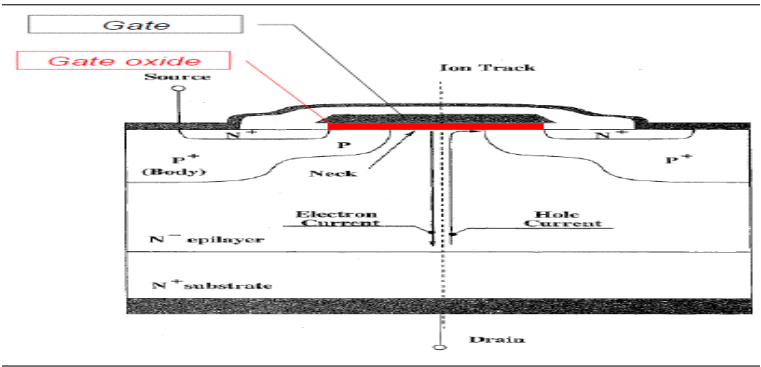


Figure B.7: Single Event Gate Rupture [30].

B.7 Summary of Single Event Effects

Table B.7 below gives a summary of different types of Single Event Effects and their impacts on electronic devices. While table B.7 provides relevant single event effects versus technology and circuit family [15].

Table B.1: Summary of Single Event Effects [30].

Single Event Effects	Impacts	Concerned circuits
Single Event Upset (SEU)	corruption of the information stored in a memory element	Memories, latches in logic devices
Multiple Bit Upset (MBU)	several memory elements corrupted by a single strike	Memories, latches in logic devices
Single Event Functional Interrupt (SEFI)	corruption of a data path leading to loss of normal operation	Complex devices with built-in state machine/control sections
Single Hard Error (SHE)	unalterable change of state in a memory element	Memories, latches in logic devices
Single Event Transient (SET)	Impulse response of certain amplitude and duration	Analog and Mixed Signal circuits, Photonics
Single Event Disturb (SED)	Momentary corruption of the information stored in a bit	combinational logic, latches in logic devices
Single Event Latchup (SEL)	high-current conditions	CMOS, BiCMOS devices
Single Event Snapback (SESB)	high-current conditions	N-channel MOSFET, SOI devices
Single Event Burnout (SEB)	Destructive burnout due to high-current conditions	BJT, N-channel Power MOSFET
Single Event Gate Rupture (SEGR)	Rupture of gate dielectric due to high electrical field conditions	Power MOSFETs, Non-volatile NMOS, VLSIs, linear devices

Table B.2: Relevant single event effects versus technology and circuit family [15].

Technology	Family	Function	SEL	SEGR	SEB	SEU	MCY/MBU	SEFI	SET
Power MOS				X	X				
CMOS, BiCMOS and SOI	Digital	SRAM	X*			X	X		
		DRAM	X*			X	X	X	
		FPGA	X*			X	X	X	X
		Flash EEPROM	X*			X		X	
		μ P μ controller	X*		X	X	X	X	
	Mixed signal	ADC	X*			X		X	X
		DAC	X*			X		X	X
	Linear		X*						X
Bipolar	Digital					X			X
	Linear					X			X

*except SOI

APPENDIX C

Sentaurus ISE-TCAD simulator

C.0.1 ISE-TCAD netlist

The ISE-TCAD simulator simulates netlist edited in language called TCL with a special syntax. The following sentences show a mixed mode netlist for a 6T-SRAM cell (Fig.C.1) :

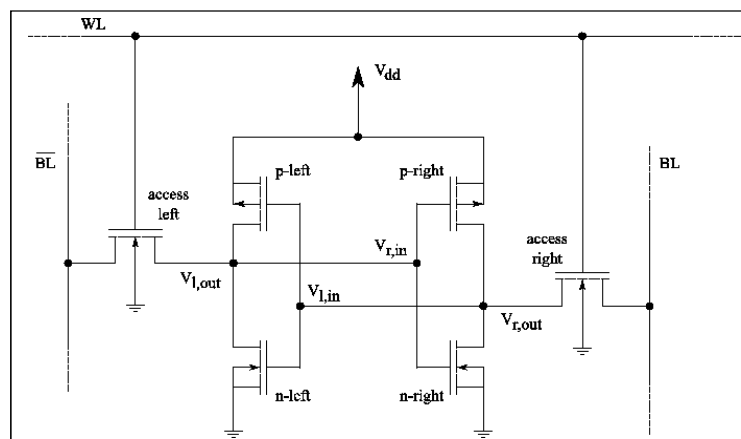


Figure C.1: 6T-SRAM cell.

Device NMOS

Electrode:

```
Name="source" Voltage=0.0
Name="drain" Voltage=0.0
Name="gate" Voltage=0.0 Barrier=-0.55
Name="substrate" Voltage=0.0
Name="bodytie" Voltage=0.0
```

Thermode:

Name="substrate" Temperature=300

File:

Grid = "soinmos - msh.tdr"

Doping = "soinmos - msh.dat"

Param = "models.par"

Physics:

Temperature=300

AreaFactor=6

eQCvanDort

EffectiveIntrinsicDensity(OldSlotboom)

Mobility(

DopingDep

eHighFieldsaturation(GradQuasiFermi)

hHighFieldsaturation(GradQuasiFermi)

Enormal

)

Recombination(

SRH(DopingDep)

)

HeavyIon(

Direction=(0,1) * is verticale in this case, (1,0) horizontale

Location=(0,0) * location of radiation is on the gate

Time=0.5e-8 * time of max radiation

Length=1.25 * deep of radiation

Wt_{hi}=0.1 * diameter of radiation

LET_f=0.342 * energie of radiation in vertical (= 0.64 in Cyclotron or =1 at tilt angle)(McV/mg/cm² = 0.64pC/um)

Gaussian * forme of ID

PicoCoulomb) * unit

Physics(RegionInterface="R.Box/R.Siliconepi") Charge(Conc=5e11)

Physics(RegionInterface="R.Gateox/R.Siliconepi") Charge(Conc=5.225e11)

System:

*BLW

Vsource - pset vblw (blw 0) dc=4.0

*BLWA

Vsource - pset vblwa (blwa 0) dc=0.0

```

*Vdd
Vsource - pset vvdv (vdd 0) dc=4.0
*CWR
Vsource - pset vcwr (cwr 0) dc=0.0
*INV1
NMOS nmos ("drain"=out1 "gate"=out2 "source"=0 "substrate"=0 "bodytie"=0)
mosbp - pset MP1 ( out1 out2 vdd vdd ) l=1e-06 w=12e-06 pd=17e-06 ps=23e-
06 ad=30e-12 as=20e-12
*mosbn - pset MN1 ( out1 out2 0 0 ) l=1e-06 w=6e-06 pd=11e-06 ps=14e-06
ad=15e-12 as=10e-12
* INV2
*NMOS nmos ("drain"=out2 "gate"=out1 "source"=0 "substrate"=0 "bodytie"=0)
mosbp - pset MP2 ( out2 out1 vdd vdd ) l=1e-06 w=12e-06 pd=17e-06 ps=23e-
06 ad=30e-12 as=20e-12
mosbn - pset MN2 ( out2 out1 0 0 ) l=1e-06 w=6e-06 pd=11e-06 ps=14e-06
ad=15e-12 as=10e-12
*SW1
*NMOS nmos ("drain"=blw "gate"=cwr "source"=out2 "substrate"=0 "bodytie"=0)
mosbn - pset MNSW1 ( blw cwr out2 0 ) l=1e-06 w=6e-06 pd=11e-06 ps=14e-
06 ad=15e-12 as=10e-12
*SW2
*NMOS nmos ("drain"=blwa "gate"=cwr "source"=out1 "substrate"=0 "bodytie"=out1)
mosbn - pset MNSW2 ( blwa cwr out1 0 ) l=1e-06 w=6e-06 pd=11e-06 ps=14e-
06 ad=15e-12 as=10e-12
Capacitor-pset C1 (vdd out1) capacitance = 542E-18
Capacitor-pset C2 (vdd out2) capacitance = 542E-18
Capacitor-pset C3 (out1 out2) capacitance = 3.44E-15
Capacitor-pset C4 (out1 0) capacitance = 54E-18
Capacitor-pset C5 (out2 0) capacitance = 54E-18

*Set (out1 = 4.0)
Set (out2 = 0.0)

Plot "node-6tsram-INV1-NMOS.plt" (time() out1 out2 cwr blw blwa vdd
i(nmos 0) i(MP1 vdd))

File:
Plot ="let-st.dat"
Current= "let-st.plt"
SPICEPath = "."

```

Plot:

eDensity hDensity
TotalCurrent
eCurrent hCurrent
eMobility hMobility
eVelocity hVelocity
eQuasiFermi hQuasiFermi
eTemperature Temperature * hTemperature
ElectricField Potential SpaceCharge
Doping DonorConcentration AcceptorConcentration
SRH Band2Band * Auger
AvalancheGeneration eAvalancheGeneration hAvalancheGeneration
eGradQuasiFermi/Vector hGradQuasiFermi/Vector
eEparallel hEparallel eENormal hENormal
BandGap
BandGapNarrowing
Affinity
ConductionBand ValenceBand
eQuantumPotential
HeavyIonChargeDensity

Math:

Extrapolate
NoAutomaticCircuitContact
WallClock
Extrapolate
Derivatives
Newdiscretization
RecBoxIntegr
Method=ILS
Spice-gmin=1e-15
Iterations=20
Notdamped =100
*RelErrControl
*Digits=4
*NoCheckTransientError
Spice-temperature=300

Solve:

initial conditions
*NewCurrentPrefix = "ignore"

```
Coupled(Iterations=100) Poisson
Coupled(Iterations=100) Poisson Circuit
Coupled(Iterations=100) Poisson Contact Circuit
Coupled(Iterations=100) Poisson Hole Contact Circuit
Coupled(Iterations=100) Poisson Hole Electron Contact Circuit
```

```
*****Only for full spice simulation
*Coupled(Iterations=100) Circuit
*Coupled(Iterations=100) Contact Circuit
*****
```

```
NewCurrentFile = "Results-RAD-INV1-NMOS"
* Unset (out1)
Unset (out2)
```

```
Transient (
InitialTime=0 FinalTime=4.5e-9
InitialStep=1e-12 MaxStep=1e-12 MinStep=1e-20
Increment=1.3
)
Coupled nmos.poisson nmos.electron nmos.hole nmos.contact circuit Plot(FilePrefix="seu1-
300K" Time=(1e-9;4.5e-9) NoOverwrite)
```

```
Transient (
InitialTime=4.5e-9 FinalTime=8e-9
InitialStep=1e-12 MaxStep=1e-12 MinStep=1e-20
Increment=1.3
)
Coupled nmos.poisson nmos.electron nmos.hole nmos.contact circuit Plot(FilePrefix="seu2-
300K" Time=(4.5e-9;5e-9;5.02e-9;5.04e-9;5.06e-9;5.1e-9;5.5e-9) NoOverwrite)
```

```
Transient (
InitialTime=8e-9 FinalTime=10e-9
InitialStep=1e-12 MaxStep=1e-9 MinStep=1e-20
Increment=1.3
)
Coupled nmos.poisson nmos.electron nmos.hole nmos.contact circuit Plot(FilePrefix="seu3-
300K" Time=(8e-9;10e-9) NoOverwrite)
```