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An electrical evaluation method for the silicidation of silicon nanowires

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Physical and electrical properties of PtSi nanowires (NWs) fabricated on a silicon-on-insulator wafer are investigated. The Si consumption rule in NW silicidation is consistent with that of planar process. The cross-sectional area ratio between PtSi NW and Si NW is about 1.5:1. An electrical method is used to evaluate the silicidation degree of NWs. According to the dependence of the current passing through the NW on the backside substrate voltage, we can determine whether the Si NW is fully or partially silicided. The electrical evaluation results are in agreement with transmission electron microscopy inspections. © *2009 American Institute of Physics*.
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Recently, silicide nanowires (NWs) have attracted much attention due to their excellent electrical properties. When the current polysilicon gates for complementary metal-oxide-semiconductor are fully silicided, polydepletion effects are subtracted.[1] Based on their low resistivity and high break-down current density, fully silicided (FUSI) NWs are used as reliable electrical interconnections for nanoelectromechanical systems[2] and nanodevices.[3] Particularly, in NW transistors, when the Si NWs linking the channel region to the source/drain terminals are replaced by FUSI NWs, the transistor performance and reliability are significantly improved.[4] Additionally, partially silicided (PASI) NWs have also been used in highly sensitive biosensors[5] and flexible optoelectronic devices.[6] Pt silicide (PtSi) has a good surface chemical stability and a low Schottky barrier on *p*-type Si.[7] These properties make PtSi a promising candidate for Ohmic contacts to *p*-type Si devices.[8] Most of the investigations of PtSi focus on the planar structures,[9] but only a few articles report on the silicidation of NWs. Although physical and electrical characteristics of PtSi NWs have been studied by high resolution transmission electron microscopy (HRTEM) (Ref. 10) and through PtSi/Si/PtSi NW transistors,[11] respectively, the PtSi NWs in these two works were obtained by bottom-up method. Alternately, Zhang *et al.*[12] measured the resistivity of PtSi NWs fabricated by sidewall transfer lithography. However, to examine whether the Si NWs have been completely converted into PtSi NWs, TEM is required. The TEM provides high resolution pictures of the material microstructure, but it is a destructive, complicated, and time-consuming characterization technique. In this work, we investigate the physical and electrical properties of PtSi NWs fabricated on a silicon-on-insulator (SOI) wafer by top-down approach. We calculate the Si consumption during the NW silicidation and the cross-sectional area ratio between PtSi NW and Si NW. More importantly, we rely on an electrical method to evaluate the silicidation degree of NWs. The main idea is to apply a voltage to the backside substrate of the SOI wafer. When a Si NW is fully silicided, the current passing though it cannot be modulated by the applied voltage. When the Si NW is partially silicided, the current depends on the applied voltage.

In order to validate the electrical method, we design 3-mm-long and 68-nm-high Si NWs with different widths of 50, 75, and 100 nm for the cross-sectional inspections by scanning electron microscopy (SEM) and TEM. The NWs are patterned on an SOI wafer by electron beam lithography and reactive ion etching. Figure 1(a) shows the top-view SEM picture of as-etched Si NWs with a width of 75 nm,

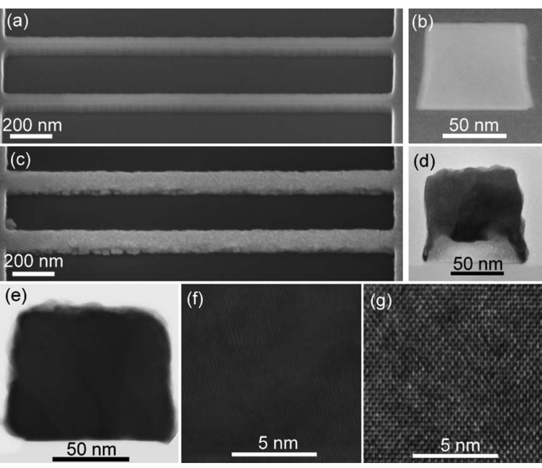

FIG. 1. (a) Top-view SEM picture of Si NWs. (b) Cross-sectional TEM picture for one of the Si NWs in (a). (c) Top-view SEM picture of PtSi NWs. (d) Cross-sectional TEM picture for one of the PASI NWs in (c). (e) Cross-sectional TEM picture of a FUSI NW. [(f) and (g)] HRTEM pictures showing FUSI NW and Si NW morphologies, respectively.

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TABLE I. Summary of Si consumption rules and dimension changes for the film and NW Pt-silicidations processed by RTA at 400 °C for 2 min.

Process	Dimension definition (D)	D_{Si}/D_{Pt}	D_{PtSi}/D_{Pt}	D_{PtSi}/D_{Si}	Dimension change
PtSi film	Thickness (nm)	1.32	1.97	1.49	0.15
PASI NW	Height (nm)	1.31	1.94	1.48	0.16
FUSI NW	Cross-section area (nm^2)	1.27	1.93	1.52	0.15

exhibiting that the Si NWs are very uniform in width. Figure 1(b) gives the cross-sectional TEM picture for one of the as-etched Si NWs, indicating that its vertical sidewalls are very steep. The uniformity and steepness ensure a continuous and straight shape of the NWs after silicidation. A 35-nm-thick layer of Pt is deposited on the surface of the Si NWs by electron beam evaporation. The silicidation step is processed in a rapid thermal annealing system at 400 °C for 2 min under forming gas (N_2:H_2 95:5). The residual Pt on the surface of the buried oxide is removed in aqua regia (HNO_3:HCl:H_2O 1:3:2) at 50 °C. Figure 1(c) shows the top-view SEM picture of the silicided NWs. The sidewalls of the NWs become rough. Even so, they are smoother than that of NiSi NWs. This is one of the advantages of PtSi NWs. Figure 1(d) gives the cross-sectional TEM picture for one of the PtSi NWs. A gray core remains, corresponding to the unreacted Si, revealing that the 35-nm-thick Pt-film is not sufficient to fully convert 68-nm-high Si NWs into PtSi NWs. Along the vertical direction, about 46-nm-high Si is consumed and converted into a darker PtSi with a height of about 68 nm. Approximately, one thickness unit of Pt consumes 1.31 thickness units of Si to form 1.94 thickness units of PtSi. This consumption rule is consistent with that of the planar process as summarized in Table I. Besides, a thin PtSi film with a thickness of about 5 nm is observed at the bottom of each sidewall. When the sidewalls of the Si NW are quite steep, only very thin deposited Pt-film can cover them, even if the NWs are tilted during the Pt deposition. Therefore, only a few Pt atoms are able to dissolve into Si for the reaction on the sidewalls. In order to fully silicide NWs, we increase the thickness of the deposited Pt-film from 35 to 50 nm and keep the annealing conditions unchanged. A cross-sectional TEM picture of a PtSi NW shown in Fig. 1(e) confirms that the Si NW has been FUSI in this case and the Pt-film thickness is appropriate for Si available to form PtSi since the residual Pt is not observed. The TEM images [Figs. 1(b) and 1(e)] have been acquired on nine NWs with identical dimensions. The cross-sectional area ratio between PtSi NW and Si NW is statistically calculated from those images. The transformation of Si NW into PtSi NW increases the cross-sectional area by 52%, in which the width and height increase by 1.33% and 1.15%, respectively. This is attributed to the molar volume change (0.15) during Pt silicidation reaction,[9] which is in agreement with the thickness change in the film silicidation and the cross-sectional area change in NW silicidation (see column 6 in Table I). The HRTEM picture of PtSi NW shown in Fig. 1(f) presents polycrystalline properties compared to the single crystalline Si NW in Fig. 1(g).

Then on a p-type SOI wafer (68-nm-thick Si film), we fabricate two kinds of fin-structures, which have a source, a drain and a NW channel. One of them is FUSI by 50-nm-thick Pt layer. The other one serves as a reference device, in which the source/drain regions are heavily doped by As, forming a n^+-p-n^+ structure. The substrate of the SOI wafer is used as a back-gate by depositing a layer of Au and the buried oxide (145-nm-thick) as the back-gate oxide. The drain current versus back-gate voltage curves of the both structures are plotted in Fig. 2(a). In the reference device, the drain current is increased with the increase in the back-gate voltage above a threshold voltage of about 5 V (blue curve). This is a classical behavior of an n-MOSFET. In the FUSI structure, the drain current is no longer modulated by the back-gate voltage (red curve). Moreover, the current value is significantly increased. These exhibit a typical property of a metallic silicide NW. Besides, we also fabricate a PASI structure on the other SOI wafer (10-nm-thick Si film) by 5-nm-thick Pt layer. Figure 2(b) demonstrates the drain current versus drain voltage curves of this structure at three different back-gate voltages (V_b) of −20, 0, and 20 V. For a given drain voltage, the current values are different at the different back-gate voltages. The reason will be explained below.

Figure 3(a) illustrates a schematic longitudinal cross section of a PASI structure, which is composed of a top PtSi layer and a bottom unreacted Si layer. It can be represented by a simplified equivalent circuit as shown in Fig. 3(b), in which R_{PtSi} and R_{Si} present the equivalent resistances of the PtSi and Si layers, respectively. The two resistances are connected by two Schottky diodes (D_S and D_D), standing for the Schottky junctions between the both layers. We first consider the case where the back-gate voltage equals to zero (V_b=0). When a voltage is applied to the drain (the source terminal being grounded), the drain current mainly flows through R_{PtSi} due to the much higher resistivity ratio (10^6:1) of Si relatively to PtSi. When a constant negative voltage is applied to the back-gate, an electron-rich layer is formed at the top of

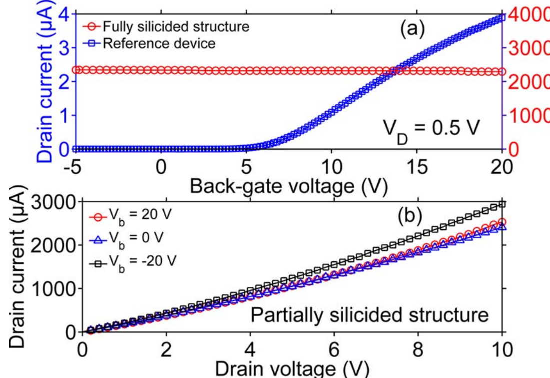

FIG. 2. (Color online) (a) Drain current versus back-gate voltage characteristics of a fully Pt-silicided fin-structure (5-μm-long, 100-nm-wide, and 78-nm thick FUSI NW), and a reference device (5-μm-long, 75-nm-wide, and 68-nm-thick Si channel), (b) Drain current versus drain voltage characteristics of a partially Pt-silicided fin-structure (5-μm-long, 50-nmm-wide, and 10-nm-thick Si NW before silicidation) at different back-gate voltages.

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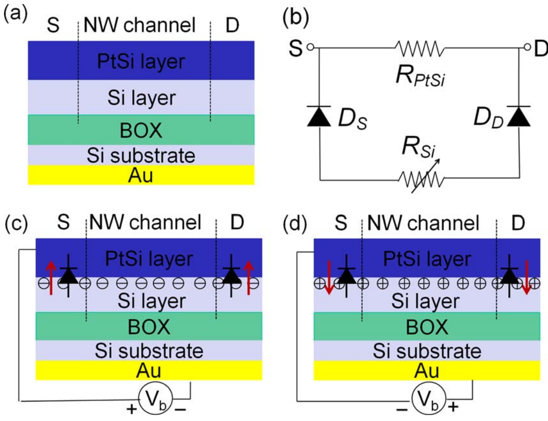

FIG. 3. (Color online) Schematic cross section (a) and simplified equivalent circuit (b) of a partially Pt-silicided fin-structure. Schematic cross sections of a partially Pt-silicided fin-structure biased by (c) negative and (d) positive back-gate voltages, respectively.

the Si layer [Fig. 3(c)], which drastically reduces R_{Si}. Moreover, the applied negative voltage lowers the barrier of the two Schottky diodes. Thus, the drain current also flows partially through the two diodes, thereby through R_{Si}. In this case, the drain current increases compared to the case where $V_b=0$. When a constant positive voltage is applied to the back-gate, a hole-rich layer is formed at the top of the Si layer [Fig. 3(d)]. However, the barrier of the two Schottky diodes is increased by the applied positive voltage. The drain current only flows through R_{PtSi}, except for a few leakage current through the two diodes. As a result, the drain current nearly remains unchanged compared to the case where $V_b=0$. Therefore, we can qualitatively determine whether the Si NWs is FUSI or PASI according to the dependence of the current on the backside substrate voltage. It is worth noting that under the same bias condition, the current flowing into the unreacted Si layer of the PASI structure is slightly larger than that flowing into the reference device. This may be explained by the fact that PtSi with a low Schottky barrier is directly used as the contact pads for the former while Au for the latter. Moreover, the substrate doping concentration is not identical for both wafers. Those result in different contact resistances, thereby, giving different currents.

Finally, we measure the resistivity of the FUSI NWs by a four-terminal structure shown in the inset to Fig. 4, in which 10 NWs with the same dimensions are connected in parallel by four contact pads. The current I flows into contact 1 and out by contact 4, and the voltage V is measured between contacts 2 and 3. The resistivity can be directly calculated by $\rho=n\times V\times w\times t/(I\times l)$, where n is the number of NWs and w, t, and l are the width, height, and length of the NW, respectively. The resistivity calculation is carried out for different lengths and widths of NWs. The results are shown in Fig. 4, giving an average value of 43 $\mu\Omega$ cm. This value is compatible with the resistivity of PtSi thin film materials (34–68 $\mu\Omega$ cm),[13] but higher than that recently reported from PtSi NWs (28–34 $\mu\Omega$ cm).[11,14] This may be explained by the different growth methods and annealing conditions, leading to different grain sizes. As shown in Fig. 4, the resistivity value decreases with the increase in the NW length. Although four-terminal structures are used for the measurements, the pad resistance (R_{pad}) between the contacting probe and the end of the NW cannot be eliminated. For long NWs, the R_{pad} influence is negligible. In contrast, R_{pad} might play a role in short NW's resistance evaluation, giving rise to a higher resistivity than the actual one.

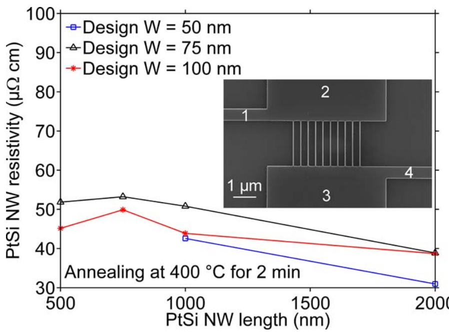

FIG. 4. (Color online) The resistivity extracted from FUSI NWs with different lengths and widths. The inset shows a top-view SEM picture of a four-terminal structure for resistivity extraction.

In conclusion, we investigate the physical and electrical characteristics of PtSi NWs. The Si consumption rules are identical in the NW and film Pt-silicidations. The cross-sectional area of Si NW increases by 52% after Pt-silicidation. This result is useful for considering the spacer of interconnections in nanodevice design and three-dimensional circuit integration. We present a simple method to evaluate the silicidation degree of Si NWs fabricated on SOI wafers. The original idea is to apply a voltage to the backside substrate of the SOI wafer: when a Si NW is converted into FUSI NW, the current passing through it remains unchanged for different applied voltages, in contrast, when the Si NW is converted into PASI NW, the current depends on the applied voltages. The evaluation results by this method are correlated with that of HRTEM inspections. The present method can provide valuable information about the silicidation process.

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