



On noise-induced transient bit flips in subthreshold SRAM[☆]

Léopold Van Brandt^{a,*}, Fernando Silveira^b, Jean-Charles Delvenne^a, Denis Flandre^a

^a ICTEAM Institute, UCLouvain, Louvain-la-Neuve, Belgium

^b Electrical Engineering Department, Universidad de la República, Uruguay

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ABSTRACT

We propose a rigorous SPICE simulation framework, compatible with industrial process design kits, to observe transient bit flips in CMOS SRAM due to the intrinsic transistor noise. The parameters of transient noise simulation are selected according to the noise behaviour and bandwidth of the inverter, however under CPU-time constraint. The methodology is illustrated in 28 nm FD-SOI technology. We study the combined effects of the random telegraph noise, flicker and thermal noise sources, for the first time to our knowledge. The extracted mean times to failure (*MTTF*) are compared to those reported in the literature in extreme voltage, temperature and variability conditions. The *MTTF* spans from below 0.1 ms to 10⁸ s, following a theoretical trend $\log MTTF \propto V_{DD}^2$.

1. Introduction

The Static Random Access Memory (SRAM) bitcell is a key building block for high-density memory arrays. Because each SRAM macro typically contains hundreds of thousands bitcells (e.g. 262 144 for 32 kB), a cell *failure probability* as low as the ppm (10⁻⁶) must be guaranteed for a given design across various process, voltage and temperature conditions [1].

The conventional Six-Transistor (6T) SRAM bitcell (sketched at the transistor level in Fig. 1) has remained very competitive thanks to its excellent scalability. Supplying the circuits at *ultra-low voltage* (ULV) operation is an efficient technique to reduce the power consumption [1, 2], and has motivated the introduction of extended SRAM architectures, like the 8T [3,4] or the 10T [5–7], which are more stable at the cost of significant area penalty [1]. This family of bitcells all use the same cross-coupled inverter pair (*latch*, dotted box in Fig. 1) for data *retention* (hold mode) [8].

A bitcell is *functional* as long as it capable of retaining a logical 0 or 1, and not losing this data during operation. The stability of “as-fabricated” bitcell at time zero, i.e. *static* stability, can be assessed with the traditional “butterfly plot” (Fig. 2(a)) [9]. The number of cross points of the mirrored transfer curve is exactly equal to three for a functional latch, the top-left and bottom-right stable points being the high and low logic levels taken by the data in retention [10]. *Static noise margin* metrics can be extracted [10] and quantify the robustness

of the bitcell against DC (static) sources of variations [11]. Although different relevant noise margins can be defined [12], we here focus on the *SNM*, referred to as “worst-case” static noise margin [10,11] and whose extraction procedure can be found for instance in [9–11].

As shown in Figs. 2(b) to 2(d), the *SNM* and hence the stability of a given bitcell is affected by supply voltage (V_{DD}) reduction (Fig. 2(b)), temperature (T) increase (which decreases the gain of the transistor and of the inverters, Fig. 2(c)) or any source of mismatch (Fig. 2(d)). Subthreshold SRAM bitcells, with V_{DD} lowered below the threshold voltages (V_{th}) of the transistors, or even below 200 mV [2,8,13], are highly sensitive to uncertainties [14]. Process *variability* has remained the major limitation to V_{DD} reduction at least up to 28 nm technology [2,14,15], given functional yield constraints. In [10], we proposed a methodology to predict the variability-induced *failure probability* of subthreshold SRAM bitcells in retention mode.

However, within a purely static formalism, any bitcell whose noise margin is positive ($SNM > 0$), even as small as a few mV, is presumptuously deemed functional. This neglects the potential effect of the noise and of any transient phenomenon (like time-dependent variability [16]) during the operation time of the memory. Launched by [17], the impact of the intrinsic *noise* of the MOS transistors on the functionality of digital logic circuits [15,18] and CMOS latches [19] operating in ultimate V_{DD} and extreme process and temperature conditions that degrade the noise margins has been addressed in a lesser extent than

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* Corresponding author.

E-mail address: leopold.vanbrandt@uclouvain.be (L. Van Brandt).

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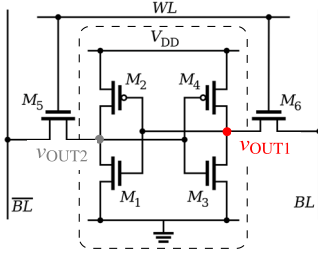


Fig. 1. 6T SRAM bitcell, whose data retention is ensured by a latch made of two back-to-back inverters.

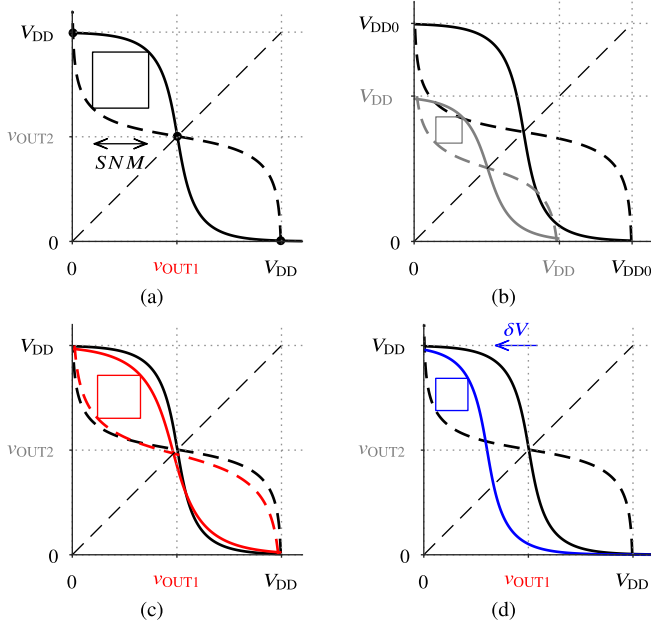


Fig. 2. (a) Nominal butterfly plot; SNM extraction. Effect of (b) supply voltage reduction, (c) temperature increase (in red) and (d) process variability on margin. SNM . Illustrated case: 28 nm FD-SOI RVT inverter of minimal transistor dimensions $L_n = L_p = 30$ nm and $W_n = W_p = 80$ nm, symmetrized, at room T , by a back-gate bias $V_{SB} = 1.6$ V applied to the pMOS. (a) $V_{DD} = 150$ mV, $T = 25$ °C; (b) $V_{DD} = 100$ mV; (c) $T = 120$ °C; (d) $\delta V = \Delta|V_{thp}| - \Delta V_{thn} = 30$ mV is an asymmetric mismatch between nMOS and pMOS transistors applied to the first inverter.

process variability. This concern is reinforced by experimental measurement of large-amplitude *random telegraph noise* (RTN), e.g. current variations of 30% in 28 nm FD-SOI [20].

It would be tempting to coarsely treat the random noise fluctuations as an additional source of variability. This approach is erroneous or, at best, overly pessimistic, because it ignores the fact that the logic gates are, by nature and as a consequence of their non-zero dynamic response time, more robust to the *dynamic* noise, i.e. that the dynamic noise margins are substantially larger than the static noise margins [21]. The impact of the RTN on SRAM stability has sometimes been studied through such pessimistic static analyses [22], or reliability-aware simulation [16]. In [23], a Monte-Carlo approach with home-made modules and model was used to simulate the circuit SRAM performance in presence of RTN. Moreover, no analysis of the combined effects of the RTN and flicker and thermal noise sources has been proposed in the literature to our best knowledge.

The *mean time to failure* $MTTF$ is a metric to quantify the SRAM reliability [19] at the bitcell level. Other statistical metrics, related to the SRAM array yield, were also introduced by [19] but are outside the scope of the present paper. The analytical prediction of the $MTTF$ is still in its infancy [15,24,25], while the need for accelerated transient

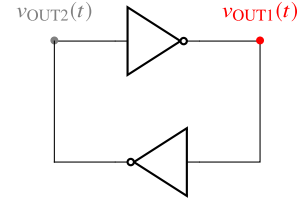


Fig. 3. The two cross-coupled CMOS inverters of Fig. 1, assumed isolated from the bit lines in retention mode.

noise simulations has been addressed by [19]. In this work extending [26], we propose a rigorous simulation framework, relying on industrial SPICE tools and process design kits (PDK), to observe noise-induced transient bit flips in various extreme voltage, temperature and RTN conditions. We apply our methodology to CMOS latches in 28 nm FD-SOI technology. We exploit the notion of static noise margin to insightfully compare and explain the different results.

2. Methodology

In retention mode, the word line voltage WL signal applied to the gates of the access transistors (M_5 and M_6 in Fig. 1) is zero or even negative, so that, in a good SRAM design, we can neglect the low leakage current and model the access transistors as ideal open circuits. The thermal noise contribution of these transistors in cutoff region is negligible (since their transconductance g_m is very small) compared to the noise of the inverters of the latch, and is thereby ignored. We thus focus here on the dynamic stability of the latch depicted in Fig. 3.

Generally, the noise can disturb the proper logic operation of a digital circuit, i.e. causing “soft errors” [18]. We call *bit* or *state flip* the (hopefully) rare event that a bitcell initially retaining a logical 0 randomly transitions to a 1 (or conversely). Such bit flips are the transient faults that we here aim at detecting with a suitable simulation framework.

2.1. Transient noise simulations

Noise simulations are traditionally performed in the frequency domain, whereas observing noise-induced bit flips requires transient experiments or simulations [27] offered in industrial SPICE simulators such as Eldo® from Siemens EDA® or Virtuoso® Spectre® from Cadence®. Any (linear or nonlinear) resistive device at temperature T is intrinsically noisy, notably the MOS transistors M_1 , M_2 , M_3 and M_4 of Fig. 1. Within the SPICE transient analysis formalism, a random noise source is added in parallel to each device [27]. Individual Gaussian noise sources are independently generated in the time domain according to the compact model of the devices, and the noise is then handled as any other electrical signal during a conventional transient simulation.

Simulated and measured signals being sampled in time, the noise is generated within a finite *bandwidth*, f_{max} , constraining the (maximum) time step (dt) to be used: $dt = 1/(2 f_{max})$. There is a CPU-time tradeoff between minimizing dt while maximizing the total duration of the simulation in order to record enough bit-flip events. Furthermore, to take into account all contributing noise components, we need to use $f_{max} \approx 10 \cdot f_p$, where f_p is the circuit bandwidth (here the inverter of Fig. 3) estimated from an AC (spectral) simulation.

2.2. NOISE (AC) simulation

Given the significant computational cost of transient noise analysis (for being experiments relying on repeated random sampling), it is important to carefully select the simulation parameters *a priori*. For this purpose, we recommend starting the study of any new case with

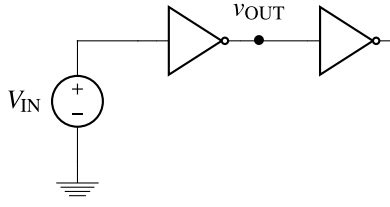


Fig. 4. Testbench used to characterize the output voltage noise of the inverter with the same fan-out as in Fig. 3, at a given DC bias point V_{IN} .

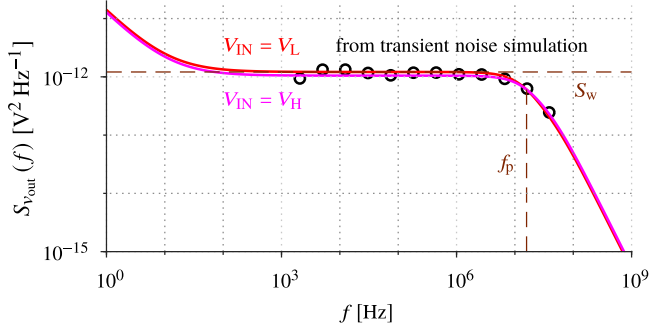


Fig. 5. PSD of the output voltage noise of the inverter, $S_{v_{out}}(f)$, extracted from a NOISE(AC) simulation of the circuit of Fig. 4 with $V_{IN} = V_L$ or V_H (solid coloured lines) or a NOISETRAN simulation (combined with a spectral estimation as in [20]) of the latch under the same conditions (circles). The horizontal dashed line denotes the thermal noise plateau S_w , the vertical dashed line the noise bandwidth f_p (defined at $S_w/2$). Illustrated case: same as Fig. 2(a).

a preliminary SPICE simulation in the frequency domain, NOISE(AC) that uses the full transistor noise compact model and accounts for the low-pass filtering effect of the gate.

We aim at assessing the contribution of the thermal and flicker noise sources of the MOS transistors of the inverters in the configuration of Fig. 3. However, the latch is not an appropriate testbench for an AC analysis because we cannot control the DC point (among the three crossings of the butterfly of Fig. 2(a)) around which the calculation is performed. Instead, we “open the feedback loop” and we work with the circuit depicted in Fig. 4, where an inverter is loaded by an identical inverter as suggested by [15]. By doing so, we characterize the intrinsic noise of the inverter in realistic fan-out conditions faithful to the latch of Fig. 3. A value of V_{IN} has to be selected to fix the bias point of the AC simulation. The only relevant points for bit-flip analyses are the two stable logic states of the latch ($V_{IN} = V_L \approx 0$ and $V_{IN} = V_H \approx V_{DD}$) [15].

The power spectral density (PSD) of the voltage noise at the output of the inverter, $S_{v_{out}}(f)$, has been extracted from a NOISE(AC) simulation and is plotted in Fig. 5. The inverter and the capacitive load low-pass filter the noise according to a first-order dominant pole transfer function. In Fig. 5, f_p is extracted as the noise bandwidth defined at $S_w/2$, where S_w is the thermal noise level. Beyond f_p , the PSD goes as expected as $1/f^2$, while the $1/f$ component is only visible at low frequency.

The total integrated noise power then writes

$$\sigma_{v_{out}}^2 = \int_{f_{min}}^{\infty} S_{v_{out}}(f) df, \quad (1)$$

while $\sigma_{v_{out}} = \sqrt{\sigma_{v_{out}}^2}$ denotes the RMS value of the noise. In (1), f_{min} is a lower cutoff frequency required for the flicker noise. Within our noise simulation formalism, we always use $f_{min} = 1/T$ where T is the total duration of the transient experiment. Importantly, a direct calculation shows that for all practical cases, the thermal noise is the dominant part of the total integrated noise power. Assimilating the inverter of Fig. 4 to a linear first-order filter (as suggested by Fig. 5) of cut-off frequency f_p , the equivalent noise bandwidth is $\frac{\pi}{2} f_p$.

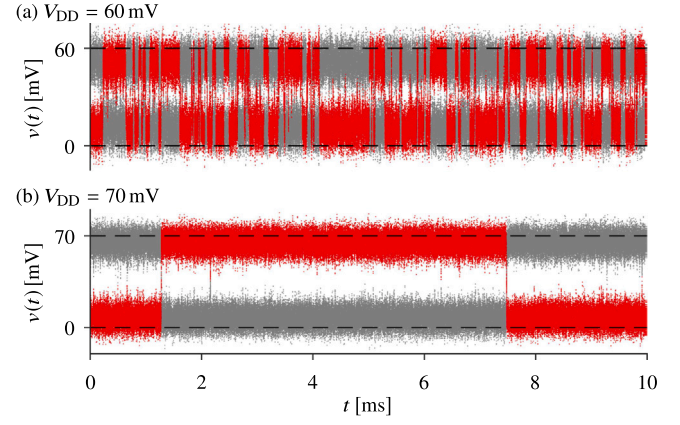


Fig. 6. Transient noise simulation of the latch (Fig. 3) at (a) $V_{DD} = 60$ mV and (b) $V_{DD} = 70$ mV. Reproduced from [26]. Illustrated case: same as Fig. 2(a) (excepted for the V_{DD} value). Bandwidth of the generated noise: $f_{max} = 10$ MHz ($dr = 50$ ns); simulation duration $T = 0.5$ s (for $V_{DD} = 70$ mV).

Then, $\sigma_{v_{out}} \approx \sqrt{\frac{\pi}{2} S_w f_p}$, i.e. proportional to $\sqrt{kT/C}$ since $S_w \propto kT g_m$, g_m being the transconductance of the transistors, while f_p is related to g_m/C where C is the total capacitance at the output of the inverter [15,17,24].

For the case simulated in Fig. 5, the noise behaviour is almost identical for the two states because the inverter is symmetrical, meaning that the driving strengths, the transconductances and hence the noise levels of the nMOS and pMOS transistor are really close. The RMS value of the noise in the latch configuration (Fig. 3) would be computed from the two PSDs obtained for the logic levels.

As a validation, we compare in Fig. 5 the PSD provided by the NOISE(AC) simulation with the PSD estimated from a transient noise simulation of the latch (circles) in the same conditions. The excellent matching confirms that the testbench of Fig. 4 is suitable to accurately characterize the small-signal noise at either stable node of the latch from a NOISE(AC) simulation. Moreover, the extracted PSD guides us in the selection of the suitable f_{max} (and the corresponding maximum time step dr); the transient simulation duration T is subsequently constrained by the maximum number of samples we can afford.

3. Transient bit-flips: Case studies

Provided with the simulation methodology described in Section 2, we perform transient noise analyses of subthreshold SRAM, first in ultra-low V_{DD} with thermal and flicker noise sources only, then in less extreme conditions but incorporating the RTN at the inverter level, in agreement with previous experimental work [20].

3.1. Ultimate V_{DD} lowering

We firstly reduce V_{DD} to the extreme in order to capture several bit flips in accessible computation time (at worse a few days on a high-performance station) and to estimate the MTTF for symmetrical latches, at room temperature (T) with only thermal and $1/f$ noise sources embedded in the model. For $V_{DD} = 60$ mV (Fig. 6(a)), 70 mV (Fig. 6(b)) on the same time scale) and 80 mV (not reproduced), we find $MTTF \approx 96 \mu s$, 8 ms and 18 s. As one might notice by comparing Figs. 6(a) and 6(b), the $MTTF$ spans across multiple orders of magnitude.

3.2. Random telegraph noise

To our best knowledge, no widespread PDK incorporates a compact model of the RTN yet. We here introduce it within the Eldo[®] NOISE-TRAN simulation framework as a series-voltage source $\delta V(t)$ (shown in

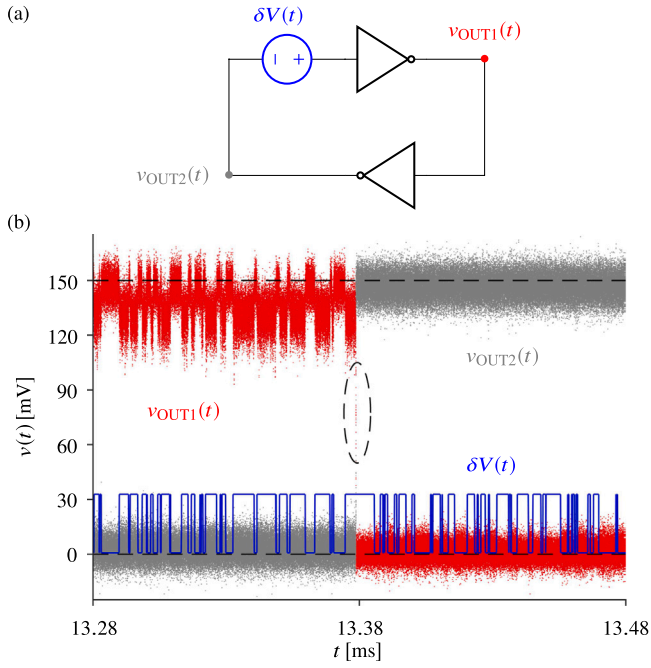


Fig. 7. Combined transient RTN and intrinsic Gaussian noise (Eldo® NOISETRAN) simulation of the latch (a), where the RTN is modelled as a series-voltage noise applied at the input of one inverter. Reproduced from [26]. The RTN parameters are $\delta V_0 = 32$ mV, $\bar{\tau}_c = \bar{\tau}_e = 2$ μ s [20]. Illustrated case: 28 nm FD-SOI Single-P-Well inverter (RVT nMOS and LVT pMOS); $V_B = 0$; $V_{DD} = 150$ mV; $T = 120$ °C. Bandwidth of the generated Gaussian noise: $f_{\max} = 500$ MHz ($dr = 1$ ns); simulation duration $T = 20$ ms.

Fig. 7(a)), whose amplitude δV_0 and the mean time constants $\bar{\tau}_c$ and $\bar{\tau}_e$ are approximated independent of the transistor biases in this first trial. The generator is however faithful to the physics of the Markov process [20]. The stochastic transitions can be observed in Fig. 7(b), for a case with $V_{DD} = 150$ mV and $T = 120$ °C. A bit flip occurs at 13.38 ms (Fig. 7(b)): when an RTN jump is high and long enough, the low logic state is weakened, so that a peak of Gaussian noise, sufficient both in amplitude and duration, causes the voltage signals to flip.

3.3. Static noise margin and Gaussian noise RMS value

The RMS value of the Gaussian noise ($\sigma_{v_{out}}$) can be estimated using several consistent approaches: either by extracting the noise power spectral density (NOISE(AC) simulation) as presented in Section 2.2; or empirically from the transient simulations of Figs. 6(a), 6(b) and 7(b). It turns out that $\sigma_{v_{out}}$ is not too sensitive to V_{DD} in deep sub-threshold and, because we keep the transistor dimensions minimal in the technology and thereby the capacitances, $\sigma_{v_{out}}$ weights about 6 mV for all the presented cases.

The relative impact of the Gaussian noise on the dynamic stability of the bitcell can then be assessed by the worst-case static noise margin (SNM) [15], that we introduced in Section 1. The SNM severely reduces with V_{DD} lowering, T increase and variability [10,14,15]. For the SRAM bitcell of Fig. 6, the SNM was respectively extracted as 10, 6 and 3 mV at $V_{DD} = 80, 70$ and 60 mV.

When RTN is considered jointly with Gaussian noise sources, as shown in Fig. 7 with $V_{DD} = 150$ mV, the large RTN dynamically reduces the SNM from 29 mV (nominal value) to 15 mV and thereby endangers the noise immunity of the latch.

4. Discussion

To observe transient bit flips due to the thermal and flicker noise sources, former works have combined extreme conditions [15,19]:

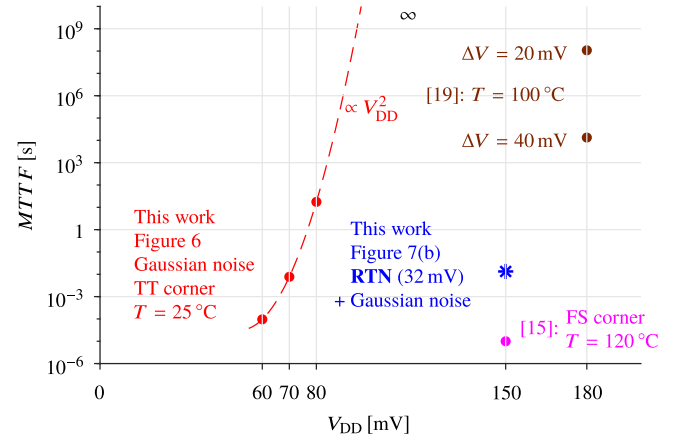


Fig. 8. $MTTF$ extracted from simulations in different technologies and various extreme voltage, temperature and variability conditions [26]. [15, Fig. 10]: 32 nm node; $T = 120$ °C; Fast/Slow (FS) corner. [19, Fig. 6]: 7 nm predictive PDK; $T = 100$ °C; the $\Delta V = |\Delta V_{th,p}| - \Delta V_{th,n} > 0$ is an asymmetric mismatch (Fig. 2(d)) applied to each inverter (FS corner).

sub-200 mV V_{DD} , high T and asymmetric process corner (Fast/Slow, resulting in imbalanced inverters). The purpose is to sufficiently reduce the SNM so as to lower the $MTTF$ to the order of a second or less (Fig. 8); rarer events are accessible to [19]'s accelerated simulator. For a symmetrical SRAM bitcell, in typical (TT) corner at room T and without additional variability, bit flips can only be recorded provided that V_{DD} gets further lowered (Fig. 6). Our results confirm the trend $\log MTTF \propto V_{DD}^2$ suggested by theoretical works [24,25] (indicated by a dashed line in Fig. 8).

We measured RTN amplitude as large as $\Delta I_D / I_D \approx 30\%$ in 28 nm FD-SOI transistors of smallest dimensions operating in subthreshold [20]. A corresponding threshold-voltage shift ΔV_{th} can be estimated through the transconductance g_m [28]:

$$\frac{\Delta I_D}{I_D} = \frac{g_m}{I_D} \Delta V_{th}, \text{ giving } \Delta V_{th} \approx 16 \text{ mV for } \frac{g_m}{I_D} \approx 19 \text{ V}^{-1}.$$

In Fig. 7, we have simulated a worst-case scenario in the inverter level where nMOS and pMOS transistors are adversely affected by a strong RTN, yielding $\delta V_0 = 32$ mV. As highlighted in Fig. 8, the $MTTF$ becomes less than a second at $V_{DD} = 150$ mV. The RTN acts as an additional source of variability reducing the noise margins.

The SNM is always less than 3σ of Gaussian noise for the presented cases. Although instantaneous peaks of 3σ are frequent for a randomly time-fluctuating Gaussian process, there is also a significant requirement on the duration of the transient noise peak to cause a bit flip [21]. This explains why the state-flip events remain rare.

5. Conclusion

Computational intensive noise transient simulations, available in industrial SPICE tools, are required to observe and analyse noise-induced bit flips in SRAM bitcells. Previous works focused on the worst process and temperature corner cases. In 28 nm FD-SOI, we have shown that Gaussian noise-induced bidirectional bit flips can probabilistically occur within an observational time scale in typical conditions when V_{DD} is reduced below 100 mV. We have further studied the combined effects of RTN, flicker and thermal noise at 150 mV. We claim that, whereas process variability remains a major concern, strong RTN jumps that are likely in the smallest transistors may lower the $MTTF$ by orders of magnitude and might thus need to be considered for subthreshold SRAM reliability assessment.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

Data will be made available on request.

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