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Heat sink implementation in back-end of line for self-heating reduction in 22 nm FDSOI MOSFETs

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ABSTRACT

This work studies the effect of heat sink in the back-end of line (BEOL) on the self-heating (SH) parameters of transistors in a Fully Depleted Silicon-on-Insulator (FDSOI) technology. The RF characterization technique, which involves S-parameter measurements over a wide frequency range, is used to evaluate SH parameters. Two types of sink configurations in the BEOL are considered; one connected to the gate and the other left floating. We experimentally demonstrate that gate-connected heat sink allows for a reduced self-heating in 22 nm FDSOI devices. Around 15% to 30% reduction in thermal resistance is observed for the gate-connected heat sink in comparison to the floating sink.

1. Introduction

The downscaling of CMOS technology has been crucial for the improvement of device performance and reduction of manufacturing costs [1]. The aggressive scaling of gate lengths and equivalent oxide thicknesses has helped in achieving lower intrinsic switching delay (CV/I) in high performance transistors [2]. Reduced gate length is highly beneficial for the MOSFET frequency performance increasing the current gain cutoff frequency f_T and maximum oscillation frequency f_{max} [3]. However, smaller device dimensions result in higher current and power densities, which potentially increases the concerns associated with self-heating (SH) effect. Higher SH with downscaling is therefore a primary observation regardless of the technology (bulk, FDSOI, FinFET, etc). Partially depleted SOI technology consists of a thick SiO_2 BOX layer that results in higher thermal resistance of this layer and worsens SH issues compared to bulk where the BOX was absent. Moving on to FDSOI technology with ultra-thin body and ultra-thin BOX (UTBB), the BOX thickness is reduced and this thinning of the BOX helps in reducing the SH issues compared to PDSOI technologies. Knowing that FDSOI is more prone to SH issues because of the presence of the less thermally conductive buried oxide (BOX) layer under the channel, our approach was tested on this technology. Furthermore, the dimensions of the thin top Silicon film (being it either in FDSOI or FinFETs or nanowires) are lower than the phonon mean free path which results in reduction of thermal conductivity of these layers due to boundary scattering [2]. Nevertheless, SH still impacts FDSOI MOSFET performance [4]. As a consequence of higher device temperatures caused by SH, undesirable effects like mobility reduction, threshold voltage shift, lower output current and reduced reliability are encountered [3].

Aiding the dissipation of this heat generated in the channel would ameliorate the issues arising from SH. Removal of the heat generated in the channel can take place through the substrate, gate and drain regions and the back-end of line (BEOL) above. Recent work of Mariniello et al [5] experimentally demonstrated the effect of heating dissipation through the gate electrode and its impact on the heating of SOI devices. In this paper, we go further in this concept and propose techniques of SH reduction using dedicated heat sinks implemented in the process' BEOL and explore them experimentally. Previously, the prospect of using thermal shunts in the BEOL to suppress SH was studied in [6], but only by simulations. Out of the aforementioned possible heat evacuation paths, the BEOL path above the MOSFET is of interest in this work. While the front-end of line (FEOL) including the substrate, BOX, source, drain and gate regions is mostly fixed by the technology, the BEOL offers the flexibility to realize desired structures. Our work experimentally addresses heat evacuation through the BEOL using various heat sink configurations.

The 22 nm fully depleted Silicon-on-Insulator (FDSOI) technology from GlobalFoundries, one of the most advanced nodes that caters to the tremendous requirements in upcoming mobile, RF and Internet-of-Things (IoT) applications [7], is used in this study. Given that FDSOI

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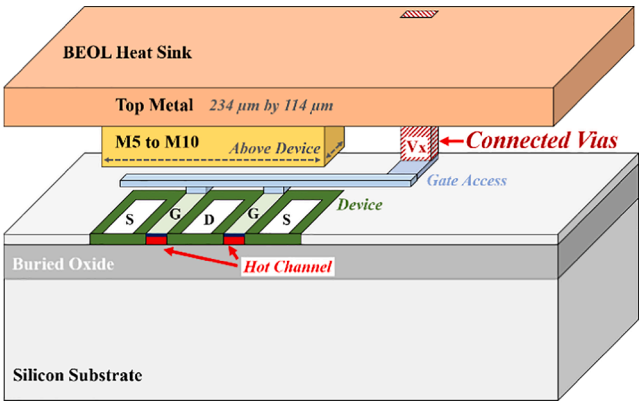

Fig. 1. Schematic of the gate-connected sink.

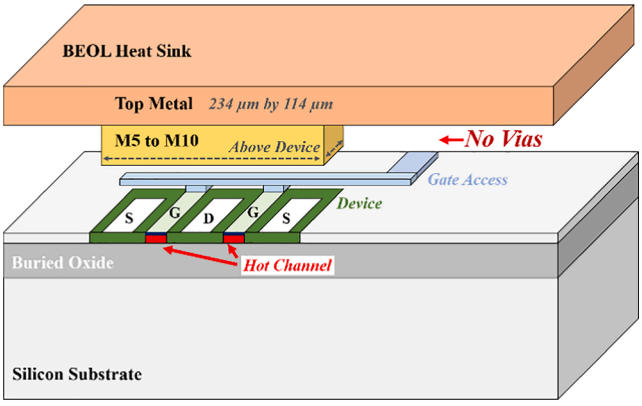

Fig. 2. Schematic of the floating sink.

technology is one of the prominent candidates for going below the 28 nm technology node, evaluating SH on this technology is of prime interest. The BEOL consisting of 11 metal layers in this technology provides ample scope of realization of heat sinks to facilitate heat dissipation. Knowing that FDSOI is more prone to SH issues relative to bulk CMOS because of the presence of the buried oxide (BOX) layer under the channel, our approach was tested on this technology [4].

In this paper, we propose a potential technique for reducing SH using dedicated heat sinks for the devices implemented in the process' BEOL and explore it experimentally. Additionally, the effect of the presence of the heat sinks on performance of the devices is studied. This paper extends our conference publication [8] by comparing different extraction methods, adding more measured dies and bias conditions. Section I introduces the background of SH and the target of this work. Section II provides details of the studied devices, the characterization technique to evaluate SH and the extraction methods. Section III discusses the results obtained from measurements and their implications and Section IV concludes the study by summing up the main outcomes of the work.

2. Experimental details and approach

In this section, the devices under study are first discussed followed by the introduction of the extraction techniques we used.

2.1. Device details

The devices used in this study originate from the 22 nm FDSOI technology from GlobalFoundries [7]. The gate length is 20 nm, total width is 30 μm for each of these devices composed of 60 fingers, each finger having a width of 0.5 μm. In this work, two identical FETs but with two different heat sink configurations are considered. One of them

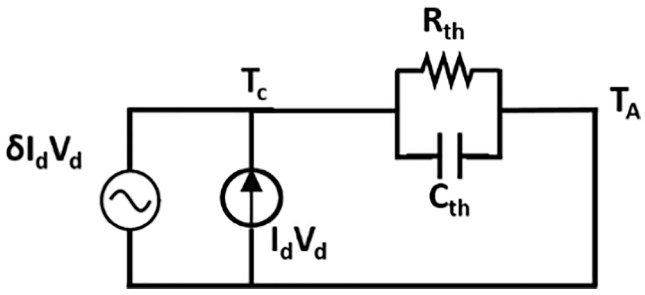

Fig. 3. First order thermal equivalent circuit modeling dynamic and static self-heating effect due to a DC bias point (I_dV_d) and AC excitation (δI_dV_d). T_c is the channel device temperature and T_A is the ambient temperature (room temperature here). Dynamic self-heating is suppressed at high frequencies.

is connected to a heat sink through the gate (called "gate-connected sink"), while the other one includes the same heat sink, which is left floating (called "floating sink").

The heat sink, introduced in the BEOL, consists of a metallic pad right above the FET over which the passivation layer is removed. With the BEOL consisting of 11 metal layers, a metal plate of 234 μm by 114 μm is used on the uppermost metal layer, connected down with vias to the fifth metal layer. Figs. 1 and 2 schematically illustrate the gate-connected sink and the floating sink configurations, respectively. The gate-connected sink (Fig. 1) comprises of a similar metal plate in the top metal layer, however, it is connected by vias to the gate above the gate accesses. The floating sink is left electrically and thermally floating above the fingers of the FET in the fifth metal layer and consists of metal rectangles that continue to stack up to the metal plate in the topmost layer. Note that there are two gate accesses that lie on either side of the gate fingers of the FET that help in connecting them to the sink (only one of these gate accesses connecting the fingers is seen in Figs. 1 and 2). The main difference between these two kinds of sinks is the electric and thermal connection to the gate with metal vias above the fifth metal layer (labelled as connected vias "Vx" in Fig. 1). The absence of these vias in case of the floating sink can also be perceived clearly in Fig. 2.

It is worth noting that the way of incorporation of the heat sink in the BEOL we propose in this work does not add a penalty in terms of area occupied by the device (or circuit) on which it is implemented. Moreover, the freedom to introduce the sink in devices which are expected to feature greater SH is one of the advantages of this implementation.

2.2. Measurements and extraction

To assess self-heating features we use in this work the RF characterization technique, which is a frequency domain method. RF technique was recently shown to be the most suitable for SH characterization in the most advanced deeply down-sized state-of-the-art devices [9], because frequencies up to a few gigahertz need to be reached to attain dynamic self-heating-free conditions in these devices. In this context, it is important to look into the thermal resistance R_{th} and thermal capacitance C_{th}. An RC thermal circuit consisting of R_{th} and C_{th} can then be used to model the complex thermal impedance as described in [10] and shown in Fig. 3. R_{th} refers to the resistance offered to the heat flow and is linked to the temperature rise ΔT and power P as

$$\Delta T = R_{th} \cdot P \tag{1}$$

While R_{th} depends on the surface area available for heat evacuation, C_{th} depends on the volume available to store heat [9]. With technology scaling down, the thermal capacitance C_{th} related to the device volume reduces, reducing the thermal time constant τ_{th} which is the product of R_{th} and C_{th}. The thermal frequency ($f_{th} = 1/(2\pi\tau_{th})$) that is inversely proportional to τ_{th}, is thereby shifted to higher values. Alternative techniques for SH characterization have shown distinct limitations especially for devices in the most advanced technology nodes. For

example, the AC conductance technique is limited in frequency to a few megahertz [9] due to which accurate estimation of SH parameters in advanced devices with a high thermal frequency is not possible. The Pulsed IV technique, on the other hand, uses pulse widths that are not sufficiently low for advanced devices with low thermal time constants [9]. For this reason, the RF technique was preferred over other characterization techniques for the devices studied in the 22 nm FDSOI technology.

For the RF characterization, S-parameters are measured in a frequency range from 100 kHz to 1 GHz and converted to Y parameters. An ENA vector network analyser and two RF |Z| probes of 100 μm pitch are used for these measurements. DC biasing of the gate and drain is done using a semiconductor analyzer HP 4145. Bias tees are used to combine the aforementioned DC bias and the RF cables to connect to the VNA. SOLT (Short-Open-Load-Thru) method is used for calibration at room temperature. The output conductance (g_d) is computed as the real part of Y_{dd}, transconductance (g_m) is the real part of Y_{dg} and the drain capacitance (C_{dd}) is the imaginary part of Y_{dd} divided by ω. Both g_d versus frequency and C_{dd} versus frequency curves show transitions caused by SH, which allows to assess SH-related features (as e.g. R_{th} and C_{th}). The transition due to source and drain coupling through the substrate is strongly attenuated by the doped back gate in our devices [11] and is neglected in this work. This is furthermore justified by the fact that the back-gate (regular threshold voltage, conventional well) and substrate network is exactly the same in both types of devices we compare in this work.

The impact of SH causes a transition from low frequency to the high frequency in Y_{dd} which can be seen in Eq. (2) [12,13]:

$$Y_{dd,HF} - Y_{dd,LF} = Z_{th}\frac{\partial I_d}{\partial T}(I_d + V_d Y_{dd}) \tag{2}$$

Following the derivation in [13] and decomposing Eq. (2) into its real and imaginary parts, Eq. (3) and Eq. (4) are obtained respectively.

$$\frac{R_{th}}{1+\omega^2 R_{th}^2 C_{th}^2} = \frac{g_d(f) - g_{d,HF}}{(I_d + V_d g_d(f))\frac{\partial I_d}{\partial T}} \tag{3}$$

$$\frac{-R_{th}^2 C_{th}}{1+\omega^2 R_{th}^2 C_{th}^2} = \frac{C_{dd}(f) - C_{dd,HF}}{(I_d + V_d g_d(f))\frac{\partial I_d}{\partial T}} \tag{4}$$

I_d is the DC drain current, V_d is drain voltage, $g_{d,HF}$ and $C_{dd,HF}$ are the output conductance g_d and drain capacitance C_{dd}, respectively, at high frequency (where dynamic self-heating effect is removed) and $\partial I_d/\partial T$ is the slope of the I_d versus temperature.

In this work both these extraction formulae have been used:

i) Extraction Method 1 uses Eq. (3) and thereby computes Rth from the real part of Ydd;
ii) Extraction Method 2 uses Eq. (4) and thereby computes Rth and Cth from the imaginary part of Y_{dd}.

In extraction Method 1, the thermal resistance R_{th} is extracted using (3): at low frequency the numerator of the right-side of Eq. (3) becomes Δg_d, the difference between the output conductance g_d at low and high frequencies. In extraction Method 2, a fourth order thermal RC network is used to fit the imaginary part of Y_{dd} measurements, similar to the procedure in [12]. For devices with different heat evacuation paths, a first order network is usually insufficient to fit the experimental data and higher order networks are found to be more appropriate. Similar to [12] as well as our previous observations on the same technology in [14] a fourth order network was found to be sufficient in our case. Based on this fitting, R_{th} is computed using extraction Method 2 as the equivalent low-frequency R_{th} of the fourth order RC network ($\sum_{i=1}^{4} R_{th,i}$). C_{th} has been computed from Eq. (4) by using the difference in C_{dd} at low and high frequencies and plugging in the value of R_{th} obtained previously. $\partial I_d/\partial T$ is extracted from I_d-V_g curves measured in a temperature range from 300 up to 400 K. This has been achieved by a Thermo-chuck from Temptronic that allows heating up the devices to the desired temperature points with good temperature control and stabilization. The extractions have been made in saturation at a V_g and V_d of 0.8 and 0.9 V. Though the nominal V_d of this technology is 0.8 V, a value of 0.9 V has been used here to increase the power in the channel and thereby stimulate higher SH. The back gate was grounded during measurements.

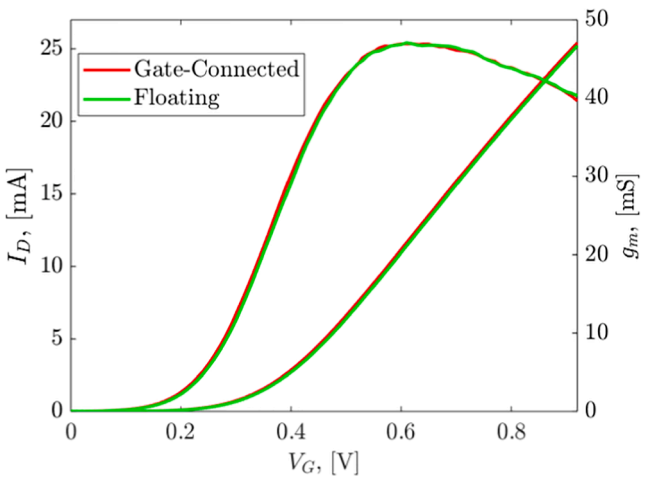

Fig. 4. Drain current I_d and transconductance g_m vs gate voltage V_g for the "gate connected" and "floating" sinks recorded in saturation at $V_d = 0.9$ V.

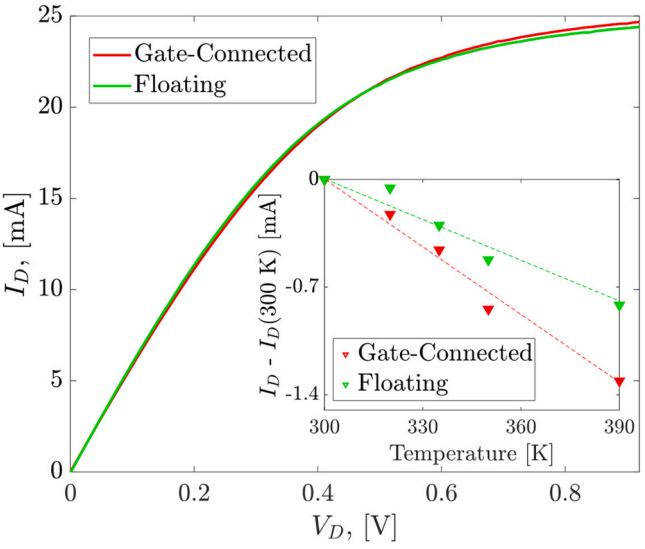

Fig. 5. Drain current I_d vs drain voltage V_d for the "gate connected" and "floating" sinks measured at $V_g = 0.9$ V, I_d vs temperature measured shown in inset.

3. Results and discussion

3.1. IV characterization

Fig. 4 shows the I_d-V_g and the g_m-V_g curves for both types of devices in saturation at $V_d = 0.9$ V. The fact that the gate connection of the sink does not affect the DC device performance is observed from the almost overlapping curves. The same threshold voltage V_{th} of 0.34 V is obtained for both types of devices from the second derivative method in the linear regime, thus allowing a fair comparison of these devices.

Fig. 5 shows the I_d-V_d curves for both types of devices for $V_g = 0.9$ V. While it is observed that the curves are mostly overlapping, the I_d and its

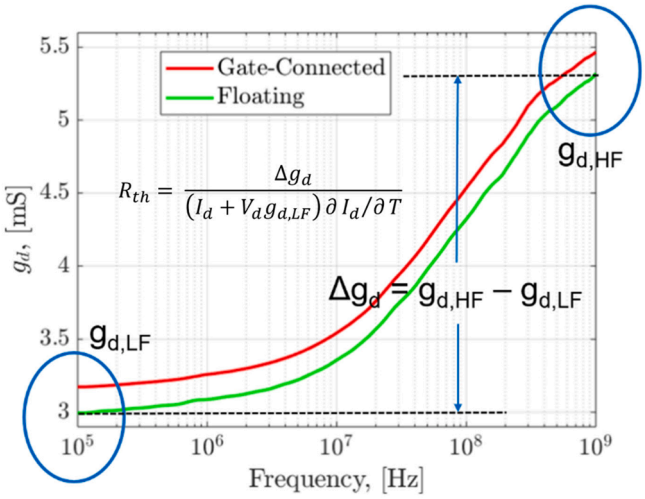

Fig. 6. Output conductance g_d vs frequency for the "gate connected" and "floating" sinks at $V_g = V_d = 0.9$ V.

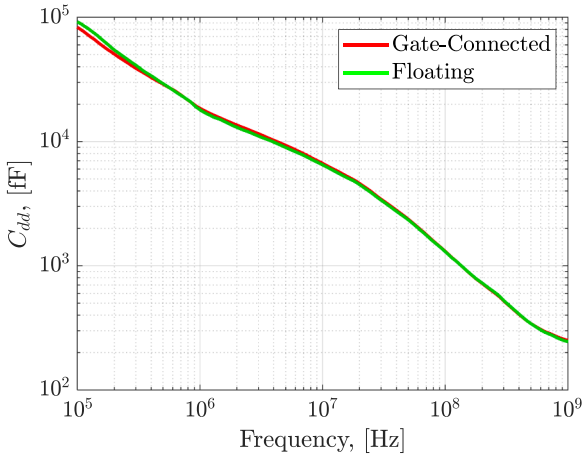

Fig. 7. Drain capacitance C_{dd} vs frequency for the "gate connected" and "floating" sinks at $V_g = V_d = 0.9$ V.

slope (i.e. g_d) for the gate-connected sink are a bit larger than that for the floating sink in saturation. This correlates with the observations from I_d-V_g plot in Fig. 4. The value of $g_{d,DC}$ for gate-connected sink is 3.2 mS and for floating sink is 3 mS at $V_g = V_d = 0.9$ V suggesting weaker SH in the gate-connected sink device. This will be further confirmed by g_d (f) measurements below.

3.2. SH characterization

Fig. 6 shows the variation of output conductance g_d with frequency. From this plot, $g_{d,LF}$ (g_d at low frequency of 100 kHz), $g_{d,HF}$ (g_d at high frequency of 1 GHz) and Δg_d (the difference between $g_{d,HF}$ and $g_{d,LF}$) are extracted, as needed for the R_{th} estimation using RF method. The values of g_d at low and high frequencies represent the cases where dynamic self-heating is present and removed, respectively. Since the lowest specified frequency of operation of the bias tees is 20 kHz, the low frequency value of 100 kHz is chosen to have reasonable results free from error. The value at 100 kHz is in fact verified to be a steady value. Higher value of $g_{d,LF}$ obtained for the gate-connected sink agrees well with conclusions drawn from I_d-V_d plots above and demonstrate the fact that device with a gate-connected sink is less affected by SH compared to the floating sink counterpart. It can be noticed that there is still a difference between $g_{d,HF}$ for two configurations. This is because at HF dynamic SH is removed,

Table 1
Extraction Method 1. Vg = Vd = 0.9 V.

Sink Type	$g_{d,LF}$ (mS)	Δg_d (mS)	$\partial I_d/\partial T$ (μA/K)	R_{th} Normalized (Kμm/mW)
Connected	3.17	2.29	−9.85	254
Floating	3	2.31	−8.17	313

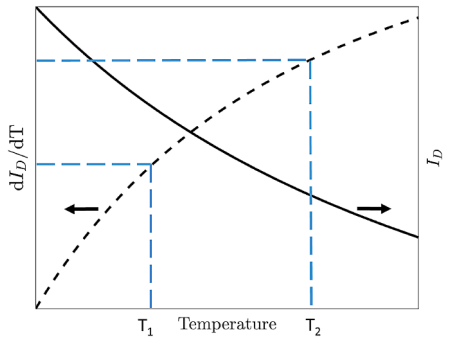

Fig. 8. Drain current I_d vs Temperature and slope dI_d/dT based on a power law $I_d/I_{d0} \sim \mu/\mu_0 \sim (T/T_0)^{-k}$.

but static SH remains, so that $g_{d,HF}$ for gate-connected sink is a bit higher. The reason that the g_d curve seems to keep slightly increasing at the HF point of 1 GHz is the fact that the measurements here are not de-embedded. From measurements on similar devices with proper de-embedding structures, it is observed that $g_{d,HF}$ reaches a plateau a bit below 1 GHz. While it is true that the $g_{d,HF}$ value extracted is a bit higher than the actual value that would have been obtained had de-embedding been present, a fair comparison is maintained by the fact that the results of both the devices being compared are not de-embedded. Furthermore, extraction Method 2 is almost unaffected by this effect. Indeed, from the C_{dd} versus frequency plot in Fig. 7, it has been observed that, firstly, the $C_{dd,HF}$ value at 1 GHz is close to the plateau. Secondly, SH-related variation of C_{dd} is seen to be around 3 orders of magnitude higher than $C_{dd,HF}$ and thus small variation of $C_{dd,HF}$ almost does not affect the SH extraction.

Table 1 summarizes the comparison of the devices with gate-connected sink and floating sink (at $V_g = V_d = 0.9$ V) not only in terms of normalized values of R_{th}, but also various parameters involved in its extraction (using Eq. (1)), such as output conductance g_d at low frequency $g_{d,LF}$ and the difference between g_d at high and low frequencies Δg_d and $\partial I_d/\partial T$.

Higher value of $g_{d,LF}$ and lower Δg_d are obtained for the gate-connected sink suggesting lower SH in such devices. It is verified that the values of g_d at DC from the I_d-V_d plots (reported in a previous section) are very similar to the $g_{d,LF}$ values obtained at 100 kHz.

The absolute value of $\partial I_d/\partial T$ is found to be higher for the gate-connected sink confirming weaker SH in this case. In order to better explain this difference, let us start by considering I_d variation versus temperature. At high-V_g values, I_d is expected to reduce with temperature mainly because of mobility degradation from phonon scattering given by a power law $I_d/I_{d0} \sim \mu/\mu_0 \sim (T/T_0)^{-k}$ [15]. Fig. 8 schematically shows I_d versus T and the slope of this variation, which is found to be more negative at lower temperatures (note that $\partial I_d/\partial T$ is negative in the plot as I_d is decreasing with temperature) compared to higher temperatures. It is clearly illustrated in Fig. 8 that with higher temperature rise coming from higher SH, a device at a lower temperature T_1 shows a higher magnitude of $\partial I_d/\partial T$ compared to the case where it experiences greater SH and is at a higher temperature T_2. This shows that the magnitude of $\partial I_d/\partial T$ is expected to be higher for the case where lesser SH is observed, that is the gate-connected sink in this work.

Combination of the above parameters, namely the g_d values at LF and

Table 2
Extraction Method 2. Vg = Vd = 0.9 V.

Sink Type	R_{th} Normalized (Kμm/mW)	C_{th} (pJ/K)	τ_{th} (ns)	f_{th} (MHz)
Connected	244	4.86	39.52	4
Floating	317	4.07	41.59	3.8

HF and the $\partial I_d/\partial T$, results in a lower value of R_{th} for the gate-connected sink. It is observed that the normalized R_{th} in the case of gate-connected sink is around 20 % lesser than for the floating sink case.

The variation of C_{dd} with frequency is shown in Fig. 7. Using the second extraction method, R_{th} and C_{th} are computed as shown in Table Table 2 for the same devices. Additionally, τ_{th} is calculated as the product of R_{th} and C_{th} and f_{th} is given as $1/(2\pi\tau_{th})$. It is important to emphasize that both extraction methods provide similar results in terms of R_{th}.

Measurements on multiple dies confirm this trend of lower normalized R_{th} in the case of gate-connected sink (Fig. 9). Furthermore, the same improvement is observed for various bias conditions (Fig. 9). In the figure, we also observe good agreement in the R_{th} reduction using the two extraction techniques. The percentage reduction in R_{th} when the sink is connected is observed to vary from 15 to 35 % over five dies. The variation in the magnitude of R_{th} reduction over dies arises in a part from die to die process variability from source, drain and extensions doping, Si and oxide layer thicknesses, gate edge roughness, metal grain granularity, etc. as for any advanced process.. Furthermore, possible variation in the BEOL stack layers thicknesses need to be considered (particularly in our case with different sink configurations). Of course, unavoidable measurements variability cannot be neglected. The observation of the general effect of variability can be clearly made from earlier work of our group in [4]. However, the main point of our work is relative improvement and it can be seen that despite the variability between dies, applied bias and extraction techniques, there is always an improvement (15–35%).

The absence of the metal vias above the fifth layer of the BEOL in the case of the floating sink was expected (theoretically) to result in a greater R_{th} of that heat evacuation path. This stems from the fact that the thermal conductivity of dielectric SiO_2 is two orders of magnitude lower than that of bulk Silicon and even lower with respect to metal [16]. Thus, the heat sink in the floating case is left thermally floating for all practical considerations, thus blocking the heat evacuation through that path. On the other hand, in case of the gate-connected sink, connections from the FET to the heat sink in the topmost layer is expected to allow easier heat evacuation, resulting in a lower overall R_{th}. The results obtained experimentally in this work validate this theoretical hypothesis.

3.3. Discussion on impact of heat sink parasitics on RF performance

It is worth emphasizing that in the proposed configuration the connection of the sink creates a parallel network to the standard/usual connection of the gate access. Therefore, we do not expect to degrade the gate resistance due to connection of the sink. The increase in gate resistance R_g due to temperature rise from SH is expected to be limited as the heat evacuation path through the gate is not the only evacuation path; the downward path through the substrate also plays an important role. However, a detailed study of R_g could not be made because of the lack of de-embedding structures for the devices.

With the main intention of the device design being to show SH reduction, it was not designed from an RF performance perspective. Also, due to lack of de-embedding structures, precise information about the RF performance could not be demonstrated. The various parasitic capacitances between the regions where the sink and the gate access paths overlap degrade the RF performance. Based on parasitic extractions from de-embedding structures of similar devices, we predict that connecting the sink degrades the f_T by a factor of ~7.5 compared to the case when the sink is not present at all for the sink geometry investigated in this work. By leaving the sink electrically floating, this degradation could be reduced to a factor of ~1.5 times. We expect that the geometry of the sink can be further optimized for better RF performance and such a study is planned in the near future.

4. Conclusion

The prospect of using a BEOL heat-evacuator in order to alleviate

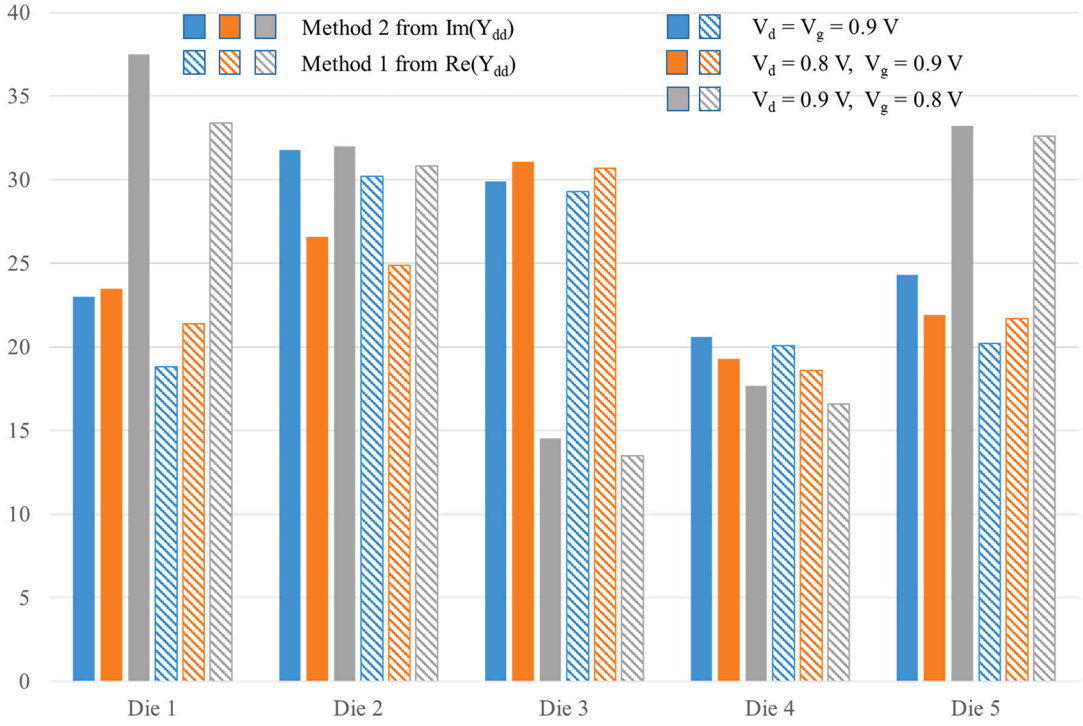

Fig. 9. Percentage reduction in R_{th} from floating sink to gate-connected sink for different bias conditions.

self-heating in advanced devices has been studied in this work. The reduction of thermal resistance (and hence temperature rise) in the case of a sink connected to the gate in comparison to it being left floating with respect to the gate has been experimentally verified. The fact that the DC performance of the two types of devices are similar (as seen from I_d-V_g, g_m-V_g curves) in order to make a fair comparison with respect to SH parameters has been confirmed. With the present configuration, we have achieved ~20–30% of the SH parameters improvement in the gate-connected sink devices. The observed trend was confirmed on different dies and at different bias conditions. Two extraction methods employed in this work (i.e. conductance and capacitance methods) provide consistent results, validating gate-sink-connected approach for SH reduction in advanced devices. Thus, the possibility of using a gate-connected sink to reduce self-heating has been put forth here as a proof of concept. While this study has been conducted on FDSOI MOSFETs, the idea of using a heat sink in the BEOL can be extended to other technologies. It is worth emphasizing that proposed configuration has two advantages: i) it does not alter the area occupied by the devices /circuit and ii) it does not expected to degrade the gate resistance. The sink is mainly aimed for use in devices where SH could be a concern and it does not affect the design of the original device. To enhance the efficiency of the heat removal by the sink and minimize the parasitic capacitance added by it, further optimization of the sink configuration is envisaged.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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